

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC74LVX00F, TC74LVX00FN, TC74LVX00FT****QUAD 2-INPUT NAND GATE**

The TC74LVX00 is a high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C<sup>2</sup>MOS technology. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low voltage and battery operated systems.

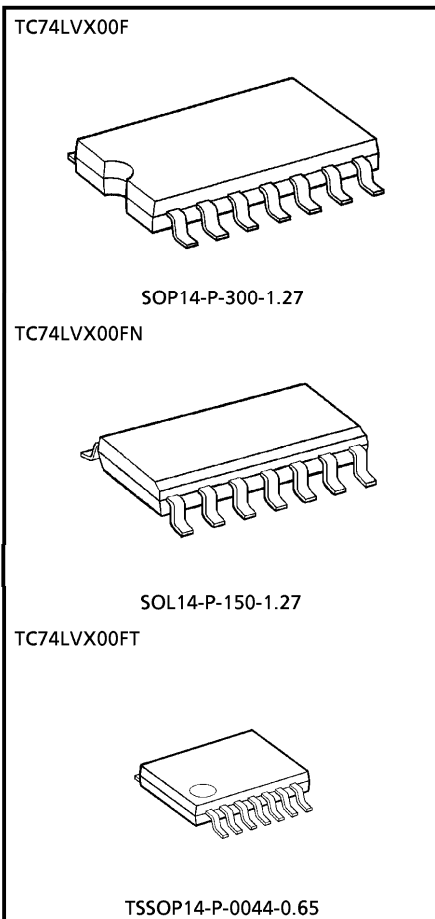
The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

**FEATURES**

- High speed :  $t_{pd} = 4.1\text{ns}$  (Typ.) ( $V_{CC} = 3.3\text{V}$ )
- Low power dissipation :  $I_{CC} = 2\mu\text{A}$  (Max.) ( $T_a = 25^\circ\text{C}$ )
- Input voltage level :  $V_{IL} = 0.8\text{V}$  (Max.) ( $V_{CC} = 3\text{V}$ )  
 $V_{IH} = 2.0\text{V}$  (Min.) ( $V_{CC} = 3\text{V}$ )
- Power down protection is provided on all inputs.
- Balanced propagation delays :  $t_{pLH} \approx t_{pHL}$
- Low noise :  $V_{OLP} = 0.5\text{V}$  (Max.)
- Pin and function compatible with 74HC00

(Note) The JEDEC SOP (FN) is not available in Japan.

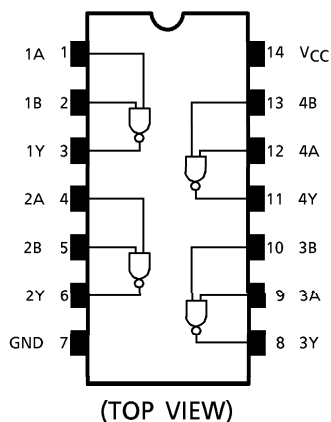


Weight  
 SOP14-P-300-1.27 : 0.18g (Typ.)  
 SOL14-P-150-1.27 : 0.12g (Typ.)  
 TSSOP14-P-0044-0.65 : 0.06g (Typ.)

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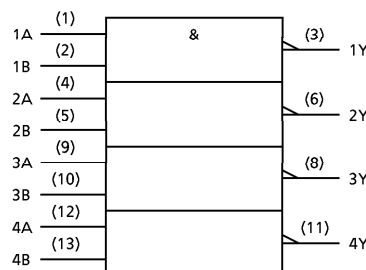
**PIN ASSIGNMENT**



**TRUTH TABLE**

INPUT		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

**IEC LOGIC SYMBOL**



**MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}$ +0.5	V
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	±20	mA
DC Output Current	$I_{OUT}$	±25	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	±50	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{stg}$	-65~150	°C

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	2.0~3.6	V
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise And Fall Time	$dt/dv$	0~100	ns/V

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- The information contained herein is subject to change without notice.

## ELECTRICAL CHARACTERISTICS

## DC characteristics

PARAMETER	SYM-BOL	TEST CONDITION	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT		
				MIN.	TYP.	MAX.	MIN.	MAX.			
Input Voltage	"H" Level	V <sub>IH</sub>	2.0	1.5	—	—	1.5	—	V		
			3.0	2.0	—	—	2.0	—			
			3.6	2.4	—	—	2.4	—			
	"L" Level	V <sub>IL</sub>	2.0	—	—	0.5	—	0.5			
			3.0	—	—	0.8	—	0.8			
			3.6	—	—	0.8	—	0.8			
Output Voltage	"H" Level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				I <sub>OH</sub> = -50 μA	3.0	2.9	3.0	—	2.9	—	
				I <sub>OH</sub> = -4mA	3.0	2.58	—	—	2.48	—	
	"L" Level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub>	I <sub>OL</sub> = 50 μA	2.0	—	0.0	0.1	—	0.1	
				I <sub>OL</sub> = 50 μA	3.0	—	0.0	0.1	—	0.1	
				I <sub>OL</sub> = 4mA	3.0	—	—	0.36	—	0.44	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5V or GND	3.6	—	—	±0.1	—	±1.0	μA		
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	3.6	—	—	2.0	—	20.0	μA		

AC characteristics (Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

PARAMETER	SYM-BOL	TEST CONDITION	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t <sub>pLH</sub> t <sub>pHL</sub>		2.7	15	—	5.4	10.1	1.0	12.5	ns
				50	—	7.9	13.6	1.0	16.0	
			3.3 ± 0.3	15	—	4.1	6.2	1.0	7.5	
				50	—	6.6	9.7	1.0	11.0	
Output To Output Skew	t <sub>osLH</sub> t <sub>osHL</sub>	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C <sub>IN</sub>	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C <sub>PD</sub>	(Note 3)			—	19	—	—	—	pF

(Note 1) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

(Note 2) Parameter guaranteed by design.

(Note 3) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

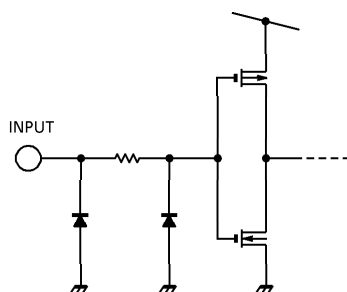
Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per Gate)}$$

Noise characteristics (Ta = 25°C, Input tr = tf = 3ns, CL = 50pF)

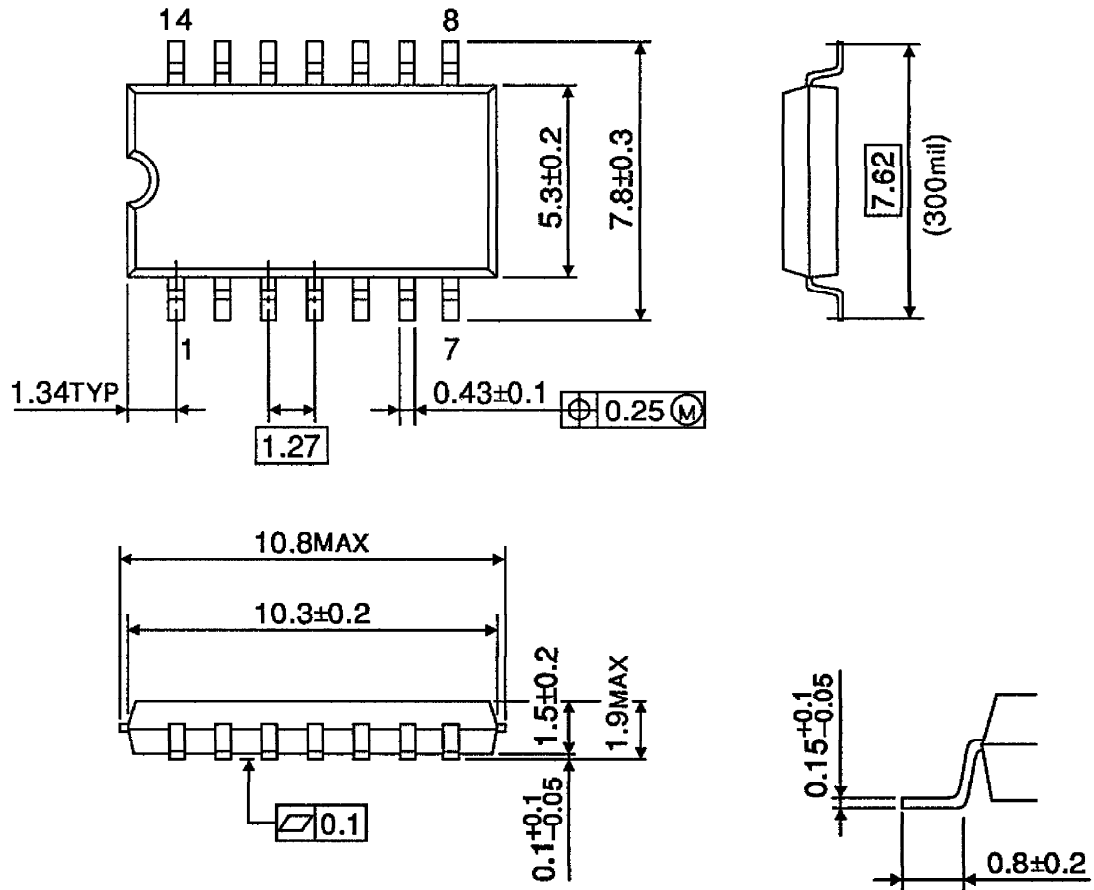
PARAMETER	SYMBOL	TEST CONDITION	VCC (V)	TYP.	LIMIT	UNIT
			3.3			
Quiet Output Maximum Dynamic VOL	VOLP		3.3	0.3	0.5	V
Quiet Output Minimum Dynamic VOL	VOLV		3.3	-0.3	-0.5	V
Minimum High Level Dynamic Input Voltage	VIHD		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	VILD		3.3	—	0.8	V

**INPUT EQUIVALENT CIRCUIT**



OUTLINE DRAWING  
SOP14-P-300-1.27

Unit : mm

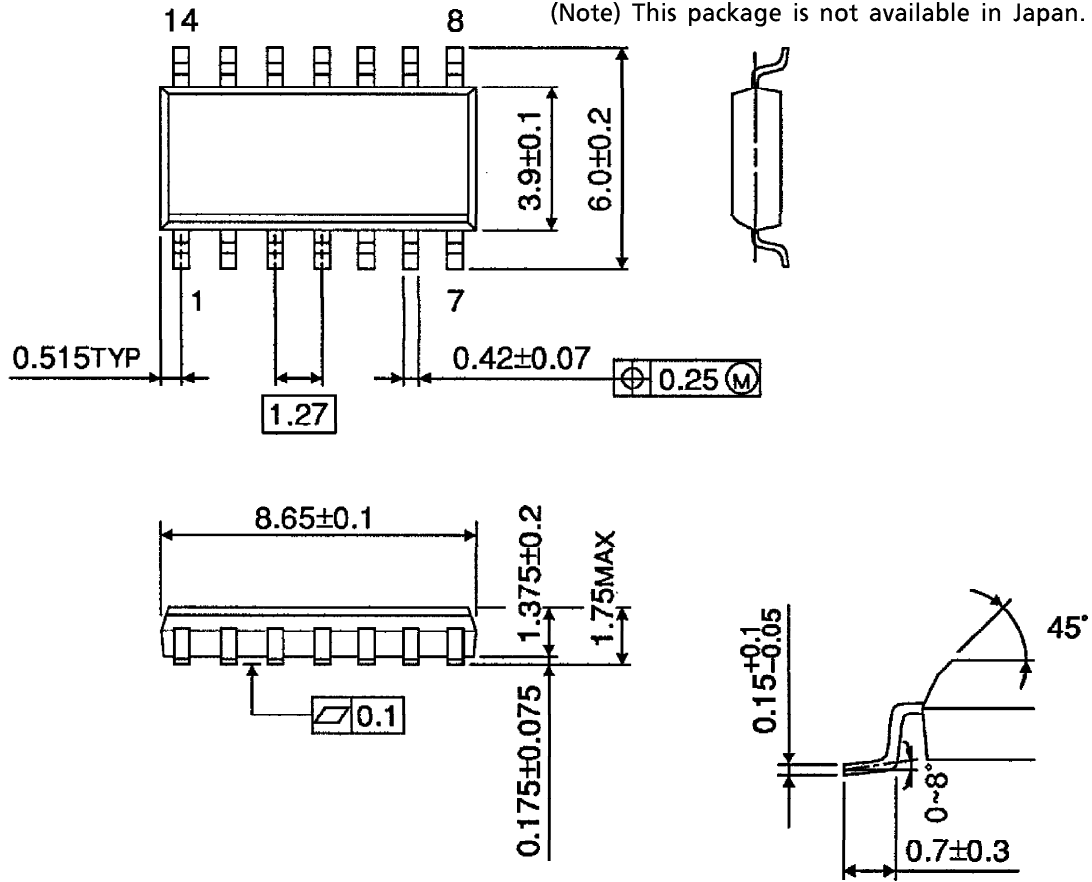


Weight : 0.18g (Typ.)

OUTLINE DRAWING  
SOL14-P-150-1.27

Unit : mm

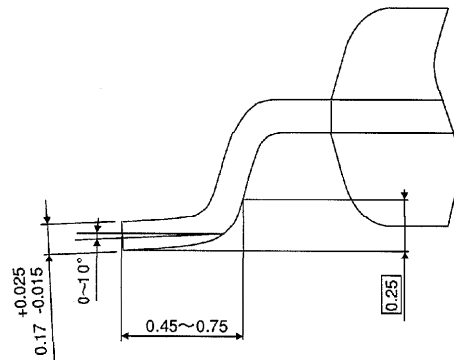
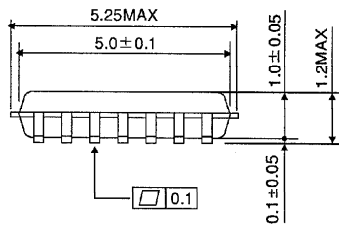
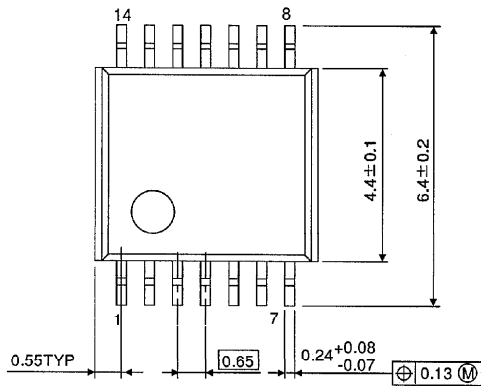
(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

**OUTLINE DRAWING**  
TSSOP14-P-0044-0.65

Unit : mm



Weight : 0.06g (Typ.)