

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

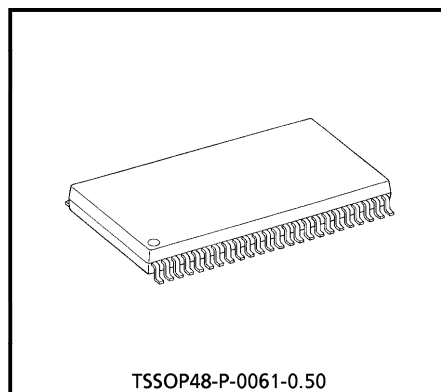
# TC74LCX16373AFT

## LOW-VOLTAGE 16-BIT D-TYPE LATCH WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX16373AFT is a high performance CMOS 16bit D-TYPE LATCH. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3V)  $V_{CC}$  applications, but it could be used to interface to 5V supply environment for both inputs and outputs. This 16-bit D-type latch is controlled by a latch enable input (LE) and a output enable input ( $\overline{OE}$ ) which are common to each byte. It can be used as two 8-bit latches or one 16-bit latch. When the  $\overline{OE}$  input is high, the outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge.

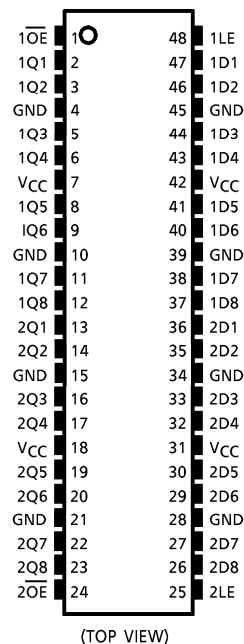


Weight : 0.25 g (Typ.)

### FEATURES

- Low Voltage Operation :  $V_{CC} = 2.0 \sim 3.6V$
- High Speed Operation :  $t_{pd} = 7.0 \text{ ns (max.)}$  at  $V_{CC} = 3.0 \sim 3.6V$
- Output Current :  $|I_{OH}| / I_{OL} = 24mA \text{ (min.)}$  at  $V_{CC} = 3.0V$
- Latch-up Performance :  $\pm 500mA$
- Package : TSSOP  
(Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.

### PIN CONNECTION



961001EBA2

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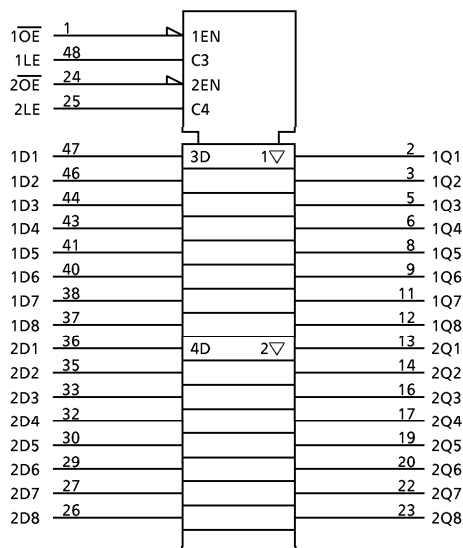
TRUTH TABLE

INPUT			OUTPUT
1OE	1LE	1D1-1D8	1Q1-1Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

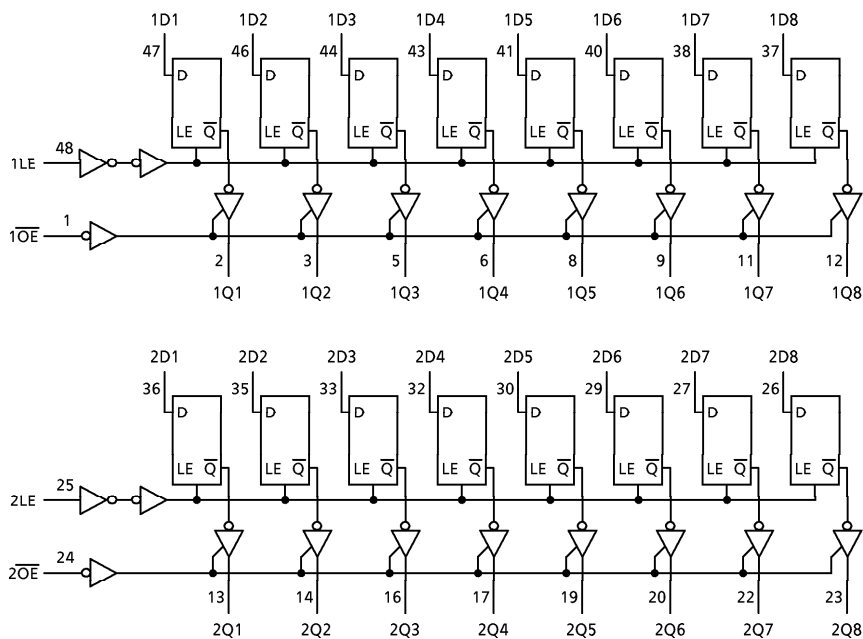
INPUT			OUTPUT
2OE	2LE	2D1-2D8	2Q1-2Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

X : Don't Care  
 Z : High impedance  
 Qn : No change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



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**MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	$V_{CC}$	-0.5~7.0	V
Input Voltage	$V_{IN}$	-0.5~7.0	V
Output Voltage	$V_{OUT}$	-0.5~7.0 (Note 1)	V
		-0.5~ $V_{CC}$ +0.5 (Note 2)	
Input Diode Current	$I_{IK}$	-50	mA
Output Diode Current	$I_{OK}$	±50 (Note 3)	mA
DC Output Current	$I_{OUT}$	±50	mA
Power Dissipation	$P_D$	400	mW
DC $V_{CC}$ /Ground Current Per Supply Pin	$I_{CC}/I_{GND}$	±100	mA
Storage Temperature	$T_{stg}$	-65~150	°C

(Note 1) Output in Off-State

(Note 2) High or Low State.  $I_{OUT}$  absolute maximum rating must be observed.

(Note 3)  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$

**RECOMMENDED OPERATING RANGE**

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	2.0~3.6	V
		1.5~3.6 (Note 4)	
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~5.5 (Note 5)	V
		0~ $V_{CC}$ (Note 6)	
Output Current	$I_{OH}/I_{OL}$	±24 (Note 7)	mA
		±12 (Note 8)	
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise And Fall Time	$dt/dv$	0~10 (Note 9)	ns/V

(Note 4) Data Retention Only

(Note 5) Output in Off-State

(Note 6) High or Low State

(Note 7)  $V_{CC} = 3.0\sim 3.6V$

(Note 8)  $V_{CC} = 2.7\sim 3.0V$

(Note 9)  $V_{IN} = 0.8\sim 2.0V$ ,  $V_{CC} = 3.0V$

## ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = -40~85°C)

PARAMETER		SYMBOL	TEST CONDITION		V <sub>CC</sub> (V)	MIN.	MAX.	UNIT
Input Voltage	"H" Level	V <sub>IH</sub>			2.7~3.6	2.0	—	V
	"L" Level	V <sub>IL</sub>			2.7~3.6	—	0.8	V
Output Voltage	"H" Level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100μA	2.7~3.6	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -12μA	2.7	2.2	—	
				I <sub>OH</sub> = -18mA	3.0	2.4	—	
				I <sub>OH</sub> = -24mA	3.0	2.2	—	
	"L" Level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100μA	2.7~3.6	—	0.2	V
				I <sub>OL</sub> = 12mA	2.7	—	0.4	
				I <sub>OL</sub> = 16mA	3.0	—	0.4	
				I <sub>OL</sub> = 24mA	3.0	—	0.55	
Input Leakage Current		I <sub>IN</sub>	V <sub>IN</sub> = 0~5.5V		2.7~3.6	—	± 5.0	μA
3-State Output Off-State Current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0~5.5V		2.7~3.6	—	± 5.0	μA
Power Off Leakage Current		I <sub>OFF</sub>	V <sub>IN</sub> / V <sub>OUT</sub> = 5.5V		0	—	10.0	μA
Quiescent Supply Current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.7~3.6	—	20.0	μA
			V <sub>IN</sub> / V <sub>OUT</sub> = 3.6~5.5V		2.7~3.6	—	± 20.0	
Increase In I <sub>CC</sub> Per Input		ΔI <sub>CC</sub>	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		2.7~3.6	—	500	μA

## AC characteristics (Ta = -40~85°C)

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	MIN.	MAX.	UNIT
Propagation Delay Time (D-Q)	t <sub>pLH</sub>	(Fig.1, 2)	2.7	—	8.0	ns
	t <sub>pHL</sub>		3.3 ± 0.3	1.5	7.0	
Propagation Delay Time (LE-Q)	t <sub>pLH</sub>	(Fig.1, 2)	2.7	—	8.0	ns
	t <sub>pHL</sub>		3.3 ± 0.3	1.5	7.0	
3-State Output Enable Time	t <sub>pZL</sub>	(Fig.1, 3)	2.7	—	8.2	ns
	t <sub>pZH</sub>		3.3 ± 0.3	1.5	7.2	
3-State Output Disable Time	t <sub>pLZ</sub>	(Fig.1, 3)	2.7	—	8.2	ns
	t <sub>pHZ</sub>		3.3 ± 0.3	1.5	7.2	
Minimum Pulse Width (LE)	t <sub>w(H)</sub>	(Fig.1, 2)	2.7	4.0	—	ns
			3.3 ± 0.3	3.0	—	
Minimum Set-up Time	t <sub>s</sub>	(Fig.1, 2)	2.7	2.5	—	ns
			3.3 ± 0.3	2.5	—	
Minimum Hold Time	t <sub>h</sub>	(Fig.1, 2)	2.7	1.5	—	ns
			3.3 ± 0.3	1.5	—	
Output To Output Skew	t <sub>osLH</sub>	(Note 10)	2.7	—	—	ns
	t <sub>osHL</sub>		3.3 ± 0.3	—	1.0	

(Note 10) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

## Dynamic switching characteristics

(Ta = 25°C, Input t<sub>r</sub> = t<sub>f</sub> = 2.5ns, C<sub>L</sub> = 50pF, R<sub>L</sub> = 500Ω)

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	TYP	UNIT
Quiet Output Maximum Dynamic V <sub>OL</sub>	V <sub>OLP</sub>	V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	0.8	V
Quiet Output Minimum Dynamic V <sub>OL</sub>	V <sub>OLV</sub>	V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	0.8	V

## Capacitive characteristics (Ta = 25°C)

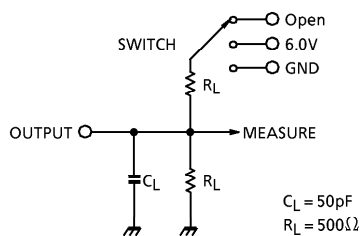
PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	TYP	UNIT
Input Capacitance	C <sub>IN</sub>	—	3.3	7	pF
Output Capacitance	C <sub>OUT</sub>		3.3	8	pF
Power Dissipation Capacitance	C <sub>PD</sub>	f <sub>IN</sub> = 10MHz (Note 11)	3.3	25	pF

(Note 11) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 16. (\text{Per bit})$$

Fig.1 Test circuit



PARAMETER	SWITCH
$t_{pLH}, t_{pHL}$	Open
$t_{pLZ}, t_{pZL}$	6.0V
$t_{pHZ}, t_{pZH}$	GND
$t_w, t_s, t_h$	Open

AC WAVEFORM

Fig.2  $t_{pLH}, t_{pHL}, t_w, t_s, t_h$

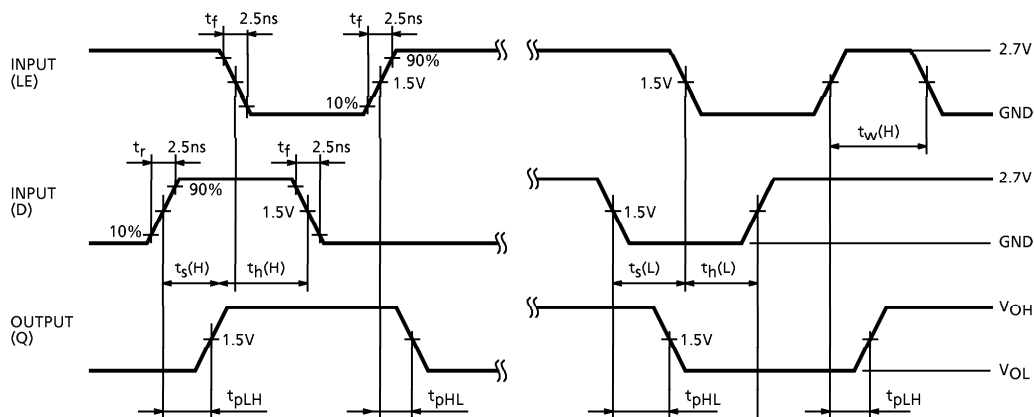
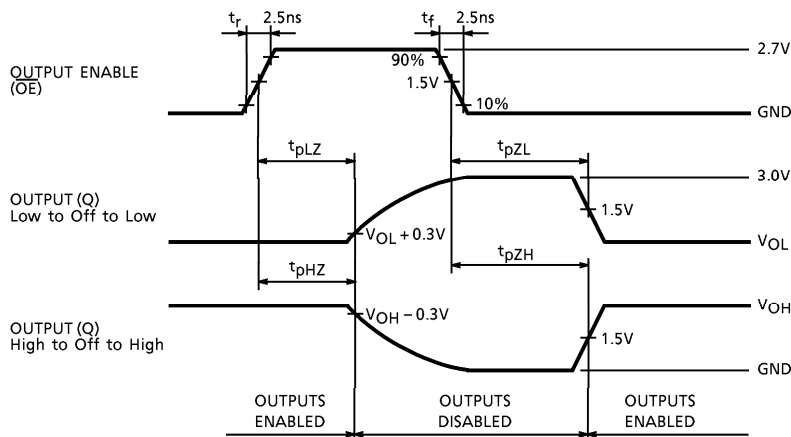


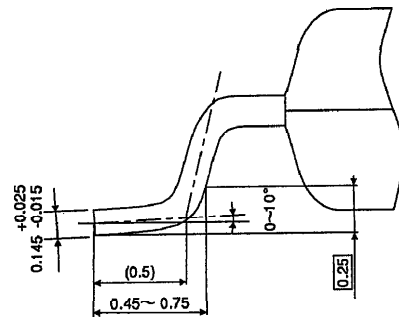
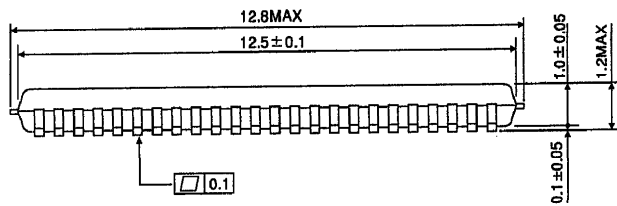
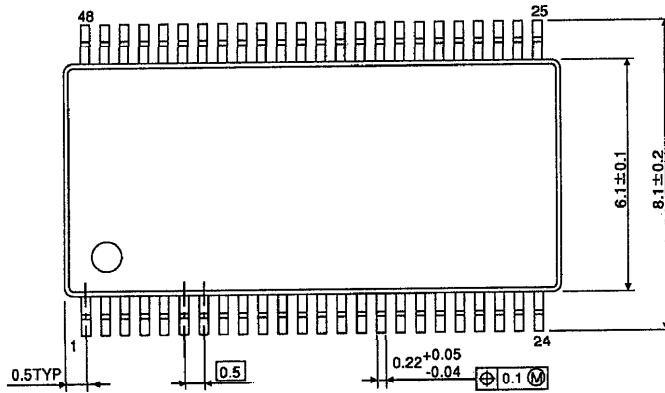
Fig.3  $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$



**OUTLINE DRAWING**

TSSOP48-P-0061-0.50

Unit : mm



Weight : 0.25g (Typ.)