TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74LCX14F,TC74LCX14FN,TC74LCX14FT,TC74LCX14FK

Low-Voltage Hex Schmitt Inverter with 5-V Tolerant Inputs and Outputs

The TC74LCX14 is a high-performance CMOS schmitt inverter. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V)  $V_{\rm CC}$  applications, but it could be used to interface to 5-V supply environment for inputs.

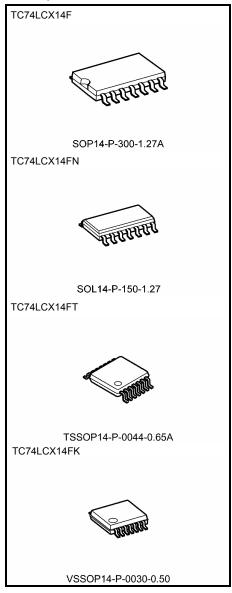
Pin configuration and function are the same as the TC74LCX04 but the inputs have hysteresis and with Schmitt trigger function, the TC74LCX14F/FN/FT can be used as a line receivers which will receive slow input signals.

All inputs are equipped with protection circuits against static discharge.

#### **Features**

- Low-voltage operation: V<sub>CC</sub> = 2.0 to 3.6 V
- High-speed operation:  $t_{pd} = 6.5 \text{ ns (max)} (V_{CC} = 3.0 \text{ to } 3.6 \text{ V})$
- Ouput current:  $|I_{OH}|/I_{OL} = 24 \text{ mA (min)} (V_{CC} = 3.0 \text{ V})$
- Latch-up performance: -500 mA
- Available in JEDEC SOP, JEITA SOP, TSSOP and VSSOP (US)
- Power-down protection provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 14 type

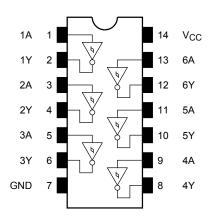
Note: xxxFN (JEDEC SOP) is not available in Japan.



Weight

SOP14-P-300-1.27A : 0.18 g (typ.) SOL14-P-150-1.27 : 0.12 g (typ.) TSSOP14-P-0044-0.65A : 0.06 g (typ.) VSSOP14-P-0030-0.50 : 0.02 g (typ.)

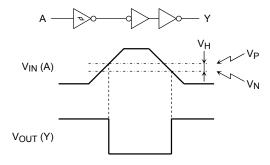
# Pin Assignment (top view)



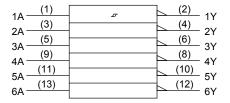
### **Truth Table**

Inputs	Outputs
Α	Y
L	Н
Н	L

# System Diagram and waveform



# **IEC Logic Symbol**





### **Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit	
Power supply voltage	V <sub>CC</sub>	-0.5 to 7.0	V	
DC input voltage	V <sub>IN</sub>	-0.5 to 7.0	V	
		-0.5 to 7.0 (Note 2)		
DC output voltage	V <sub>OUT</sub>	$-0.5$ to $V_{CC}$ + $0.5$ (Note 3)	V	
Input diode current	I <sub>IK</sub>	-50	mA	
Output diode current	lok	±50 (Note 4)	mA	
DC output current	lout	±50	mA	
Power dissipation	PD	180	mW	
DC V <sub>CC</sub> /ground current	I <sub>CC</sub> /I <sub>GND</sub>	±100	mA	
Storage temperature	T <sub>stg</sub>	-65 to 150	°C	

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2:  $V_{CC} = 0 V$ 

Note 3: High or low state. IOUT absolute maximum rating must be observed.

Note 4: Vout < GND, Vout > Vcc

### **Operating Ranges (Note 1)**

Characteristics	Symbol	Rating	Unit	
Power supply voltage	Vcc	2.0 to 3.6	V	
Tower supply voltage	VCC	1.5 to 3.6 (Note 2)	V	
Input voltage	V <sub>IN</sub>	0 to 5.5	V	
Output voltage	V <sub>OUT</sub>	0 to 5.5 (Note 3)	٧	
		0 to V <sub>CC</sub> (Note 4)	V	
Output current	la/la.	±24 (Note 5)	mA	
	I <sub>OH</sub> /I <sub>OL</sub>	±12 (Note 6)	IIIA	
Operating temperature	T <sub>opr</sub>	-40 to 85	°C	

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.

Note 2: Data retention only

Note 3:  $V_{CC} = 0 V$ 

Note 4: High or low state

Note 5:  $V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$ 

Note 6:  $V_{CC} = 2.7 \text{ to } 3.0 \text{ V}$ 



#### **Electrical Characteristics**

### DC Characteristics ( $Ta = -40 \text{ to } 85^{\circ}\text{C}$ )

Characteri	stics	Symbol	Test Condition		V <sub>CC</sub> (V)	Min	Max	Unit
	H-level	VP		_	3.0	1.2	2.2	
Threshold voltage	L-level	V <sub>N</sub>		_	3.0	0.6	1.5	V
Hysteresis voltage	1	VH		_	3.0	0.4	1.2	V
H-level		$V_{IN} = V_{IL}$	$I_{OH} = -100 \mu A$	2.7 to 3.6	V <sub>CC</sub> - 0.2	_		
	VOH		$I_{OH} = -12 \text{ mA}$	2.7	2.2	_		
		0.1		I <sub>OH</sub> = -18 mA	3.0	2.4	_	V
Output voltage  L-level				I <sub>OH</sub> = -24 mA	3.0	2.2	_	
		.,	V V	$I_{OL} = 100 \mu A$	2.7 to 3.6	_	0.2	
	Llavel			I <sub>OL</sub> = 12 mA	2.7	_	0.4	
	V <sub>OL</sub>	$V_{IN} = V_{IH}$	I <sub>OL</sub> = 16 mA	3.0	_	0.4		
			I <sub>OL</sub> = 24 mA	3.0	_	0.55		
Input leakage current I <sub>IN</sub>		I <sub>IN</sub>	V <sub>IN</sub> = 0 to 5.5 V		2.7 to 3.6	_	±5.0	μА
Power-off leakage of	urrent	I <sub>OFF</sub>	V <sub>IN</sub> /V <sub>OUT</sub> = 5.5 V		0	_	10.0	μΑ
Quiescent supply current I <sub>CC</sub>		laa	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.7 to 3.6	_	10.0	
		ICC	V <sub>IN</sub> = 3.6 to 5.5 V		2.7 to 3.6	_	±10.0	μΑ
Increase in Icc per i	nput	Δl <sub>CC</sub>	V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		2.7 to 3.6	_	500	

### AC Characteristics ( $Ta = -40 \text{ to } 85^{\circ}\text{C}$ )

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Max	Unit
Propagation delay time	t <sub>pLH</sub>	Figure 1, Figure 2	2.7	_	7.5	ns
	$t_{pHL}$		$3.3 \pm 0.3$	1.5	6.5	
Output to output skew	t <sub>osLH</sub>	(Note)	2.7	_	_	20
	t <sub>osHL</sub>	(Note)	$3.3 \pm 0.3$		1.0	ns

Note: Parameter guaranteed by design.

 $(t_{\text{OSLH}} = |t_{\text{PLHm}} - t_{\text{PLHn}}|, \, t_{\text{OSHL}} = |t_{\text{PHLm}} - t_{\text{PHLn}}|)$ 

### Dynamic Switching Characteristics (Ta = 25°C, input: $t_r$ = $t_f$ = 2.5 ns, $C_L$ = 50 pF, $R_L$ = 500 $\Omega$ )

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	0.8	V



### Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Input capacitance	C <sub>IN</sub>	_	3.3	7	pF
Output capacitance	C <sub>OUT</sub>	_	0	8	pF
Power dissipation capacitance	C <sub>PD</sub>	$f_{IN} = 10 \text{ MHz}$ (No	e) 3.3	25	pF

Note: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per gate)}$ 

#### **AC Test Circuit**

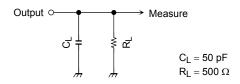


Figure 1

#### **AC Waveform**

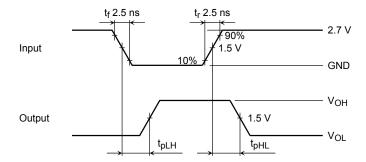
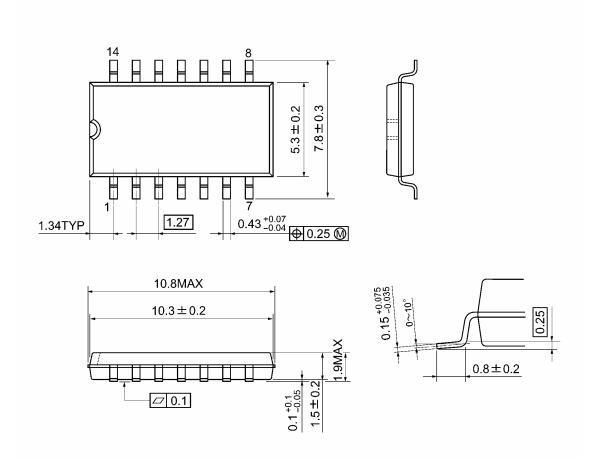


Figure 2 t<sub>pLH</sub>, t<sub>pHL</sub>

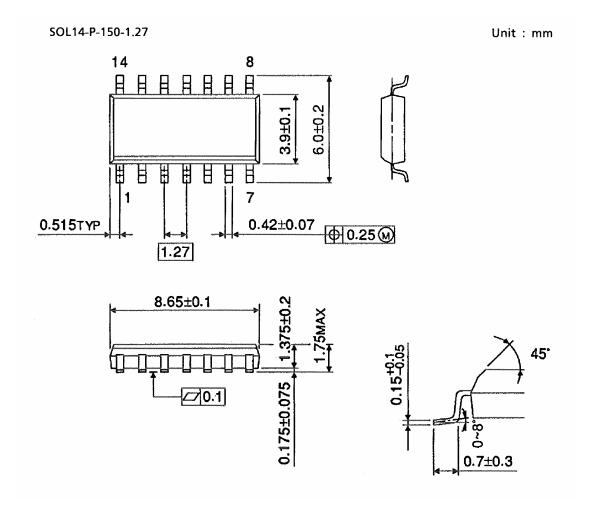
# **Package Dimensions**

SOP14-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

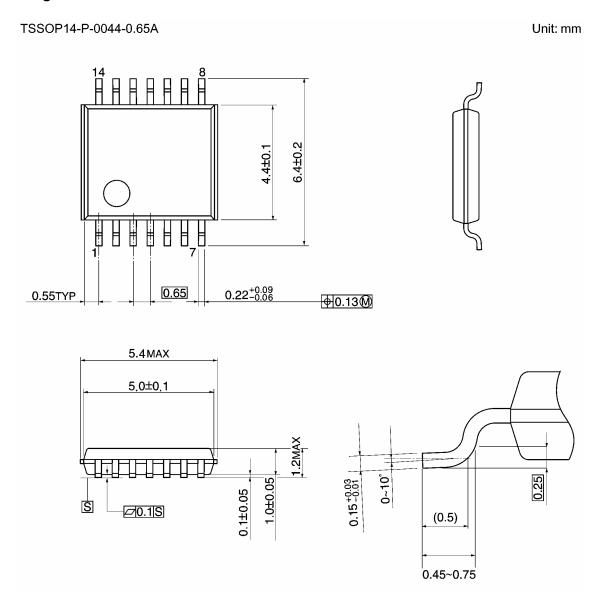
# **Package Dimensions (Note)**



Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

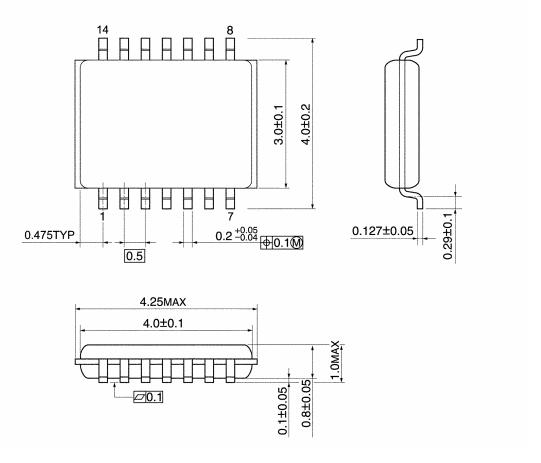
# **Package Dimensions**



Weight: 0.06 g (typ.)

# **Package Dimensions**

VSSOP14-P-0030-0.50 Unit: mm



Weight: 0.02 g (typ.)

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20070701-EN GENERAL

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