

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74LCX00F, TC74LCX00FN, TC74LCX00FT**LOW-VOLTAGE QUAD 2-INPUT NAND GATE
WITH 5V TOLERANT INPUTS AND OUTPUTS**

The TC74LCX00 is a high performance CMOS 2-INPUT NAND GATE. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

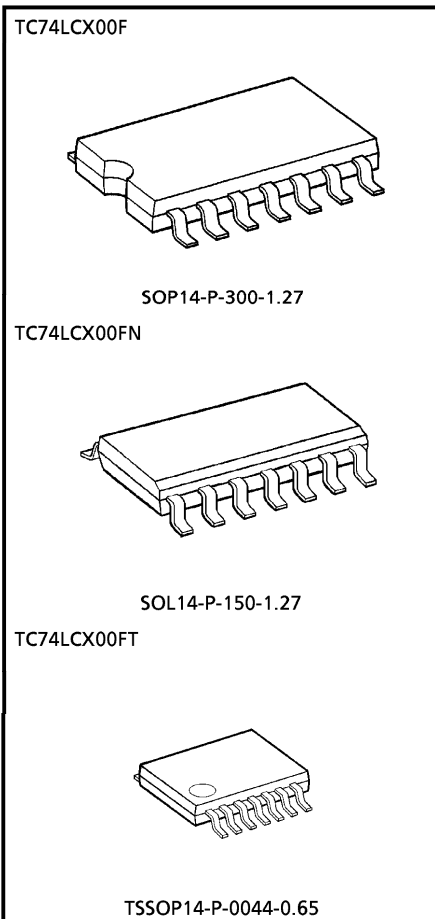
The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for inputs.

All inputs are equipped with protection circuits against static discharge.

FEATURES

- Low voltage operation : $V_{CC} = 2.0 \sim 3.6V$
- High speed operation : $t_{pd} = 5.2ns$ (Max.) at $V_{CC} = 3.0 \sim 3.6V$
- Output current : $|I_{OH}| / I_{OL} = 24mA$ (Min.) at $V_{CC} = 3.0V$
- Latch-up performance : $\pm 500mA$
- Available in JEDEC SOP, EIAJ SOP and TSSOP
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 00 type.

(Note) The JEDEC SOP (FN) is not available in Japan.

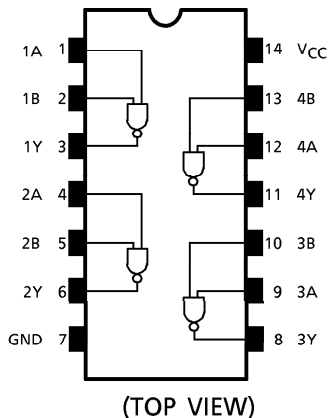


Weight
 SOP14-P-300-1.27 : 0.18g (Typ.)
 SOL14-P-150-1.27 : 0.12g (Typ.)
 TSSOP14-P-0044-0.65 : 0.06g (Typ.)

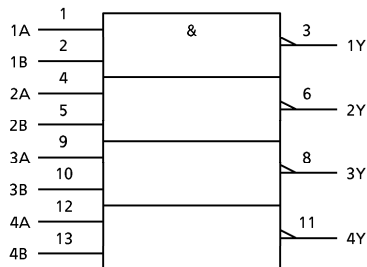
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PIN CONNECTION



IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	- 0.5~7.0	V
DC Input Voltage	V_{IN}	- 0.5~7.0	V
DC Output Voltage	V_{OUT}	- 0.5~7.0 (Note 1)	V
		- 0.5~ $V_{CC} + 0.5$ (Note 2)	
Input Diode Current	I_{IK}	- 50	mA
Output Diode Current	I_{OK}	± 50 (Note 3)	mA
DC Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	180	mW
DC V_{CC} /Ground Current	I_{CC}/I_{GND}	± 100	mA
Storage Temperature	T_{stg}	- 65~150	$^{\circ}C$

(Note 1) $V_{CC} = 0V$

(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.

(Note 3) $V_{OUT} < GND, V_{OUT} > V_{CC}$

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RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
		1.5~3.6 (Note 4)	
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5 (Note 5)	V
		0~ V_{CC} (Note 6)	
Output Current	I_{OH}/I_{OL}	± 24 (Note 7)	mA
		± 12 (Note 8)	
Operating Temperature	T_{opr}	-40~85	°C
Input Rise And Fall Time	dt/dv	0~10 (Note 9)	ns/V

(Note 4) Data Retention Only

(Note 5) $V_{CC} = 0V$

(Note 6) High or Low State

(Note 7) $V_{CC} = 3.0\sim 3.6V$ (Note 8) $V_{CC} = 2.7\sim 3.0V$ (Note 9) $V_{IN} = 0.8\sim 2.0V$, $V_{CC} = 3.0V$

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS ($T_a = -40\sim 85^\circ C$)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}						
	"L" Level	V_{IL}			2.7~3.6	—	0.8	V
Output Voltage	"H" Level	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -100\mu A$	2.7~3.6	$V_{CC} - 0.2$	—	V
				$I_{OH} = -12mA$	2.7	2.2	—	
				$I_{OH} = -18mA$	3.0	2.4	—	
				$I_{OH} = -24mA$	3.0	2.2	—	
	"L" Level	V_{OL}	$V_{IN} = V_{IH}$	$I_{OL} = 100\mu A$	2.7~3.6	—	0.2	V
				$I_{OL} = 12mA$	2.7	—	0.4	
				$I_{OL} = 16mA$	3.0	—	0.4	
				$I_{OL} = 24mA$	3.0	—	0.55	
Input Leakage Current	I_{IN}	$V_{IN} = 0\sim 5.5V$		2.7~3.6	—	± 5.0	μA	
Power Off Leakage Current	I_{OFF}	$V_{IN}/V_{OUT} = 5.5V$		0	—	10.0	μA	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } GND$		2.7~3.6	—	10.0	μA	
		$V_{IN}/V_{OUT} = 3.6\sim 5.5V$		2.7~3.6	—	± 10.0		
Increase In I_{CC} Per Input	ΔI_{CC}	$V_{IH} = V_{CC} - 0.6V$		2.7~3.6	—	500	μA	

AC CHARACTERISTICS (Ta = -40~85°C)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	MIN.	MAX.	UNIT
Propagation Delay Time	t _{pLH}	(Fig.1, 2)	2.7	—	6.0	ns
	t _{pHL}		3.3 ± 0.3	1.5	5.2	
Output To Output Skew	t _{osLH}	(Note 10)	2.7	—	—	ns
	t _{osHL}		3.3 ± 0.3	—	1.0	

(Note 10) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

DYNAMIC SWITCHING CHARACTERISTICS (Ta = 25°C, Input t_r = t_f = 2.5ns, C_L = 50pF, R_L = 500Ω)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V

CAPACITIVE CHARACTERISTICS (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Input Capacitance	C _{IN}	—	3.3	7	pF
Output Capacitance	C _{OUT}		0	8	pF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10MHz (Note 11)	3.3	25	pF

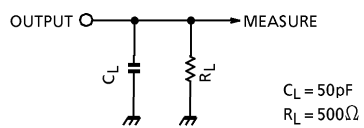
(Note 11) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (Per gate)}$$

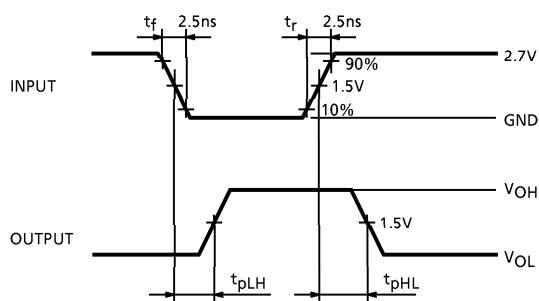
TEST CIRCUIT

Fig.1



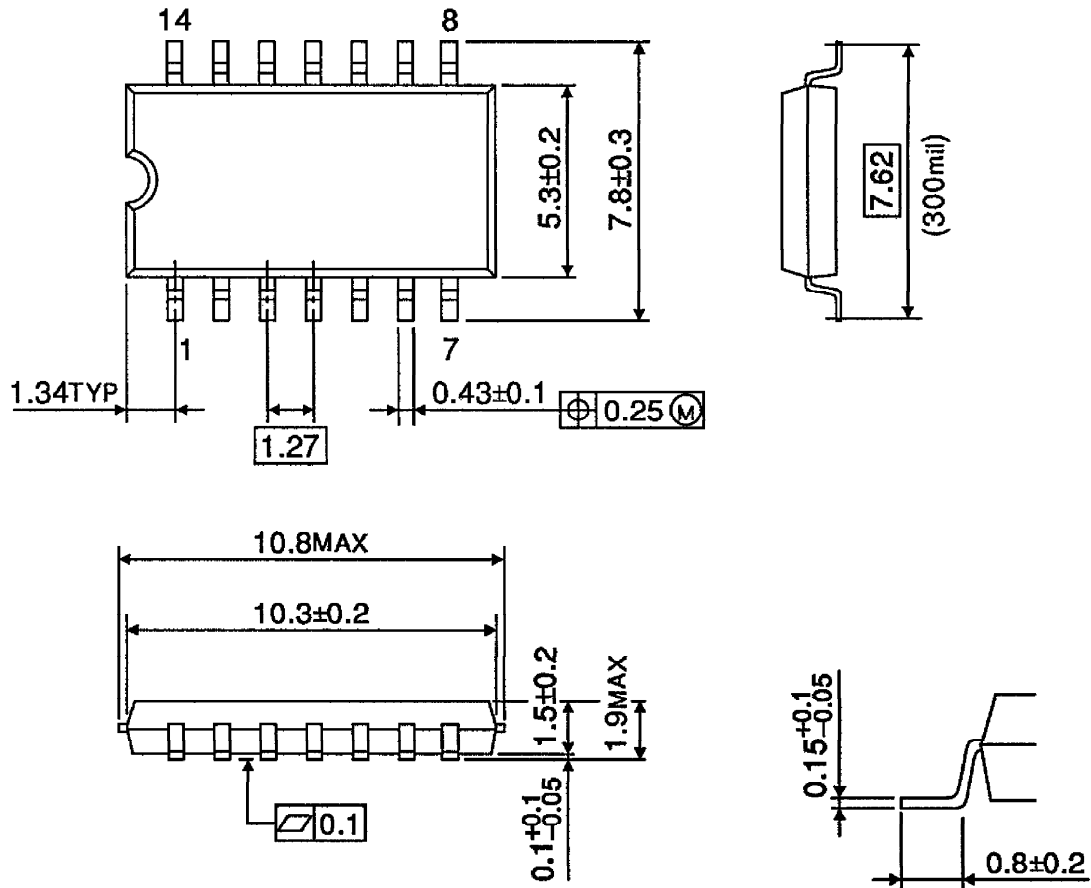
AC WAVEFORM

Fig.2 t_{pLH} , t_{pHL}



OUTLINE DRAWING
SOP14-P-300-1.27

Unit : mm

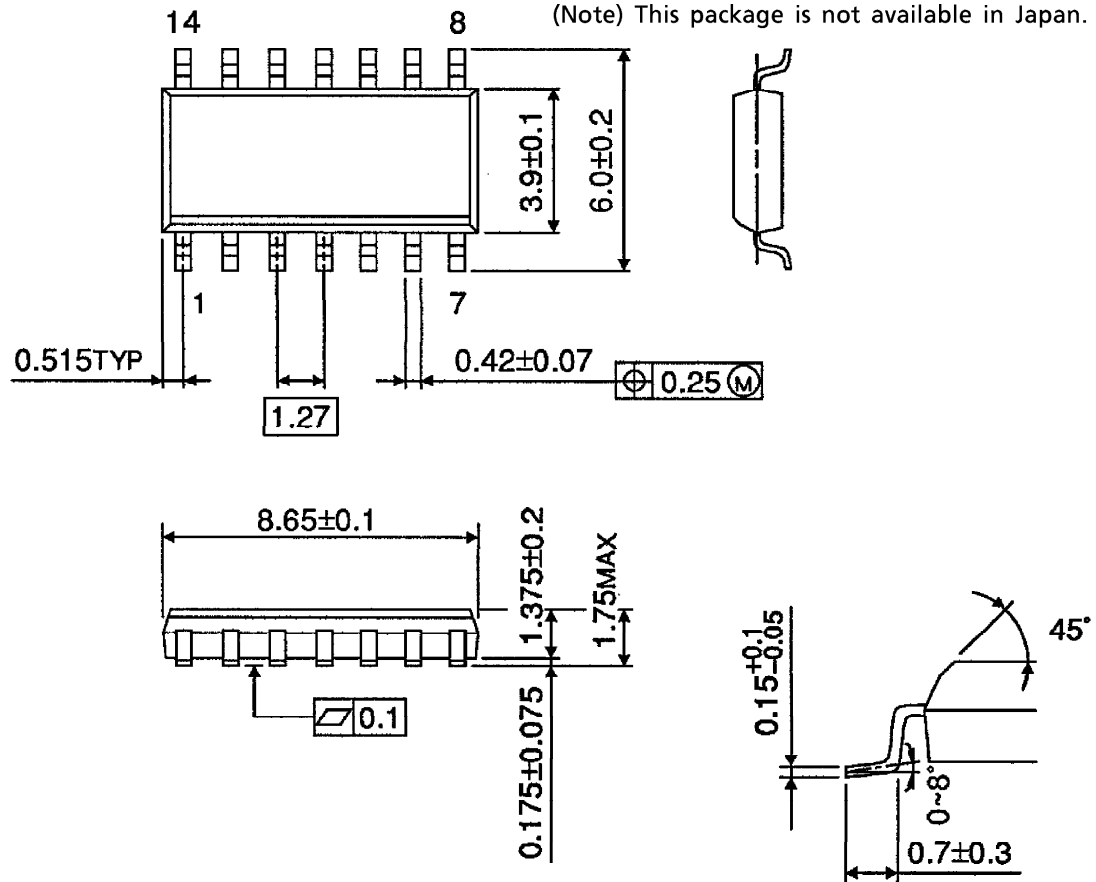


Weight : 0.18g (Typ.)

OUTLINE DRAWING
SOL14-P-150-1.27

Unit : mm

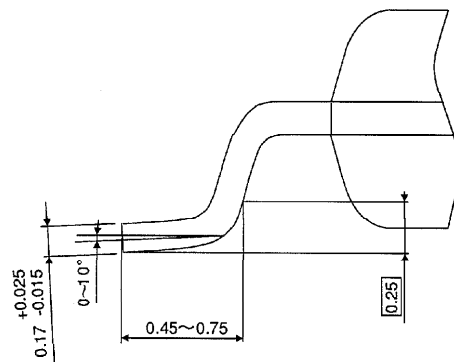
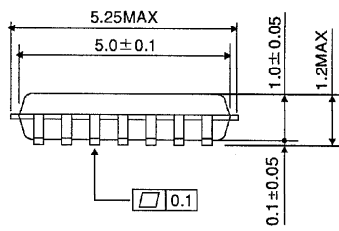
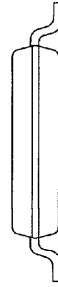
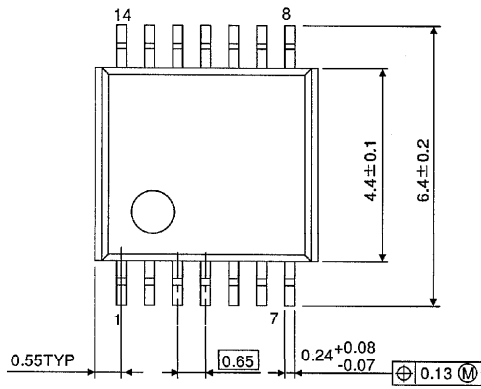
(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

OUTLINE DRAWING
TSSOP14-P-0044-0.65

Unit : mm



Weight : 0.06g (Typ.)