SC1480A
DDR and DDR2 Memory VTT Power Supply Controller

POWER MANAGEMENT

Description

The SC1480A is a single output, constant on-time synchronous-buck, pseudo fixed frequency, PWM controller intended for use in notebook computers and other battery operated portable devices. Features include high efficiency and fast dynamic response with no minimum on time, a reference input and a buffered REFOUT pin capable of sourcing 3mA. The excellent transient response means that SC1480A based solutions will require less output capacitance than competing fixed frequency converters.

The frequency is constant until a step in load or line voltage occurs, at which time the pulse density and frequency will increase or decrease to counter the change in output or input voltage. After the transient event, the controller frequency will return to steady state operation.

The SC1480A incorporates two power-reducing states, standby and shutdown. In standby mode, the switcher output is shutdown but the buffered reference output stays up, reducing quiescent current to a low 125µA. This is particularly useful for reducing battery draw in systems which implement a suspend-to-RAM (S3) state. The SC1480A can be completely shut down, drawing less than 10µA.

The integrated gate drivers feature adaptive shoot-through protection and soft switching. Additional features include cycle-by-cycle current limit, digital soft-start, overvoltage and under-voltage protection, and a PGOOD output.

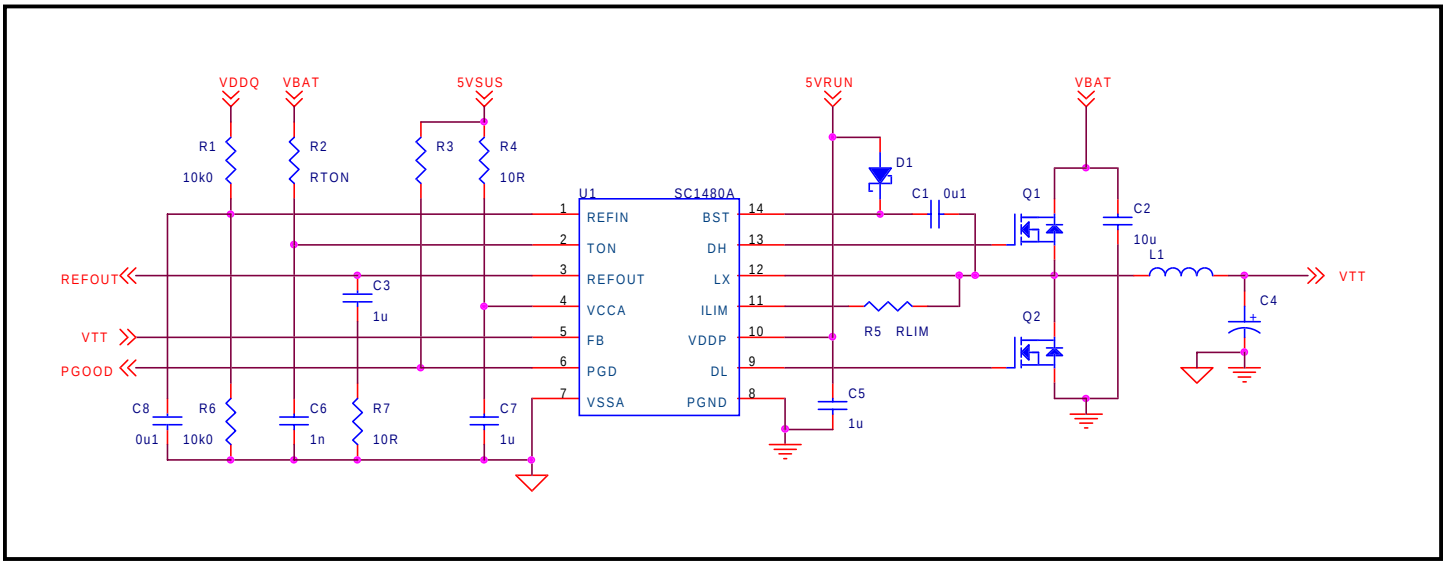
Features

- Compatible with DDR & DDR2 memory power requirements
- Constant on-time for fast dynamic response
- Programmable VOUT based on external reference
- VBAT range = 1.8V – 25V
- DC current sense using low-side RDS(ON) sensing or sense resistor
- 3mA reference output buffer
- Low power S3 state
- Resistor programmable frequency
- Cycle-by-cycle current limit
- Digital soft start
- Output current source-sink capability
- Overvoltage/under-voltage fault protection and PGOOD output
- Under 10uA typical shutdown current
- Low quiescent power dissipation
- 14 Lead TSSOP
- Industrial temperature range
- Integrated gate drivers with soft switching
- Efficiency >80%

Applications

- Notebook computers
- CPU I/O supplies
- Handheld terminals and PDAs
- LCD monitors
- Network power supplies

Typical Application Circuit



Absolute Maximum Ratings(3)

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Pin Combination	Symbol	Maximum	Units
TON to VSSA		-0.3 to +25.0	V
DH, BST to PGND		-0.3 to +30.0	V
LX to PGND		-2.0 to +25.0	V
VSSA to PGND		-0.3 to +0.3	V
BST to LX		-0.3 to +6.0	V
DL, ILIM, VDDP to PGND		-0.3 to +6.0	V
FB, PGD, REFIN, REFOUT, VCCA to VSSA		-0.3 to +6.0	V
VCCA to FB, PGD, REFIN, REFOUT		-0.3 to +6.0	V
Thermal Resistance, Junction to Ambient(4)	θ_{JA}	100	°C/W
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C

Electrical Characteristics

Test Conditions: V_{BAT} = 2.5V, REFIN = 1.25, VCCA = VDDP = 5.0V, V_{OUT} = 1.25V, R_{TON} = 1MΩ

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Input Supplies							
VCCA Input Voltage			5.0		4.5	5.5	V
VDDP Input Voltage			5.0		4.5	5.5	V
VBAT Input Voltage				25			V
VDDP Operating Current	FB > regulation point, I_{LOAD} = 0A		75			160	µA
VCCA Operating Current	FB > regulation point, I_{LOAD} = 0A		700			1100	µA
VCCA Standby Current	VDDP < VDDP UV Threshold No Load On REFOUT		125				µA
TON Operating Current	R_{TON} = 1MΩ, V_{BAT} = 25V		24				µA
REFIN Bias Current	REFIN = 1.25V					1	µA
Shutdown Current	REFIN		0			1	µA
(REFIN = 0V)	VCCA		5			10	µA
	VDDP		5			10	µA
	TON, V_{BAT} = 25V		0			1	µA

Electrical Characteristics Cont.

Test Conditions: V_{BAT} = 2.5V, REFIN = 1.25, VCCA = VDDP = 5.0V, V_{OUT} = 1.25V, R_{TON} = 1MΩ

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Controller							
Error Comparator Threshold (FB Turn-on Threshold) (1)	VCCA = 4.5V to 5.5V		REFOUT		REFOUT -10	REFOUT +10	mV
On-Time	R_{TON} = 1MΩ		1660		1411	1909	ns
	R_{TON} = 500kΩ		913		776	1050	ns
Minimum Off Time			400			550	ns
FB Input Resistance			500				kΩ
Over-Current Sensing							
ILIM Sink Current	DL high		10		9	11	µA
Current Comparator Offset	PGND - ILIM				-10	+10	mV
Reference Buffer							
REFOUT Source Current					3		mA
REFIN Enable Threshold	REFIN rising		0.50			0.60	V
REFIN Enable Hysteresis			30				mV
REFOUT DC Accuracy	No load, REFIN = 1.25V	1.240		1.260	1.238	1.262	mV
Fault Protection							
Current Limit (Positive) (2)	PGND-LX, R_{ILIM} = 5kΩ		50		35	65	mV
	PGND-LX, R_{ILIM} = 10kΩ		100		80	120	mV
	PGND-LX, R_{ILIM} = 20kΩ		200		170	230	mV
Current Limit (Negative)	PGND-LX		-125		-160	-90	mV
Output Under-Voltage Fault	With respect to REFOUT		-20		-28	-15	%
Output Over-Voltage Fault	With respect to REFOUT		+10		+8	+12	%
Over-Voltage Fault Delay	FB forced above OV threshold		5				µs
PGD Low Output Voltage	Sink 1mA					0.4	V
PGD Leakage Current	FB in regulation, PGD = 5V					1	µA
PGD UV Threshold	With respect to REFOUT		-10		-15	-8	%

Electrical Characteristics Cont.

Test Conditions: V_{BAT} = 2.5V, REFIN = 1.25, VCCA = VDDP = 5.0V, V_{OUT} = 1.25V, R_{TON} = 1MΩ

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Fault Protection (Cont.)							
PGD Fault Delay	FB forced outside PGD window		5				µs
VCCA Under Voltage Threshold	Falling (100mV hysteresis)		4.0		3.7	4.3	V
VDDP Under Voltage Threshold	Falling		3.5				V
VDDP Under Voltage Hysteresis			250				mV
Over Temperature Lockout	10°C Hysteresis		165				C
Soft Start							
Soft-Start Ramp Time	REFIN high to PGD high		440				clks(5)
Under-Voltage Blank Time	REFIN high to UV high		440				clks(5)
Gate Drivers							
Shoot-Through Delay(6)	DH or DL rising		30				ns
DL Pull-Down Resistance	DL low		0.8			1.6	Ω
DL Pull-Up Resistance	DL high		2			4	Ω
DH Pull-Down Resistance	DH low, BST - LX = 5V		2			4	Ω
DH Pull-Up Resistance(7)	DH high, BST - LX = 5V		2			4	Ω
DL Sink Current	V_{DL} = 2.5V		3.1				A
DL Source Current	V_{DL} = 2.5V		1.3				A
DH Sink/Source Current	V_{DH} = 2.5V		1.3				A

Notes:

(1) The output voltage will have a DC regulation level higher than the error-comparator threshold by 50% of the ripple voltage.

(2) Using a current sense resistor, this measurement relates to PGND minus the voltage of the source on the low-side MOSFET.

(3) This device is ESD sensitive. Use of ESD handling precautions is required.

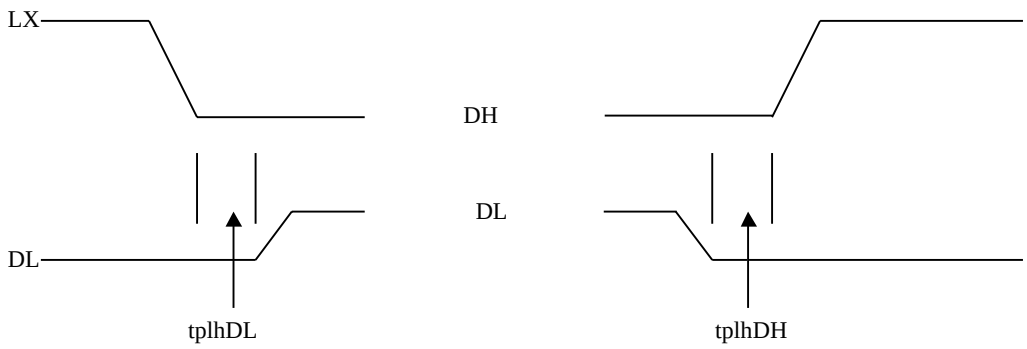
(4) Measured in accordance with JESD51-1, JESD51-2 and JESD51-7.

(5) clks = switching cycles.

(6) Guaranteed by design. Please see Shoot-Through Delay Timing Diagram on Page 5.

(7) Semtech's SmartDriver™ FET drive first pulls DH high with a pull-up resistance of 10Ω (typ.) until LX = 1.5V (typ.). At this point, an additional pull-up device is activated, reducing the resistance to 2Ω (typ.).

Shoot-Through Delay Timing Diagram



Block Diagram

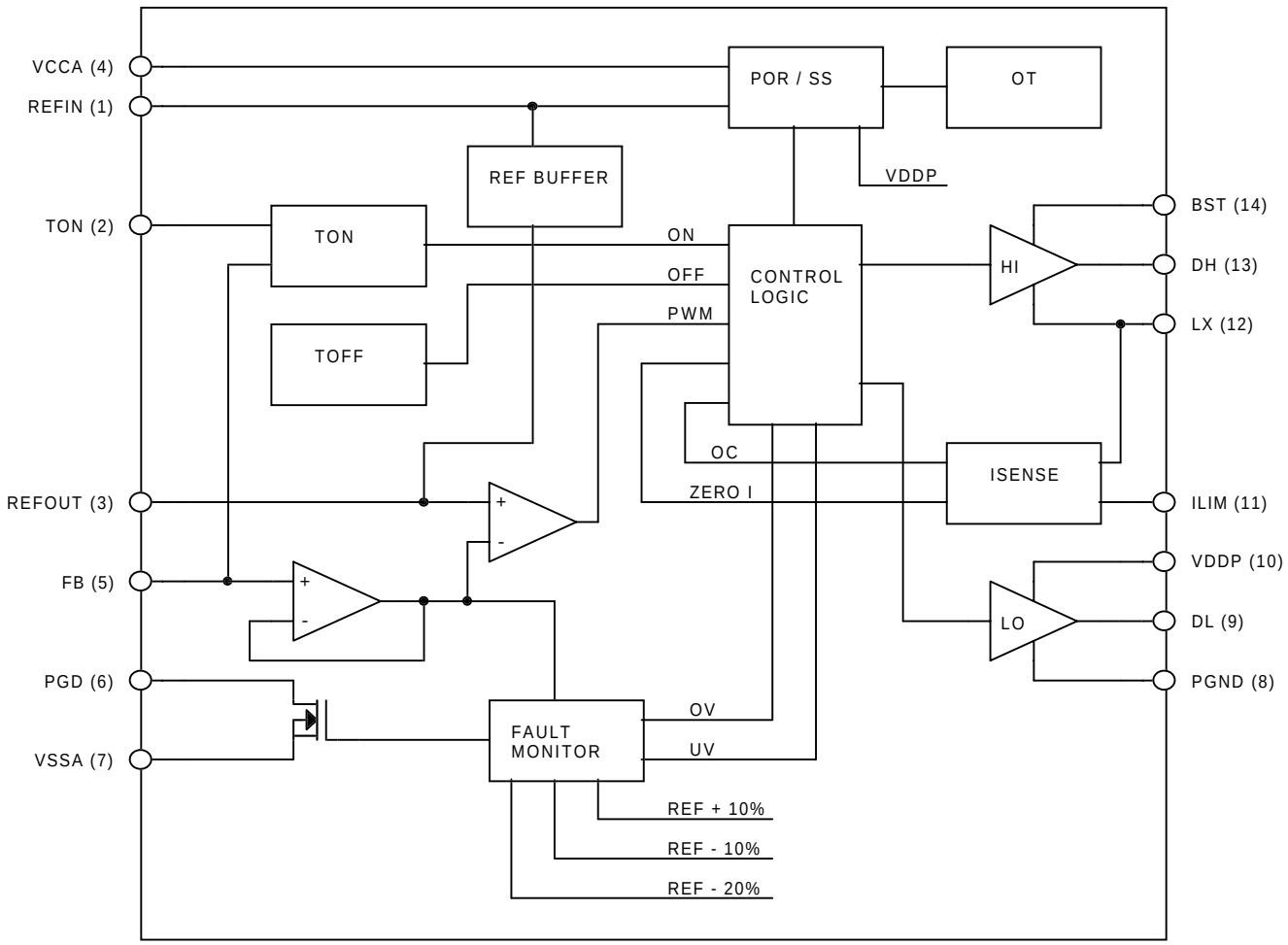
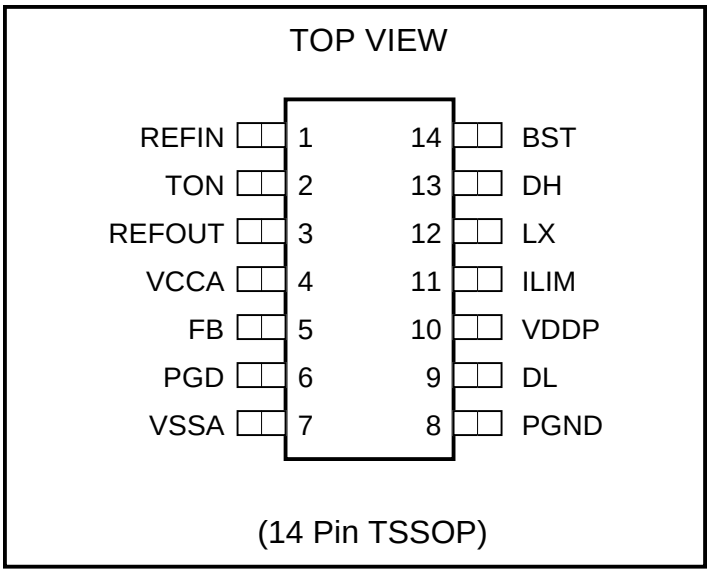


FIGURE 1: Block Diagram

Pin Configuration



Ordering Information

Device [1]	Package
SC1480AITSTRT[2]	TSSOP-14
SC1480AEVB	Evaluation Board

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE, RoHS and J-STD-020B compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	REFIN	Reference input. A 10kOhm + 10kOhm resistor divider from VDDQ to VSSA sets this voltage. A 0.1µF input filter capacitor is recommended.
2	TON	This pin is used to sense VBAT through a pull-up resistor, RTON, and to set the top MOSFET on-time. Bypass this pin with a 1nF ceramic capacitor to VSSA.
3	REFOUT	Buffered REFIN output. The switching controller regulates to this voltage. Connect a series 10 Ohm and 1µF from this pin to VSSA.
4	VCCA	Supply voltage input for the analog supply. Use a 10 Ohm/1µF RC filter from 5VSUS to VSSA.
5	FB	Feedback input. Connect to the output at the output capacitor.
6	PGD	Power Good open drain NMOS output. Goes high after a fixed clock cycle delay (440 cycles) following power up.
7	VSSA	Ground reference for analog circuitry. Connect to bottom of the output capacitor(s).
8	PGND	Power ground.
9	DL	Gate drive output for the low side MOSFET switch.
10	VDDP	+5V supply voltage input for the gate drivers. Decouple this pin with a 1µF ceramic capacitor to PGND.
11	ILIM	Current limit input pin. Connect to drain of low-side MOSFET for RDS(ON) sensing or the source for resistor sensing through a threshold sensing resistor.
12	LX	Phase node (junction of top and bottom MOSFETs and the output inductor) connection.
13	DH	Gate drive output for the high side MOSFET switch.
14	BST	Boost capacitor connection for the high side gate drive.

Applications Information

+5V Bias Supplies

The SC1480A requires an external +5V bias supply in addition to the battery. If stand-alone capability is required, the +5V supply can be generated with an external linear regulator such as the Semtech LP2951.

For optimal operation, the controller has its own ground reference, VSSA, which should be tied by a single trace to PGND at the negative terminal of the output capacitor (see Layout Guidelines). All external components referenced to VSSA in the Typical Applications Circuit on Page 1 should be connected to VSSA. The supply decoupling capacitor should be tied directly between the VCCA and VSSA pins. A 10Ω resistor should be used to decouple VCCA from the main 5V supply, which may or may not be the same 5V supply that powers VDDP. PGND can then be a separate plane which is not used for routing traces. All PGND connections are connected directly to the ground plane with special attention given to avoiding indirect connections which may create ground loops. As mentioned above, VSSA must be connected to the PGND plane at the negative terminal of the output capacitor(s) only. The VDDP input provides power to the upper and lower gate drivers. A decoupling capacitor is required. No series resistor between VDDP and 5V is required. See layout guidelines for more details.

Pseudo-fixed Frequency Constant On-Time PWM Controller

The PWM control architecture consists of a constant on-time, pseudo fixed frequency PWM controller (see Figure 1, SC1480A Block Diagram). The output ripple voltage developed across the output filter capacitor's ESR provides the PWM ramp signal eliminating the need for a current sense resistor. The high-side switch on-time is determined by a one-shot whose period is directly proportional to output voltage and inversely proportional to input voltage. A second one-shot sets the minimum off-time which is typically 400ns.

On-Time One-Shot (t_{ON})

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage-proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to VOUT, thereby making the on-time of the high-side switch directly proportional to output voltage and inversely proportional to input voltage. This implementation results in a nearly constant switching frequency without the need for a clock generator.
For VOUT < 3.3V:

$$t_{ON} = 3.3x10^{-12} \bullet (R_{TON} + 37x10^{3}) \bullet \left(\frac{V_{OUT}}{V_{BAT}} \right) + 50ns$$

R_{TON} is a resistor connected from the input supply (VBAT) to the TON pin. Due to the high impedance of this resistor, the TON pin should always be bypassed to VSSA using a 1nF ceramic capacitor.

Enabling

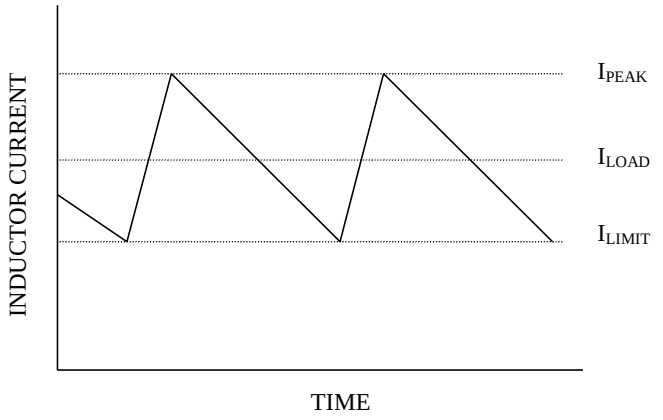
REFIN enables the REFOUT buffered reference (assuming VCCA is present) and VDDP enables the VTT output (assuming VCCA and REFIN are present). It is usual to use a resistor divider from VDDQ to generate REFIN, so if VDDQ is not present, neither REFOUT nor VTT will be present. For S3 mode, VDDP may be removed, disabling VTT but leaving REFOUT present.

Current Limit Circuit

Current limiting of the SC1480A can be accomplished in two ways. The on-state resistance of the low-side MOSFETs can be used as the current sensing element or sense resistors in series with the low-side sources can be used if greater accuracy is desired. $R_{DS(ON)}$ sensing is more efficient and less expensive. In both cases, the R_{ILIM} resistors between the ILIM pin and LX pin set the over current threshold. This resistor R_{ILIM} is connected to a 10µA current source within the SC1480A which is turned on when the low side MOSFET turns on. When the voltage drop across the sense resistor or low side MOSFET equals the voltage across the RILIM resisor, positive current limit will activate. The high side MOSFET will not be turned on until the voltage drop across the sense element (resistor or MOSFET) falls below the voltage across the R_{ILIM} resistor. In an extreme over-current situation, the top MOSFET will never turn back on and eventually the part will latch off due to output undervoltage (see Output Undervoltage Protection).

Applications Information (Cont.)

The current sensing circuit actually regulates the inductor valley current (see Figure 2). This means that if the current limit is set to 3A, the peak current through the inductor would be 3A plus the peak ripple current, and the average current through the inductor would be 3A plus 1/2 the peak-to-peak ripple current. The equations for setting the valley current and calculating the average current through the inductor are shown below:



Valley Current-Limit Threshold Point

Figure 2: Valley Current Limiting

The equation for the current limit threshold is as follows:

$$I_{LIMIT} = 10e^{-6} \bullet \frac{R_{ILIM}}{R_{SENSE}} A$$

Where (referring to Figure 3 on Page 14) R_{ILIM} is R5 and R_{SENSE} is the $R_{DS(ON)}$ of the bottom FET of Q1.

For resistor sensing, a sense resistor is placed between the source of the bottom FET of Q1 and PGND. The current through the source sense resistor develops a voltage that opposes the voltage developed across R_{ILIM}. When the voltage developed across the R_{SENSE} resistor reaches the voltage drop across R_{ILIM}, a positive over-current exists and the high side MOSFET will not be allowed to turn on. When using an external sense resistor R_{SENSE} is the resistance of the sense resistor.

The current limit circuitry also protects against negative over-current (i.e. when the current is flowing from the load to PGND through the inductor and bottom MOSFET). In this case, when the bottom MOSFET is turned on, the phase node, LX, will be higher than PGND initially. The SC1480A monitors the voltage at LX, and if it is greater than a set threshold voltage of 125mV (nom.) the bottom MOSFET is turned off. The device then waits for approximately 2µs and then DL goes high for 300ns (typ.) once more to sense the current. This repeats until either the over-current condition goes away or the part latches off due to output overvoltage (see Output Overvoltage Protection).

Power Good Output (VTT)

The ower good is an open-drain output and requires a pull-up resistor. When the output voltage is 10% above or below its set voltage (REFOUT), PGD gets pulled low. It is held low until the output voltage returns to within 10% of the output set voltage. PGD is also held low during start-up and will not be allowed to transition high until soft start is over (440 switching cycles) and the output reaches 90% of its set voltage. There is a 5µs delay built into the PGD circuitry to prevent false transitions.

Output Overvoltage Protection (VTT)

When the output exceeds 10% of the its set voltage (REFOUT) the low-side MOSFET is latched on. It stays latched on and the controller is latched off until reset (see below). There is a 5µs delay built into the OV protection circuit to prevent false transitions. Note: to reset VTT from any fault, VCCA or REFIN must be toggled.

Output Undervoltage Protection (VTT)

When the output is 20% below its set voltage (REFOUT) the output is latched in a tri-stated condition. It stays latched and the controller is latched off until reset (see below). There is a 5µs delay built into the UV protection circuit to prevent false transitions. Note: to reset VTT from a any fault, VCCA or REFIN must be toggled.

POR, UVLO and Softstart

An internal power-on reset (POR) occurs when VCCA exceeds 3V, starting up the internal biasing. VCCA undervoltage lockout (UVLO) circuitry inhibits switching and also inhibits the REFOUT buffer. When VCCA rises above 4.2V, the VCCA UVLO circuitry enables the REFOUT buffer, resets the fault latch and soft start timer, and

Applications Information (Cont.)

allows switching to occur, if enabled (see below). When REFIN rises above the REFIN threshold, REFOUT will start to rise. The switching controller is enabled by two things: REFIN being greater than the REFIN threshold **and** VDDP being greater than the VDDP UVLO of 3.3V, above which switching will commence (assuming VCCA is present). Switching always starts with DL to charge up the BST capacitor. With the softstart circuit (automatically) enabled, the SC1480A will progressively limit the VTT output current (by limiting the current out of the ILIM pin) over a predetermined time period of 440 switching cycles.

The ramp occurs in four steps:
1) 110 cycles at 25% ILIM with double minimum off-time
2) 110 cycles at 50% ILIM with normal minimum off-time
3) 110 cycles at 75% ILIM with normal minimum off-time
4) 110 cycles at 100% ILIM with normal minimum off-time. At this point the output undervoltage and power good circuitry is enabled.

If VDDP falls below 3.5V (nom.) the VTT regulator will shut down. If REFIN falls below the REFIN threshold, REFOUT and VTT will shut down. There is 100mV of hysteresis built into the VCCA UVLO circuit and when VCCA falls to 4.1V (nom.) the output drivers are shut down and tristated and the REFOUT buffer shut down and disabled.

MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is fully off (below ~1V). Conversely, it monitors the phase node, LX, to determine the state of the high side MOSFET, and prevents the low-side MOSFET from turning on until DH is fully off (LX below ~1V). Be sure there is low resistance and low inductance between the DH and DL outputs to the gate of each MOSFET.

DDR Reference Buffer

The reference buffer is capable of driving 3mA and sinking 25µA. Since the output is class A, if additional sinking is required an external pulldown resistor can be added. Make sure that the ground side of this pulldown is tied to VSSA. As with most opamps, a small resistor is required when driving a capacitive load. To ensure stability use either a 10Ω resistor in series with a 1µF capacitor or a 100Ω resistor in series with a 0.1µF capacitor from REFOUT to VSSA.

Since it is possible to have as much as 10µF to 20µF of capacitance at the memory socket or on-board the DIMMs, it is recommended that a 0Ω resistor is placed between REFOUT and the DIMM sockets. This allows the addition of extra resistance between REFOUT and the DIMMs to avoid spurious OVP at startup, which can occur if REFOUT rises really slowly and VTT overshoots it. The extra resistance allows REFOUT to rise faster, avoiding this issue.

REFIN should also be filtered so that VDDQ ripple does not appear at the REFIN pin. If a resistor divider is used to create REFIN from VDDQ, then a 0.1µF capacitor from REFIN to VSSA will provide adequate filtering.

VTT Dropout Performance

The output voltage adjust range for continuous-conduction operation is limited by the fixed 550ns (maximum) minimum off-time one-shot. For best dropout performance, use the slowest on-time setting of 200kHz. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times. The IC duty-factor limitation is given by:

$$DUTY = \frac{t_{ON(MIN)}}{t_{ON(MIN)} + t_{OFF(MAX)}}$$

Be sure to include inductor resistance and MOSFET on-state voltage drops when performing worst-case dropout duty-factor calculations.

SC1480A System DC Accuracy (VTT)

Two IC parameters effect system DC accuracy, the error comparator offset voltage, and the switching frequency variation with line and load. The SC1480A regulates to the REFOUT voltage not the REFIN voltage. Since DDR specifications are written with respect to REFOUT, the offset of the reference buffer does not create a regulation error.

The error comparator offset does not drift significantly with supply and temperature. Thus, the error comparator contributes 1% or less to DC system inaccuracy.

Applications Information (Cont.)

The on pulse in the SC1480A is calculated to give a pseudo fixed frequency. Nevertheless, some frequency variation with line and load can be expected. This variation changes the output ripple voltage. Because constant on regulators regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if REFOUT=0.9V, then the valley of the output ripple will be 0.9V. If the ripple is 20mV with VBAT = 6V, then the DC output voltage will be 0.91V. If the ripple is 30mV with VBAT = 25V, then the DC output voltage will be 0.915V.

The output inductor value may change with current. This will change the output ripple and thus the DC output voltage. It will not change the frequency.

Switching frequency variation with load can be minimized by choosing MOSFETs with lower $R_{DS(ON)}$. High $R_{DS(ON)}$ MOSFETs will cause the switching frequency to increase as the load current increases. This will reduce the ripple and thus the DC output voltage.

Input (VBAT) Supply Selection

The SC1480A can be configured so that VTT is generated directly from the battery. Alternatively, VTT can be generated from VDDQ. Since the battery configuration generally yields better overall efficiency and performance, the recommended method is to generate VTT from the battery.

Design Procedure

Prior to designing an output and making component selections, it is necessary to determine the input voltage range and the output voltage specifications. For purposes of demonstrating the procedure the VTT output for the schematic in Figure 3 on Page 14 will be designed.

The maximum input voltage ($V_{BAT(MAX)}$) is determined by the highest AC adaptor voltage. The minimum input voltage ($V_{BAT(MIN)}$) is determined by the lowest battery voltage after accounting for voltage drops due to connectors, fuses and battery selector switches. For the purposes of this design example we will use a V_{BAT} range of 8V to 20V.
Four parameters are needed for the output:
1) nominal output voltage, V_{OUT} (for DDR2 this is 0.9V)
2) static (or DC) tolerance, TOL_{ST} (for DDR2 this is +/-40mV, or 4.44%, we will design for 4%)
3) transient tolerance, TOL_{TR} and size of transient (for DDR2 this is undefined, so assume +/-8% for purposes of this demonstration).
4) maximum output current, I_{OUT} (we will design for 3A)

Switching frequency determines the trade-off between size and efficiency. Increased frequency increases the switching losses in the MOSFETs, since losses are a function of VIN^2. Knowing the maximum input voltage and budget for MOSFET switches usually dictates where the design ends up. A default R_{tON} value of 715kΩ is suggested as a starting point, but this is not set in stone. The first thing to do is to calculate the on-time, t_{ON}, at $V_{BAT(MIN)}$ and $V_{BAT(MAX)}$, since this depends only upon V_{BAT}, V_{OUT} and R_{tON}. For V_{OUT} < 3.3V:

$$t_{ON\_VBAT(MIN)} = \left[3.3 \bullet 10^{-12} \bullet \left(R_{tON} + 37 \bullet 10^{3}\right) \bullet \frac{V_{OUT}}{V_{BAT(MIN)}}\right] + 50 \bullet 10^{-9} s$$

From this value of t_{ON} we can calculate the nominal switching frequency as follows:

$$f_{SW\_VBAT(MIN)} = \frac{V_{OUT}}{\left(V_{BAT(MIN)} \bullet t_{ON\_VBAT(MIN)}\right)} Hz$$

and

$$f_{SW\_VBAT(MAX)} = \frac{V_{OUT}}{\left(V_{BAT(MAX)} \bullet t_{ON\_VBAT(MAX)}\right)} Hz$$

t_{ON} is generated by a one-shot comparator that samples V_{BAT} via R_{tON}, converting this to a current. This current is used to charge an internal 3.3pF capacitor to V_{OUT}. The equations above reflect this along with any internal components or delays that influence t_{ON}. For our DDR2 VTT example we select R_{tON} = 715kΩ:

$t_{ON\_VBAT(MIN)}$ = 329ns and $t_{ON\_VBAT(MAX)}$ = 162ns

$f_{SW\_VBAT(MIN)}$ = 342kHz and $f_{SW\_VBAT(MAX)}$ = 278kHz

Now that we know t_{ON} we can calculate suitable values for the inductor. To do this we select an acceptable inductor ripple current. The calculations below assume 50% of I_{OUT} which will give us a starting place.

Applications Information (Cont.)

$$L_{VBAT(MIN)} = (V_{BAT(MIN)} - V_{OUT}) \bullet \frac{t_{ON\_VBAT(MIN)}}{(0.5 \bullet I_{OUT})} H$$

and

$$L_{VBAT(MAX)} = (V_{BAT(MAX)} - V_{OUT}) \bullet \frac{t_{ON\_VBAT(MAX)}}{(0.5 \bullet I_{OUT})} H$$

For our DDR2 VTT example:

$L_{VBAT(MIN)}$ = 1.6µH and $L_{VBAT(MAX)}$ = 2.1µH

We will select an inductor value of 2.2µH to reduce the ripple current, which can be calculated as follows:

$$I_{RIPPLE\_VBAT(MIN)} = (V_{BAT(MIN)} - V_{OUT}) \bullet \frac{t_{ON\_VBAT(MIN)}}{L} A_{P-P}$$

and

$$I_{RIPPLE\_VBAT(MAX)} = (V_{BAT(MAX)} - V_{OUT}) \bullet \frac{t_{ON\_VBAT(MAX)}}{L} A_{P-P}$$

For our DDR2 VTT example:

$I_{RIPPLE\_VBAT(MIN)}$ = 1.06A_{P-P} and $I_{RIPPLE\_VBAT(MAX)}$ = 1.4A_{P-P}

From this we can calculate the minimum inductor current rating for normal operation:

$$I_{INDUCTOR(MIN)} = I_{OUT(MAX)} + \frac{I_{RIPPLE\_VBAT(MAX)}}{2} A_{(MIN)}$$

For our DDR2 VTT example:

$I_{INDUCTOR(MIN)}$ = 3.7$A_{(MIN)}$

Next we will calculate the maximum output capacitor equivalent series resistance (ESR). This is determined by calculating the remaining static and transient tolerance allowances. Then the maximum ESR is the smaller of the calculated static ESR ($R_{ESR\_ST(MAX)}$) and transient ESR ($R_{ESR\_TR(MAX)}$):

$$R_{ESR\_ST(MAX)} = \frac{(ERR_{ST} - ERR_{DC}) \bullet 2}{I_{RIPPLE\_VBAT(MAX)}} Ohms$$

Where ERR_{ST} is the static output tolerance and ERR_{DC} is the DC error. The DC error will be 1% plus the tolerance of the feedback resistors, thus 2% total for 1% feedback resistors.

For our DDR2 VTT example:

ERR_{ST} = 36mV and ERR_{DC} = 18mV, therefore

$R_{ESR\_ST(MAX)}$ = 26mΩ

$$R_{ESR\_TR(MAX)} = \frac{(ERR_{TR} - ERR_{DC})}{\left(I_{OUT} + \frac{I_{RIPPLE\_VBAT(MAX)}}{2}\right)} Ohms$$

Where ERR_{TR} is the transient output tolerance. Note that this calculation assumes that the worst case load transient is full load. For half of full load, divide the I_{OUT} term by 2.

For our DDR2 VTT example:

ERR_{TR} = 72mV and ERR_{DC} = 18mV, therefore

$R_{ESR\_TR(MAX)}$ = 14.6mΩ for a 3A load transient

We will select a value of 15mΩ maximum for our design.

Note that for constant-on converters there is a minimum ESR requirement for stability which can be calculated as follows:

$$R_{ESR(MIN)} = \frac{3}{2 \bullet \pi \bullet C_{OUT} \bullet f_{SW}}$$

This criteria should be checked once the output capacitance has been determined.

Now that we know the output ESR we can calculate the output ripple voltage:

$$V_{RIPPLE\_VBAT(MAX)} = R_{ESR} \bullet I_{RIPPLE\_VBAT(MAX)} V_{P-P}$$

and

$$V_{RIPPLE\_VBAT(MIN)} = R_{ESR} \bullet I_{RIPPLE\_VBAT(MIN)} V_{P-P}$$

For our DDR2 VTT example:

Applications Information (Cont.)

$V_{RIPPLE\_VBAT(MAX)}$ = 21mV$_{P-P}$ and $V_{RIPPLE\_VBAT(MIN)}$ = 16mV$_{P-P}$

Note that in order for the device to regulate in a controlled manner, the ripple content at the feedback pin, V_{OUT}, should be approximately 15mV$_{P-P}$ at minimum V_{BAT}, and worst case no smaller than 10mV$_{P-P}$. If $V_{RIPPLE\_VBAT(MIN)}$ is less than 15mV$_{P-P}$ the above component values should be revisited in order to improve this.

Next we need to calculate the minimum output capacitance required to ensure that the output voltage does not exceed the transient maximum limit, $POSLIM_{TR}$, starting from the actual static maximum, $V_{OUT\_ST\_POS}$, when a load release occurs:

$$V_{OUT\_ST\_POS} = V_{OUT} + ERR_{DC}\ V$$

For our DDR2 VTT example:

$V_{OUT\_ST\_POS}$ = 0.918V

$$POSLIM_{TR} = V_{OUT} \bullet TOL_{TR}\ V$$

Where TOL_{TR} is the transient tolerance. For our DDR2 VTT example:

$POSLIM_{TR}$ = 1.972V

The minimum output capacitance is calculated as follows:

$$C_{OUT(MIN)} = L \bullet \frac{\left(I_{OUT} + \frac{I_{RIPPLE\_VBAT(MAX)}}{2}\right)^2}{\left(POSLIM_{TR}^{\ 2} - V_{OUT\_ST\_POS}^{\ 2}\right)} F$$

This calculation assumes the absolute worst case condition of a full-load to no load step transient occurring when the inductor current is at its highest. The capacitance required for smaller transient steps my be calculated by substituting the desired current for the I_{OUT} term.

For our DDR2 VTT example:

$C_{OUT(MIN)}$ = 295µF.

We will select 220µF, using one 220µF, 15mΩ capacitor.

Next we calculate the RMS input ripple current, which is largest at the minimum battery voltage:

$$I_{IN(RMS)} = \sqrt{V_{OUT} \bullet \left(V_{BAT(MIN)} - V_{OUT}\right)} \bullet \frac{I_{OUT}}{V_{BAT\_MIN}}\ A_{RMS}$$

For our DDR2 VTT example:

$I_{IN(RMS)}$ = 0.95A$_{RMS}$

Input capacitors should be selected with sufficient ripple current rating for this RMS current, for example a 10µF, 1210 size, 25V ceramic capacitor can handle up to 3A$_{RMS}$. Refer to manufacturer's data sheets.

Finally, we calculate the current limit resistor value. As described in the current limit section, the current limit looks at the "valley current", which is the average output current minus half the ripple current. We use the maximum room temperature specification for MOSFET $R_{DS(ON)}$ at V_{GS} = 4.5V for purposes of this calculation:

$$I_{VALLEY} = I_{OUT} - \frac{I_{RIPPLE\_VBAT(MIN)}}{2}\ A$$

The ripple at low battery voltage is used because we want to make sure that current limit does not occur under normal operating conditions.

$$R_{ILIM} = \left(I_{VALLEY} \bullet 1.2\right) \bullet \frac{R_{DS(ON)} \bullet 1.4}{10 \bullet 10^{-6}}\ Ohms$$

For our DDR2 VTT example:

I_{VALLEY} = 2.47A and R_{ILIM} = 9.12kΩ

We select the next lowest 1% resistor value: 9.09kΩ

Thermal Considerations

The junction temperature of the device may be calculated as follows:

$$T_J = T_A + P_D \bullet \theta_{JA}\quad °C$$

Where:

Applications Information (Cont.)

T_A = ambient temperature (°C)
P_D = power dissipation in (W)
θ_{JA} = thermal impedance junction to ambient from absolute maximum ratings (°C/W)

The power dissipation may be calculated as follows:

$$P_D = VCCA \bullet I_{VCCA} + V_g \bullet Q_g \bullet f \quad W$$

Where:
VCCA = chip supply voltage (V)
I_{VCCA} = operating current (A)
V_g = gate drive voltage, typically 5V (V)
Q_g = FET gate charge, from the FET datasheet (C)
f = switching frequency (kHz)

Inserting the following values as an example:
T_A = 85°C
θ_{JA} = 100°C/W
VCCA = 5V
I_{VCCA} = 1100µA (data sheet maximum)
V_g = 5V
Q_g = 60nC
f = 342kHz
gives us:

$$P_D = 5 \bullet 1100 \bullet 10^{-6} + 5 \bullet 60 \bullet 10^{-9} \bullet 342 \bullet 10^{3} = 0.108 \quad W$$

and

$$T_J = 85 + 0.108 \bullet 100 = 95.8 \quad °C$$

As can be seen, the heating effects due to internal power dissipation are practically negligible, thus requiring no special consideration thermally during layout.

Application Information (Cont.)

Layout Guidelines

One (or more) ground planes is/are recommended to minimize the effect of switching noise and copper losses, and maximize heat dissipation. The IC ground reference, VSSA, should be kept separate from power ground. All components that are referenced to VSSA should connect to it locally at the chip. VSSA should connect to power ground at the output capacitor(s) only.

Feedback traces must be kept far away from noise sources such as switching nodes, inductors and gate drives. Route the feedback trace with VSSA as a differential pair from the output capacitor back to the chip. Run them in a "quiet layer" if possible.

Chip decoupling capacitors (VDDP, VCCA) should be located next to the pins (VDDP and PGND, VCCA and VSSA) and connected directly to them on the same side.

Power sections should connect directly to the ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses. Make all the connections on one side of the PCB using wide copper filled areas if possible. Do not use "minimum" land patterns for power components. Minimize trace lengths between the gate drivers and the gates of the MOSFETs to reduce parasitic impedances (and MOSFET switching losses), the low-side MOSFET is most critical. Maintain a length to width ratio of <20:1 for gate drive signals. Use multiple vias as required by current handling requirement (and to reduce parasitics) if routed on more than one layer

Current sense connections must always be made using Kelvin connections to ensure an accurate signal.

We will examine the SC1480A DDR2 reference design used in the Design Procedure section while explaining the layout guidelines in more detail.

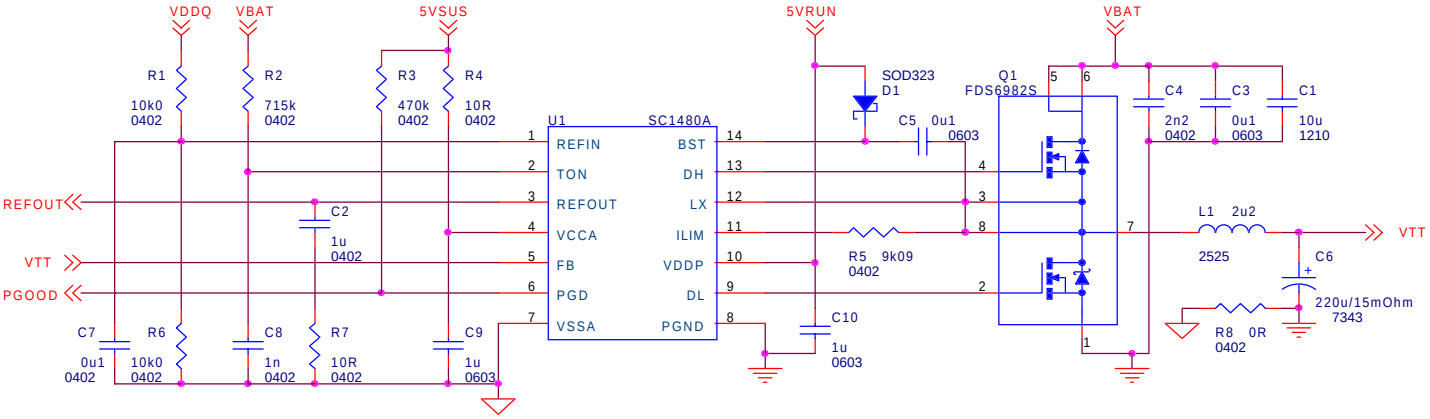


Figure 3: Reference Design and Layout Example for VBAT = 8V to 20V, VTT = 0.9V, 3A

Note R8 is present to facilitate isolation of power ground and VSSA during layout.

Application Information (Cont.)

The layout can be considered in two parts, the control section referenced to VSSA and the power section. Looking at the control section first, locate all components referenced to VSSA on the schematic and place these components at the chip. Connect VSSA using either a wide (>0.020") trace or a copper pour if room allows. Very little current flows in the chip ground therefore large areas of copper are not needed.

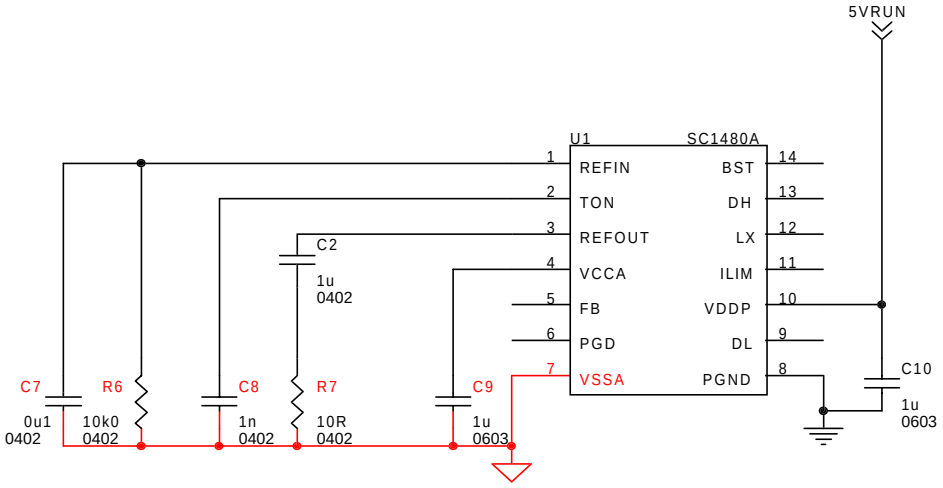


Figure 4: Components Connected to VSSA

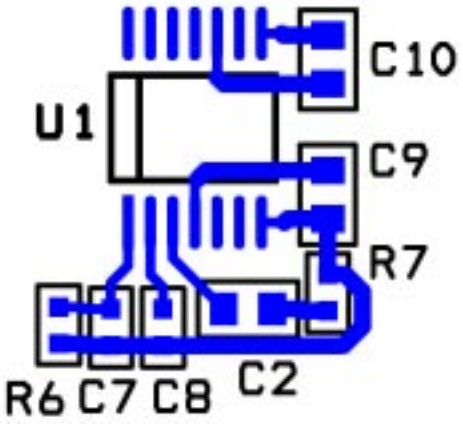


Figure 5: Example VSSA 0.020" Trace

In Figure 5 above, all components referenced to VSSA have been placed and connected using a 0.020" trace. Decoupling capacitors C9 and C10 are as close as possible to their pins. C10 should connect to the PGND plane using two vias.

Application Information (Cont.)

As shown below, FB and VSSA should be routed as a differential pair to the output capacitor.

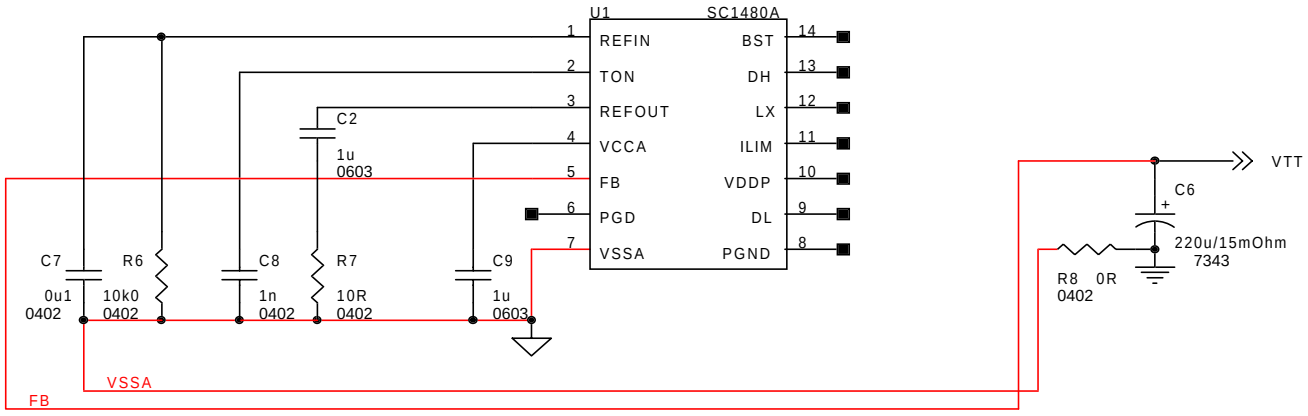


Figure 6: Differential Routing of Feedback and Ground Reference Traces

Next, looking at the power section, the schematic in Figure 7 below shows the power section. The highest di/dts occur in the input loop (highlighted in red) and thus this loop should be kept as small as possible.

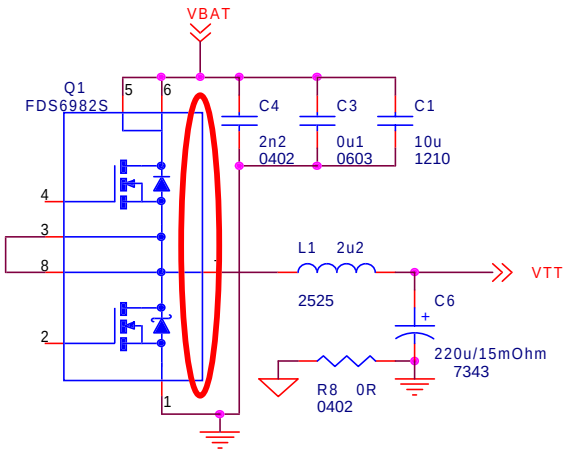


Figure 7: Power Section and Input Loop

The input capacitors should be placed with the highest frequency capacitors closest to the loop to reduce EMI. Use large copper pours to minimize parasitics and losses. See Figure 8 on Page 17 for an example.

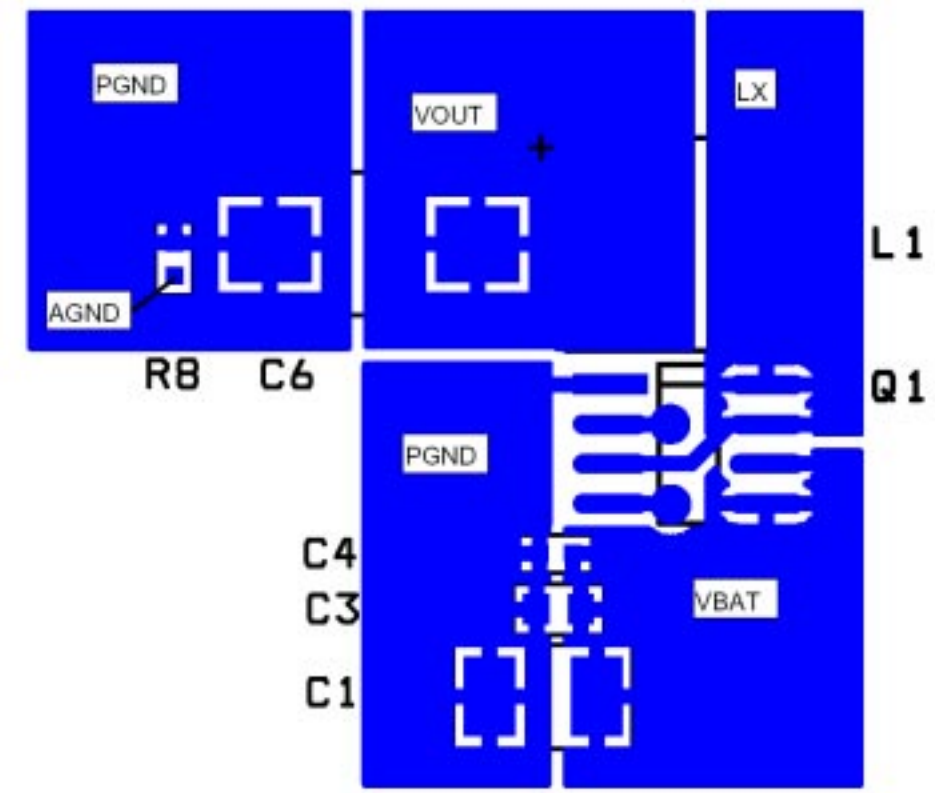


Figure 8: Power Section Component Placement and Copper Pours

Key points for the power section:
1) there should be a very small input loop, well decoupled.
2) the phase node should be a large copper pour, but compact since this is the noisiest node.
3) input power ground and output power ground should not connect directly, but through the ground planes instead.
4) Notice in Figure 8 above placement of 0Ω resistor at the bottom of the output capacitor to connect to VSSA.
5) The current limit resistor should be placed as close as possible to the ILIM and LX pins.

Connecting the control and power sections should be accomplished as follows (see Figure 9 on Page 18):
1) Route VSSA and FB feedback traces as a differential pair routed in a “quiet” layer away from noise sources.
2) Route DL, DH and LX (low side FET gate drive, high side FET gate drive and phase node) to chip using wide traces with multiple vias if using more than one layer. These connections to be as short as possible for loop minimization, with a length to width ratio less than 20:1 to minimize impedance. DL is the most critical gate drive, with power ground as its return path. LX is the noisiest node in the circuit, switching between PWR_SRC and ground at high frequencies, thus should be kept as short as practical. DH has LX as its return path.
3) BST is also a noisy node and should be kept as short as possible.
4) Connect PGND pins on the chip directly to the VDDP decoupling capacitor and then drop vias directly to the ground plane.

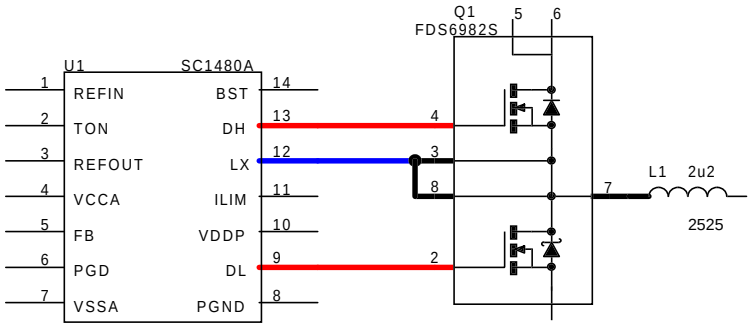
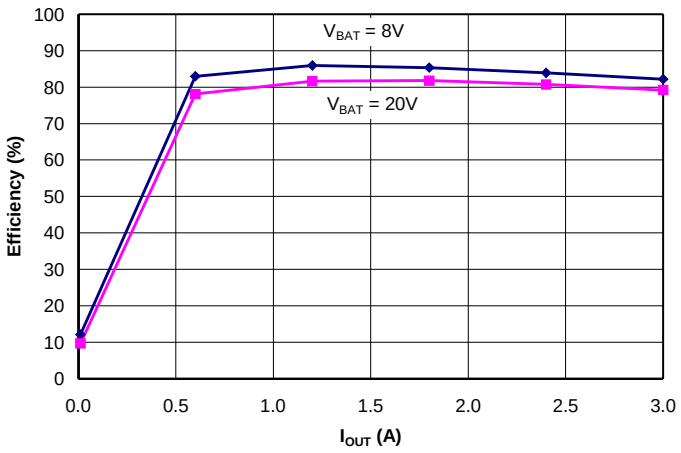


Figure 9: Connecting Control and Power Sections

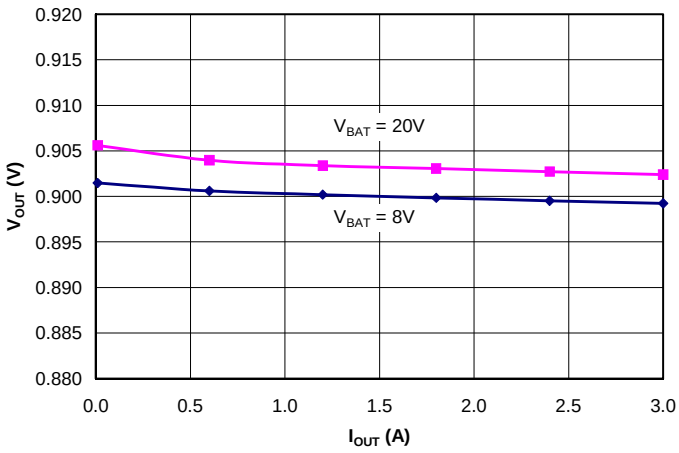
Phase node (black) to be copper pours (preferred) or wide copper traces.
Gate drive traces (red) and phase node trace (blue) to be wide copper traces (L:W < 20:1) and as short as possible, with DL the most critical.

Typical Characteristics

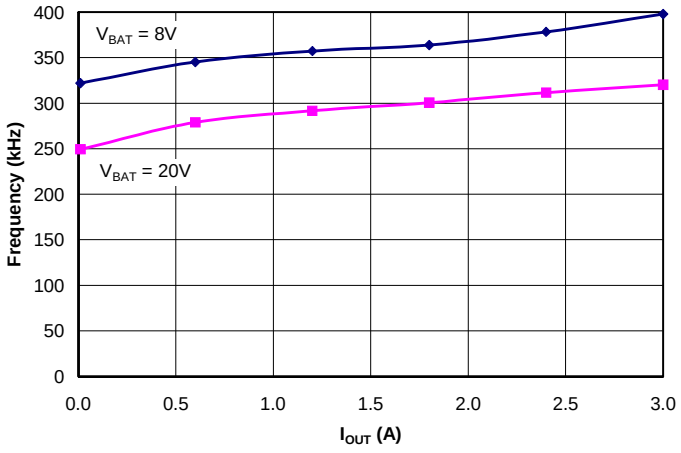
Efficiency vs. Output Current vs. Input Voltage



Output Voltage vs. Output Current vs. Input Voltage



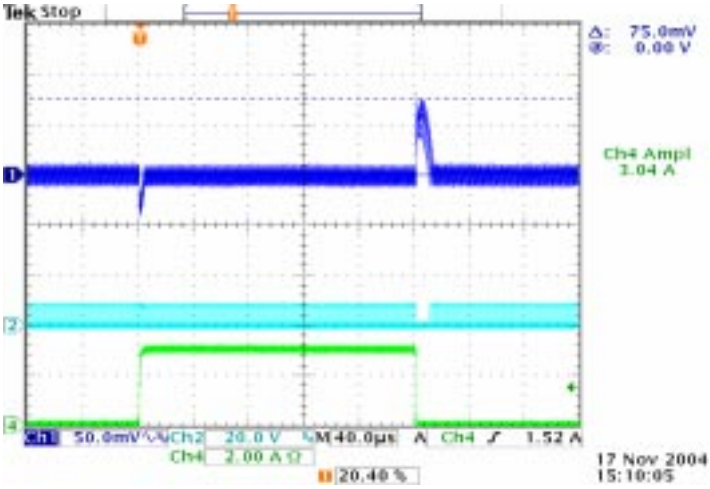
Switching Frequency vs. Output Current vs. Input Voltage



Please refer to Figure 3 on Page 14 for test schematic

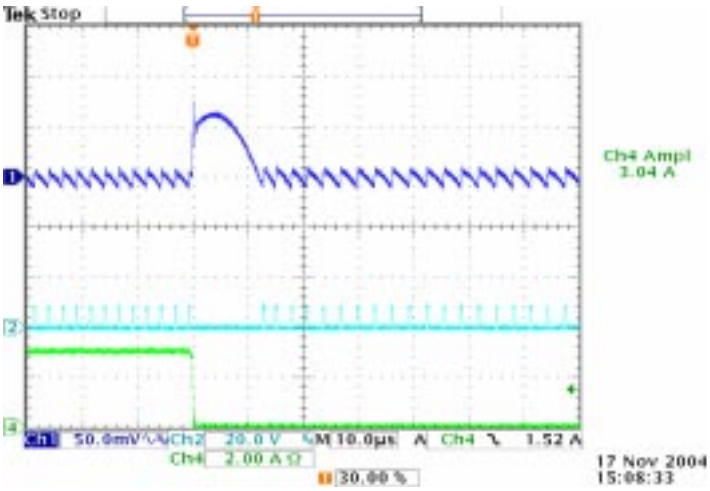
Typical Characteristics (Cont.)

VTT Load Transient Response, 0A to 3A to 0A



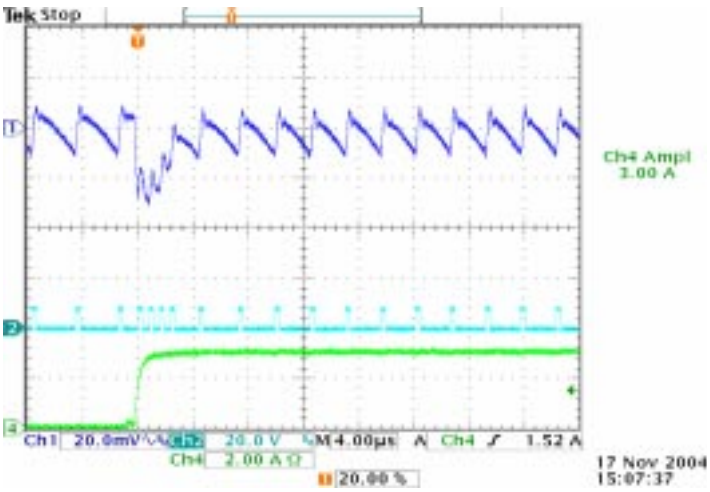
Trace 1: VTT, 50mV/div., AC coupled
Trace 2: LX, 20V/div.
Trace 3: not connected
Trace 4: load current, 2A/div
Timebase: 40µs/div.
V_{BAT} = 8V

VTT Load Transient Response, 3A to 0A Zoomed



Trace 1: VTT, 50mV/div., AC coupled
Trace 2: LX, 20V/div.
Trace 3: not connected
Trace 4: load current, 2A/div
Timebase: 10µs/div.
V_{BAT} = 8V

VTT Load Transient Response, 0A to 3A Zoomed

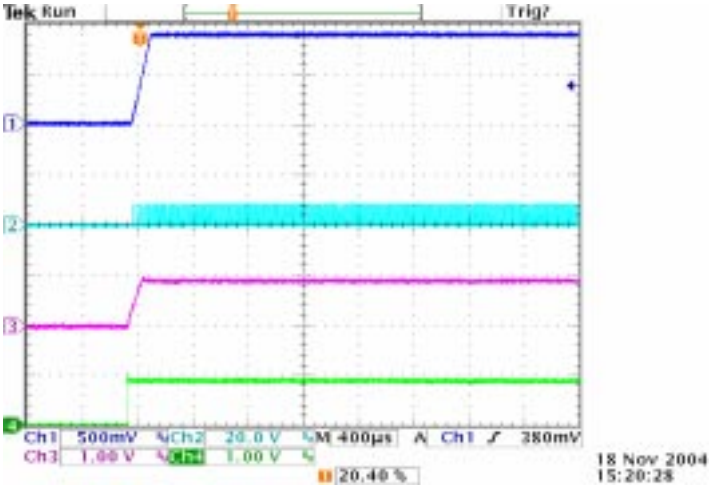


Trace 1: VTT, 20mV/div., AC coupled
Trace 2: LX, 20V/div.
Trace 3: not connected
Trace 4: load current, 2A/div
Timebase: 4µs/div.
V_{BAT} = 8V

Please refer to Figure 3 on Page 14 for test schematic

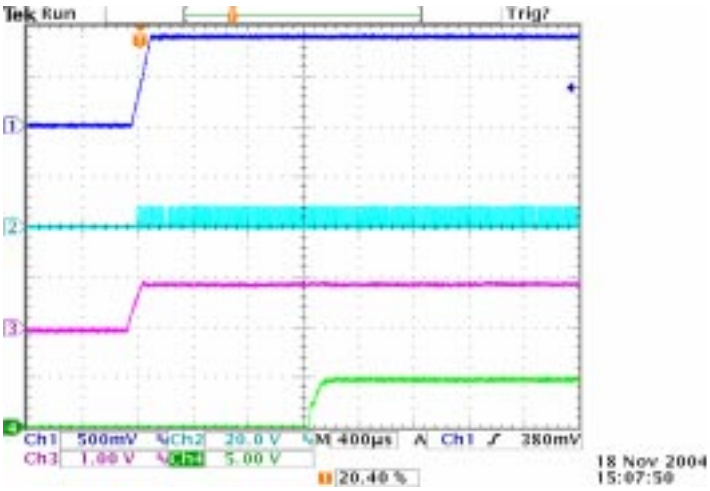
Typical Characteristics (Cont.)

Startup, REFIN Going 0V to 0.9V



Trace 1: VTT, 0.5V/div.
Trace 2: LX, 20V/div.
Trace 3: REFOUT, 1V/div.
Trace 4: REFIN, 1V/div.
Timebase: 400µs/div.
V_{BAT} = 8V

Startup, REFIN Going 0V to 0.9V Showing PGD

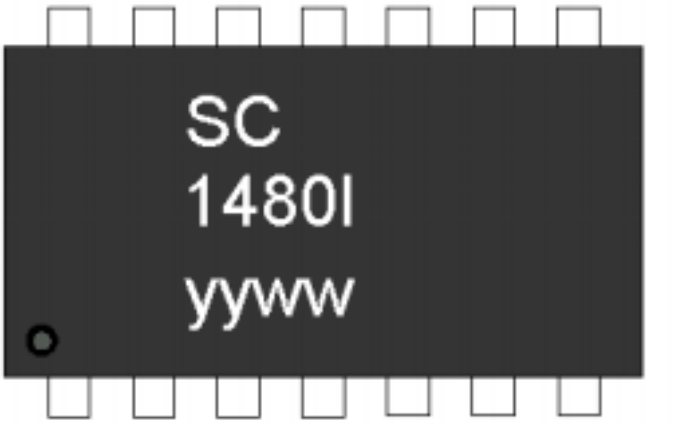


Trace 1: VTT, 0.5V/div.
Trace 2: LX, 20V/div.
Trace 3: REFOUT, 1V/div.
Trace 4: PGD, 5V/div.
Timebase: 400µs/div.
V_{BAT} = 8V

Please refer to Figure 3 on Page 14 for test schematic

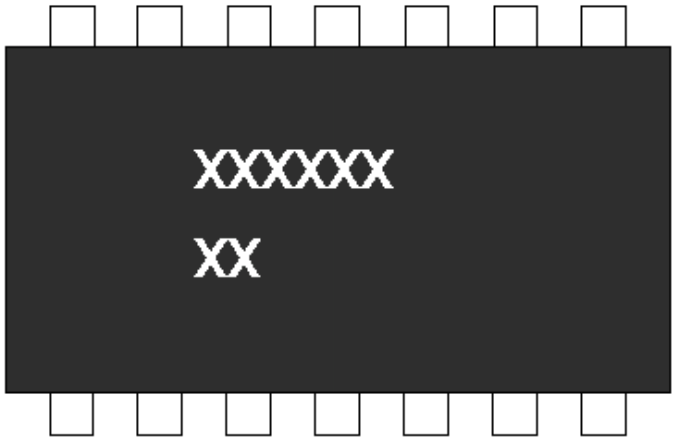
Marking Diagram

Top Mark



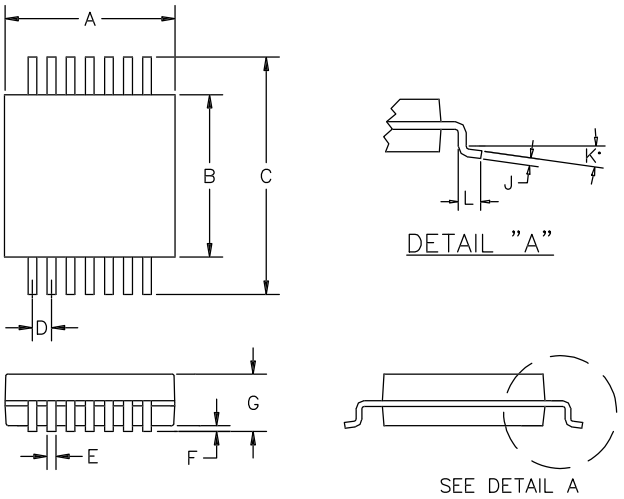
yy = two-digit year of manufacture
ww = two-digit week of manufacture

Bottom Mark



xxxxxx = Wafer Lot Number
xx = Assembly Lot Number

Outline Drawing - TSSOP-14

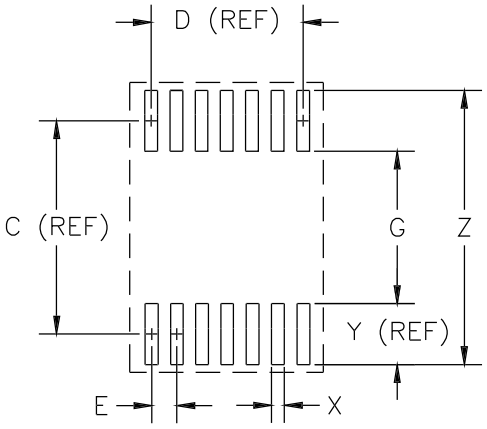


DIMENSIONS (1)					
DIMN	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.193	.201	4.90	5.10	(2)
B	.169	.177	4.30	4.50	(2)
C	.252 BSC		6.40 BSC		–
D	.026 BSC		.65 BSC		–
E	.007	.012	.19	.30	–
F	.002	.006	.05	.15	–
G		.047		1.20	–
J	.004	.008	.09	.20	–
K	0°	8°	0°	8°	–
L	.018	.030	.45	.75	–

JEDEC MO–153AB1

(2) DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.
(1) CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - TSSOP-14



DIMENSIONS (1)					
DIMN	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.218	–	5.53	REF
D	–	.156	–	3.96	REF
E	–	.026	–	0.65	BSC
G	.155	–	3.947	–	–
X	–	.013	–	0.323	REF
Y	–	.062	–	1.583	–
Z	–	.280	–	7.113	–

(2) GRID PLACEMENT COURTYARD IS 10 X 15 ELEMENTS (5mm X 7.5mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

(1) CONTROLLING DIMENSIONS: MILLIMETERS.

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