

POWER MANAGEMENT

Description

The SC1454 contains two ultra low dropout voltage regulators (ULDOs). It operates from an input voltage range of 2.25V to 6.5V, and a wide variety of output voltage options are available. One ULDO has a fixed output, and the other is either fixed (SETA pin grounded) or adjustable using external resistors. Each ULDO has an independent enable pin.

The SC1454 has a bypass pin to enable the user to capacitively decouple the bandgap reference for very low output noise ($50\mu\text{V}_{\text{RMS}}$ typically).

Designed specifically for battery operated systems, the devices utilize CMOS technology to require very low operating currents (typically $130\mu\text{A}$ with both outputs supplying 150mA). In addition, the dropout voltage is typically 155mV at 150mA, helping to prolong battery life further. The devices are designed to provide 400mA of peak current for applications which require high initial inrush current.

They have been designed to be used with low ESR ceramic capacitors to save cost and PCB area.

The SC1454 is available with a wide variety of voltage options as standard. It comes in the tiny 8 lead MSOP surface mount package.

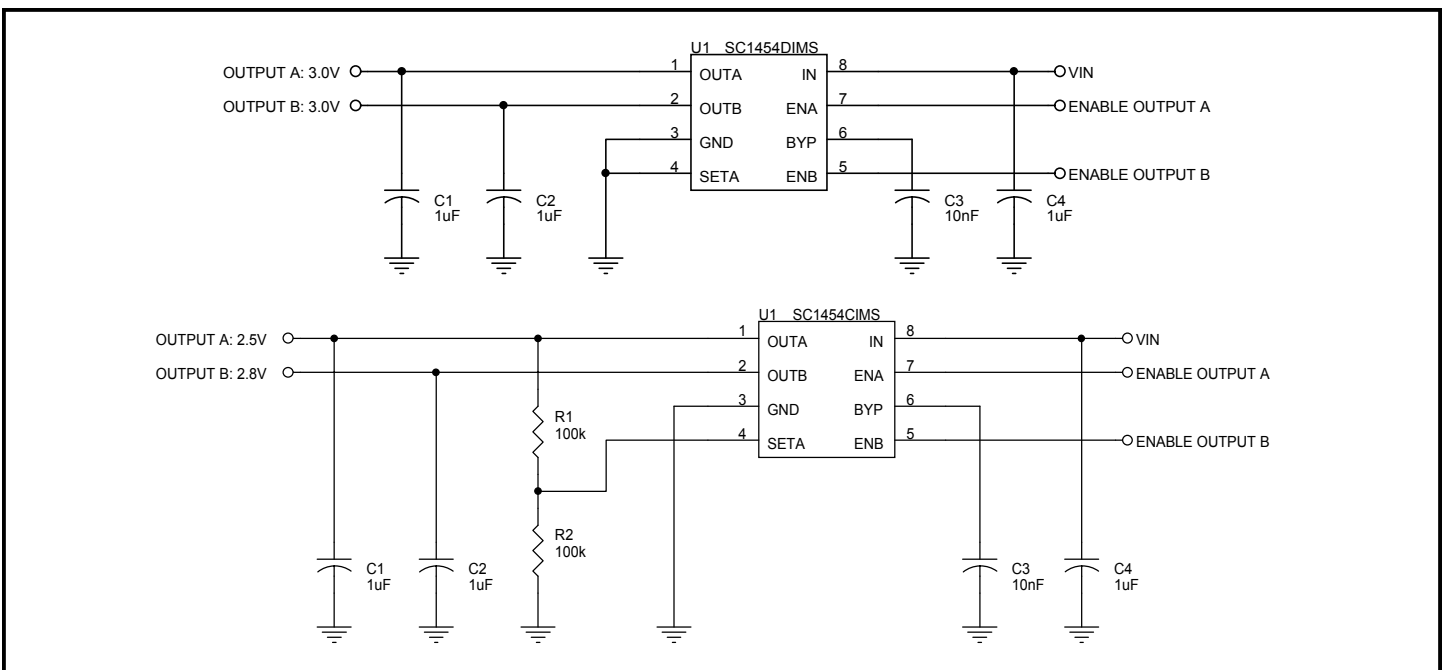
Features

- ◆ Up to 150mA per regulator output
- ◆ Low quiescent current
- ◆ Low dropout voltage
- ◆ Stable operation with ceramic caps
- ◆ Very low $50\mu\text{V}_{\text{RMS}}$ output noise
- ◆ Wide selection of output voltages
- ◆ Tight load and line regulation
- ◆ Current and thermal limiting
- ◆ Reverse input polarity protection
- ◆ $<1.5\mu\text{A}$ off-mode current
- ◆ Logic controlled enable

Applications

- ◆ Cellular telephones
- ◆ Palmtop/Laptop computers
- ◆ Battery-powered equipment
- ◆ Bar code scanners
- ◆ SMPS post regulator/dc to dc modules
- ◆ High efficiency linear power supplies

Typical Application Circuit



POWER MANAGEMENT
Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
Input Supply Voltage	V_{IN}	-5 to +7	V
Enable Input Voltage	V_{EN}	-5 to + V_{IN}	V
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-60 to +150	°C
Thermal Impedance Junction to Ambient ⁽¹⁾	θ_{JA}	206	°C/W
Thermal Impedance Junction to Ambient ⁽²⁾	θ_{JA}	95	°C/W
Thermal Impedance Junction to Case	θ_{JC}	39	°C/W
ESD Rating (Human Body Model)	ESD	2	kV

Notes:

(1) Minimum pad size.

(2) 1 square inch of FR-4, double sided, 1oz. minimum copper weight.

Electrical Characteristics

Unless specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{OUT} + 1\text{V}$, $I_{OUTA} = I_{OUTB} = 1\text{mA}$, $C_{IN} = C_{OUT} = 1.0\ \mu\text{F}$, $V_{ENA} = V_{ENB} = V_{IN}$.
 Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
IN						
Input Supply Voltage	V_{IN}		2.25		6.50	V
Quiescent Current	I_Q	$V_{ENA} = 0\text{V}$, $V_{ENB} = V_{IN}$, $I_{OUTB} = 150\text{mA}$ or		100	150	μA
		$V_{ENB} = 0\text{V}$, $V_{ENA} = V_{IN}$, $I_{OUTA} = 150\text{mA}$			200	
		$V_{ENA} = V_{ENB} = V_{IN}$, $I_{OUTA} = I_{OUTB} = 150\text{mA}$		130	200	μA
		$V_{IN} = 6.5\text{V}$, $V_{ENA} = V_{ENB} = 0\text{V}$ (OFF)			250	
				0.2	1.0	μA
					1.5	
OUTA, OUTB						
Output Voltage ⁽¹⁾	V_{OUT}	$I_{OUT} = 1\text{mA}$	-1%	V_{OUT}	+1%	V
		$0\text{mA} \leq I_{OUT} \leq 150\text{mA}$, $V_{OUT} + 1\text{V} \leq V_{IN} \leq 5.5\text{V}$	-2%		+2%	
Line Regulation ⁽¹⁾	$REG_{(LINE)}$	$V_{OUT} + 1\text{V} \leq V_{IN} \leq 5.5\text{V}$, $I_{OUT} = 1\text{mA}$		2.5	10	mV
					12	
Load Regulation ⁽¹⁾	$REG_{(LOAD)}$	$0.1\text{mA} \leq I_{OUT} \leq 150\text{mA}$		-5	-20	mV
					-30	

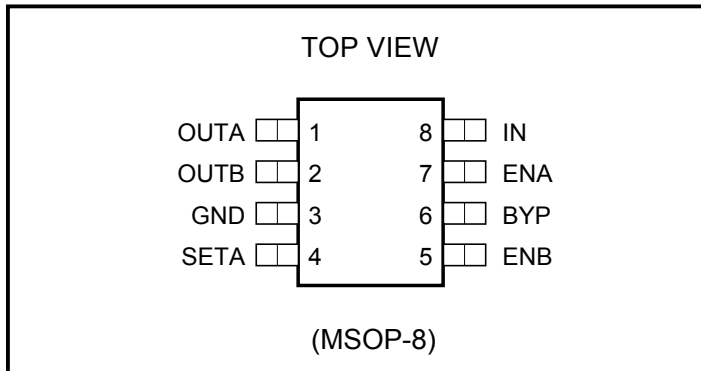
POWER MANAGEMENT
Electrical Characteristics

Unless specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{OUT} + 1\text{V}$, $I_{OUTA} = I_{OUTB} = 1\text{mA}$, $C_{IN} = C_{OUT} = 1.0\ \mu\text{F}$, $V_{ENA} = V_{ENB} = V_{IN}$.
 Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTA, OUTB (Cont.)						
Dropout Voltage ⁽¹⁾⁽²⁾	V_D	$I_{OUT} = 1\text{mA}$		1		mV
		$I_{OUT} = 50\text{mA}$		52	70	
					90	
		$I_{OUT} = 150\text{mA}$		155	210	
					270	
Current Limit	I_{LIM}		400			mA
Ripple Rejection	PSRR	$f = 120\text{Hz}$, $C_{BYP} = 10\text{nF}$		61		dB
Output Voltage Noise	e_n	$f = 10\text{Hz to } 100\text{kHz}$, $I_{OUT} = 50\text{mA}$, $C_{BYP} = 10\text{nF}$, $C_{OUT} = 2.2\ \mu\text{F}$, 1.8V output		27		μV_{RMS}
		$f = 10\text{Hz to } 100\text{kHz}$, $I_{OUT} = 50\text{mA}$, $C_{BYP} = 10\text{nF}$, $C_{OUT} = 2.2\ \mu\text{F}$, 3.3V output		55		
ENA, ENB						
Enable Input Threshold	V_{IH}		1.6			V
	V_{IL}				0.4	
Enable Input Bias Current ⁽³⁾	I_{EN}	$0\text{V} \leq V_{ENA/B} \leq V_{IN}$	-0.5		0.5	μA
BYP						
Start-Up Rise Time	t_r	$C_{BYP} = 10\text{nF}$		1.25		ms
SETA						
Sense/Select Threshold	V_{TH}		20	40	80	mV
SETA Reference Voltage	V_{SETA}	$V_{IN} = 2.5\text{V}$, $I_{OUT} = 1\text{mA}$	-1%	1.250	+1%	V
		$0\text{mA} \leq I_{OUT} \leq 150\text{mA}$, $2.5\text{V} \leq V_{IN} \leq 5.5\text{V}$	-2%		+2%	
SETA Input Leakage Current ⁽³⁾	I_{SETA}	$V_{SETA} = 1.3\text{V}$		0.015	50	nA
Over Temperature Protection						
High Trip Level	T_{HI}			150		$^\circ\text{C}$
Hysteresis	T_{HYST}			20		$^\circ\text{C}$

NOTES:

- (1) Low duty cycle pulse testing with Kelvin connections required.
- (2) Defined as the input to output differential at which the output drops 100mV below the value measured at a differential of 1V. Not measurable on outputs less than 2.25V due to minimum V_{IN} constraints.
- (3) Guaranteed by design.

POWER MANAGEMENT
Pin Configuration

Ordering Information

Part Numbers	Package
SC1454XIMSTR ⁽¹⁾⁽²⁾	MSOP-8
SC1454XIMSTR ⁽¹⁾⁽²⁾⁽³⁾	

Notes:

(1) Where X denotes voltage options - see Voltage Options table.

(2) Only available in tape and reel packaging. A reel contains 2500 devices.

(3) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	OUTA	Regulator A output.
2	OUTB	Regulator B output.
3	GND	Ground pin.
4	SETA	Connecting this pin to ground results in the internally preset value for V_{OUT} . Connecting to an external resistor divider changes V_{OUTA} to: $V_{OUTA} = 1.250 \cdot \left(1 + \frac{R1}{R2}\right)$
5	ENB	Active high enable pin for output B. CMOS compatible input. Connect to IN if not being used.
6	BYP	Bypass pin for bandgap reference. Connect a 10nF capacitor, C_{BYP} , between this pin and ground for low noise operation.
7	ENA	Active high enable pin for output A. CMOS compatible input. Connect to IN if not being used.
8	IN	Input pin for both regulators.

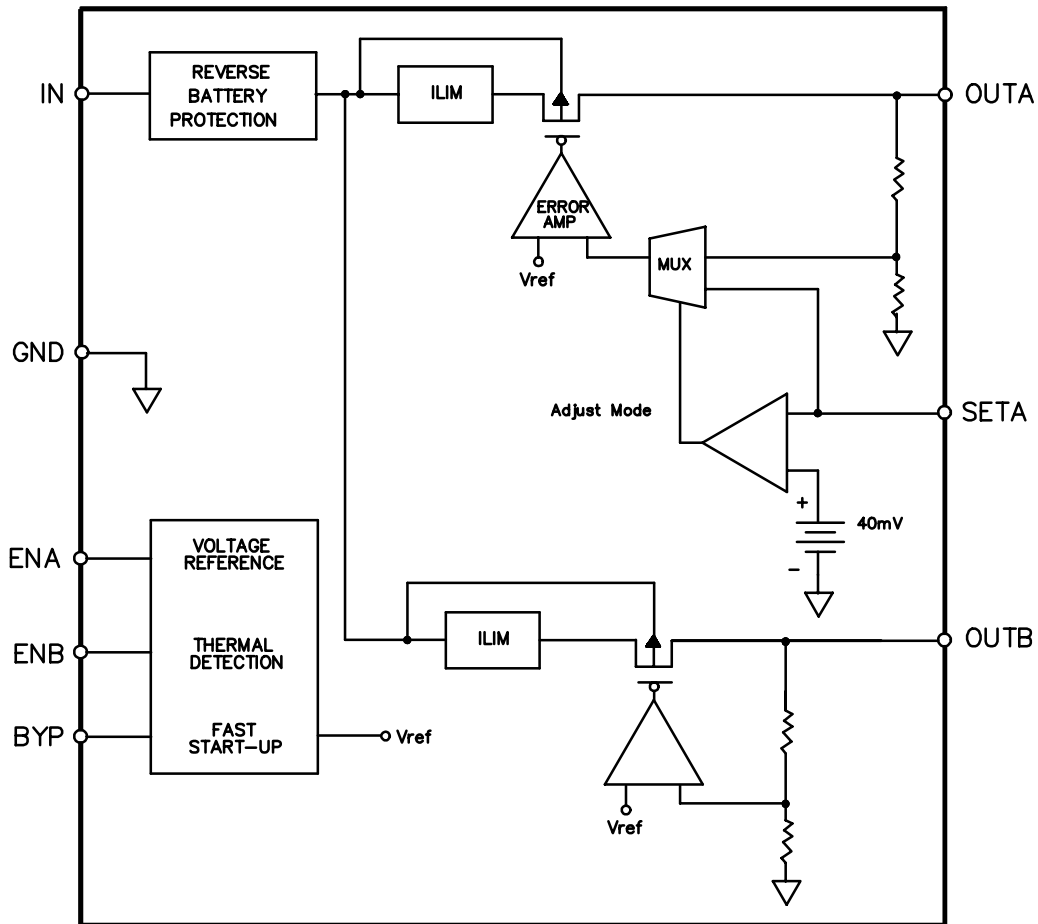
Voltage Options

Replace X in the part number (SC1454XIMS) by the letter shown below for the corresponding voltage option:

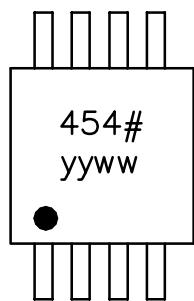
X	V_{OUTA} (V)	V_{OUTB} (V)
A	1.8	1.8
B	2.5	2.5
C	2.8	2.8
D	3.0	3.0
E	3.3	3.3
F	3.0	2.5
G	3.0	1.8
H	3.0	2.8
J	3.3	2.5
K	3.3	2.8

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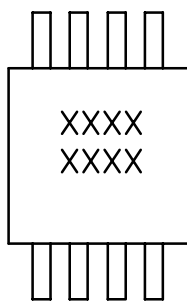
Block Diagram



Marking Information



TOP



BOTTOM

= Voltage option (Example: 454F)
 yyww = Datecode (Example: 0008)
 XXXX = Lot number (Example: E90101-1)

POWER MANAGEMENT
Applications Information
Theory Of Operation

The SC1454 is intended for applications where very low dropout voltage, low supply current and low output noise are critical. Furthermore, the SC1454, by combining two ultra low dropout (ULDO) regulators, along with enable controls and output voltage adjustability for one output, provides a very space efficient solution for multiple supply requirements.

The SC1454 contains two ULDOs, both of which are supplied by one input supply, between IN and GND. Each ULDO has its own active high enable pin (ENA/ENB). Pulling this pin low causes that specific ULDO to enter a very low power shutdown state.

The SC1454 contains an internal bandgap reference which is fed into the inverting input of two error amplifiers, one for each output. The output voltage of each regulator is divided down internally using a resistor divider and compared to the bandgap voltage. The error amplifier drives the gate of a low $R_{DS(ON)}$ P-channel MOSFET pass device.

Output A has both a fixed and adjustable output voltage mode. Grounding the SETA pin (pulling it below the Sense/Select threshold of 40mV) will connect the internal resistor divider to the error amplifier resulting with the internally preset output voltage. If SETA is pulled above this threshold, then the Sense/Select switch will connect the SETA pin to the error amplifier. Output A will then be regulated such that the voltage at SETA will equal V_{SETA} , the SETA reference voltage (typically 1.250V).

A bypass pin (BYP) is provided to decouple the bandgap reference to reduce output noise (on both outputs) and also to improve power supply rejection.

Each regulator has its own current limit circuitry to ensure that the output current will not damage the device during output short, overload or start-up. The current limit is guaranteed to be greater than 400mA to allow fast charging of the output capacitor and high initial currents for DSP initialization.

The SC1454 has a fast start-up circuit to speed up the initial charging time of the bypass capacitor to enable the output voltage to come up quicker.

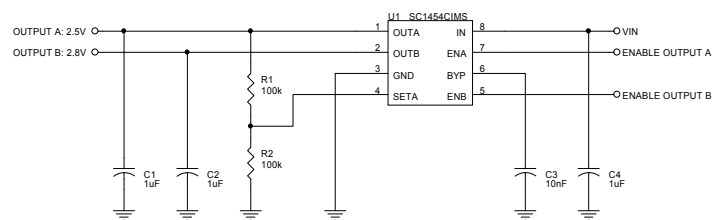
The SC1454 includes thermal shutdown circuitry to turn off the device if T_J exceeds 150°C (typical), with the device remaining off until T_J drops by 20°C (typical). Reverse battery protection circuitry ensures that the device cannot be damaged if the input supply is accidentally reversed, limiting the reverse current to less than 1.5mA.

Component Selection - General

Output capacitor - Semtech recommends a minimum capacitance of 1 μ F at the output with an equivalent series resistance (ESR) of < 1 Ω over temperature. While the SC1454 has been designed to be used with ceramic capacitors, it does not have to be used with ceramic capacitors, allowing the designer a choice. Increasing the bulk capacitance will further reduce output noise and improve the overall transient response.

Input capacitor - Semtech recommends the use of a 1 μ F ceramic capacitor at the input. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, input droop due to load transients is reduced, improving overall load transient response.

Bypass capacitor - Semtech recommends the use of a 10nF ceramic capacitor to bypass the bandgap reference. Increasing this capacitor to 100nF will further improve power supply rejection. Reducing this capacitor below 1nF may result in output overshoot at turn-on.

Component Selection - Externally Setting Output


Referring to the circuit above, the output voltage of output A can be externally adjusted anywhere within the range from 1.25V to $(V_{IN(MAX)} - V_{D(MAX)})$. The output voltage will be in accordance with the following equation:

$$V_{OUTA} = 1.250 \cdot \left(1 + \frac{R1}{R2}\right)$$

1% tolerance resistors are recommended. The values of

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Applications Information (Cont.)

R1 and R2 should be selected such that the current flowing through them is $\geq 10\mu\text{A}$ (thus $R2 \leq 120\text{k}\Omega$).

Thermal Considerations

The worst-case power dissipation for this part is given by:

$$P_{D(\text{MAX})} = (V_{\text{IN}(\text{MAX})} - V_{\text{OUTA}(\text{MIN})}) \cdot I_{\text{OUTA}(\text{MAX})} + (V_{\text{IN}(\text{MAX})} - V_{\text{OUTB}(\text{MIN})}) \cdot I_{\text{OUTB}(\text{MAX})} + V_{\text{IN}(\text{MAX})} \cdot I_{\text{Q}(\text{MAX})} \quad (1)$$

For all practical purposes, equation (1) can be reduced to the following expression:

$$P_{D(\text{MAX})} = (V_{\text{IN}(\text{MAX})} - V_{\text{OUTA}(\text{MIN})}) \cdot I_{\text{OUTA}(\text{MAX})} + (V_{\text{IN}(\text{MAX})} - V_{\text{OUTB}(\text{MIN})}) \cdot I_{\text{OUTB}(\text{MAX})} \quad (2)$$

Looking at a typical application:

$$V_{\text{IN}(\text{MAX})} = 4.2\text{V}$$

$$V_{\text{OUTA}} = 3\text{V} - 2\% \text{ (worst case)} = 2.94\text{V}$$

$$V_{\text{OUTB}} = 3.3\text{V} - 2\% \text{ (worst case)} = 3.234\text{V}$$

$$I_{\text{OUTA}} = I_{\text{OUTB}} = 150\text{mA}$$

$$T_{\text{A}} = 85^{\circ}\text{C}$$

Inserting these values into equation (2) above gives us:

$$P_{D(\text{MAX})} = (4.2 - 2.94) \cdot 0.15 + (4.2 - 3.234) \cdot 0.15 = 0.189 + 0.145 = 0.334\text{W}$$

Using this figure, we can calculate the maximum thermal

impedance allowable to maintain $T_{\text{J}} \leq 125^{\circ}\text{C}$:

$$\theta_{\text{JA}(\text{MAX})} = \frac{(T_{\text{J}(\text{MAX})} - T_{\text{A}(\text{MAX})})}{P_{\text{D}(\text{MAX})}} = \frac{(125 - 85)}{0.334} = 120^{\circ}\text{C/W}$$

This target value can be achieved by using one square inch of board copper connected to the GND pin (pin 3), which connects directly to the device substrate. Increasing this area or the use of multi layer boards will lower the junction temperature and improve overall output voltage accuracy.

Layout Considerations

While layout for linear devices is generally not as critical as for a switching application, careful attention to detail will ensure reliable operation.

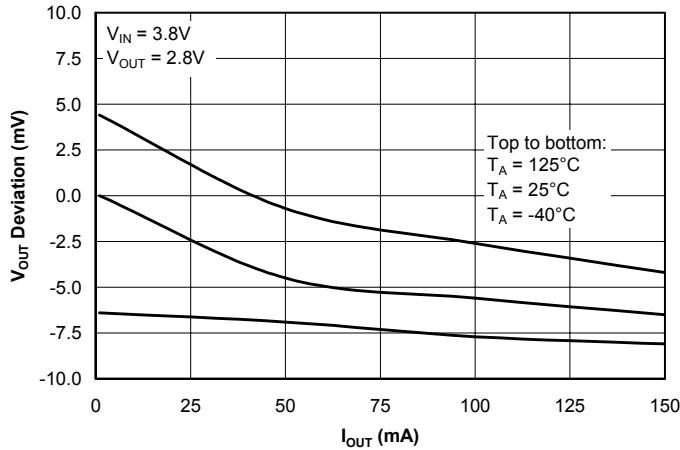
- 1) Attaching the part to a larger copper footprint will enable better heat transfer from the device, especially on PCBs where there are internal ground and power planes.
- 2) Place the input, output and bypass capacitors close to the device for optimal transient response and device behaviour.
- 3) Connect all ground connections directly to the ground plane. If there is no ground plane, connect to a common local ground point before connecting to board ground.

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Typical Characteristics

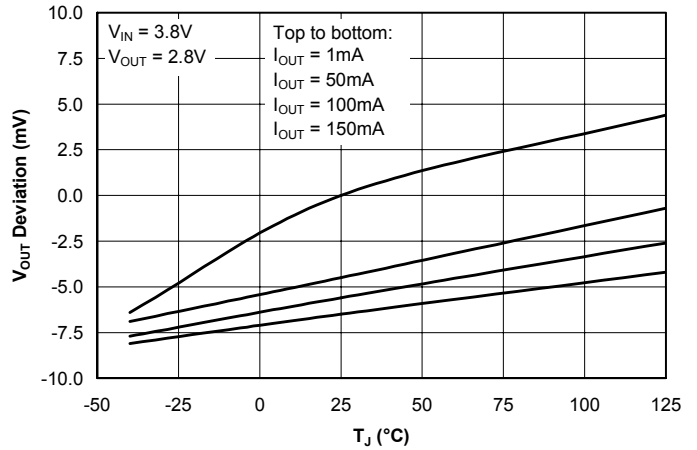
Output Voltage vs. Output Current

vs. Junction Temperature, $V_{OUT} = 2.8V$



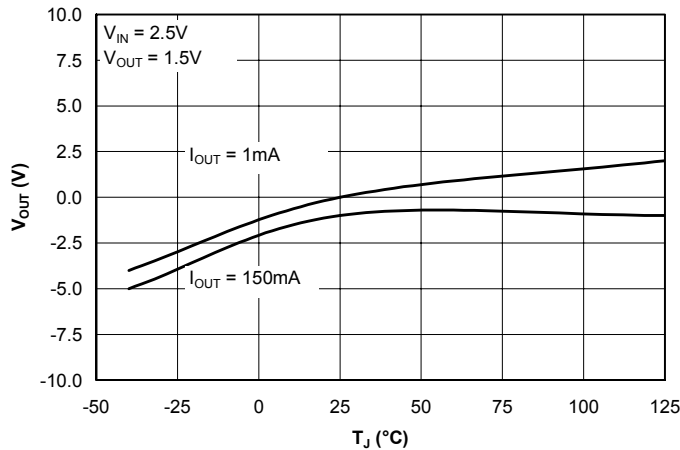
Output Voltage vs. Junction Temperature

vs. Output Current, $V_{OUT} = 2.8V$



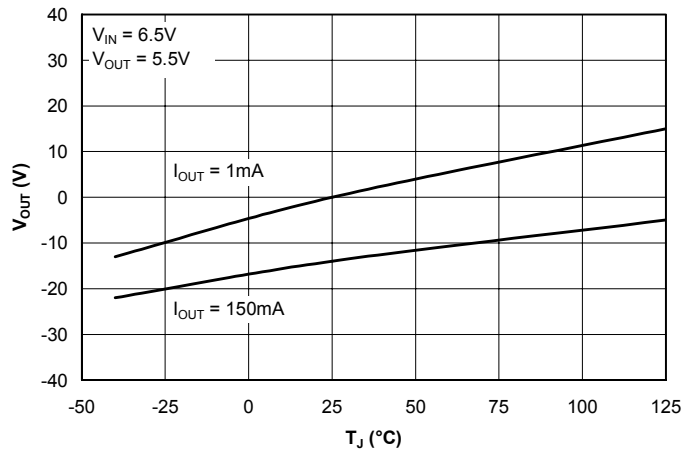
Output Voltage vs. Junction Temperature

vs. Output Current, $V_{OUT} = 1.5V$



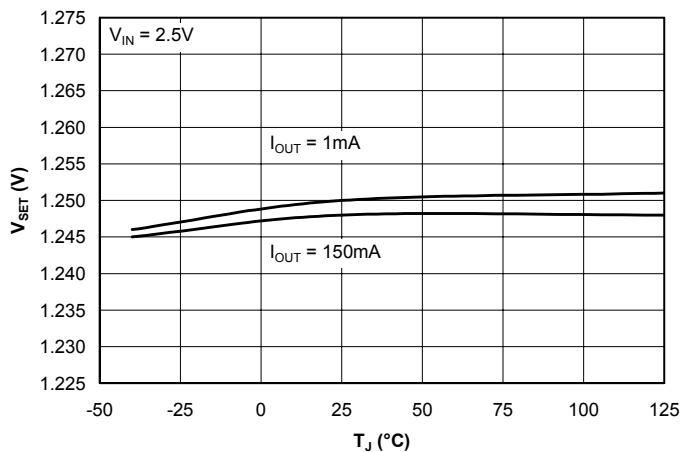
Output Voltage vs. Junction Temperature

vs. Output Current, $V_{OUT} = 5.5V$



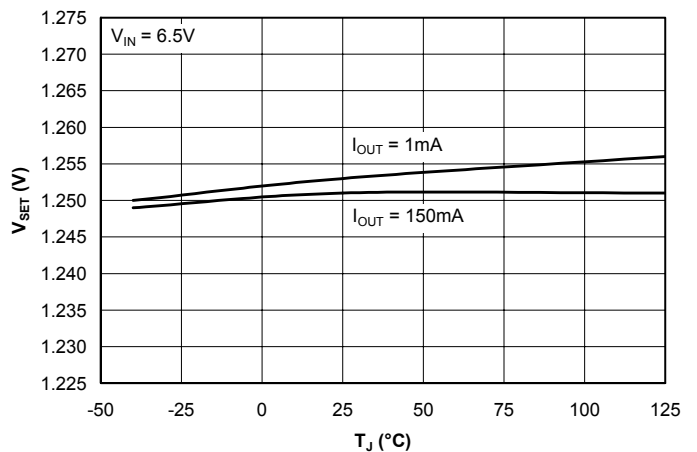
SETA Reference Voltage vs. Junction Temperature

vs. Output Current, $V_{IN} = 2.5V$



SETA Reference Voltage vs. Junction Temperature

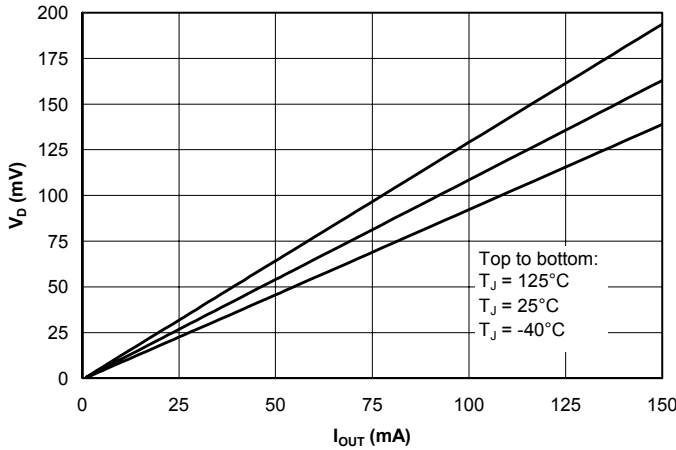
vs. Output Current, $V_{IN} = 6.5V$



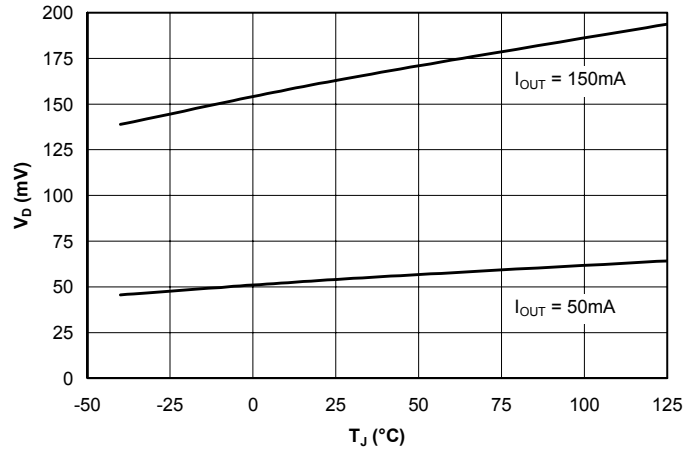
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Typical Characteristics (Cont.)

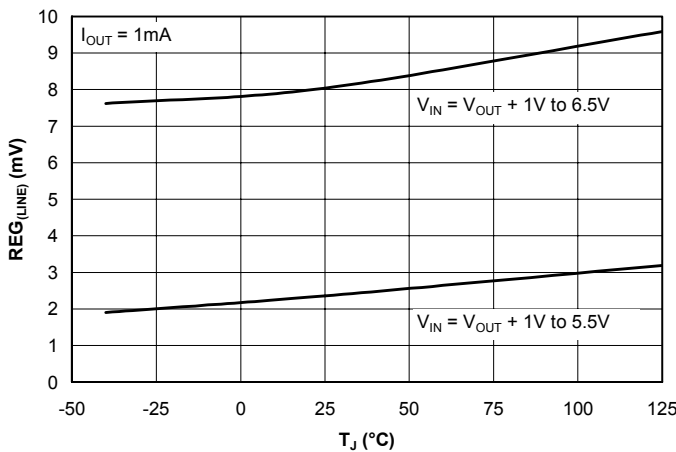
Dropout Voltage vs. Output Current vs. Junction Temperature



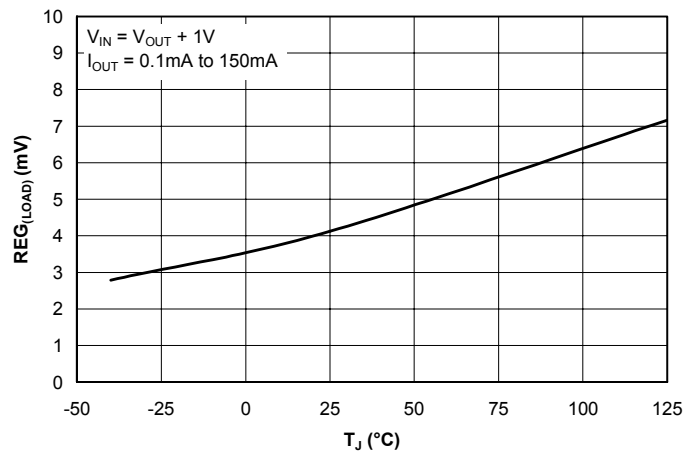
Dropout Voltage vs. Junction Temperature vs. Output Current



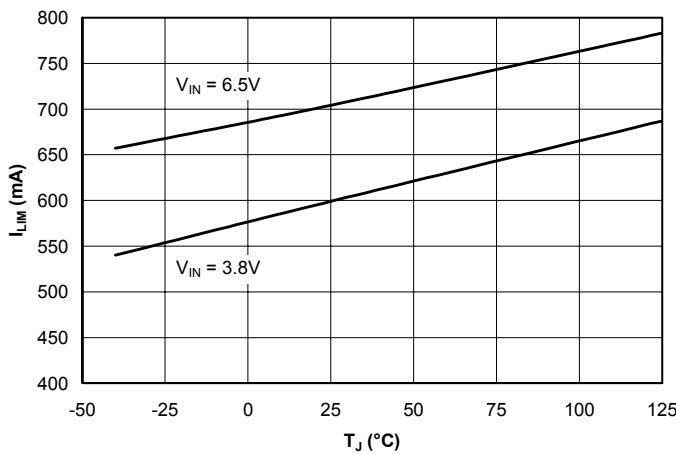
Line Regulation vs. Junction Temperature



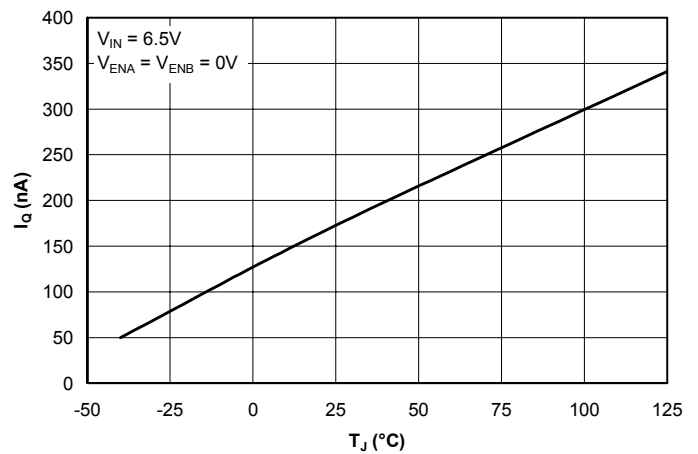
Load Regulation vs. Junction Temperature



Current Limit vs. Junction Temperature vs. Input Voltage



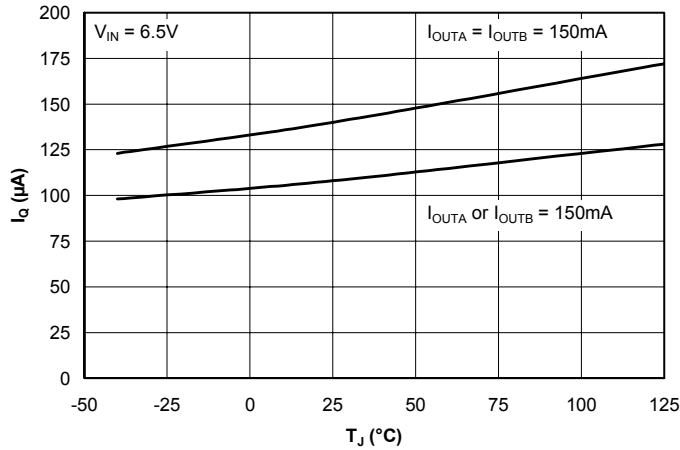
Off-State Quiescent Current vs. Junction Temperature



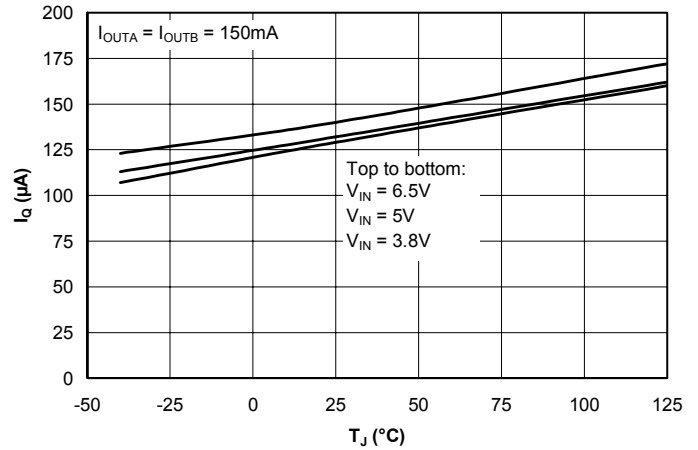
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Typical Characteristics (Cont.)

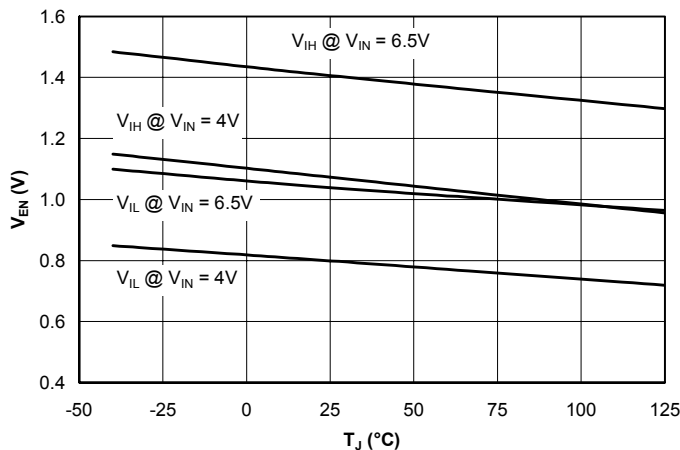
Quiescent Current vs. Junction Temperature vs. Output Current



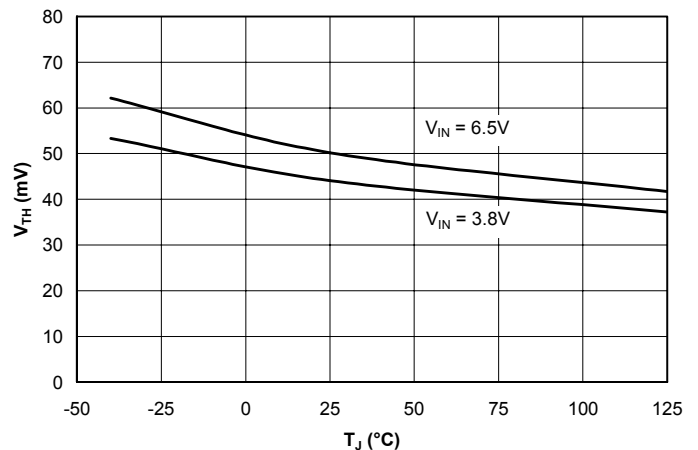
Quiescent Current vs. Junction Temperature vs. Input Voltage



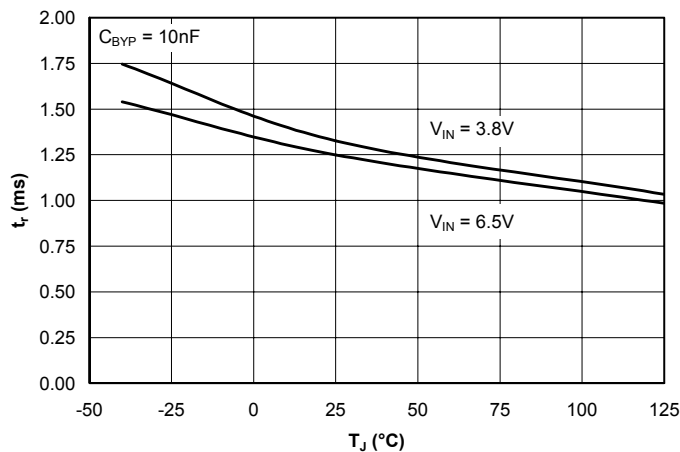
Enable Input Voltage vs. Junction Temperature vs. Input Voltage



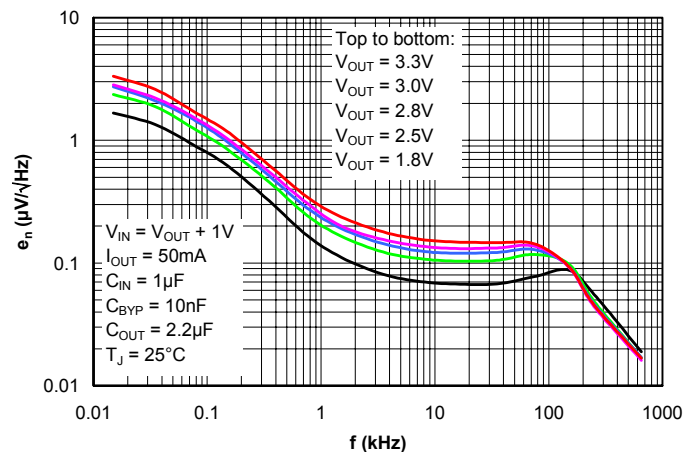
Sense/Select Threshold Voltage vs. Junction Temperature vs. Input Voltage



Bypass Start-up Rise Time vs. Junction Temperature vs. Input Voltage



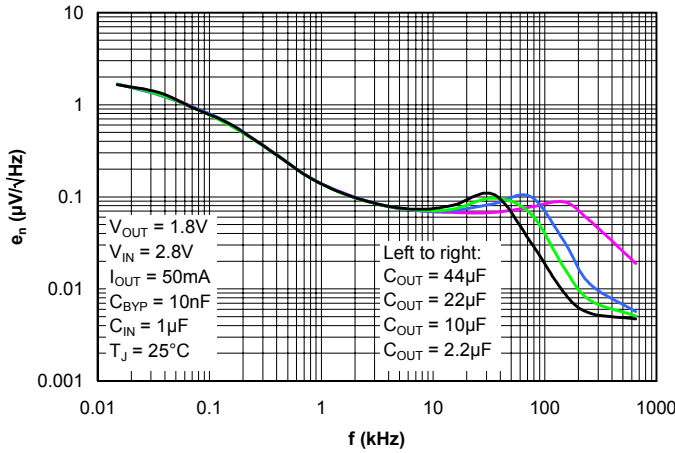
Output Spectral Noise Density vs. Frequency vs. Output Voltage



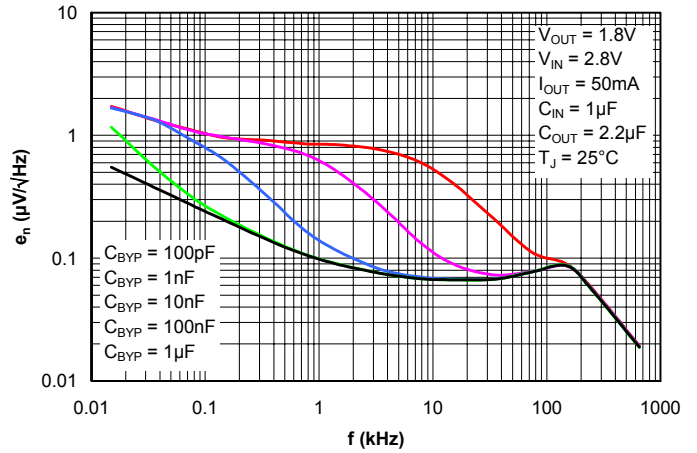
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Typical Characteristics (Cont.)

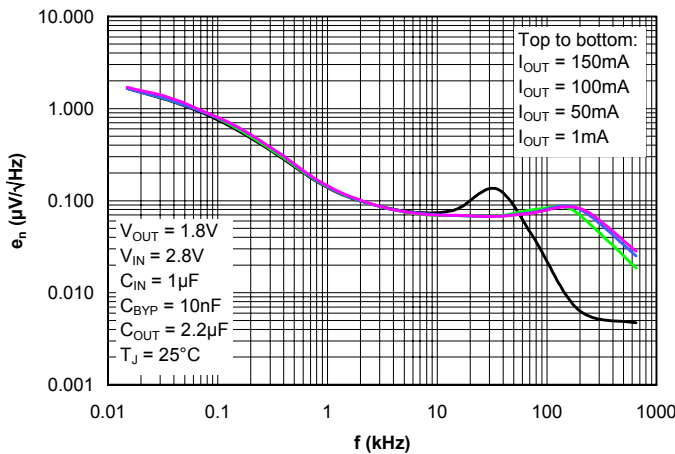
Output Spectral Noise Density vs. Frequency vs. Output Capacitance



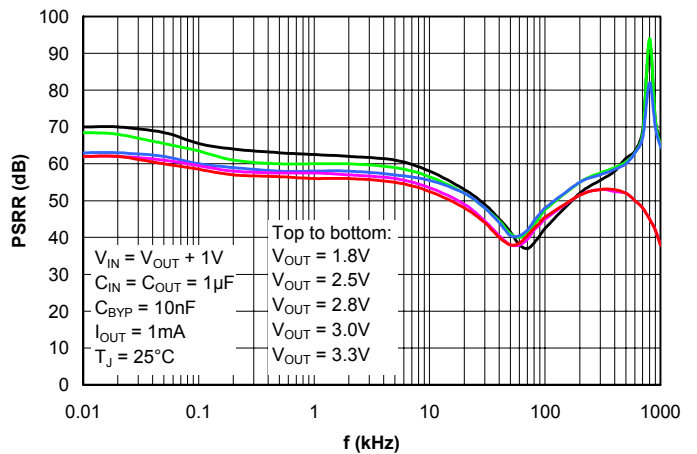
Output Spectral Noise Density vs. Frequency vs. Bypass Capacitance



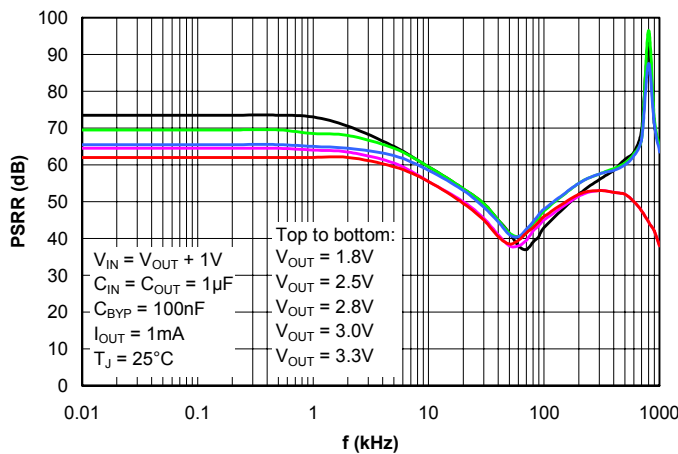
Output Spectral Noise Density vs. Frequency vs. Output Current



PSRR vs. Frequency vs. Output Voltage (C_BYP = 10nF)

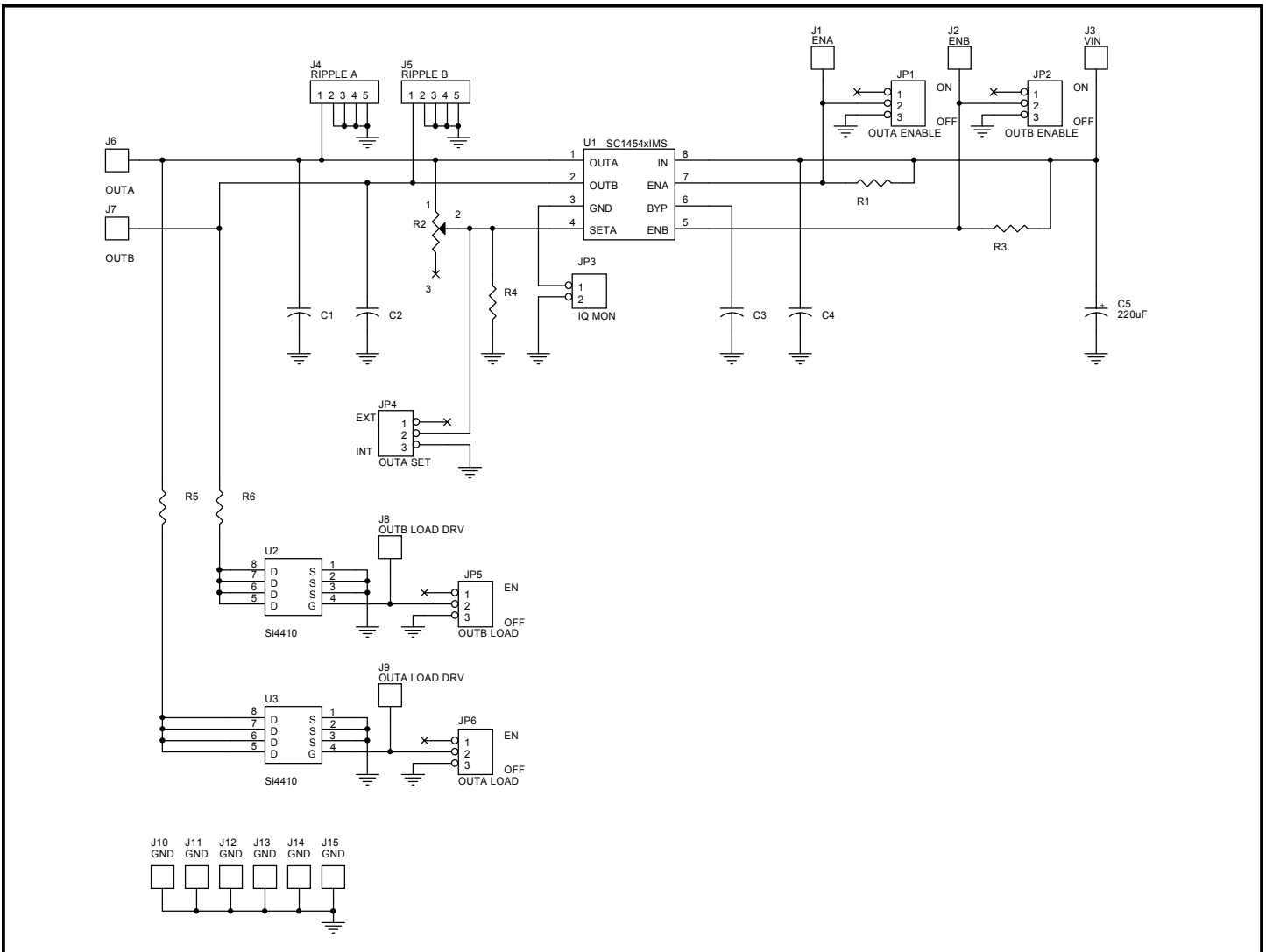


PSRR vs. Frequency vs. Output Voltage (C_BYP = 100nF)

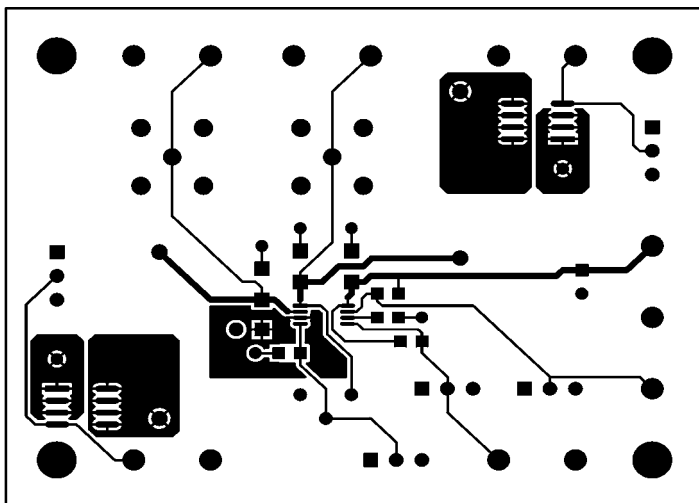


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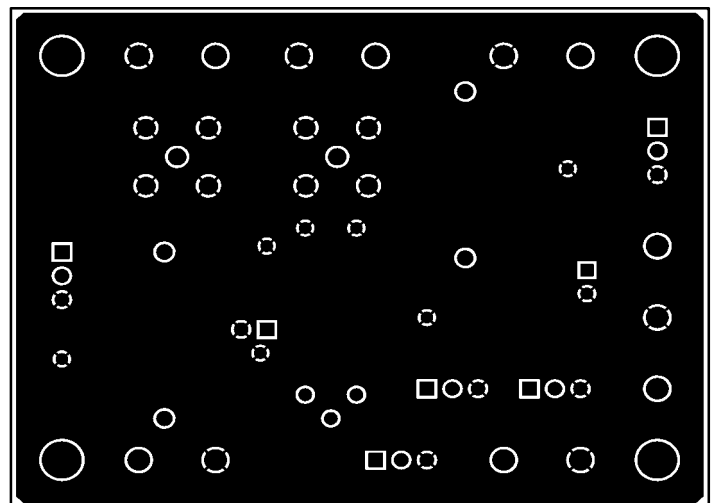
Evaluation Board Schematic



Evaluation Board Gerber Plots



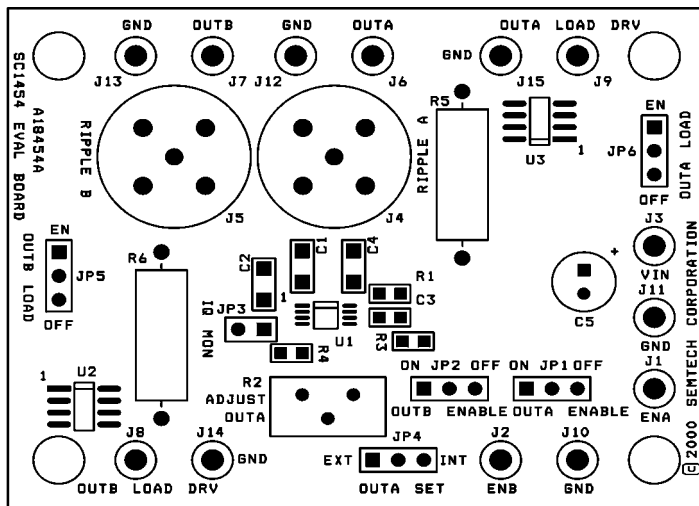
Top Copper



Bottom Copper

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Evaluation Board Gerber Plots (Cont.)



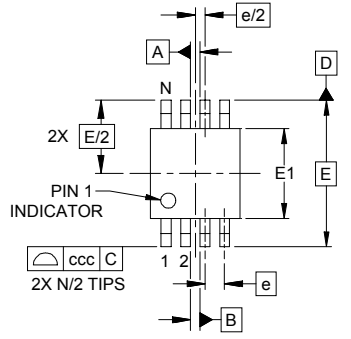
Top Assembly

Evaluation Board Bill Of Materials

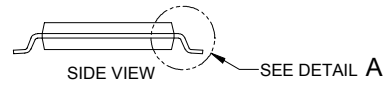
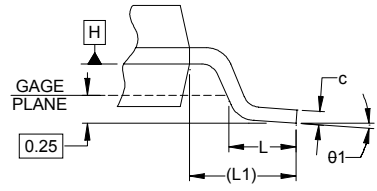
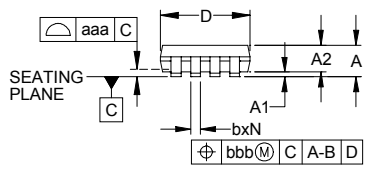
Quantity	Reference	Part/Description	Vendor	Notes
2	C1, C2	2.2µF ceramic	Murata	GRM42-6X7R225K16
1	C3	10nF ceramic	Various	
1	C4	1µF ceramic	Murata	GRM42-6X7R105K25
1	C5	220µF, 10V	Various	
2	J1, J2	Test pin	Various	White
3	J3, J6, J7	Test pin	Various	Red
2	J4, J5	BNC socket	Various	V _{OUT} ripple monitor
2	J8, J9	Test pin	Various	Orange
6	J10 - J15	Test pin	Various	Black
5	JP1, JP2, JP4 - JP6	Header, 3 pin	Various	
1	JP3	Header, 2 pin	Various	
2	R1, R3	10kΩ, 1/10W	Various	
1	R2	250kΩ, 25T	Bourns	Trimmer potentiometer
1	R4	62kΩ, 1/10W	Various	
2	R5, R6	150mA load	Various	1W, may not be same value
1	U1	SC1454xIMS	Semtech	
2	U2, U3	Si4410	Vishay	

POWER MANAGEMENT

Outline Drawing - MSOP-8

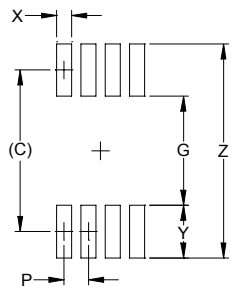


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.009	-	.015	0.22	-	0.38
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.026 BSC			0.65 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.005			0.13		
ccc	.010			0.25		



- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
 2. DATUMS [-A-] AND [-B-] TO BE DETERMINED AT DATUM PLANE [-H-]
 3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
 4. REFERENCE JEDEC STD MO-187, VARIATION AA.

Land Pattern - MSOP-8



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.026	0.65
X	.016	0.40
Y	.063	1.60
Z	.224	5.70

- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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