**SEMTECH**

POWER MANAGEMENT

Description

The SC1437 is a battery over voltage detection circuit with driver for external MOSFET. The trip point is adjustable with an external resistor divider connected to the SENSE pin. The trip point is preset to a nominal trip voltage of 4.2V if no external divider is used. Other internal trip voltages of 4.5V and 4.7V are available, specified by different part numbers. An internal delay, with two selectable times or bypass, is on-board to suppress accidental over voltage conditions due to glitches on the battery supply voltage, V+. The delay is externally adjustable by pulling the SEL pin high, low, or left floating. During an actual over voltage condition, the internal driver will pull the over voltage pin (OV) down to the voltage present at the V- pin. This insures the external N-Channel MOSFET will be completely off during an over voltage condition. Supply current during the monitoring mode of operation is approximately 10μA. If an over voltage condition is detected, supply currents increase when the timer is started. A voltage comparator will engage at voltages greater than 6.8V, which bypasses the timer and open circuits the battery by turning off the external MOSFET. This important function protects the battery during the timer delay in the event of a charger failure. There are three functional options available. With the B option the OV pin is active low. With the L option the OV pin is active high. With the H option the OV pin is open drain, active high. All options are available in a 5 lead SOT-23 package.

Features

◆ Low quiescent current, less than 10μA typical
◆ Input voltage range 1.8V to 6.8V
◆ Adjustable or preset voltage trip point
◆ Selectable timer delays of 0, 40 and 80ms without use of external resistor
◆ SOT-23 5 lead package
◆ Accuracy is 2% over specified temperature range
◆ 30V maximum rating

Applications

◆ Battery packs
◆ Portable electronics
◆ Lithium Ion protection circuits
◆ Programmable Fuse
◆ Power Monitoring
◆ CPU Reset Circuits

Typical Application Circuit

$$VTRIP = 2.1(1 + {}^{R2}/_{R1})$$

$$0.476 < ({}^{R2}/_{R1}) < 2$$

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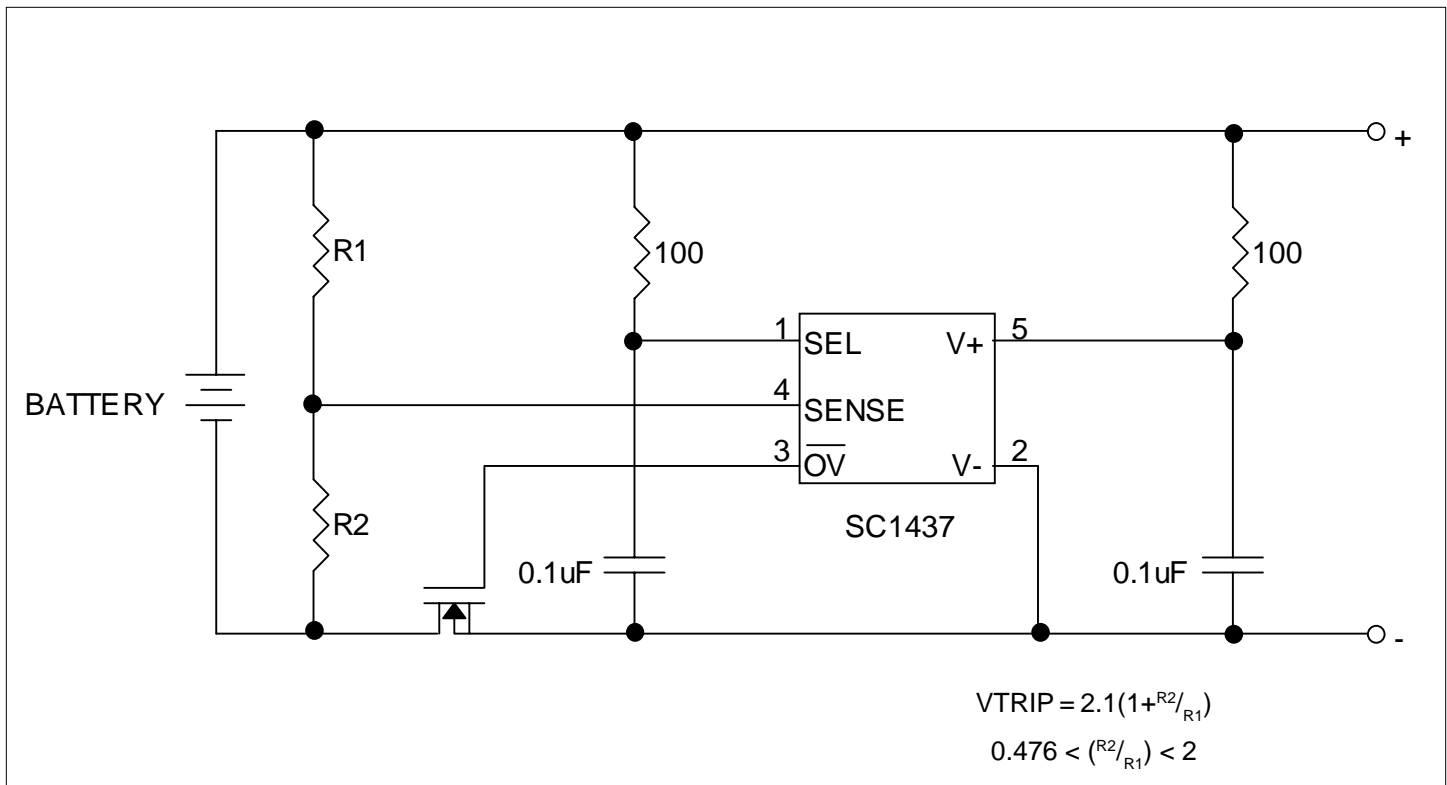
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Absolute Maximum Rating

Parameter	Symbol	Maximum	Units
V+ Supply Voltage to (V-)	V+	-0.3 to 30	V
Over Voltage Output to (V-)	OV	-0.3 to 8	V
Select to (V-)	SEL	-0.3 to 7	V
Sense to (V-)	SENSE	-0.3 to 7	V
Thermal Resistance Junction to Ambient	θ_{JA}	256	°C/W
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 sec.	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

## Electrical Characteristics

Unless specified, TA = 25 °C, V+ = 1.8V to 6.3V. Values in **bold** apply over the full operating temperature range.

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Supply Voltage	V+	Battery input voltage	1.8		6.3	V
Input Supply Current	I+	With internal divider; V+ = 4.7V		10	14	µA
Over Voltage Threshold with Respect to V-	V_{TRIP}	SENSE = V-, 4.2V Option	4.12	4.2	4.28	V
		SENSE = V-, 4.5V Option	4.41	4.5	4.59	V
		SENSE = V-, 4.7V Option	4.61	4.7	4.79	V
		External Divider, V_{SENSE} + 2.1V, V_{SENSE} = 1V to 4.2V		2		%
Input Bias Current	I_{BSEN}	Sense Pin			1	µA
	I_{BSEL}	Select Pin			1	µA
OV Threshold Hystersis	hyst	SENSE = V-, 4.2V Option		420		mV
		SENSE = V-, 4.5V Option		450		
		SENSE = V-, 4.7V Option		470		
		SENSE = resistor divider		V_{TRIP} * 0.1		
OV Drive Current	OV_{DRV}	B Version		150		uA
		H & L Version; R = 100K, V+ = 4.2V		42		uA
Delay	t_{delay}	With SEL = V+		0		ms
		With SEL = V-	24	40	56	
		With SEL = no connect	48	80	112	
Clamp Voltage	V_{CLMP}	Step Voltage = 3V to 15V		6.8		V
Turn Off Time	t_{off}	Turn off time of external FET with gate cap = 1nF			50	µsec
Turn-Off Time	t_{offbpt}	6.8V Bypass Timer Comparator		50		µsec

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Pin Configuration

Top View

| SEL | 1 | | 5 | V+ |

| V- | 2 | | | |

| OV | 3 | | 4 | SENSE |
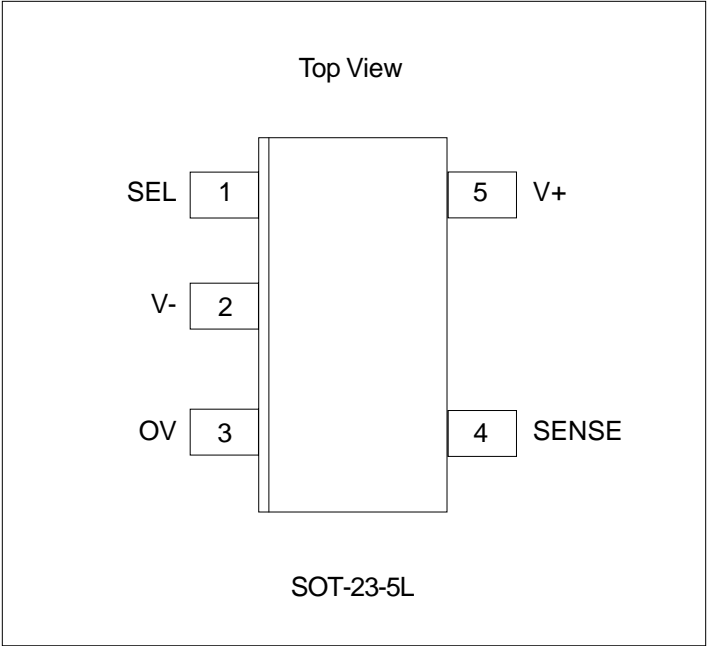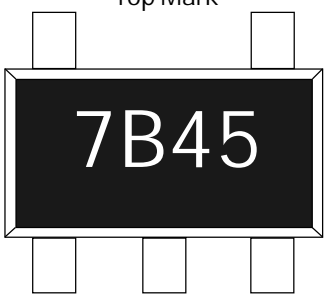
SOT-23-5L

Ordering Information

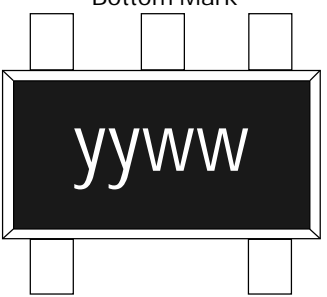| DEVICE[1]	PACKAGE
SC1437ISK-BXXTR	SOT-23-5L
SC1437ISK-HXXTR	SOT-23-5L
SC1437ISK-LXXTR	SOT-23-5L

Notes:
(1) Where XX = 42 (4.2V), 45 (4.5V), 47 (4.7V)
Only available in tape and reel packaging.
A reel contains 3,000 devices.

Marking Information

Top Mark

7B45

Bottom Mark

yyww

7 = SC1437 Device
Output Option: B = Output active low
                 L = Output active high
                 H = Output active high, with open drain
Voltage Option: 42 = 4.2V; 45 = 4.5V; 47 = 4.7V

yy = two-digit year of manufacture
ww = two-digit week of manufacture

Pin Descriptions

Pin #	Pin Name	Pin Function
1	SEL	Input for timer delay selection (V+, gnd or no connect).
2	V-	Negative terminal of charger.
3	OV	Over-voltage output. Active low for version B. Active high for versions H & L.
4	SENSE	Voltage divider input for adjusting over voltage trip point. Tie to V- for voltage monitor configuration.
5	V+	Input supply pin.

Block Diagram

* Based on version selected 4.2V, 4.5V, 4.7V
t B option: Output active low
 L option: Output active high
 H option: Output active high, open drain

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Applications Information

The SC1437 can be used as a battery over voltage detection circuit with driver for an external MOSFET. In this configuration the SC1437 is capable of protecting the battery if the charger circuit fails. Because of its low cost, the SC1437 is an excellent choice in cases when primary discharge protection is not required. The part is an excellent choice for secondary over voltage protection where the battery has primary fault and discharge protection, but could benefit by adding another line of defense against charger failure.

The SC1437 comes in three voltage trip options and three function options. The voltage options are 4.2V, 4.5V or 4.7V. In addition, the trip voltage levels can be adjusted with an external resistive divider.

The SC1437 also has three separate functional options that affect the OV pin action:

With the B option, the OV pin is active low and is used to drive an N-Channel MOSFET.

With the H option, the OV pin is active high with open drain to drive a P-Channel MOSFET.

Finally, the L option is active high and it's output is 5V logic high for specific use as a voltage detector flag.

Any part can be configured as a voltage detector as shown in Figure 1. A programmable trip delay can be set as indicated by Table 1. In Figure 1, the trip voltage is set externally by R1 & R2. while the trip delay is set to 0 seconds plus any propagation delay of the SC1437 to allow the MOSFET to turn off, specified by parameter toff.

TABLE 1

SEL CONNECTION	DELAY
V+	NO DELAY
V-	40mS
OPEN	80mS

CHARGER OVERVOLTAGE PROTECTION

The SC1437 configuration for secondary overvoltage protection is shown in Figure 2. This is the Evaluation Board schematic. The Evaluation Board is set up to work with either internal trip voltage or external trip voltage via R1 and R2. It also can set the trip delay to all three values through jumper selection of JP2 and JP3.

With CHARGER+ and CHARGER- input applied, the charger voltage will be filtered by R3 and C1. The filtered voltage will then be sensed by the V+ input. In this case the trip voltage can be set to a value other than the internal setting of 4.2V. This is done by using the on-board external resistor divider and removing JP1 shunt jumper that will allow the resistors R1 and R2 to program a trip voltage of 5.75V. The Evaluation Board also

allows the trip delay to be set to 0S, 40mS or 80mS by application of a jumper JP2, JP3 or leaving the jumper off, respectively. Configuration of timing delays are shown in Table 1. Once the trip delay is set to the required value the SC1437 will monitor the charger voltage. If the charger voltage equals or exceeds 5.5V the OV pin will transition from high to low (Version B) turning Q1 off, thereby breaking the circuit and protecting the battery from overvoltage.

Figure 3 shows the trip delay of 80mS, while Figure 4 shows the trip delay set to 40mS and Figure 5 shows no delay set.

FIGURE 1
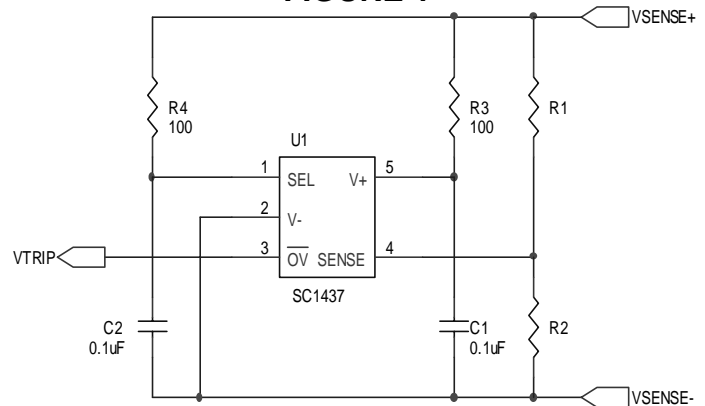
VOLTAGE DETECTOR: TRIP DELAY = 0

$$VTRIP = 2.1(1 + {}^{R2}/_{R1})$$

$$0.476 < ({}^{R2}/_{R1}) < 2$$

When using the program resistors R1 & R2, Figure 2, to set an alternate trip voltage, be sure these resistors are placed across the battery on the drain side of the MOSFET. This will eliminate any voltage drop errors caused by the MOSFET on resistance. Figure 6 and Figure 7 shows the normalized trip voltage variation with respect to temperature. Note that in all cases the trip voltage remains within its 2% specified range. This is true for both the internal trip voltage and externally set trip voltage, however when using an external resistor divider, the tolerance and temperature coefficient of the resistors will add to the overall device error. Choice of the resistor tolerance and temperature coefficient will depend on your error budget. We also recommend using high value resistors to limit battery current drain. Values between 100K and 1M should suffice without introducing excessive noise into the IC.

CHOOSING THE EXTERNAL MOSFET

The external switch must be a logic level MOSFET. Most logic level MOSFETs have threshold voltages in the 1V range and can handle a gate to source voltage (VGS) of 12V which is well above the clamp voltage of the SC1437. In addition, the selection should be able to handle the charging current of the battery over all temperature ranges. Whether to use a P-Channel or N-Channel MOSFET depends upon the option chosen. The B option requires the use of a N-Channel MOSFET while the H option uses a P-Channel MOSFET.
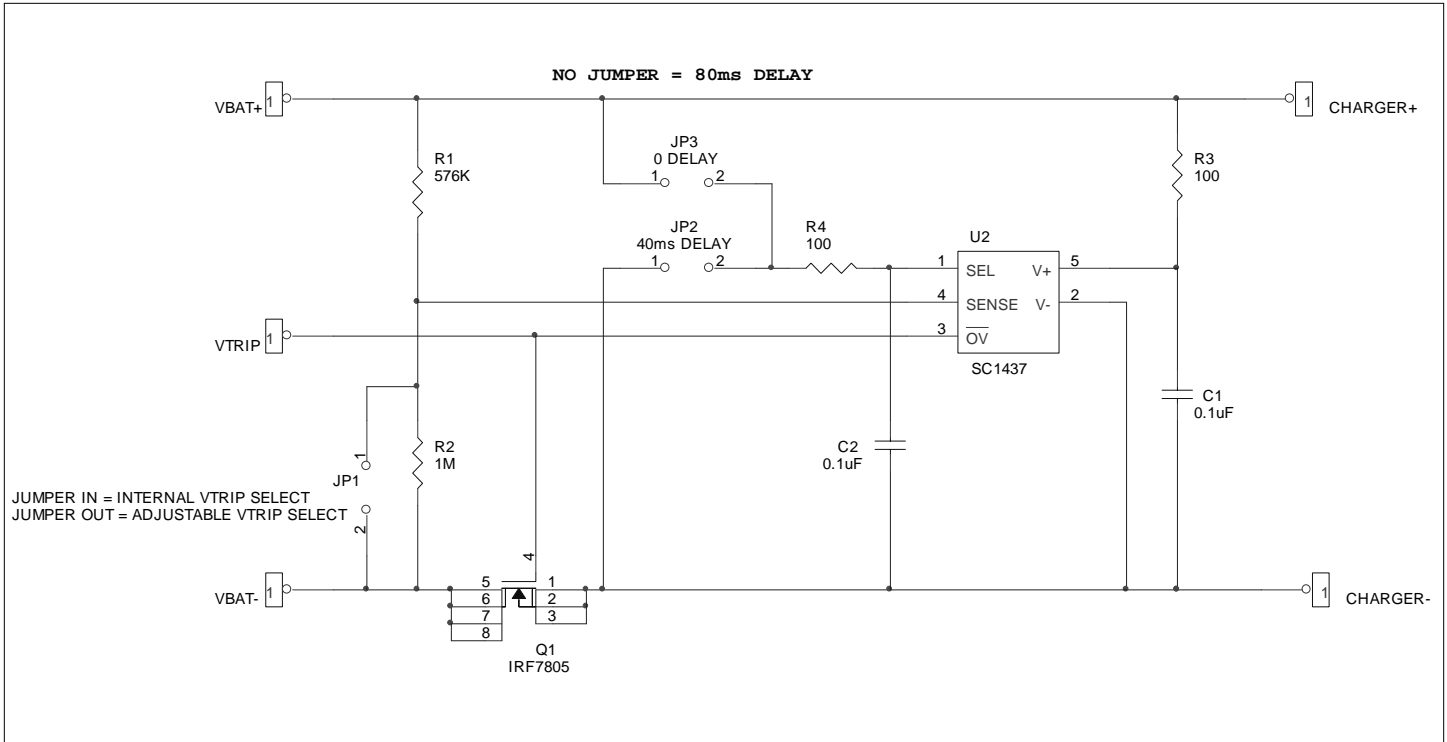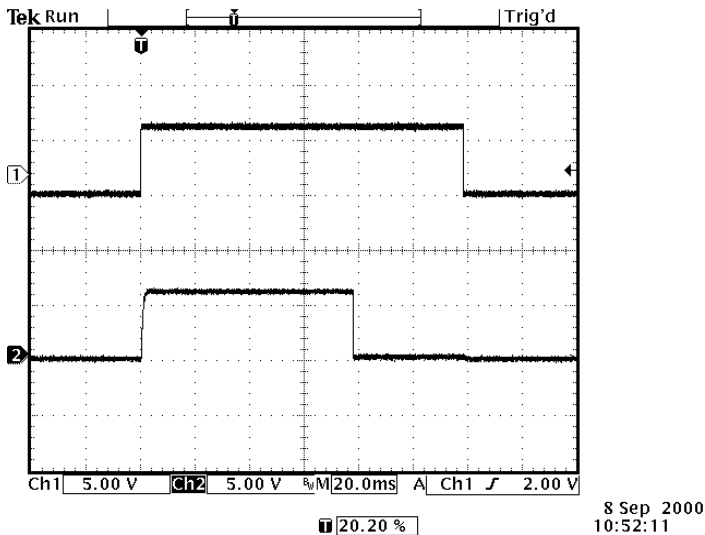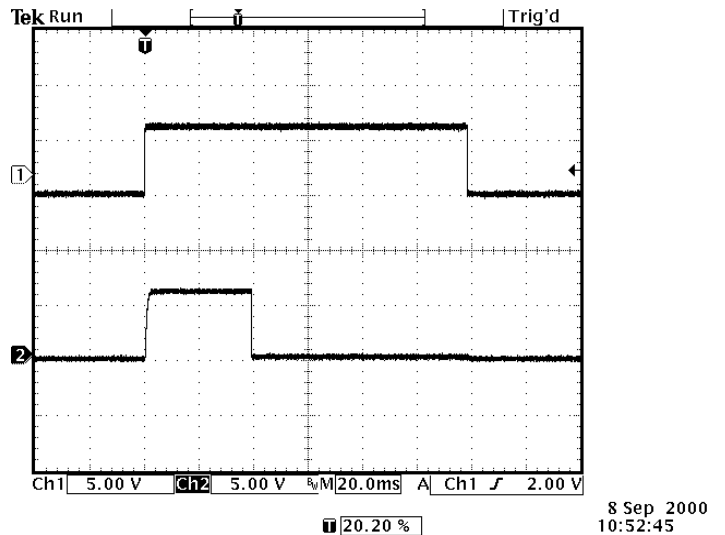
FIGURE 2

FIGURE 3: Trip Delay set to 80mS, JP3 & JP2 Open.

Top Trace: Charger Voltage, 5V/div

Bottom Trace: VTRIP, 5V/div

Timebase: 20ms/div
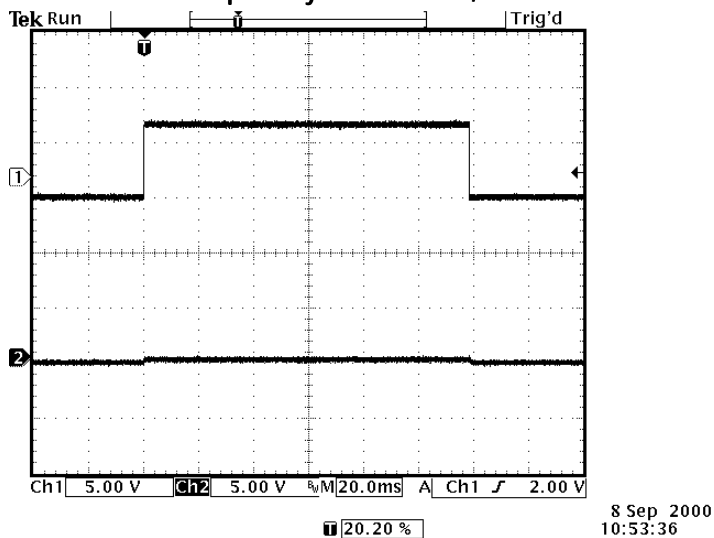
FIGURE 4: Trip delay Set to 40mS, JP2 Shorted.

Top Trace: Charger Voltage, 5V/div

Bottom Trace: VTRIP, 5V/div

Timebase: 20ms/div

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Applications Information Continued

FIGURE 5: Trip delay Set to 0mS, JP3 Shorted.

Top Trace: Charger Voltage, 5V/div

Bottom Trace: VTRIP, 5V/div

Timebase: 20ms/div

FIGURE 6: Internal Trip Voltage (4.7V) Deviation Plotted Against Temperature.
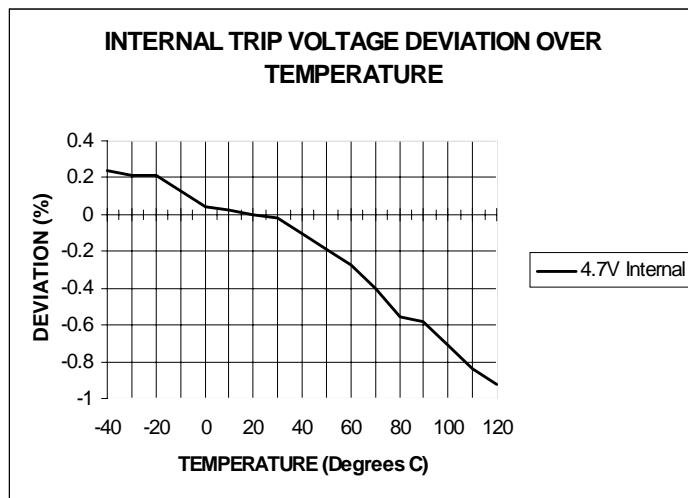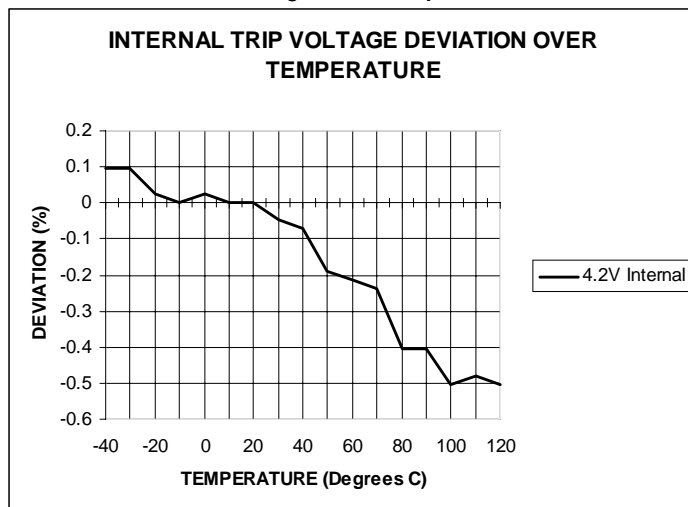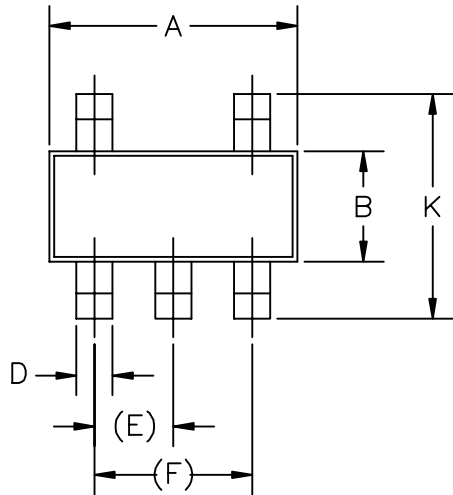

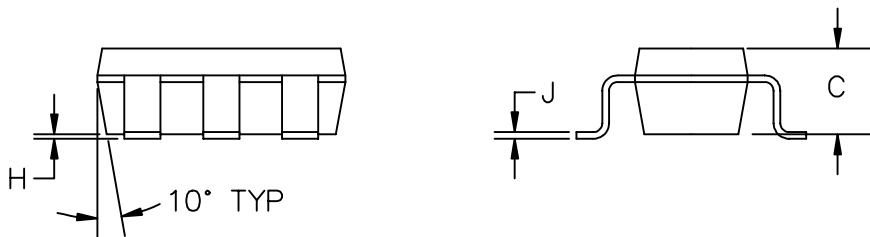**FIGURE 7: Internal Trip Voltage (4.2V) Deviation Plotted Against Temperature.**

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Outline Drawing - SOT23-5

DIMENSIONS					
DIMⁿ	INCHES		MM [1]		NOTE
	MIN	MAX	MIN	MAX	
A	.110	.120	2.80	3.05	–
B	.059	.070	1.50	1.75	–
C	.036	.051	.90	1.30	–
D	.014	.020	.35	.50	–
E	–	.037	–	0.95	REF
F	–	.075	–	1.90	REF
H	–	.006	–	.150	–
J	.0035	.008	.090	.20	–
K	.102	.118	2.6	3.00	–

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - SOT23-5
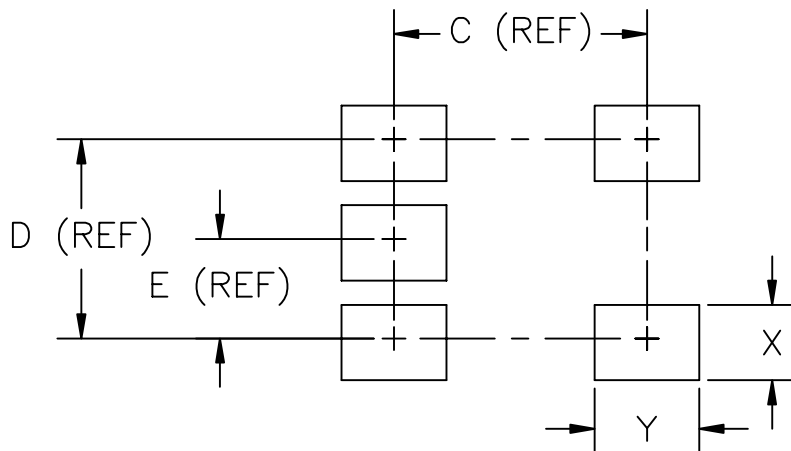
DIMENSIONS			
DIMⁿ	INCHES	MM	NOTE
C	.094	2.4	–
D	.074	1.9	–
E	.037	.95	–
X	.028	.7	–
Y	.039	1.0	–

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