DATA SHEET

74AHC377; 74AHCT377
Octal D-type flip-flop with data enable; positive-edge trigger

Product specification
File under Integrated Circuits, IC06

2000 Aug 15

Philips Semiconductors

Octal D-type flip-flop with data enable; positive-edge trigger

74AHC377; 74AHCT377

FEATURES

- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V
  CDM EIA/JESD22-C101 exceeds 1000 V
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Ideal for addressable register applications
- Data enable for address and data synchronization
- Eight positive-edge triggered D-type flip-flops
- See “273” for master reset version
- See “373” for transparent latch version
- See “374” for 3-state version
- For AHC only: operates with CMOS input levels
- For AHCT only: operates with TTL input levels
- Specified from –40 to +85 and from –40 to +125 °C.

DESCRIPTION

The 74AHC/AHCT377 D-type flip-flops are high-speed silicon-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74AHC/AHCT377 devices have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. A common clock (CP) input loads all flip-flops simultaneously when the data enable ($\overline{E}$) is LOW. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

The $\overline{E}$ input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC	AHCT	
t_{PHL}/t_{PLH}	propagation delay; CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	3.9	4.0	ns
f_{max}	maximum clock frequency	C_L = 15 pF; V_{CC} = 5 V	175	140	MHz
C_I	input capacitance	$V_I = V_{CC}$ or GND	3.0	3.0	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; notes 1 and 2	20	23	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{E}$	CP	D_n	Q_n
load “1”	l	↑	h	H
load “0”	l	↑	l	L
hold (do nothing)	h	↑	X	no change
	H	X	X	no change

Note

1. H = HIGH voltage level;
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
   L = LOW voltage level;
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
   X = don’t care;
   ↑ = LOW-to-HIGH CP transition.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74AHC377D	20	SO	plastic	SOT163-1
74AHC377PW	20	TSSOP	plastic	SOT360-1
74AHCT377D	20	SO	plastic	SOT163-1
74AHCT377PW	20	TSSOP	plastic	SOT360-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{E}$	data enable input (active LOW)
2, 5, 6, 9, 12, 15, 16 and 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17 and 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge triggered)
20	V_{CC}	DC supply voltage

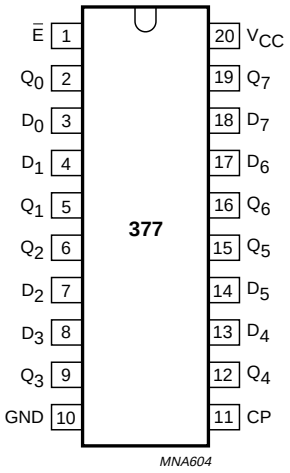


Fig.1 Pin configuration.

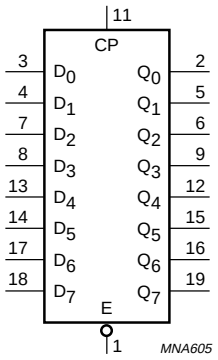


Fig.2 Logic symbol.

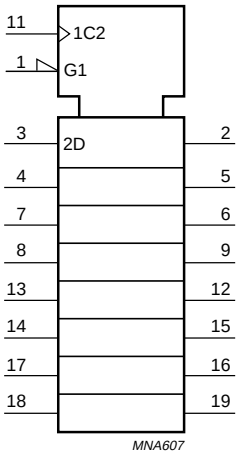


Fig.3 IEC logic symbol

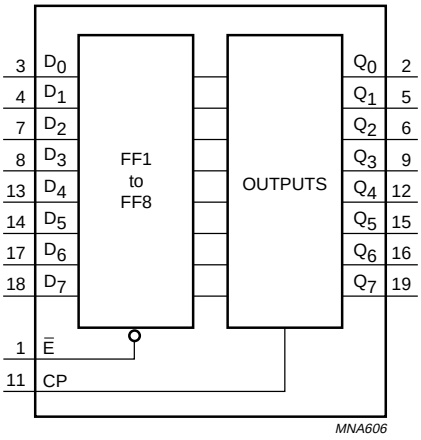


Fig.4 Functional diagram.

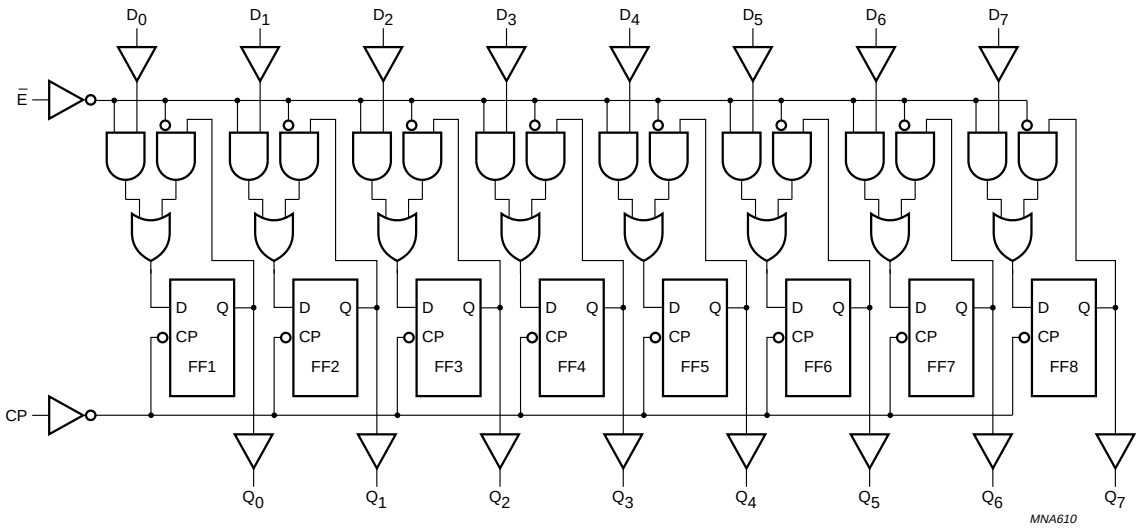


Fig.5 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC			74AHCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	DC supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	+25	+125	–40	+25	+125	°C
t_r, t_f ($\Delta t/\Delta f$)	input rise and fall rates	V_{CC} = 3.3 V ±0.3 V	–	–	100	–	–	–	ns/V
		V_{CC} = 5 V ±0.5 V	–	–	20	–	–	20	

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		–0.5	+7.0	V
V_I	input voltage range		–0.5	+7.0	V
I_{IK}	DC input diode current	V_I < –0.5 V; note 1	–	–20	mA
I_{OK}	DC output diode current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V; note 1	–	±20	mA
I_O	DC output source or sink current	–0.5 V < V_O < V_{CC} + 0.5 V	–	±25	mA
I_{CC}	DC V_{CC} or GND current		–	±75	mA
T_{stg}	storage temperature range		–65	+150	°C
P_D	power dissipation per package	for temperature range: –40 to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO packages: above 70 °C the value of P_D derates linearly by 8 mW/K.
   For TSSOP packages: above 60 °C the value of P_D derates linearly by 5.5 mW/K.

DC CHARACTERISTICS

74AHC family

With regard to recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			–40 to +85		–40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	1.5	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	2.1	–	
			5.5	3.85	–	–	3.85	–	3.85	–	
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	–	0.9	
			5.5	–	–	1.65	–	1.65	–	1.65	
V_{OH}	HIGH-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; $I_O = -50$ µA	2.0	1.9	2.0	–	1.9	–	1.9	–	V
			3.0	2.9	3.0	–	2.9	–	2.9	–	
			4.5	4.4	4.5	–	4.4	–	4.4	–	
	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -4.0$ mA	3.0	2.58	–	–	2.48	–	2.40	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -8.0$ mA	4.5	3.94	–	–	3.8	–	3.70	–	
V_{OL}	LOW-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; $I_O = 50$ µA	2.0	–	0	0.1	–	0.1	–	0.1	V
			3.0	–	0	0.1	–	0.1	–	0.1	
			4.5	–	0	0.1	–	0.1	–	0.1	
	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 4$ mA	3.0	–	–	0.36	–	0.44	–	0.55	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 8$ mA	4.5	–	–	0.36	–	0.44	–	0.55	
I_I	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	0.1	–	1.0	–	2.0	µA
I_{OZ}	3-state output OFF current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	5.5	–	–	±0.25	–	±2.5	–	±10.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	4.0	–	40	–	80	µA
C_I	input capacitance		–	–	3	10	–	10	–	10	pF

74AHCT family

With regard to recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			–40 to +85		–40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	2.0	–	2.0	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	–	0.8	–	0.8	V
V_{OH}	HIGH-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; $I_O = –50$ µA	4.5	4.4	4.5	–	4.4	–	4.4	–	V
	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = –8.0$ mA	4.5	3.94	–	–	3.8	–	3.70	–	V
V_{OL}	LOW-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; $I_O = 50$ µA	4.5	–	0	0.1	–	0.1	–	0.1	V
	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 8$ mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I_I	input leakage current	$V_I = V_{IH}$ or V_{IL}	5.5	–	–	0.1	–	1.0	–	2.0	µA
I_{OZ}	3-state output OFF current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$	5.5	–	–	±0.25	–	±2.5	–	±10.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	4.0	–	40	–	80	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} – 2.1$ V other inputs at V_{CC} or GND; $I_O = 0$	4.5 to 5.5	–	–	1.35	–	1.5	–	1.5	mA
C_I	input capacitance		–	–	3	10	–	10	–	10	pF

AC CHARACTERISTICS

Type 74AHC377

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

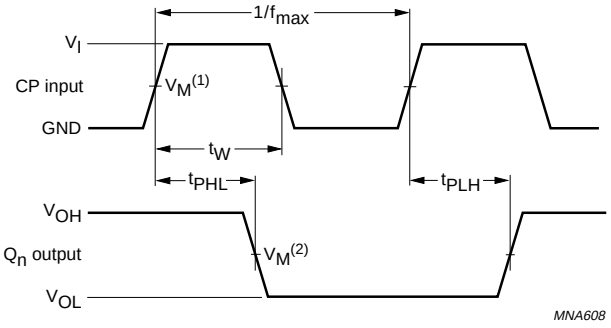
SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	C_L	25			–40 to +85		–40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 3.0 to 3.6 V; typical values at V_{CC} = 3.3 V											
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	see Figs 6 and 8	15 pF	–	5.6	12.8	1.0	15.0	1.0	16.0	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 8		80	125	–	70	–	70	–	MHz
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	see Figs 6 and 8	50 pF	–	8.0	16.0	1.0	18.0	1.0	20.0	ns
t_W	clock pulse width HIGH or LOW	see Figs 6 and 8		5.0	–	–	5.0	–	5.0	–	ns
t_{su}	set-up time D_n to CP	see Figs 7 and 8		5.0	–	–	5.0	–	5.0	–	ns
	set-up time $\overline{E}$ to CP			5.0	–	–	5.0	–	5.0	–	ns
t_h	hold time D_n to CP			1.5	–	–	1.5	–	1.5	–	ns
	hold time $\overline{E}$ to CP			1.5	–	–	1.5	–	1.5	–	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 8		50	75	–	45	–	45	–	MHz
V_{CC} = 4.5 to 5.5 V; typical values at V_{CC} = 5.0 V											
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	see Figs 6 and 8	15 pF	–	3.9	9.0	1.0	10.5	1.0	11.5	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 8		125	175	–	110	–	110	–	MHz
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	see Figs 6 and 8	50 pF	–	5.6	10.5	1.0	12.0	1.0	13.5	ns
t_W	clock pulse width HIGH or LOW	see Figs 6 and 8		5.0	–	–	5.0	–	5.0	–	ns
t_{su}	set-up time D_n to CP	see Figs 7 and 8		4.5	–	–	4.5	–	4.5	–	ns
t_{su}	set-up time $\overline{E}$ to CP			4.5	–	–	4.5	–	4.5	–	ns
t_h	hold time D_n to CP			2.0	–	–	2.0	–	2.0	–	ns
t_h	hold time $\overline{E}$ to CP			2.0	–	–	2.0	–	2.0	–	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 8		85	120	–	75	–	75	–	MHz

Type 74AHCT377

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

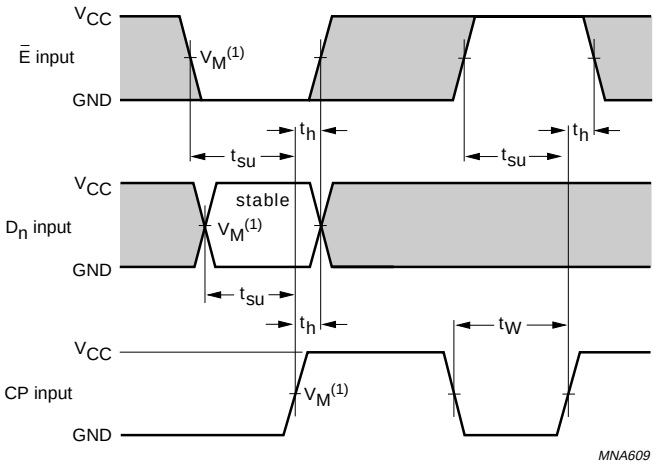
SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	C_L	25			–40 to +85		–40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 4.5 to 5.5 V; typical values at V_{CC} = 5.0 V											
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	see Figs 6 and 8	15 pF	–	4.0	9.0	1.0	10.5	1.0	11.5	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 8		90	140	–	80	–	80	–	MHz
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	see Figs 6 and 8	50 pF	–	5.7	10.5	1.0	12.0	1.0	13.5	ns
t_W	clock pulse width HIGH or LOW	see Figs 6 and 8		5.0	–	–	5.0	–	5.0	–	ns
t_{su}	set-up time D_n to CP	see Figs 7 and 8		4.5	–	–	4.5	–	4.5	–	ns
	set-up time $\overline{E}$ to CP			4.5	–	–	4.5	–	4.5	–	ns
t_h	hold time D_n to CP			2.0	–	–	2.0	–	2.0	–	ns
	hold time $\overline{E}$ to CP			2.0	–	–	2.0	–	2.0	–	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 8		85	130	–	75	–	75	–	MHz

AC WAVEFORMS



FAMILY	V_I INPUT REQUIREMENTS	V_M(1) INPUT	V_M(2) OUTPUT
AHC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT	GND to 3.0 V	1.5 V	50% V_{CC}

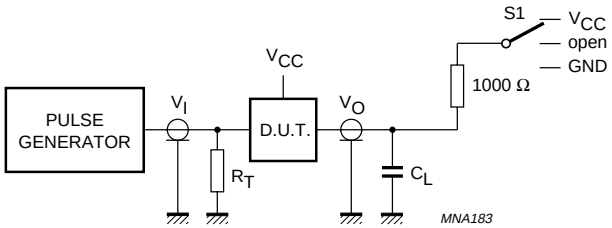
Fig.6 The clock (CP) to output (Q_n) propagation delays.



FAMILY	V_I INPUT REQUIREMENTS	V_M(1) INPUT
AHC	GND to V_{CC}	50% V_{CC}
AHCT	GND to 3.0 V	1.5 V

The shaded areas indicate when the input is permitted to change for predicable output performance.

Fig.7 The data set-up and hold times for D_n input

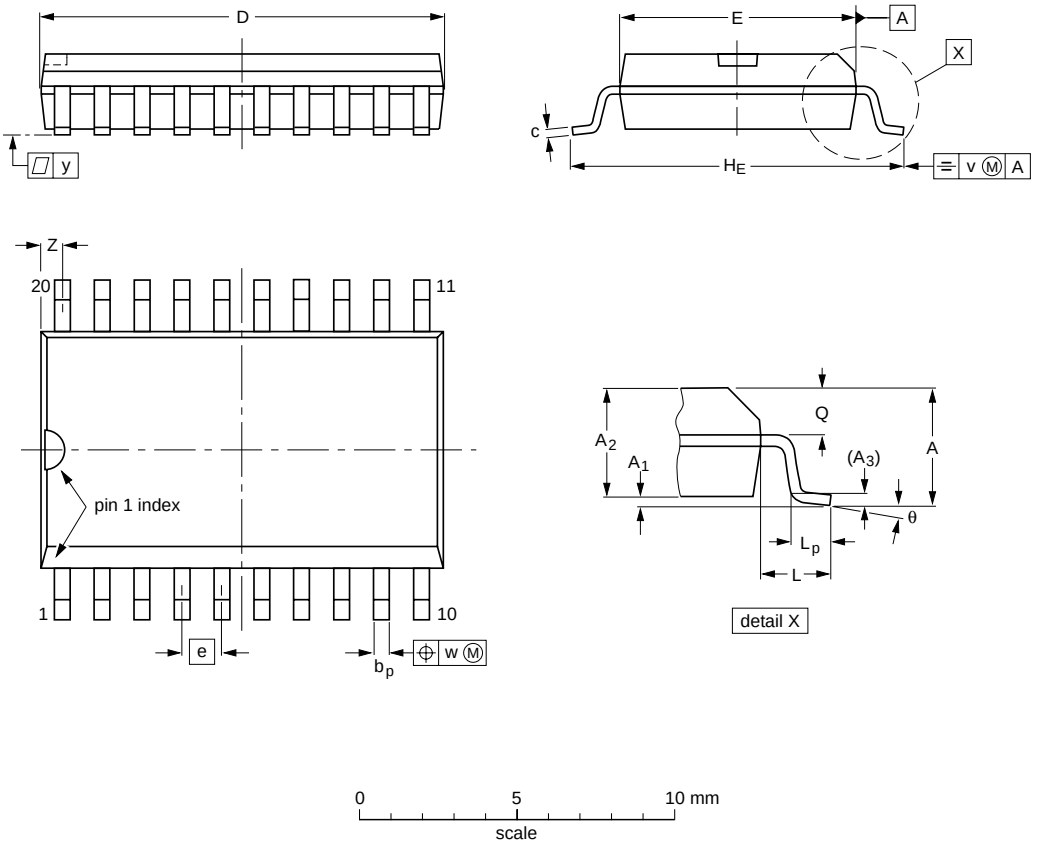


TEST	S_1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.8 Load circuit for switching times.

PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

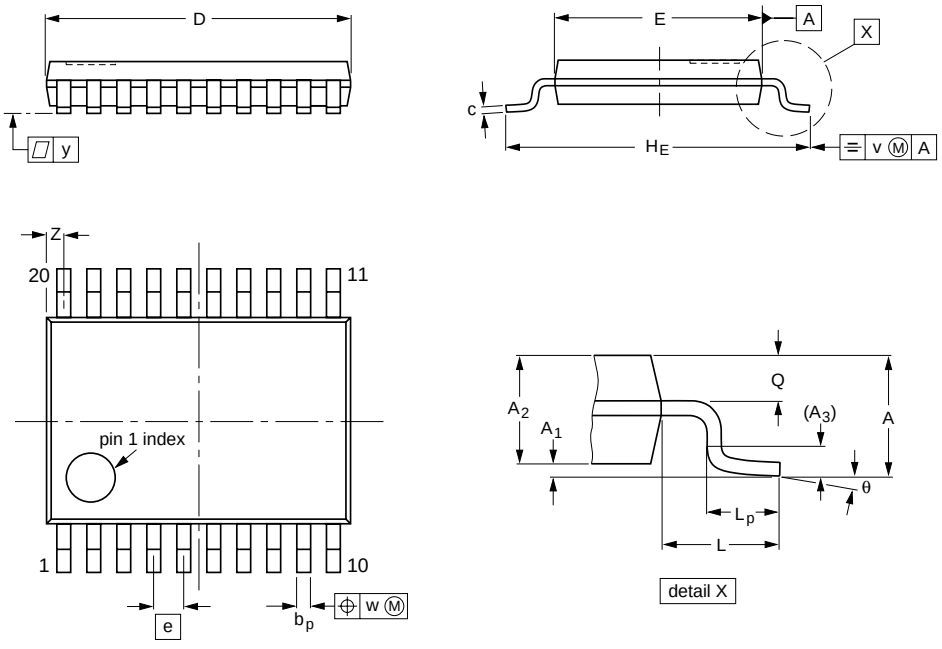
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

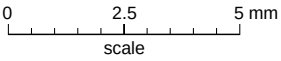
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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