TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74ACT139P, TC74ACT139F, TC74ACT139FN, TC74ACT139FT

DUAL 2-TO-4 LINE DECODER

The TC74ACT139 is an advanced high speed CMOS 2 to 4 LINE DECODER fabricated with silicon gate and double layer metal wiring C2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

The active low enable input can be used for gating or it can be used as a data input for demultiplexing applications.

When the enable input is held "H", all four outputs are fixed at a high logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

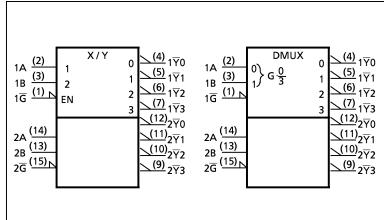
- High Speed······ $t_{pd} = 5.5 \text{ns}(typ.)$ at $V_{CC} = 5V$
- \bullet Compatible with TTL outputs $\cdots\,V_{I\,L}=0.8V$ (Max.)

 $V_{IH} = 2.0V (Min.)$

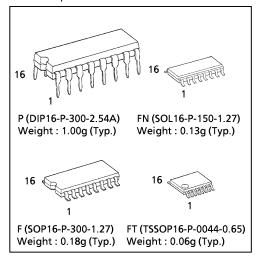
- Symmetrical Output Impedance··· $| I_{OH} | = I_{OL} = 24$ mA(Min.)

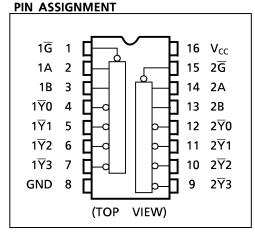
 Capability of driving 50Ω transmission lines.
 -
- \bullet Balanced Propagation Delays…… $t_{pLH}\!\simeq\!t_{pHL}$
- Pin and Function Compatible with 74F139

IEC LOGIC SYMBOL



(Note) The JEDEC SOP (FN) is not available in Japan.



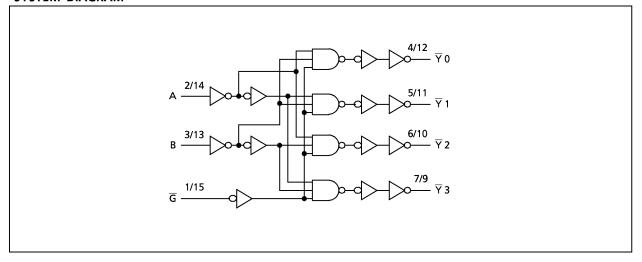


TRUTH TABLE

INP	INPUTS			DUT				
ENABLE	SELECT		∀ 0	<u>₹</u> 1	<u> </u>	<u></u>	SELECTED OUTPUT	
G	В	Α	Y 0	YI	Y 2	13	COTPUT	
Н	Х	Х	Н	Н	Н	Н	NONE	
L	L	L	L	Н	Н	Н	∀ 0	
L	L	Н	Н	L	Н	Н	∀ 1	
L	Н	L	Η	Н	L	Н	₹2	
L	Н	Η	Η	Н	Н	L	₹3	

X : Don't Care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{cc}	-0.5~7.0	V
DC Input Voltage	V _{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V _{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	IIK	± 20	mA
Output Diode Current	I _{OK}	± 50	mΑ
DC Output Current	I _{OUT}	± 50	mΑ
DC V _{CC} /Ground Current	I _{cc}	± 200	mΑ
Power Dissipation	P _D	500 (DIP)* /180 (SOP/TSSOP)	mW
Storage Temperature	T _{stg}	−65~150	°C

^{*500}mW in the range of Ta = -40° C ~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{CC}	4.5~5.5	V
Input Voltage	VIN	0~V _{cc}	٧
Output Voltage	V _{OUT}	0~V _{cc}	٧
Operating Temperature	T _{opr}	−40~85	°C
Input Rise and Fall Time	dt/dV	0~10	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CO	TEST CONDITION		Ta = 25°C			Ta = -4	UNIT	
FARAIVICIER SYN		TEST CONDITION		V _{cc} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	OIVIII
High - Level Input Voltage	V _{IH}			4.5 \$ 5.5	2.0	ı	_	2.0	_	V
Low - Level Input Voltage	VIL			4.5 \$ 5.5	_	ı	0.8	_	0.8	V
High - Level Output Voltage	V _{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50 \mu A$ $I_{OH} = -24 m A$ $I_{OH} = -75 m A^*$	4.5 4.5 5.5	4.4 3.94 —	4.5 — —		4.4 3.80 3.85	_ _ _	V
Low - Level Output Voltage	V _{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50 \mu A$ $I_{OL} = 24 m A$ $I_{OL} = 75 m A*$	4.5 4.5 5.5		0.0 _ _	0.1 0.36 —	1 1 1	0.1 0.44 1.65	V
Input Leakage Current	I _{IN}	$V_{IN} = V_{CC}$ or GND		5.5	_	1	± 0.1	_	± 1.0	
	I _{cc}	V _{I N} = V _{CC} or GND PER INPUT : V _{IN} = 3.4V OTHER INPUT : V _{CC} or GND		5.5	_	_	8.0	_	80.0	μΑ
Quiescent Supply Current	I _C			5.5	_	_	1.35	_	1.5	mA

^{* :} This spec indicates the capability of driving 50Ω transmission lines. One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500 Ω , Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		-	Ta = 25°C	•	$Ta = -40 \sim 85^{\circ}C$		UNIT
	STIVIBUL		V _{cc} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	OIVII
Propagation Delay Time (A, $B-\overline{Y}$)	t _{pLH} t _{pHL}		5.0 ± 0.5	1	6.2	9.2	1.0	10.5	
Propagation Delay Time $(\overline{G}-\overline{Y})$	t _{pLH} t _{pHL}		5.0 ± 0.5	1	6.3	9.6	1.0	11.0	ns
Input Capacitance	C _{IN}			1	5	10	_	10	рF
Power Dissipation Capacitance	C _{PD} (1)			-	51	_	_	_	рг

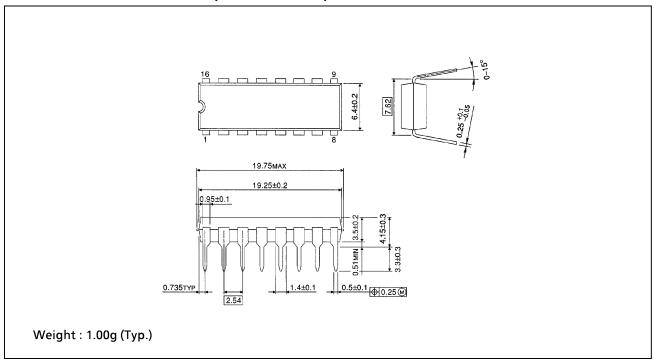
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per Decoder)}$$

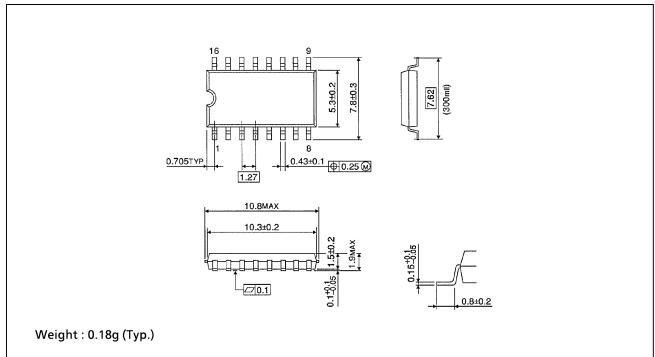
DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

Unit in mm



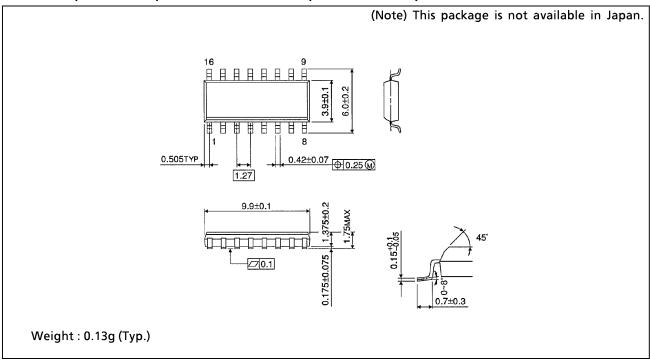
SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm



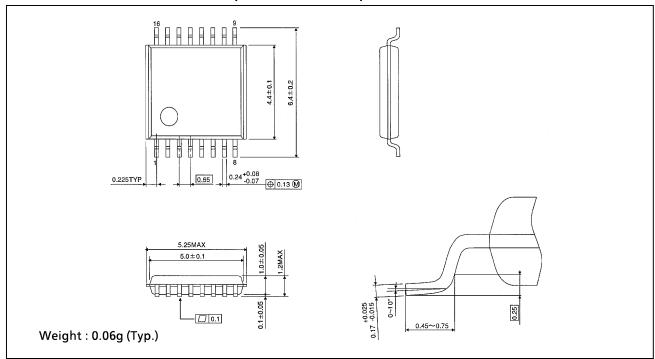
SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150-1.27)

Unit in mm



TSSOP 16PIN PACKAGE DIMENSIONS (TSSOP16-P-0044-0.65)

Unit in mm



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