PI5A3159

SOTINY™ 1Ω Low-Voltage SPDT Analog Switch

Features

- CMOS Technology for Bus and Analog Applications
- Low On-Resistance: 2Ω at 3.0V
- Wide V_{CC} Range: +1.8V to +5.5V
- Low Power Consumption : 5µW
- Rail-to-Rail switching throughout Signal Range
- Fast Switching Speed: 30ns max. at 5V
- High Off Isolation: –57dB at 10MHz
- –57dB (1 MHz) Crosstalk Rejection Reduces Signal Distortion
- Break-Before-Make Switching
- Extended Industrial Temperature Range: –40°C to 85°C
- Low On-Resistance Replacement for NC7SB3157
- Packaging (Pb-free & Green available):
  - 6-pin SOT-23 (T)
  - 6-contact TDFN-6 (ZC)

Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Battery Powered Communications
- Computer Peripherals

Pin Description

Pin Number	Name	Description
1	B_1	Data Port
2	GND	Ground
3	B_0	Data Port (Normally Closed)
4	A	Common Output/Data Port
5	V_{CC}	Positive Power Supply
6	S	Logic Control

Logic Function Table

Logic Input(s)	Function
0	B_0 Connected to A
1	B_1 Connected to A

Description

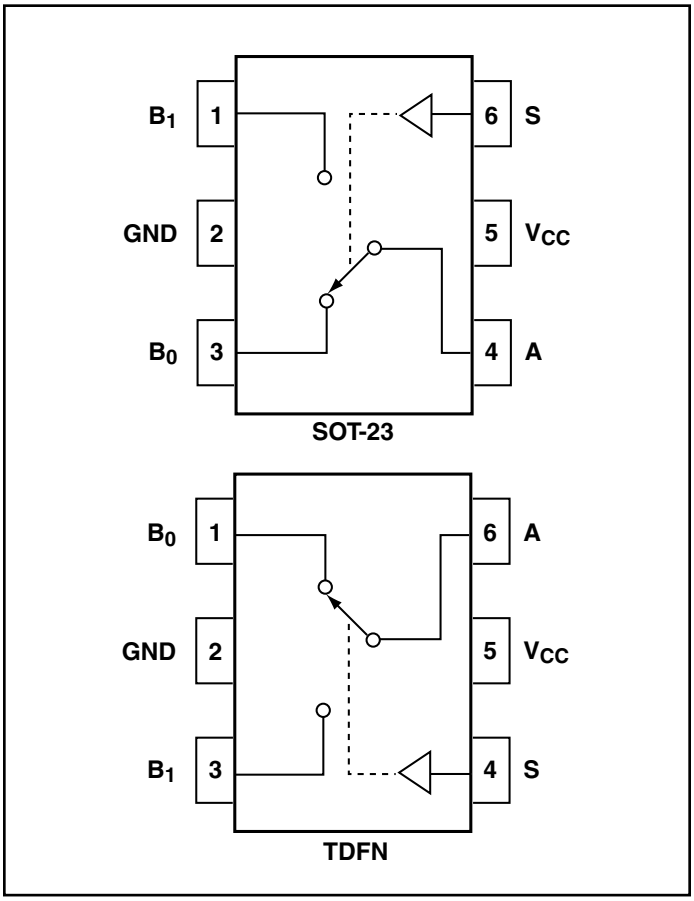
The PI5A3159 is a high-bandwidth, fast single-pole double-throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage range, 1.8V to 5.5V, the PI5A3159 has a maximum On-Resistance of 4Ω at 1.8V, 2.4Ω at 2.3V & 1Ω at 4.5V.

Break-before-make switching prevents both switches being enabled simultaneously. This eliminates signal disruption during switching.

Control input, S, tolerates input drive signals up to 5.5V, independent of supply voltage.

PI5A3159 is a low On-Resistance replacement for the PI5A3157 and NC7SB3157.

Connection Diagrams



Absolute Maximum Ratings

Voltages Referenced to GND
V+ ..... –0.5V to +5.5V

V_{IN}, V_{COM}, V_{NC}, V_{NO} (1) ..... –0.5V to V_+ +0.3V
or 30mA, whichever occurs first

Current (any terminal) ..... ±200mA

Peak Current, COM, NO, NC
(Pulsed at 1ms, 10% duty cycle) ..... ±400mA

Thermal Information

Continuous Power Dissipation

SOT23 (derate 7.1mW/ºC above +70ºC) 0.5W

Storage Temperature ..... –65ºC to +150ºC

Lead Temperature (soldering, 10s) ..... +300ºC

Note:

1. Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to 30mA.

***Caution**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Single +5V Supply

(V+ = +5V ± 10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp(°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch							
Analog Signal Range(3, 4)	V_{ANALOG}		Full	0		V+	V
On-Resistance	R_{ON}	V+ = 4.5V, I_{COM} = -30mA, V_{NO} or V_{NC} = +2.5V	25		0.70	0.90	Ω
			Full			1.1	
On-Resistance Match Between Channels(5)	ΔR_{ON}		25		0.03	0.05	
			Full			0.10	
On-Resistance Flatness(6)	$R_{FLAT(ON)}$	V+ = 4.5V, I_{COM} = -30mA, V_{NO} or V_{NC} = 1V, 1.5V, 2.5V	25		0.08	0.12	
			Full			0.15	
NO or NC Off Leakage Current (7)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 0V, V_{NO} or V_{NC} = 4.5V	25	2	0.01	2	nA
			Full	-20		20	
COM On Leakage Current(7)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} or V_{NC} = 4.5V	25	-4		4	
			Full	-40	0.3	40	

Electrical Specifications - Single +5V Supply (continued)

(V+ = + 5V ± 10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp(°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH level					V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW level				0.8	
Input Current with HIGH Voltage	I_{INH}	V_{IN} = 2.4V, all others = 0.8V		-1	0.005	1	µA
Input Current with LOW Voltage	I_{INL}	V_{IN} = 0.8V, all others = 2.4V		-1	0.005	1	
Dynamic							
Turn-On-Time	t_{ON}	V_{CC} = 5V, See Fig. 1	25		20	35	ns
			Full			40	
Turn-Off-Time	t_{OFF}		25		15	20	
			Full			35	
Break-Before-Make	t_{BBM}	See Fig. 3	25	1	12	14.5	
			Full	1	17.5		
Charge Injection(3)	Q	C_L -1nF, V_{GEN} = 0V, R_{GEN} = 0V, See Fig 2	25		40		pC
Off Isolation	O_{IRR}	R_L = 50Ω, f = 1MHz, See Fig 4			-57		dB
CrossTalk(9)	X_{TALK}	R_L = 50Ω, f = 1MHz, See Fig 4			-57		
NC or NO Capacitance	$C_{NC/NO(OFF)}$	f = 1MHz, See Fig 6			42		pF
COM Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, See Fig 6			83		
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, See Fig 7			130		
Supply							
Power-Supply Range	V+		Full	1.8		5.5	V
Positive Supply Current	1+	V+ = 5.5V, V_{IN} = 0V or V+, All Channels ON or OFF	Full		0.5	1	µA

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. Device is NOT guaranteed to function per the datasheet specification outside of 0 to V+ range.
5. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
6. Flatness is defined as the difference between the maximum and minimum value of On-resistance measured.
7. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
8. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NC})]. See Figure 4.
9. Between any two switches. See Figure 5.

Electrical Specifications - Single +3.3V Supply

(V+ = +3.3V ± 10%, GND = 0V, V_{INH} = 2.0V, V_{INL} = 0.6V)

Parameter	Symbol	Conditions	Temp(°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V+	V
On-Resistance	R_{ON}	V+ = 3V, I_{COM} = -24mA, V_{NO} or V_{NC} = 2.0V	25		1.4	1.8	Ω
			Full			2.2	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V+ = 3.3V, I_{COM} = -24mA, V_{NO} or V_{NC} = 0.8V, 2.0V	25		0.04	0.05	
			Full		0.11		
On-Resistance Flatness	$R_{FLAT(ON)}$		25		0.17	0.2	
			Full		0.25		
Dynamic							
Turn-On-Time	t_{ON}	V_{CC} = 5V, See Fig. 1	25		30	40	ns
			Full			55	
Turn-Off-Time	t_{OFF}		25		20	25	
			Full			40	
Break-Before-Make	t_{BBM}	See Fig. 3	25	1	21	29	
Charge Injection(3)	Q	C_L -1nF, V_{GEN} = 0V, R_{GEN} = 0V, See Fig 2	25		30		pC
Supply							
Positive Supply Current	1+	V+ = 3.6V, V_{IN} = 0V or V+, All Channels ON or OFF	Full		0.5	1	µA
Logic Input							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH level	Full	2			V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW level	Full			0.6	
Input HIGH Current	I_{INH}	V_{IN} = 2.4V, all others = 0.8V	Full	-1		1	µA
Input LOW Current	I_{INL}	V_{IN} = 0.8V, all others = 2.4V	Full	-1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.

Electrical Specifications - Single +2.5V Supply

(V+ = +2.5V ± 10%, GND = 0V, V_{INH} = 1.8V, V_{INL} = 0.6V)

Parameter	Symbol	Conditions	Temp(°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V+	V
On-Resistance	R_{ON}	V+ = 1.8V, I_{COM} = -2mA, V_{NO} or V_{NC} = 1.5V	25		1.6	2	Ω
			Full			2.7	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V+ = 1.8V, I_{COM} = -2mA, V_{NO} or V_{NC} = 0.8V, 1.5V	25		0.13	0.16	
			Full		0.2		
On-Resistance Flatness	$R_{FLAT(ON)}$		25		0.25	0.3	
			Full		0.45		
Dynamic							
Turn-On-Time	t_{ON}	V+ = 2.5V, V_{NO} or V_{NC} = 1.8V, See Fig. 1	25		40	55	ns
			Full			70	
Turn-Off-Time	t_{OFF}		25		30	40	
			Full			55	
Break-Before-Make	t_{BBM}	See Fig. 3	25	1	33	39	
Make-Before-Break	t_{MBB}	See Fig. 4	25	1	9	13	
Charge Injection(3)	Q	C_L -1nF, V_{GEN} = 0V, R_{GEN} = 0V, See Fig 2	25		20		pC
Supply							
Positive Supply Current	1+	V+ = 2.75V, V_{IN} = 0V or V+, All Channels ON or OFF	Full		0.5	1	µA
Logic Input							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH level	Full	1.8			V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW level	Full			0.6	
Input HIGH Current	I_{INH}	V_{IN} = 2.0V, all others = 0.8V	Full	-1		1	µA
Input LOW Current	I_{INL}	V_{IN} = 0.8V, all others = 2.0V	Full	-1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.

Electrical Specifications - Single +1.8V Supply

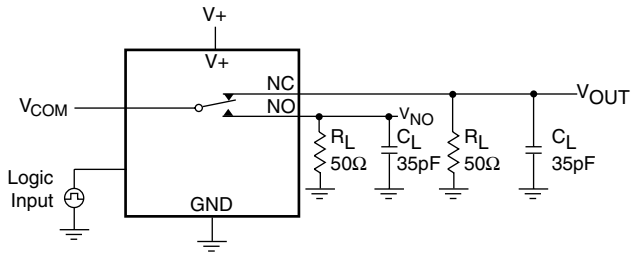
(V+ = +1.8V ± 10%, GND = 0V, V_{INH} = 1.5V, V_{INL} = 0.6V)

Parameter	Symbol	Conditions	Temp(°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V+	V
On-Resistance	R_{ON}	V+ = 1.8V, I_{COM} = -2mA, V_{NO} or V_{NC} = 1.5V	25		2.8	4	Ω
			Full			5	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V+ = 1.8V, I_{COM} = -2mA, V_{NO} or V_{NC} = 0.6V, 1.5V	25		0.44	0.6	
			Full		0.7		
On-Resistance Flatness	$R_{FLAT(ON)}$		25		0.5	0.6	
			Full		0.9		
Dynamic							
Turn-On-Time	t_{ON}	V+ = 1.8V, V_{NO} or V_{NC} = 1.5V, See Fig. 1	25		65	70	ns
			Full			95	
Turn-Off-Time	t_{OFF}		25		40	55	
			Full			70	
Break-Before-Make	t_{BBM}	See Fig. 3	25	1	60	72	
Charge Injection(3)	Q	C_L -1nF, V_{GEN} = 0V, R_{GEN} = 0V, See Fig 2	25		10		pC
Supply							
Positive Supply Current	1+	V+ = 2.0, V_{IN} = 0V or V+, All Channels ON or OFF	Full		0.5	1	µA
Logic Input							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH level	Full	1.8			V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW level	Full			0.6	
Input HIGH Current	I_{INH}	V_{IN} = 1.5V, all others = 0.8V	Full	-1		1	µA
Input LOW Current	I_{INL}	V_{IN} = 0.8V, all others = 1.5V	Full	-1		1	

Notes:

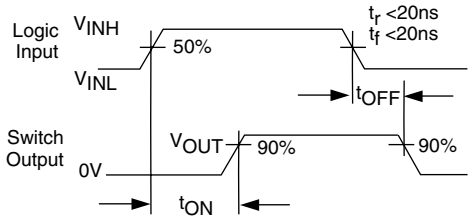
1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.

Test Circuits/Timing Diagrams



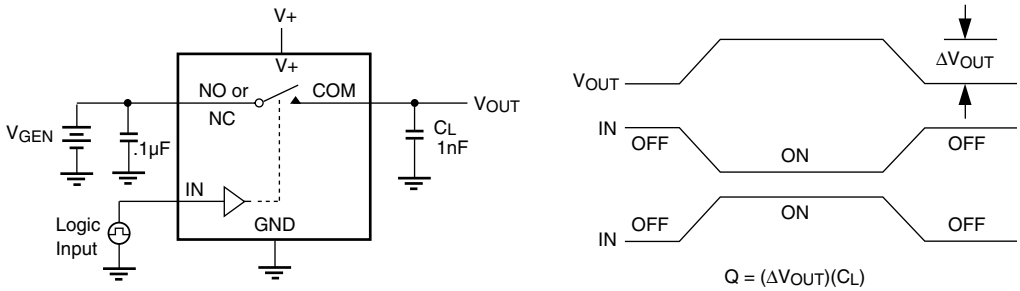
C_L INCLUDES FIXTURE AND STRAY CAPACITANCE

$$V_{OUT} = V_{NO}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



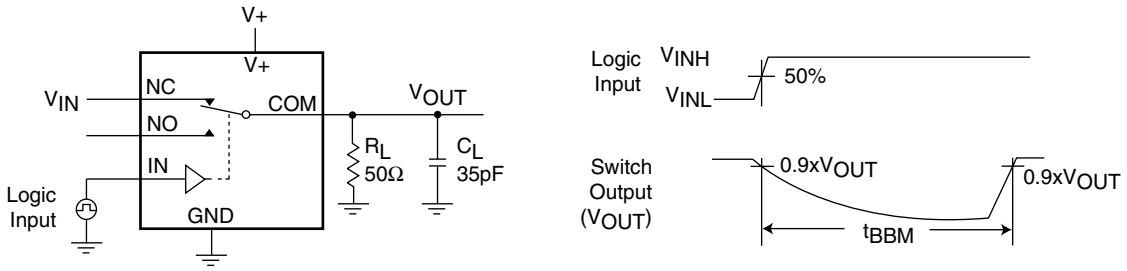
LOGIC INPUT WAVEFORMS INVERTED FOR SWITCHES THAT HAVE OPPOSITE LOGIC
* 1.5V FOR 3.3V SUPPLY

Figure 1. Switching Time



$Q = (\Delta V_{OUT})(C_L)$

Figure 2. Charge Injection



C_L INCLUDES FIXTURE AND STRAY CAPACITANCE

Figure 3. Break-Before-Make Interval

Test Circuits/Timing Diagrams (continued)

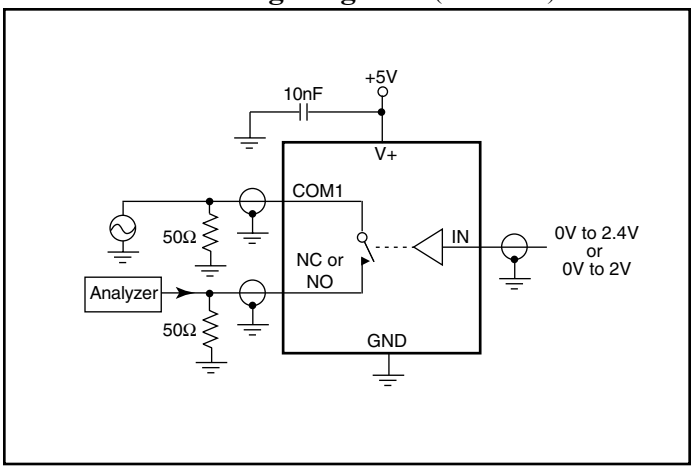


Figure 4. Off Isolation/On-Channel Bandwidth

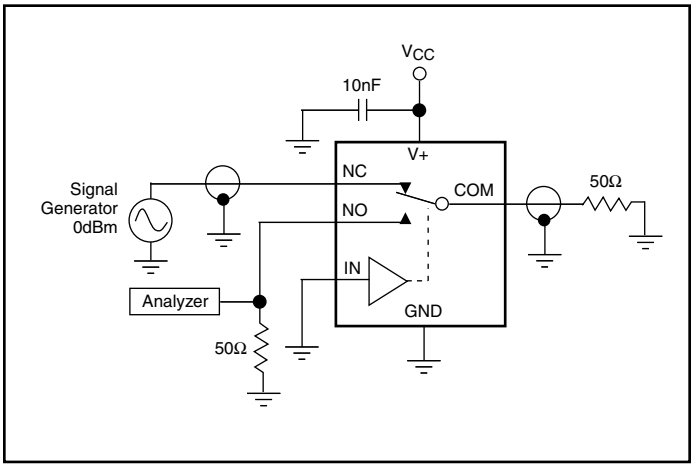


Figure 5. Crosstalk

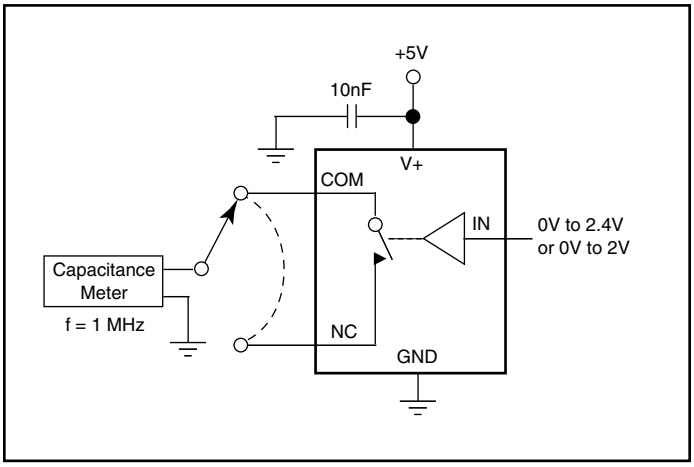


Figure 6. Channel-Off Capacitance

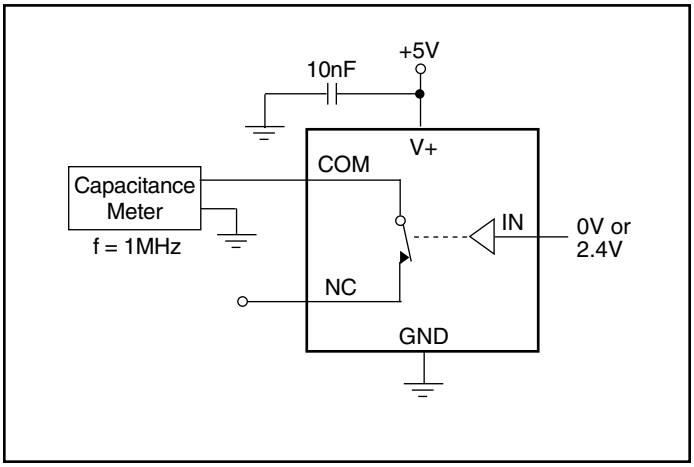


Figure 7. Channel-On Capacitance

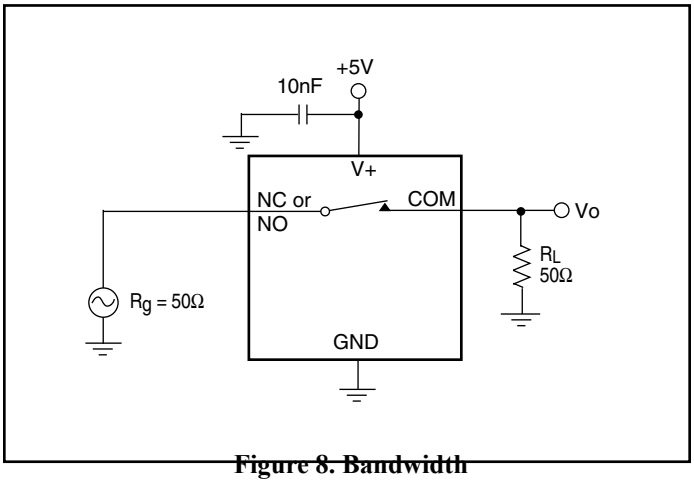
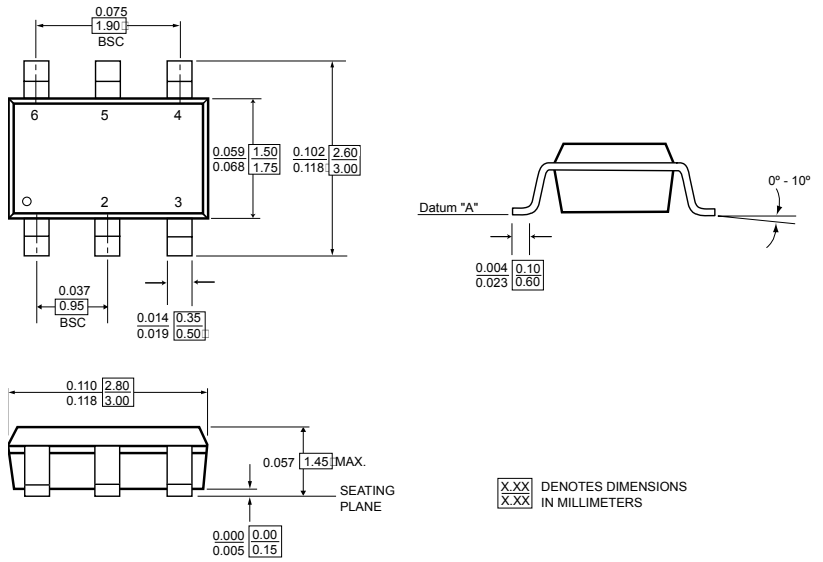
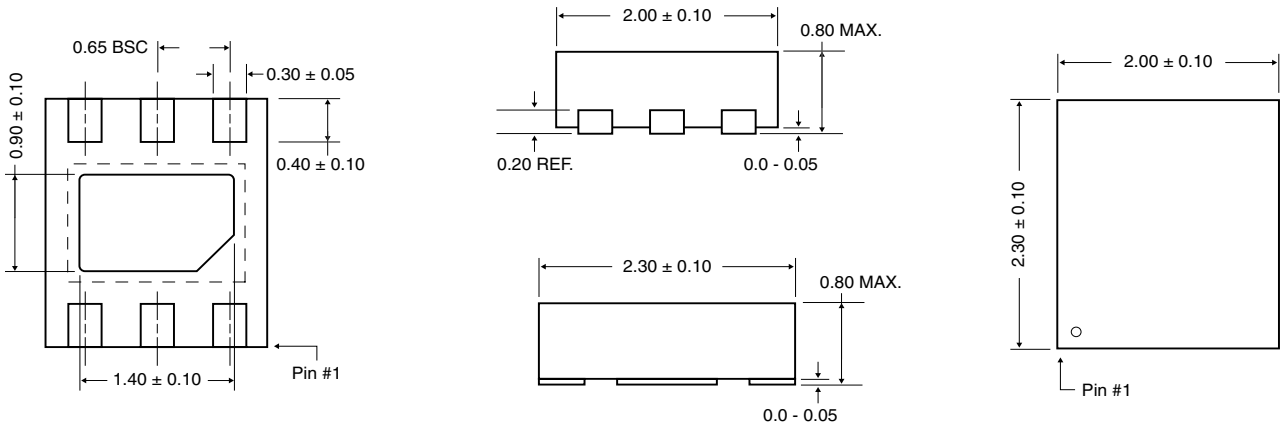


Figure 8. Bandwidth

Packaging Mechanical: 6-Pin SOT-23(T)



Packaging Mechanical: 6-Pin TDFN (ZC)



Ordering Information

Ordering Code	Package Code	Package Description	Top Marking
PI5A3159TX	T	6-pin SOT-23	ZL
PI5A3159TEX	T	6-pin SOT-23	$\overline{Z}$L
PI5A3159ZCX(1)	ZC	6-contact TDFN	ZL
PI5A3159ZCEX	ZC	Pb-free & Green 6-contact TDFN	ZL

Notes:
1. This product has always shipped as only a lead free product, but since it was introduced prior to Pericom's strategy of adding an E to all Green/ Lead free parts many customers order it without the E suffix. Please migrate new designs and qualification to include the E suffix. Pericom at this point in time will continue to offer devices marked both ways, but may at a later date eliminate the non-E part number.
2. Thermal Characteristics can be found on the world wide web at www.pericom.com/packaging/
3. Number of transistors : 753
4. X = Tape and reel