2 pF Off Capacitance, 1 pC Charge Injection, ±15 V/12 V *i*CMOS™ Dual SPDT Switch

Preliminary Technical Data

ADG1236

FEATURES

2 pF off capacitance
1 pC charge injection
33 V supply range
120 Ω on resistance
Fully specified at +12 V, ±15 V
No V_L supply required
3 V logic-compatible inputs
Rail-to-rail operation
16-lead TSSOP and 12-lead LFCSP packages
Typical power consumption: <0.03 µW

APPLICATIONS

Automatic test equipment
Data aquisition systems
Battery-powered systems
Sample-and-hold systems
Audio signal routing
Communication systems

FUNCTIONAL BLOCK DIAGRAM

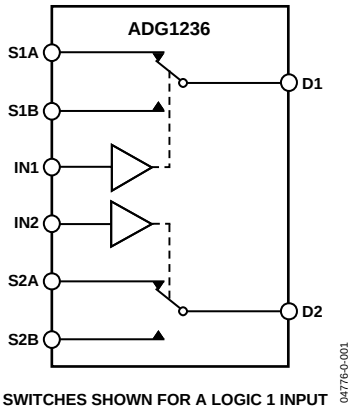

Figure 1.

GENERAL DESCRIPTION

The ADG1236 is a monolithic CMOS device containing two independently selectable SPDT switches. It is designed on an *i*CMOS process. *i*CMOS (industrial-CMOS) is a modular manufacturing process combining high voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 30 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages, while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and charge injection of the part make it an ideal solution for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make the part suitable for video signal switching. *i*CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. Both switches exhibit break-before-make switching action for use in multiplexer applications.

PRODUCT HIGHLIGHTS

1. 2 pF off capacitance (±15 V supply).
2. 1 pC charge injection.
3. 3 V logic-compatible digital inputs: V_{IH} = 2.0 V, V_{IL} = 0.8 V.
4. No V_L logic power supply required.
5. Ultralow power dissipation: <0.03 µW.
6. 16-lead TSSOP and 12-lead 3 mm × 3 mm LFCSP packages.

Rev. PrD

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

REVISION HISTORY

11/04—Revision PrD: Preliminary Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameters	25°C	85°C	Y Version[1]	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})				Ω typ	V_S = ±10 V, I_S = −10 mA; Figure 21
	120	220	260	Ω max	
On Resistance Match between Channels (ΔR_{ON})	5			Ω typ	V_S = ±10 V, I_S = −10 mA
				Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	25			Ω typ	V_S = −5 V/0 V/+5 V; I_S = −10 mA
			50	Ω max	
LEAKAGE CURRENTS					V_{DD} = +10 V, V_{SS} = −10 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 0 V/10 V, V_D = 10 V/0 V; Figure 22
	±0.5	±1	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = 0 V/10 V, V_D = 10 V/0 V; Figure 22
	±0.5	±1	±5	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04			nA typ	V_S = V_D = 0 V or 10 V; Figure 23
	±1	±2	±5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.5	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	50			ns typ	R_L = 50 Ω, C_L = 35 pF
				ns max	V_S = ±10 V; Figure 24
t_{OFF}	20		100	ns typ	R_L = 50 Ω, C_L = 35 pF
				ns max	V_S = ±10 V; Figure 24
Break-before-Make Time Delay, t_D	15		40	ns typ	R_L = 50 Ω, C_L = 35 pF
			1	ns min	V_{S1} = V_{S2} = 10 V; Figure 25
Charge Injection	1			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Figure 26
Off Isolation	75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 27
Channel-to-Channel Crosstalk	85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 28
Total Harmonic Distortion + Noise	0.002			% typ	R_L = 600 Ω, 5 V rms, f = 20 Hz to 20 kHz
−3 dB Bandwidth	700			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 29
C_S (Off)	2			pF typ	
C_D(Off)	2			pF typ	
C_D, C_S (On)	5			pF typ	
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.001			μA typ	Digital Inputs = 0 V or V_{DD}
			5.0	μA max	
I_{DD}	150			μA typ	Digital Input = 5 V
			300	μA max	
I_{SS}	0.001			μA typ	Digital Inputs = 0 V or V_{DD}
			5.0	μA max	

Parameters	25°C	85°C	Y Version[1]	Unit	Test Conditions/Comments
I_{GND}	0.001			µA typ	Digital Inputs = 0 V or V_{DD}
			5.0	µA max	
I_{GND}	150			µA typ	Digital Input = 5 V
		300		µA max	

[1] Temperature range for Y Version is −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameters	25°C	85°C	Y Version[1]	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	220			Ω typ	V_S = +10 V, I_S = −10 mA; Figure 21
				Ω max	
On Resistance Match between Channels (ΔR_{ON})	10			Ω typ	V_S = +10 V, I_S = −10 mA
				Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	40			Ω typ	V_S = +3 V/+6 V/+9 V, I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = 12 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; Figure 22
	±0.5	±1	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; Figure 22
	±0.5	±1	±5	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04			nA typ	V_S = V_D = 1 V or 10 V, Figure 23
	±1	±2	±5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2.0		V min	
Input Low Voltage, V_{INL}		0.8		V max	
Input Current, I_{INL} or I_{INH}	0.001			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.5	µA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	50			ns typ	R_L = 50 Ω, C_L = 35 pF
				ns max	V_S = 8 V; Figure 24
t_{OFF}	15			ns typ	R_L = 50 Ω, C_L = 35 pF
				ns max	V_S = 8 V; Figure 24
Break-before-Make Time Delay, t_D	15			ns typ	R_L = 50 Ω, C_L = 35 pF
			1	ns min	V_{S1} = V_{S2} = 8 V; Figure 25
Charge Injection	5			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Figure 26
				pC typ	
Off Isolation	75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 27;
Channel-to-Channel Crosstalk	85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 28
−3 dB Bandwidth	700			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 29
C_S (Off)	2			pF typ	
C_D (Off)	2			pF typ	
C_D, C_S (On)	5			pF typ	

Parameters	25°C	85°C	Y Version[1]	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.001			µA typ	Digital Inputs = 0 V or V_{DD}
			5.0	µA max	
I_{DD}	150			µA typ	Digital Inputs = 5 V
			300	µA max	

[1] Temperature range for Y Version is −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Ratings
V_{DD} to V_{SS}	38 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Inputs	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	30 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance	150.4°C/W
12-Lead LFCSP, θ_{JA} Thermal Impedance	TBD°C/W
Lead Temperature, Soldering	
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°C

[1] Over voltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLE FOR SWITCHES

Table 4.

IN	Switch A	Switch B
0	Off	On
1	On	Off

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

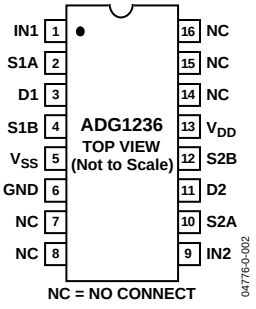

Figure 2.TSSOP Pin Configuration

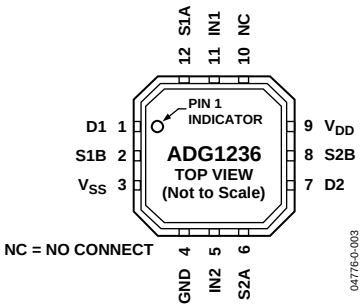

Figure 3. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Function**
1	11	IN1	Logic Control Input.
2	12	S1A	Source Terminal. Can be an input or output.
3	1	D1	Drain Terminal. Can be an input or output.
4	2	S1B	Source Terminal. Can be an input or output.
5	3	V_{SS}	Most Negative Power Supply Potential.
6	4	GND	Ground (0 V) Reference.
7, 8, 14–16	10	NC	No Connect.
9	5	IN2	Logic Control Input.
10	6	S2A	Source Terminal. Can be an input or output.
11	7	D2	Drain Terminal. Can be an input or output.
12	8	S2B	Source Terminal. Can be an input or output.
13	9	V_{DD}	Most Positive Power Supply Potential.

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D (V_S)
The analog voltage on Terminals D and S.

R_{ON}
The ohmic resistance between D and S.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL} (I_{INH})
The input current of the digital input.

C_S (Off)
The off switch source capacitance, measured with reference to ground.

C_D (Off)
The off switch drain capacitance, measured with reference to ground.

C_D, C_S (On)
The on switch capacitance, measured with reference to ground.

C_{IN}
The digital input capacitance.

t_{ON}
The delay between applying the digital control input and the output switching on. See Figure 24.

t_{OFF}
The delay between applying the digital control input and the output switching off.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4. On Resistance as a Function of V_D (V_S) for Single Supply

Figure 5, On Resistance as a Function of V_D (V_S) for Dual Supply

Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

Figure 8, On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

Figure 9. Leakage Current as a Function of V_D (V_S)

Figure 10. Leakage Currents as a Function of V_D (V_S)

Figure 11. Leakage Current as a Function of V_D (V_S)

Figure 12. Leakage Currents as a Function of Temperature

Figure 13. Leakage Currents as a Function of Temperature

Figure 14. Supply Currents vs. Input Switching Frequency

Figure 15. Charge Injection vs. Source Voltage

Figure 16. t_{ON}/t_{OFF} Times vs. Temperature

Figure 17. Off Isolation vs. Frequency

Figure 18. Crosstalk vs. Frequency

Figure 19. On Response vs. Frequency

Figure 20. THD + N vs. Frequency

TEST CIRCUITS

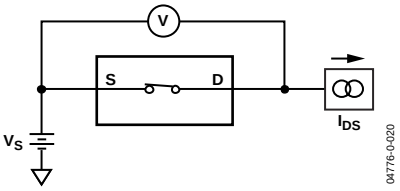

Figure 21. Test Circuit 1—On Resistance

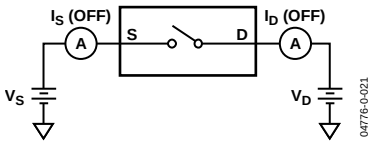

Figure 22. Test Circuit 2— Off Resistance

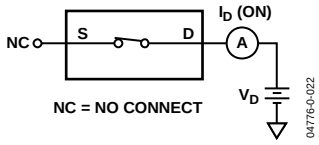

Figure 23. Test Circuit 3—On Leakage

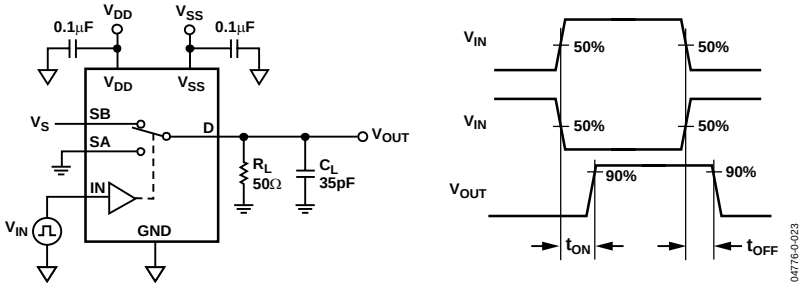

Figure 24. Test Circuit 4—Switching Times

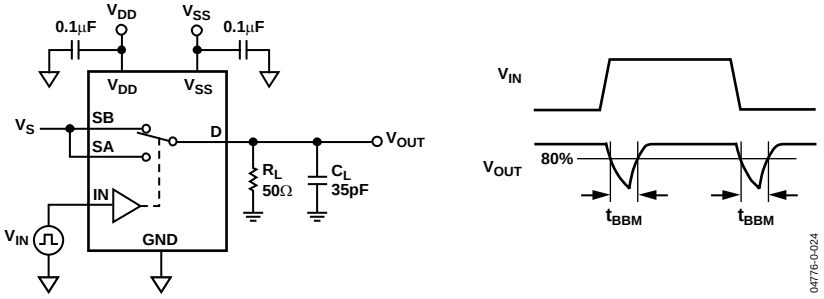

Figure 25. Test Circuit 5—Break-before-Make Time Delay

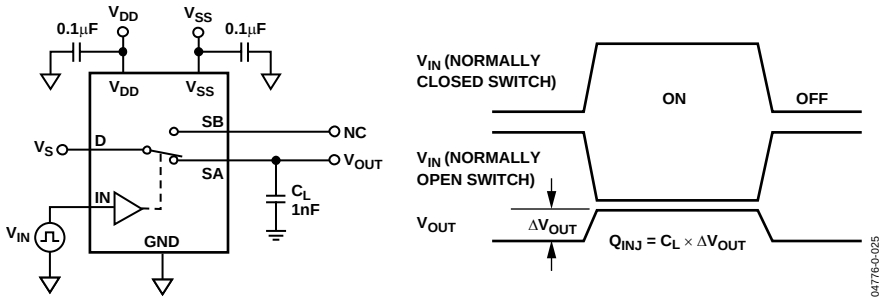

Figure 26. Test Circuit 6—Charge Injection

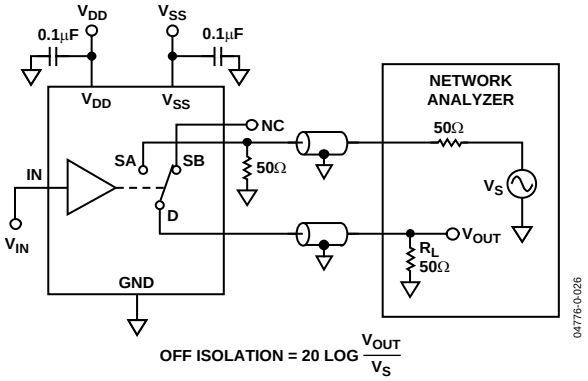

Figure 27. Test Circuit 7—Off Isolation

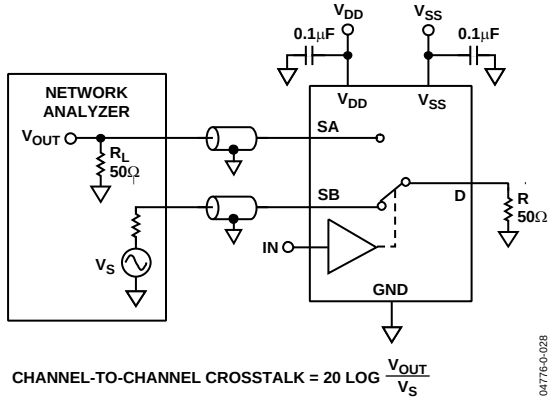

Figure 29. Test Circuit 9— Bandwidth

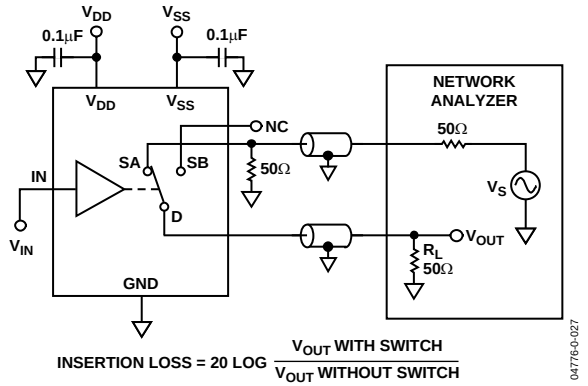

Figure 28. Test Circuit 8—Channel-to-Channel Crosstalk

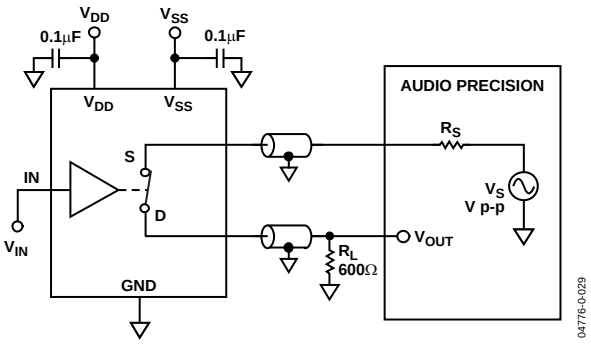

Figure 30. Test Circuit 10—THD + Noise

OUTLINE DIMENSIONS

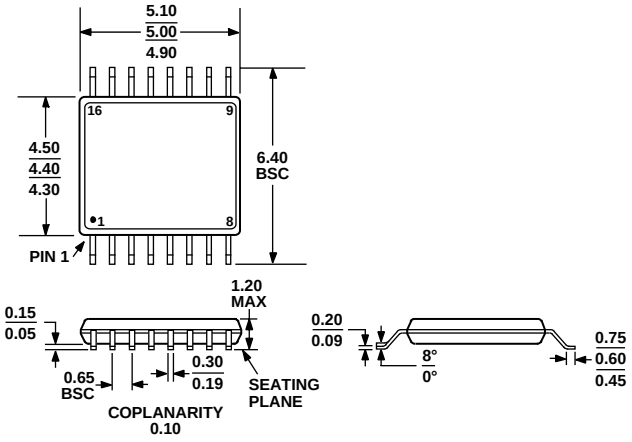

Figure 31. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in inches and (millimeters

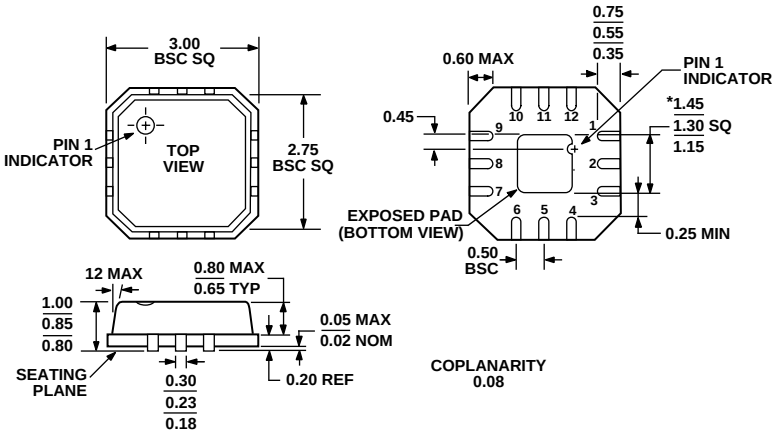

Figure 32. 12-Lead Lead Frame Chip Scale Package [VQ_LFCSP]
3 mm × 3 mm Body, Very Thin Quad
(CP-12-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1236YRU	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1236YCP	−40°C to +125°C	Lead Frame Chip Scale Package (LFCSP)	CP-12-1

NOTES

NOTES

PR04776–0–11/04(PrD)