Low-Voltage, Dual Supply, Low R_{ON}, Quad SPST Analog Switches

DESCRIPTION

The DG9424, DG9425, DG9426 are low voltage precision monolithic quad single-pole-single-throw analog switches.

Using BiCMOS wafer fabrication technology allows the DG9424, DG9425, DG9426 to operate on single and dual supplies. Single supply voltage ranges from 3 to 12 V while dual supply operation is recommended with ± 3 to ± 6 V.

Combining high speed (t_{ON}: 42 ns), flat $R_{DS(on)}$ over the analog signal range (Ω), minimal insertion lose (- 3 dB at 190 MHz), and excellent crosstalk and off-isolation performance, the DG9424, DG9425, DG9426 are ideally suited for audio and video signal switching.

The DG9424 and DG9425 respond to opposite control logic as shown in the Truth Table. The DG9426 has two normally open and two normally closed switches.

FEATURES

- 2.7 V thru 12 V single supply or ± 3 thru ± 6 dual supply
- On-resistance - $R_{DS(on)}$: 1.7 Ω
- Fast switching - t_{ON}: 42 ns
  - t_{OFF}: 28 ns
- TTL, CMOS compatible
- Low leakage: 0.2 nA
- 2000 V ESD protection

BENEFITS

- Widest dynamic range
- Low signal errors and distortion
- Break-before-make switching action
- Simple interfacing

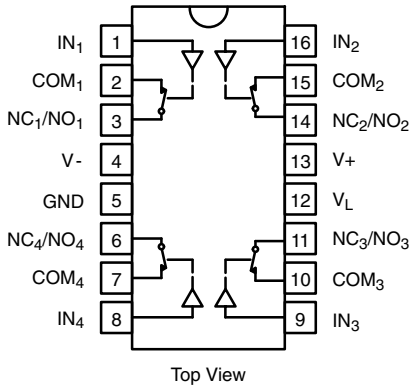
APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Communication systems
- ADC systems
- xDSL and PBX/PABX
- Audio signal routing

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG9424/DG9425

TSSOP

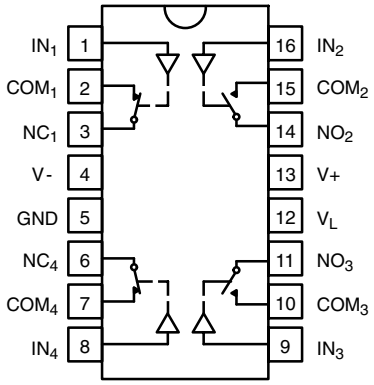


Top View

TRUTH TABLE		
Logic	**DG9424**	**DG9425**
0	OFF	ON
1	ON	OFF

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG9426
TSSOP



Top View

TRUTH TABLE		
Logic	**SW_1, SW_4**	**SW_2, SW_3**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp. Range	**Package**	**Part Number**
DG9424, DG9425		
- 40 °C to 85 °C	16-Pin TSSOP	DG9424DQ
		DG9425DQ
DG9426		
- 40 °C to 85 °C	16-Pin TSSOP	DG9426DQ

ABSOLUTE MAXIMUM RATINGS			
Parameter		**Limit**	**Unit**
V+ to V-		- 0.3 to 13	V
GND to V-		7	
V_L		(GND - 0.3) to (V+) + 0.3	
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3)	
Continuous Current (NO, NC, COM Pins)		100	mA
Peak Current, S or D (Pulsed 1 ms, 10 % Duty Cycle)		200	
Storage Temperature		- 65 to 150	°C
Power Dissipation (Package)[b]	16-Pin TSSOP[c]	450	mW
Thermal Resistance[b]		178	°C/W

Notes:
a. Signals on NC, NO, COM or IN exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 7 mW/°C above 25 °C.

SPECIFICATIONS[a] Single Supply 12 V							
Parameter	**Symbol**	**Test Conditions Unless Specified** V+ = 12 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	**Temp.**[b]	**Limits** - 40 °C to 85 °C **Min.**[d]	**Typ.**[c]	**Ma.x**[d]	**Unit**
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	0		12	V
On-Resistance	R_{ON}	V+ = 10.8 V, V- = 0 V I_{NO}, I_{NC} = 50 mA, V_{COM} = 2/9 V	Room Full		1.8	3 4	Ω
Digital Control							
Input Current	I_{INL} or I_{INH}		Full	- 1	0.01	1	µA
Dynamic Characteristics							
Turn-On Time[e]	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_{NO}, V_{NC} = 5 V, See Figure 2	Room Full		42	57 65	ns
Turn-Off Time[e]	t_{OFF}		Room Full		28	42 44	
Break-Before-Make Time Delay[e]	t_D	DG9426 Only, V_{NO}, V_{NC} = 5 V R_L = 300 Ω, C_L = 35 pF	Room	2			
Charge Injection[e]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room		38		pC
Off-Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	Room		- 56		dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room		- 77		
NO, NC Off Capacitance[e]	$C_{NO(off)}$ $C_{NC(off)}$	f = 1 MHz	Room		49		pF
COM Off Capacitance[e]	$C_{COM(off)}$		Room		37		
Channel On Capacitance[e]	$C_{COM(on)}$		Room		89		
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 or V_L	Room Full		0.02	1 5	µA
Negative Supply Current	I-		Room Full	- 1 - 5	- 0.002		
Logic Supply Current	I_L		Room Full		0.002	1 5	
Ground Current	I_{GND}		Room Full	- 1 - 5	- 0.002		

SPECIFICATIONS[a] Dual Supply ± 5 V							
Parameter	**Symbol**	**Test Conditions Unless Specified** V+ = 5 V, V- = 5 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	**Temp.**[b]	**Limits** - 40 °C to 85 °C **Min.**[d]	**Typ.**[c]	**Max.**[d]	**Unit**
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	- 5		5	V
On-Resistance	R_{ON}	V+ = 4.5 V, V- = - 4.5 V I_{NO}, I_{NC} = 50 mA, V_{COM} = ± 3.5 V	Room Full		2	3.3 4.3	Ω
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 5.5 V, V- = - 5.5 V V_{COM} = ± 4.5 V, V_{NO}, V_{NC} = ± 4.5 V	Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10		1 10	
Channel On Leakage Current	$I_{COM(on)}$	V+ = 5.5 V, V- = - 5.5 V, V_{NO}, V_{NC} = V_{COM} = ± 4.5 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input Current[a]	I_{INL} or I_{INH}		Full	- 1	0.05	1	µA
Dynamic Characteristics							
Turn-On Time[e]	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_{NO}, V_{NC} = ± 3.5 V, See Figure 2	Room Full		56	74 81	ns
Turn-Off Time[e]	t_{OFF}		Room Full		42	64 67	
Break-Before-Make Time Delay[e]	t_D	DG9426 Only, V_{NO}, V_{NC} = 3.5 V R_L = 300 Ω, C_L = 35 pF	Room	2			
Charge Injection[e]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room		112		pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 56		dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room		- 82		
Source Off Capacitance[e]	$C_{NO(off)}$ $C_{NC(off)}$	f = 1 MHz	Room		38		pF
Drain Off Capacitance[e]	$C_{COM(off)}$		Room		38		
Channel On Capacitance[e]	$C_{COM(on)}$		Room		89		
Power Supplies							
Positive Supply Current[e]	I+	V_{IN} = 0 or V_L	Room Full		0.03	1 5	µA
Negative Supply Current[e]	I-		Room Full	- 1 - 5	- 0.002		
Logic Supply Current[e]	I_L		Room Full		0.002	1 5	
Ground Current[e]	I_{GND}		Room Full	- 1 - 5	- 0.002		

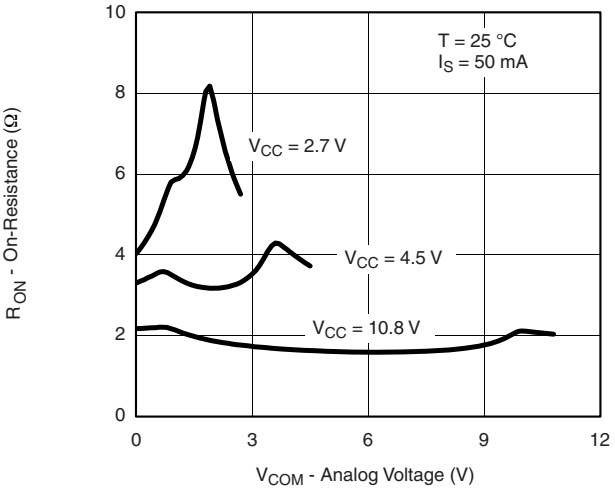
SPECIFICATIONS[a] Single Supply 5 V							
Parameter	**Symbol**	**Test Conditions Unless Specified** V+ = 5 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	**Temp.**[b]	**Limits** - 40 °C to 85 °C **Min.**[d]	**Typ.**[c]	**Max.**[d]	**Unit**
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full			5	V
On-Resistance[e]	R_{ON}	V+ = 4.5 V, I_{NO}, I_{NC} = 50 mA V_{COM} = 1 V, 3.5 V	Room Full		3.4	4.8 5.8	Ω
Dynamic Characteristics							
Turn-On Time[e]	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_{NO}, V_{NC} = 3.5 V, See Figure 2	Room Hot		71	86 106	ns
Turn-Off Time[e]	t_{OFF}		Room Hot		37	51 56	
Break-Before-Make Time Delay[e]	t_D	DG9426 Only, V_{NO}, V_{NC} = 3.5 V R_L = 300 Ω, C_L = 35 pF	Room	5			
Charge Injection[e]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room		10		pC
Power Supplies							
Positive Supply Current[e]	I+	V_{IN} = 0 or V_L	Room Hot		0.02	1 5	µA
Negative Supply Current[e]	I-		Room Hot	- 1 - 5	- 0.002		
Logic Supply Current[e]	I_L		Room Hot		0.002	1 5	
Ground Current[e]	I_{GND}		Room Hot	- 1 - 5	- 0.002		

SPECIFICATIONS[a] Single Supply 3 V							
Parameter	**Symbol**	**Test Conditions Unless Specified** V+ = 3 V, V- = 0 V V_L = 3 V, V_{IN} = 2.4 V, 0.4 V[f]	**Temp.**[b]	**Limits** - 40 °C to 85 °C **Min.**[d]	**Typ.**[c]	**Max.**[d]	**Unit**
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	0		3	V
On-Resistance	R_{ON}	V+ = 2.7 V, V- = 0 V I_{NO}, I_{NC} = 5 mA, V_{COM} = 0.5, 2.2 V	Room Full		8	13.8 15.1	Ω
Switch Off Leakage Current[a]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V, V- = 0 V V_{COM} = 0.3, 3 V, V_{NO}, V_{NC} = 3, 0.3 V	Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10		1 10	
Channel On Leakage Current[a]	$I_{COM(on)}$	V+ = 3.3 V, V- = 0 V, V_{NO}, V_{NC} = V_{COM} = 0.3, 3 V	Room Full	- 1 - 10		1 10	
Digital Control[e]							
Input Current	I_{INL} or I_{INH}		Full	- 1	0.005	1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_{NO}, V_{NC} = 1.5 V, See Figure 2	Room Full		140	163 193	ns
Turn-Off Time	t_{OFF}		Room Full		65	80 89	
Break-Before-Make Time Delay	t_D	DG9426 Only, V_{NO}, V_{NC} = 1.5 V R_L = 300 Ω, C_L = 35 pF	Room	5			
Charge Injection[e]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room		15		pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	Room		- 56		dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room		- 80		
Source Off Capacitance[e]	$C_{NO(off)}$ $C_{NC(off)}$	f = 1 MHz	Room		53		pF
Drain Off Capacitance[e]	$C_{COM(off)}$		Room		42		
Channel On Capacitance[e]	$C_{COM(on)}$		Room		92		

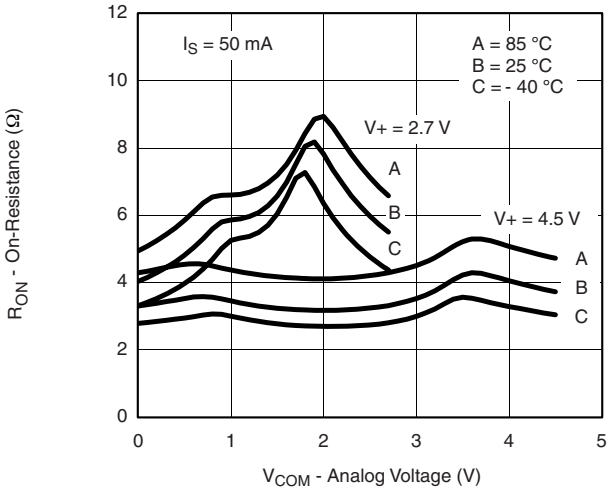
Notes:
a. Leakage parameters are guaranteed by worst case test conditions and not subject to production test.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

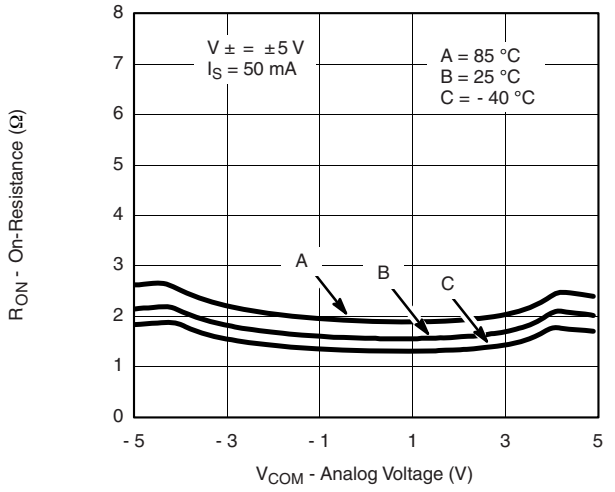
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



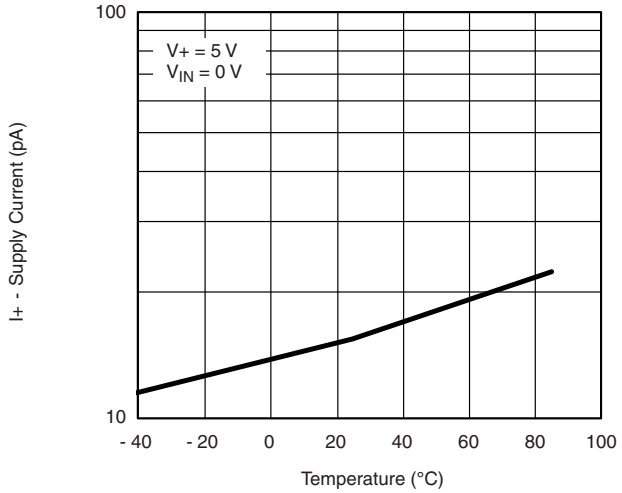
R_{ON} vs. V_{COM} and Supply Voltage



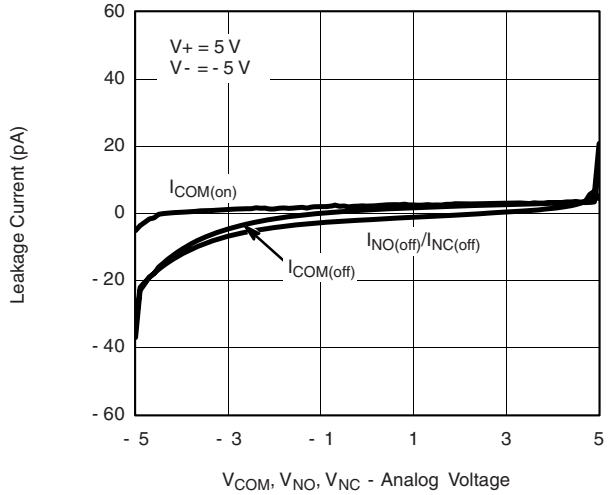
R_{ON} vs. Analog Voltage and Temperature



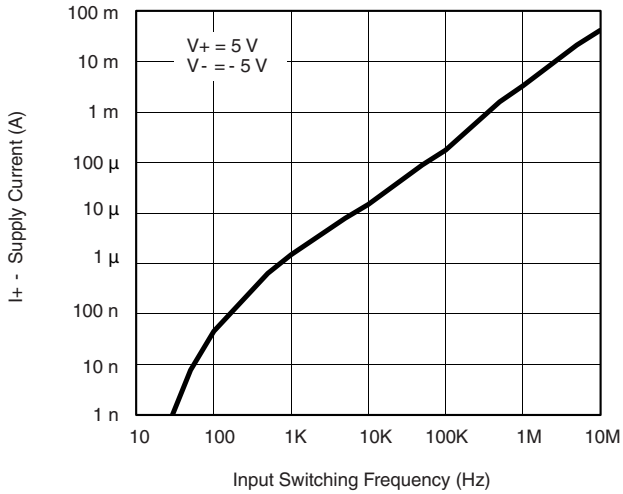
R_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature

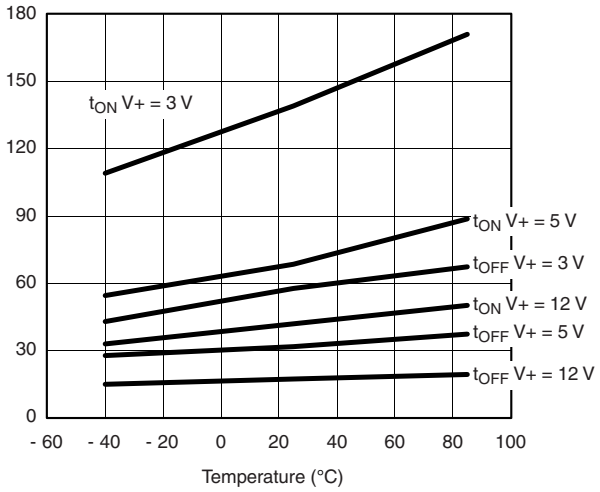


Leakage Current vs. Analog Voltage

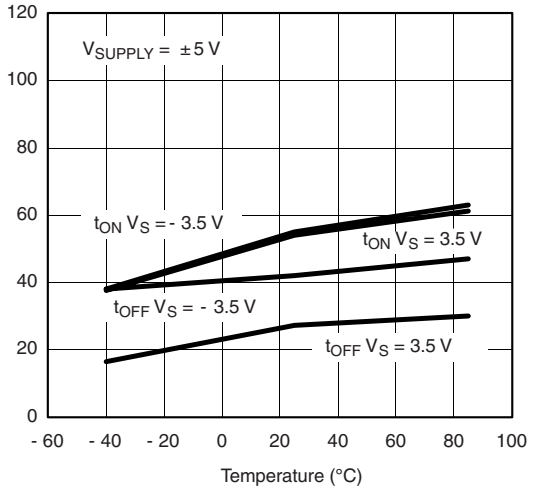


Switching Current vs. Input Switching Frequency

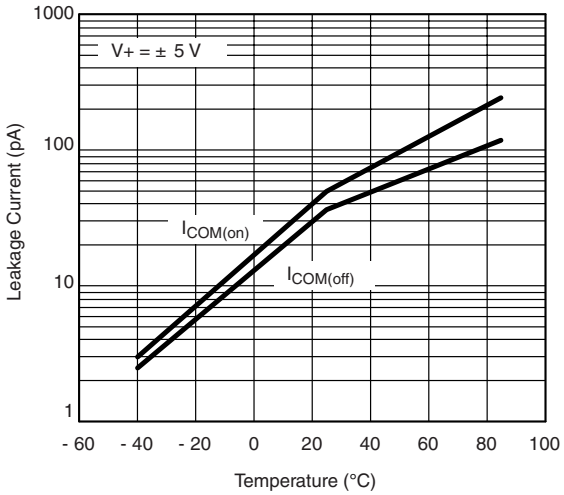
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



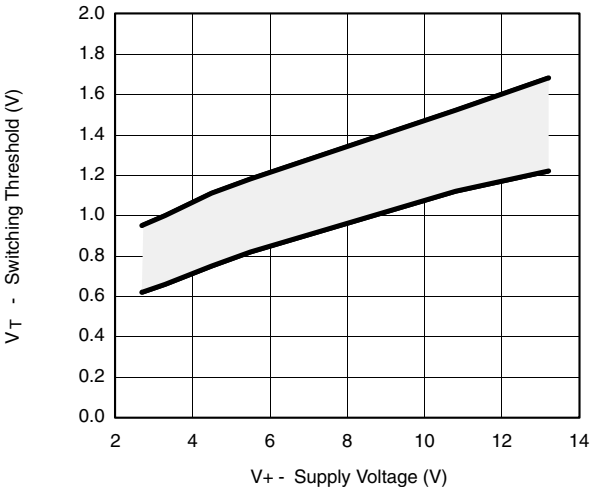
Switching Time vs. Temperature and Single Supply Voltage



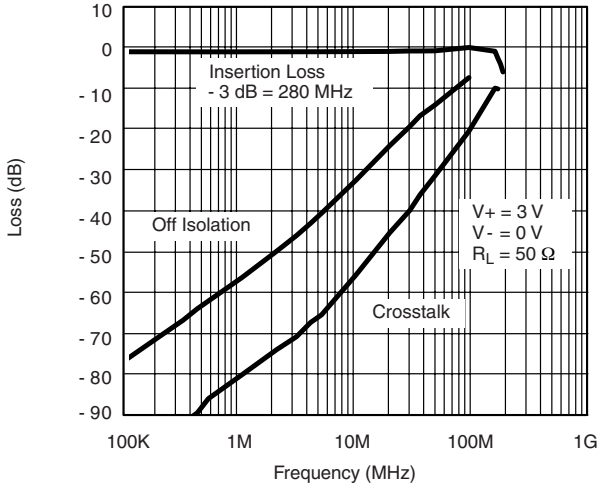
Switching Time vs. Temperature and Dual Supply Voltage



Leakage Current vs. Temperature



Switching Threshold vs. Supply Voltage



Insertion Loss, Off Isolation and Crosstalk vs. Frequency

SCHEMATIC DIAGRAM Typical Channel

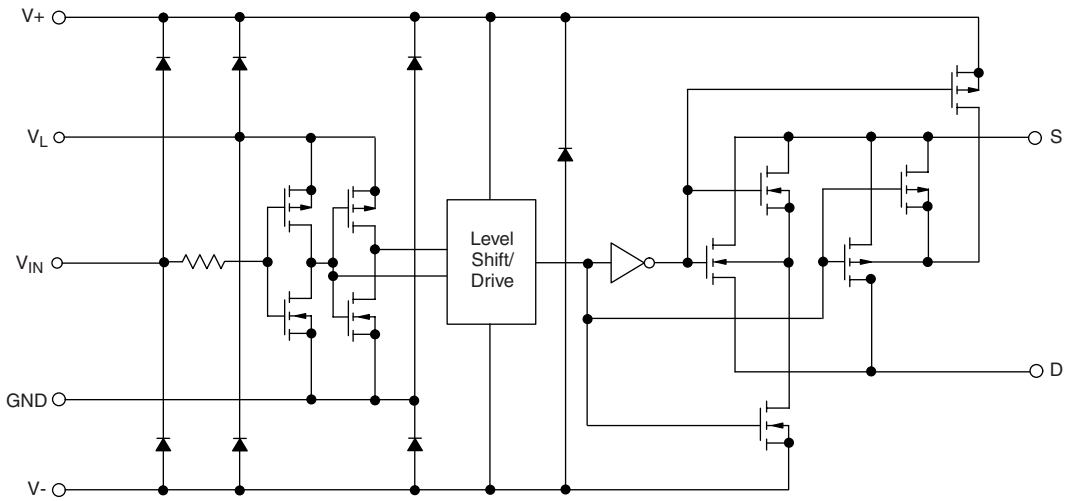
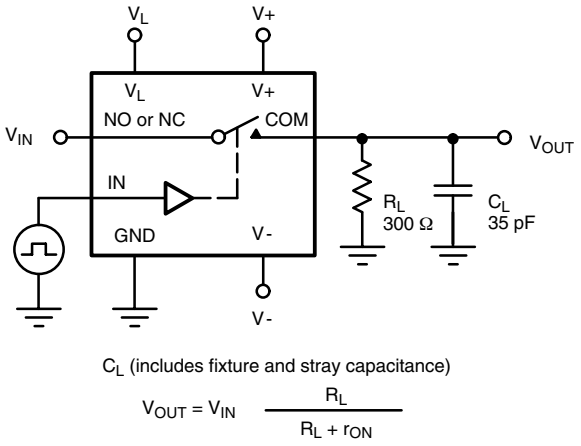


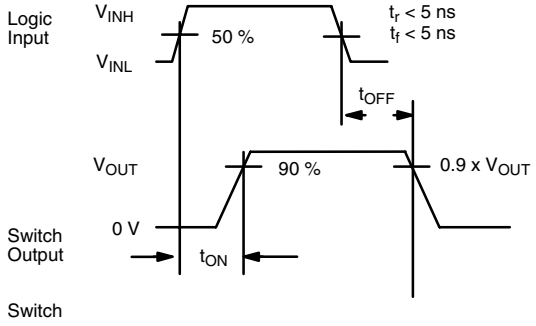
Figure 1.

TEST CIRCUITS



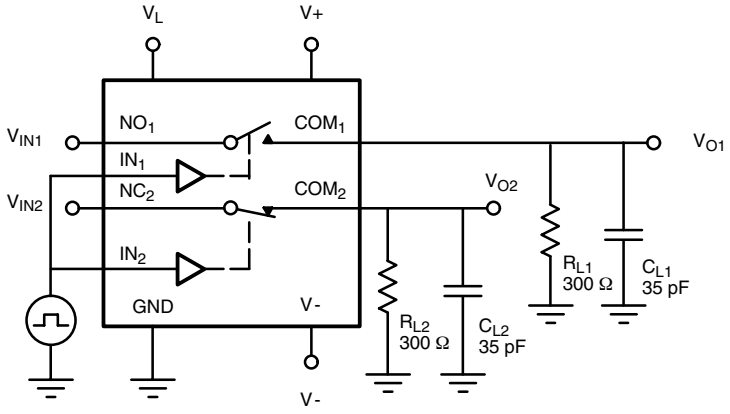
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{IN} \frac{R_L}{R_L + r_{ON}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Figure 2. Switching Time



C_L (includes fixture and stray capacitance)

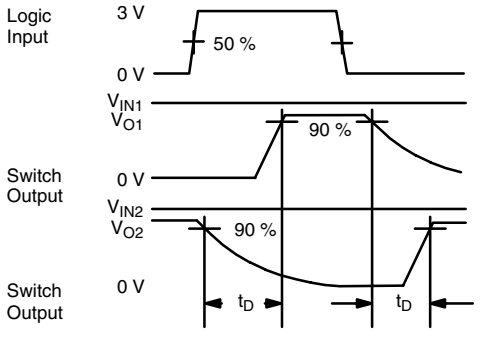
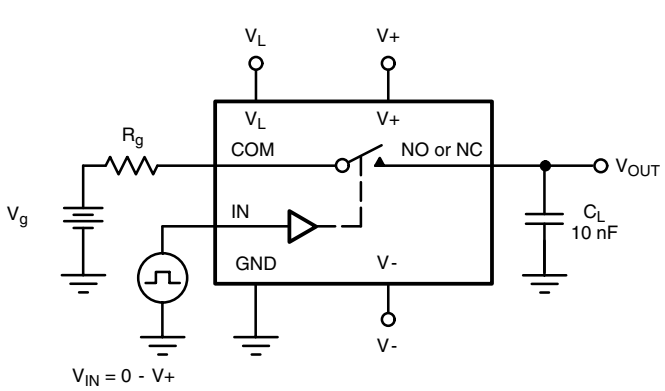
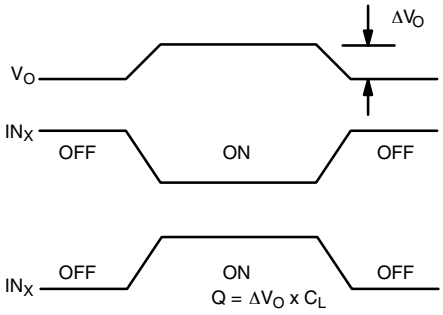


Figure 3. Break-Before-Make (DG9426)

TEST CIRCUITS





IN$_X$ dependent on switch configuration Input polarity determined by sense of switch.

Figure 4. Charge Injection

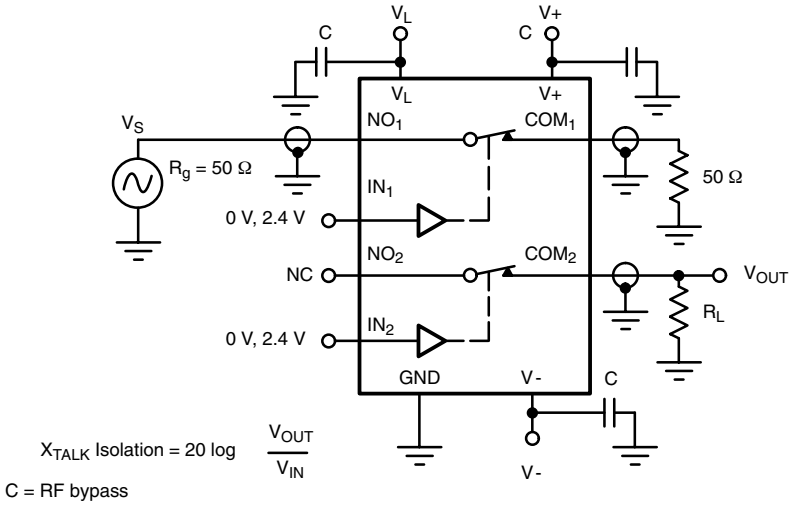


Figure 5. Crosstalk

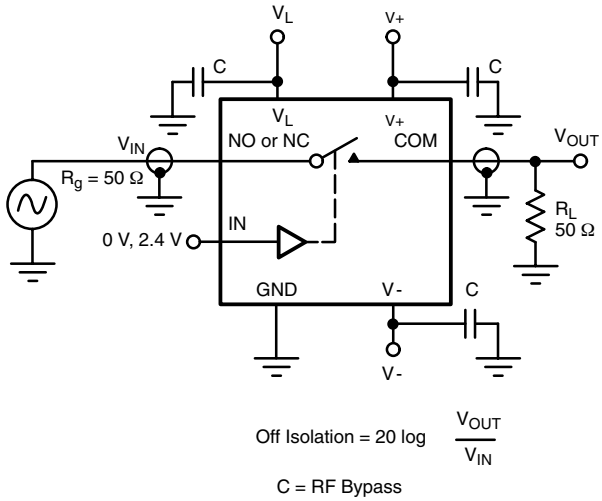


Figure 6. Off-Isolation

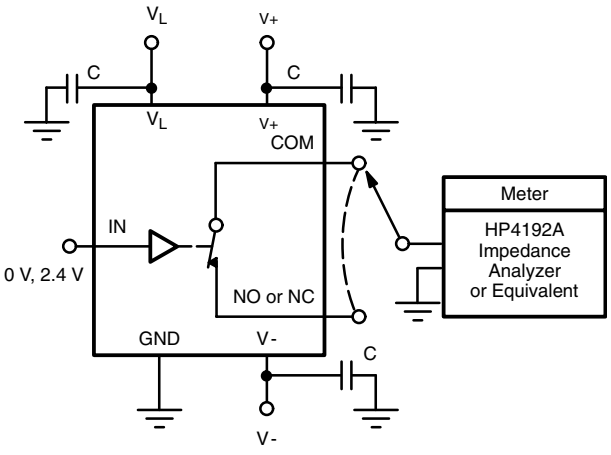
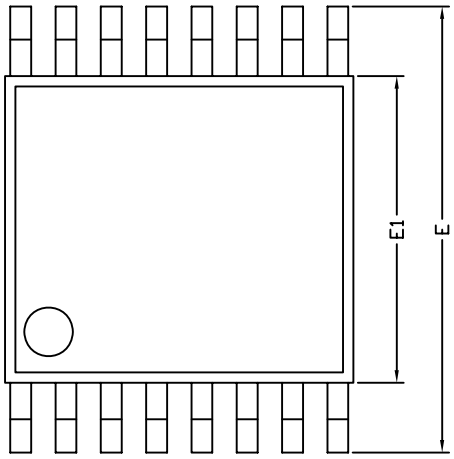
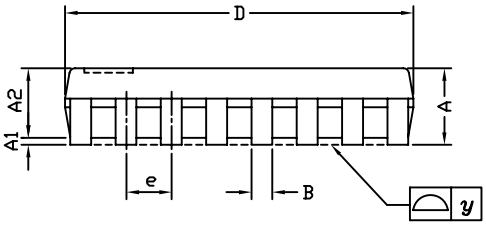


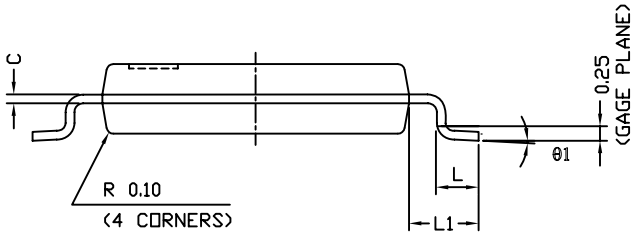
Figure 7. Source/Drain Capacitances

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71807.

TSSOP: 16-LEAD







Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

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