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ICs for Chip Cards

SLE 4418 / SLE 4428
Intelligent 8-Kbi t EEPROM

Data Sheet 04.94

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Previous Releases: 09.92	
Page	Subjects (changes since last revision)
	Update

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled. Important:

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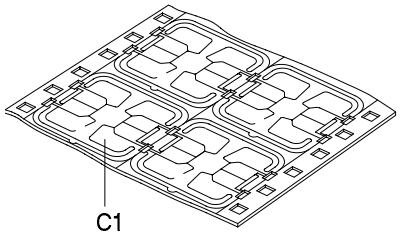
Intelligent 1-KByte EEPROM with Write Protect Function SLE 4418

Intelligent 1-KByte EEPROM with Write Protect Function and Programmable Security Code (PSC) SLE 4428

Features

- 1024 x 8 bit EEPROM organization
- Byte-wise addressing
- Irreversible byte-wise write protection
- 1024 x 1 bit protection memory organization
- Serial three-wire bus
- End of programming indicated on data output
- Minimum of 10^4 write/erase cycles
- Data retention for minimum of ten years
- Contact configuration and serial interface in accordance to ISO standard 7816 (synchronous transmission)

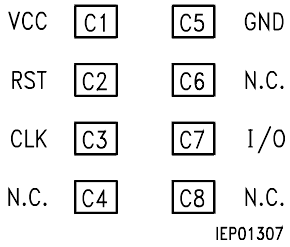


M2.2

Additional Feature of SLE 4428

- Data can only be changed after entry of the correct 2-byte programmable security code (PSC)

Type	Ordering Code	Package
SLE 4418 C	on request	Chip
SLE 4418 M2.2	on request	Wire-Bonded Module M2.2
SLE 4428 C	on request	Chip
SLE 4428 M2.2	on request	Wire-Bonded Module M2.2



M2 (Card Contacts)

Pin Configurations (top view)

Pin Definitions and Functions

Pin	Card Contact	Symbol	Function
1	C1	VCC	Operating voltage 5 V
2	C2	RST	Chip control
3	C3	CLK	Clock
4	C4	N.C.	Not connected
5	C5	GND	Ground
6	C6	N.C.	Not connected
7	C7	I / O	Data line (open drain)
8	C8	N.C.	Not connected

SLE 4418/4428 comes out as a M2.2 wire-bonded module for embedding in plastic cards or as a die for customer packaging.

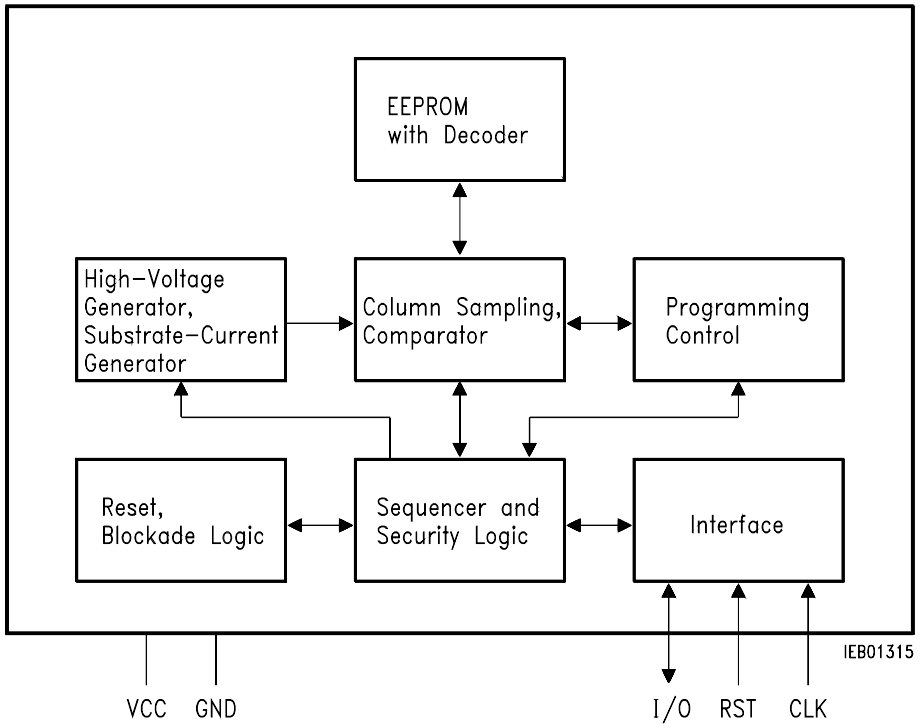


Figure 1
Block Diagram

1 Functional Description

1.1 SLE 4418

The chip contains an EEPROM organized 1024 x 8 bit offering the possibility of programmable write protection for each byte. Reading of the whole memory is always possible. The memory can be written and erased byte by byte. Input data and the contents of the adressed byte are compared so that only bits are written which were not written before. Erasing is only possible byte-wise, even if only one bit is to be erased, but bits may be written individually. Each byte can be write/erase-protected individually by setting a protect bit (EEPROM → ROM). The protect bit is only one time programmable and cannot be erased.

1.2 SLE 4428

Additionally to the above functions this version has a PSC verification logic. All the memory, except for the PSC, can always be read. The memory can be written or erased only after PSC verification. The error counter can always be written. After eight successive incorrect entries the error counter will block any subsequent attempt at PSC verification and hence any possibility to write and erase.

2 Reset and Answer-to-Reset

2.1 Reset

When the operating voltage is applied, the chip goes into the power-on reset (POR) state. POR is terminated by reset. Reset is started by RST changing from “0” to “1” and finished by CLK going from “0” to “1”. This reset operation aborts any currently active command. After POR a read operation must be performed before any change of data is possible.

2.2 Answer to Reset (ISO 7816)

Answer to reset sets the address counter to “0” and the first data bit appears on the output. The contents of the following addresses can be read out with the following clock pulses. Answer to reset is executed by the following steps **(Fig. 2)** :

- RST goes from “0” to “1”,
- clock pulse is applied,
- RST changes back from “1” to “0”.

3 Commands

The state of RST defines the data direction on I/O.

RST	I/O
1	Command entry
0	Data output

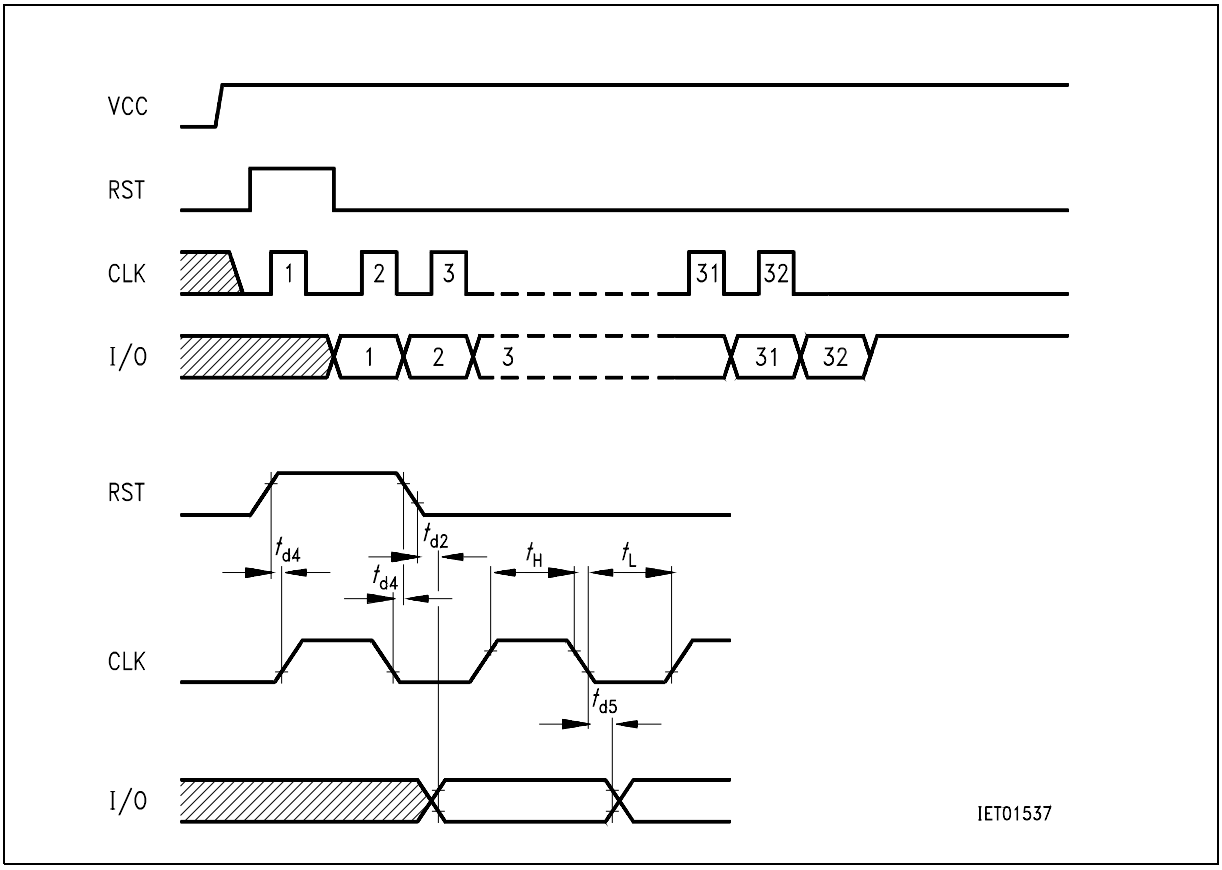


Figure 2
Reset and Answer-to-Reset

The possible commands are listed in **table 1.**

Table 1
Control Words for Command Entry

Byte 1								Byte 2	Byte 3	Operation
S0	S1	S2	S3	S4	S5	A8	A9	A0-A7	D0-D7	
1	0	0	0	1	1	Address bit		Address bit	Input data	Write and erase with protect bit
1	1	0	0	1	1				Input data	Write and erase without protect bit
0	0	0	0	1	1				Comparison data	Write protect bit with data comparison (verification)
0	0	1	1	0	0	8 and 9		0 – 7	No effect	Read 9 bits, data with protect bit
0	1	1	1	0	0				No effect	Read 8 bits, data without protect bit

Figure 3 shows the command entry, whereas the general timing is given in **figure 4**.

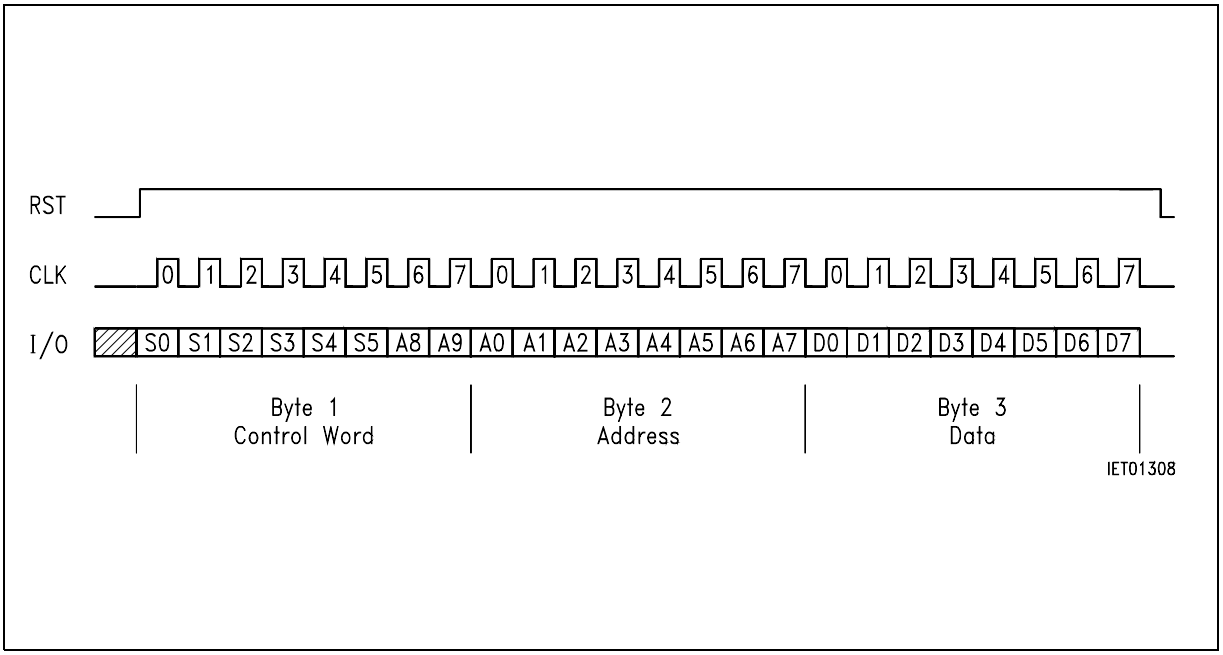


Figure 3
Command Entry

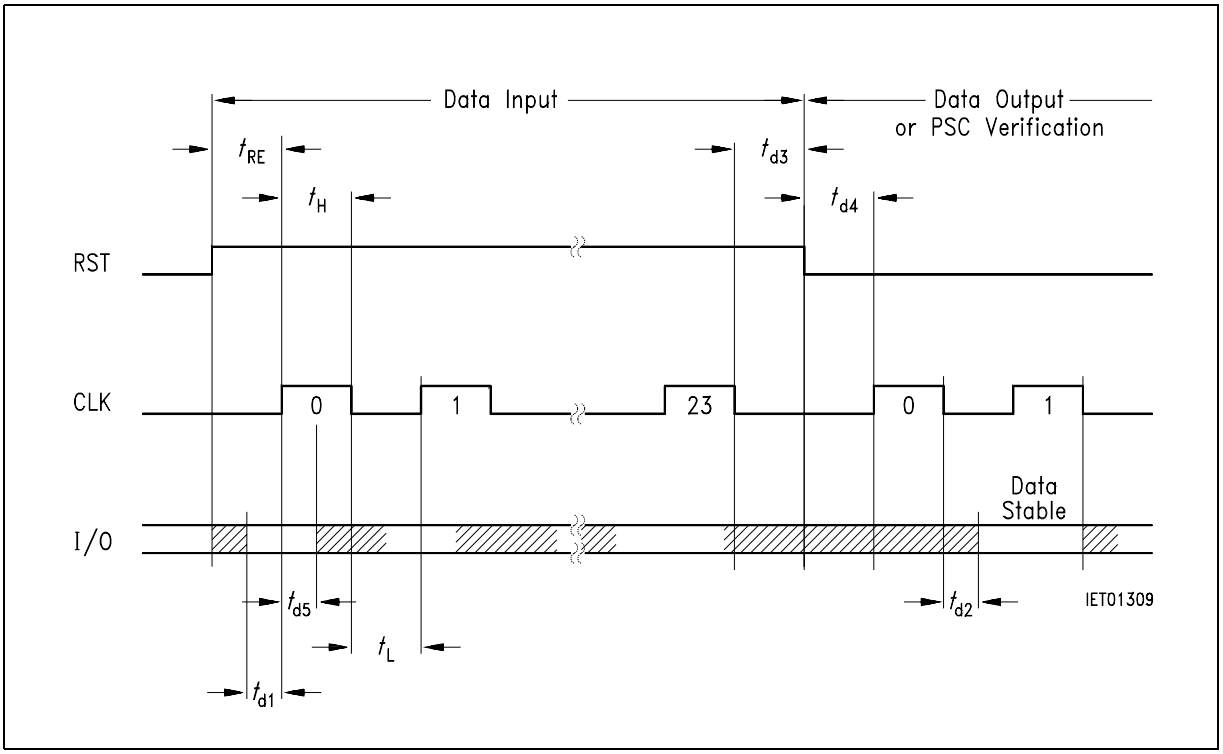


Figure 4
General Timing for Data Input, Data Output and PSC Verification

3.1 Write/Erase Operations

Write/Erase Data Byte without Protect Bit

Remark: Erase means “0” →“1”, write means “1” → “0”.

There are three kinds of write/erase operations which are automatically executed by the chip:

- Erase and subsequent write (duration 203 clock pulses, $f \leq 20$ kHz) **(Fig.5)**
- Write only: This procedure is suitable if single bits of one byte shall be changed only from “1” to “0”. (duration 103 clock pulses, $f \leq 20$ kHz) **(Fig.6)**
- Erase only (= FF; duration 103 clock pulses, $f \leq 20$ kHz) **(Fig.6)**.

Write/Erase Data Byte with Protect Bit

The protect bit is erased at delivery, it can be written only once. Write procedure see above.

Write Protect Bit with Data Comparison

The data has to be entered a second time. The protect bit is only written if the old and the new data are identical.
The execution of write/erase commands are terminated internally after a given number of clock cycles. The end of the operation is indicated by the transition from “1” to “0” on I/O. Only RST transition from “0” to “1” sets I/O to state “1”.

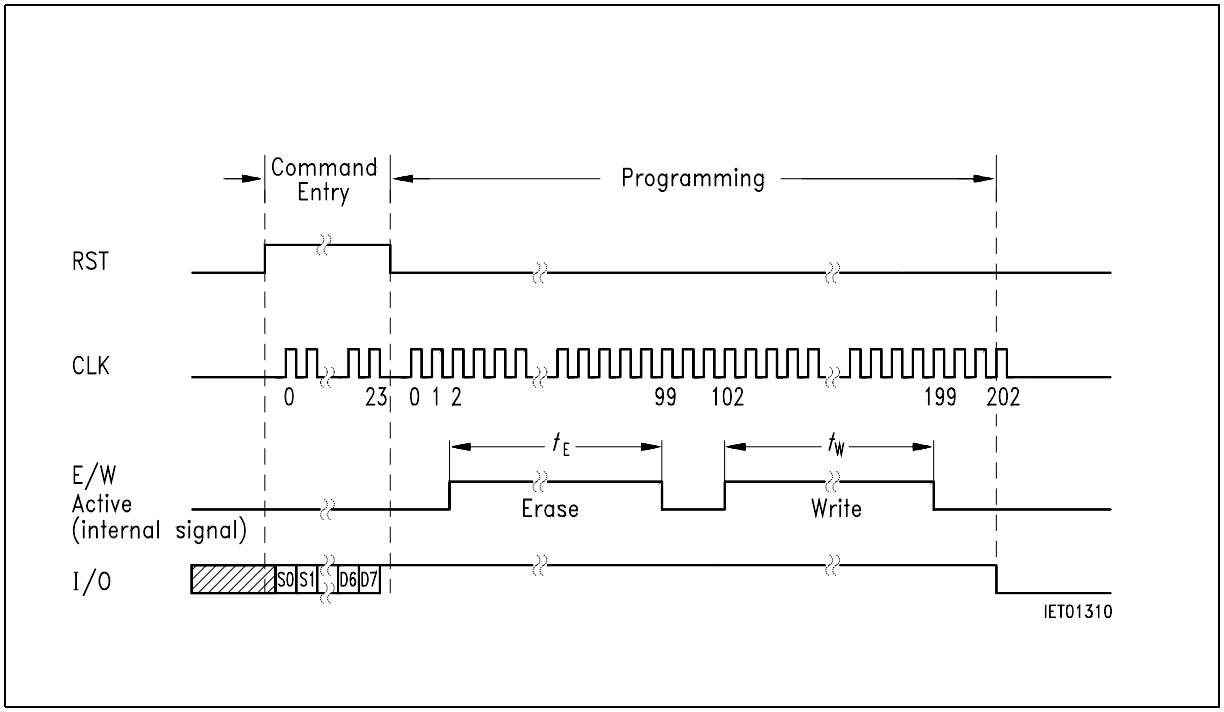


Figure 5
Programming: Erase and Write

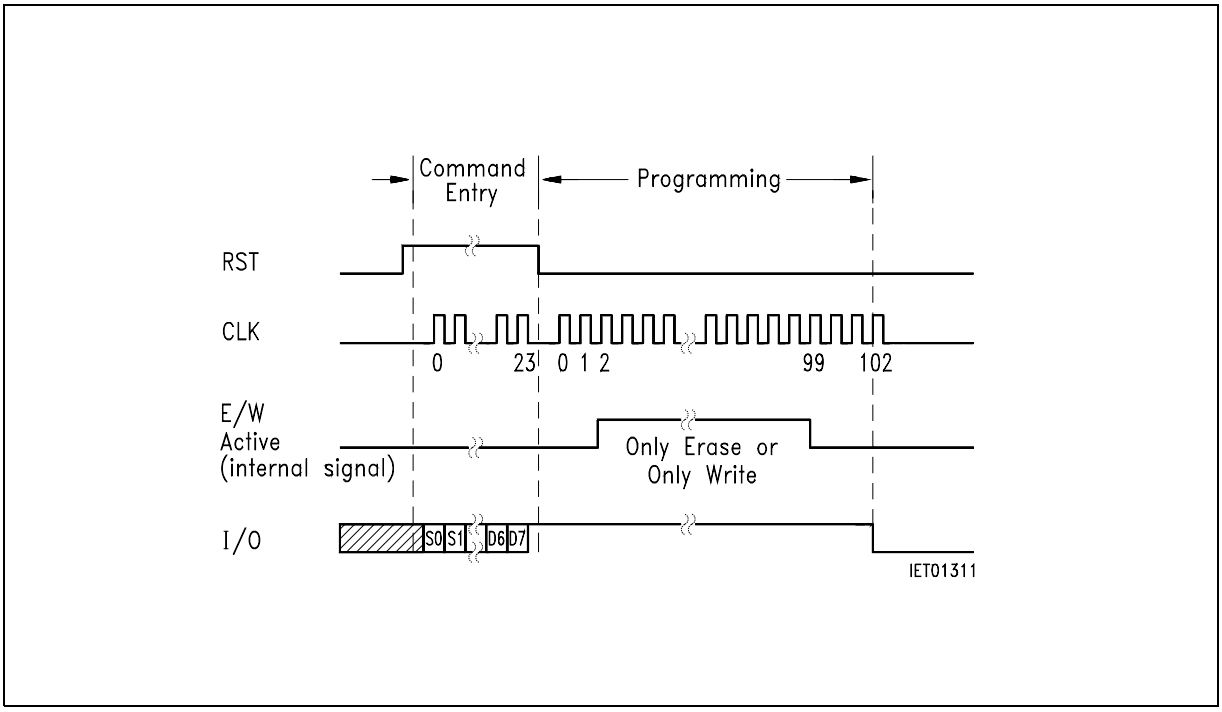


Figure 6
Programming: Only Erase or Only Write

3.2 Read Operations with Address Increment

Read Data Byte (Read 8 Bits) (Fig.7)

In this operation the output of the protect bit is suppressed. The address is incremented after the eighth clock pulse.

Read Data Byte together with Protect Bit (Read 9 Bits) (Fig. 8)

After command entry the eight data bits are read out by eight consecutive clock pulses, and the protect bit on the ninth pulse. After the ninth clock pulse the address counter is incremented.

The read operation is terminated by a RST transition “0” to “1”.

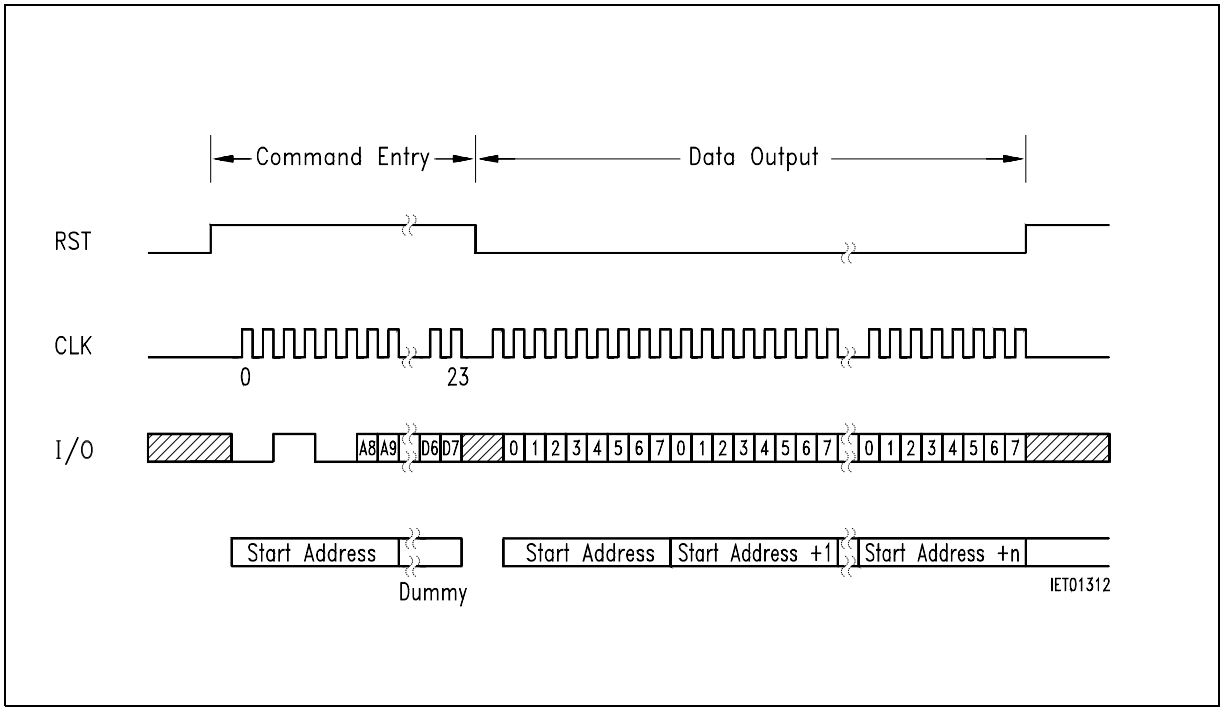


Figure 7
Read Data Byte: Read 8 Bits, Data D0-D7

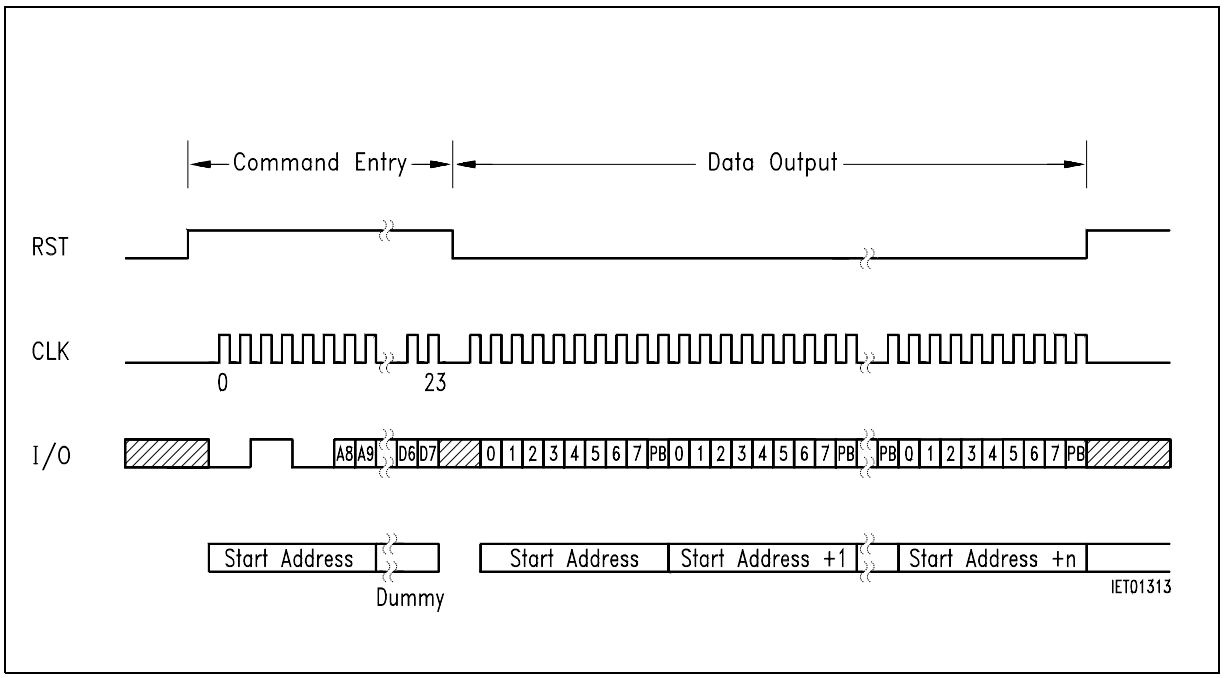


Figure 8
Read Data Byte together with Protect Bit: Read 9 Bits, Data D0-D7 and Protect Bit PB

4 Security Features SLE 4428

Extra Operation for User Identification (Fig. 9)

Without a PSC entry only reading is possible. The contents of the PSC addresses cannot be read out. If reading is attempted, "00" will appear. The verification procedure of the chip must be performed in the following sequence **(Table 1)**:

- write one not written error-counter bit, address "1021",
- enter first PSC-code byte, address "1022",
- enter second PSC-code byte, address "1023",
- after correct input the error counter can be erased.

After the PSC verification, I/O goes from "1" to "0". It is switched back to “1” by RST transition “0” to “1”. The error counter is not automatically erased.

Writing Error Counter

Before PSC entry only writing of the error counter is possible. The number of erased bits of the error counter determines the number of possible attempts (max. 8). After successful access the error counter should be erased before disconnecting the supply voltage in order to reactivate the 8 attempts. Each error when entering the PSC requires the writing of a new counter bit.

Entry of PSC

The least-significant PSC byte beginning with the least significant bit must be entered first and then the most-significant one. If the internal data comparison proves correct, the EEPROM is enabled for erasing and writing as long as the operating voltage is applied. After enabling, the PSC may be altered as wished, except the corresponding protect bits are "0".

Condition when supplied

SLE 4428 is only supplied by the producer with a 2-byte PSC (transport code) which is agreed with the customer.

Table 1
Control Words for Command Entry, User Identification

Byte 1								Byte 2	Byte 3	Operation
S0	S1	S2	S3	S4	S5	A8A9		A0-A7	D0-D7	
0	1	0	0	1	1	1	1	253	Bit mask	Write error counter
1	0	1	1	0	0	1	1	254	PSC byte 1	Verify 1st PSC byte
1	0	1	1	0	0	1	1	255	PSC byte 2	Verify 2nd PSC byte

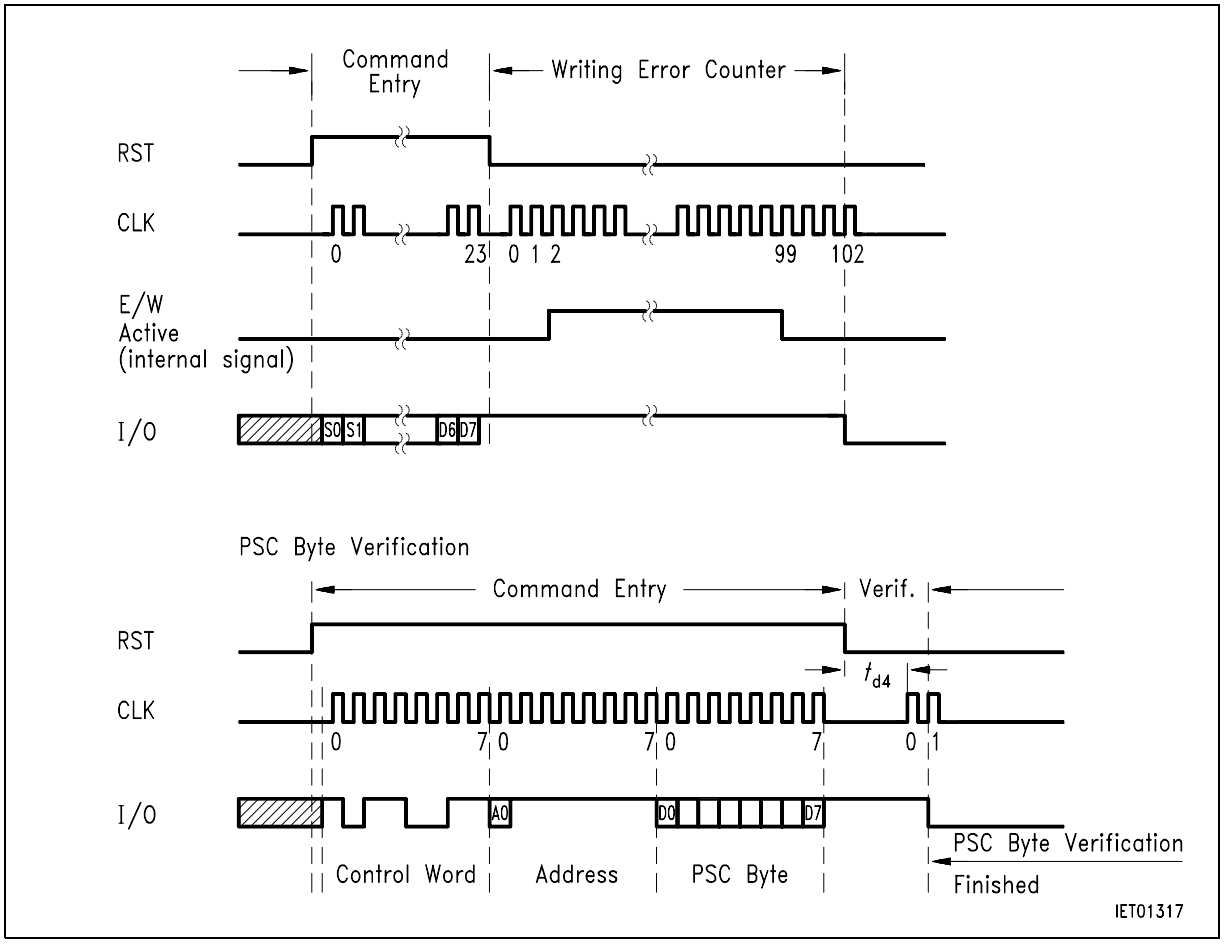


Figure 9
PSC Verification

5 Technical Data

Absolute Maximum Ratings

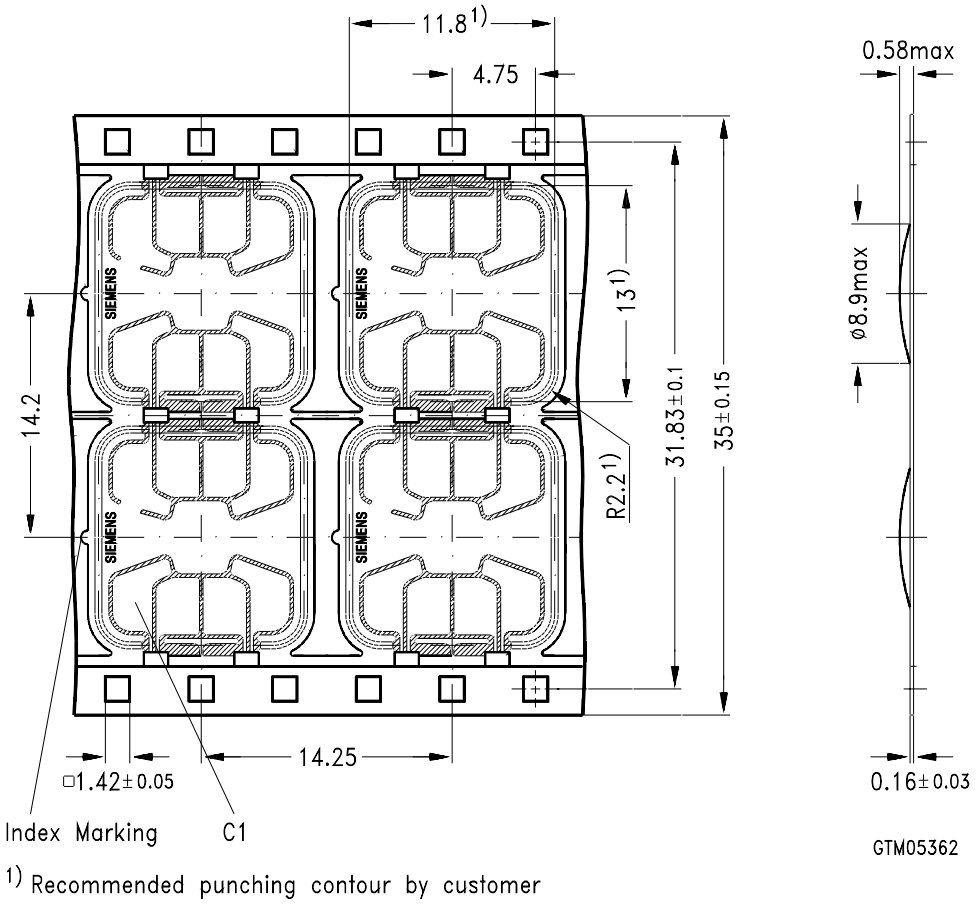
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{CC}	– 0.3		6	V
Input voltage	V_I	– 0.3		6	V
Storage temperature	T_{stg}	– 40		125	°C
Power dissipation	P_{tot}			60	mW

Operating Range

Supply voltage	V_{CC}	4.5		5.5	V
Ambient temperature	T_A	– 35		100	°C

DC Characteristics

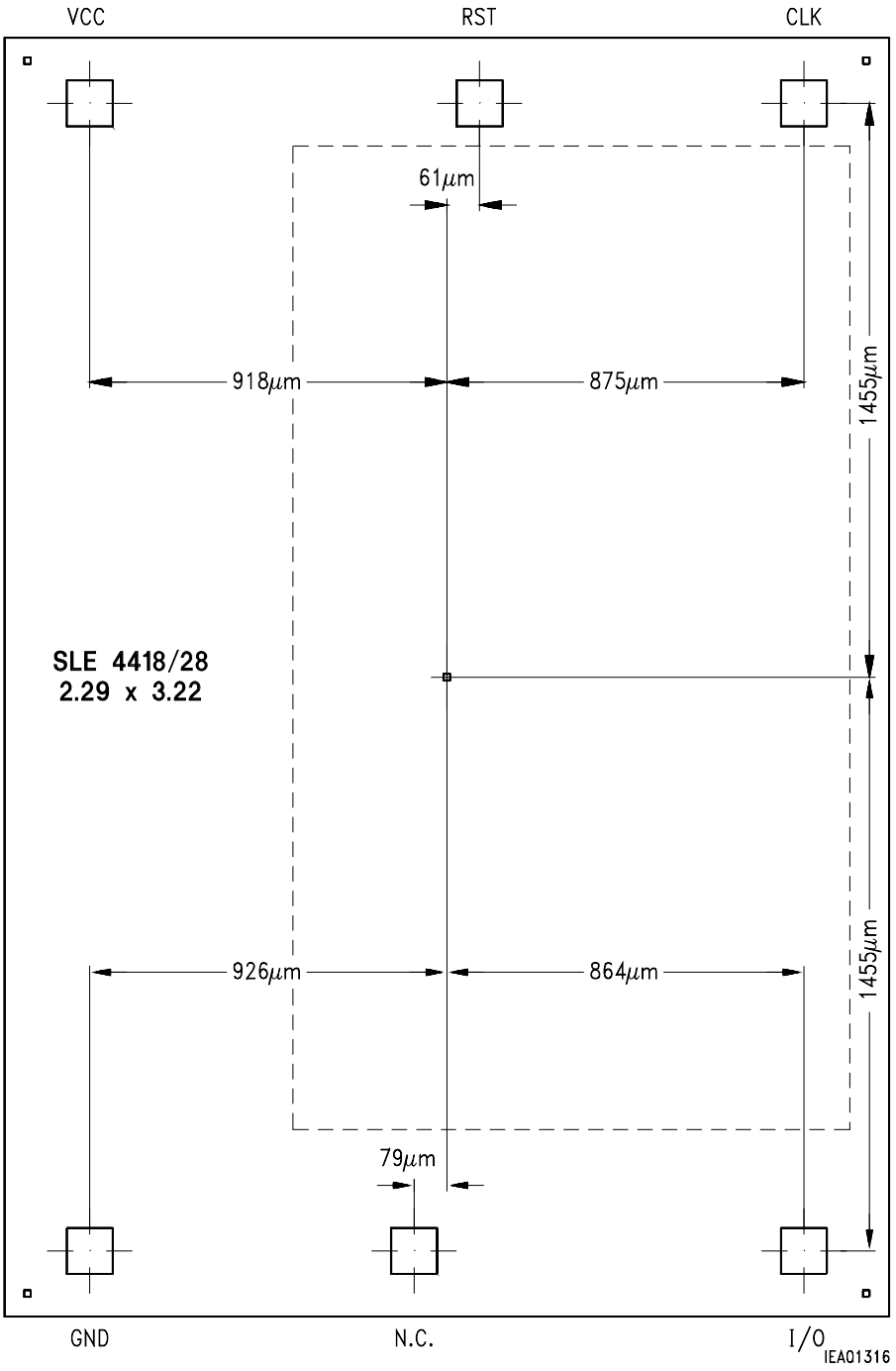
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply					
Supply voltage	V_{CC}	4.5	5	5.5	V
Supply current	I_{CC}	–	3	10	mA
Data Input					
H input voltage (I/O, CLK, RST)	V_H	3.5	–	V_{CC}	V
L input voltage (I/O, CLK, RST)	V_L	0	–	0.8	V
H input current (I/O, CLK, RST)	I_H	–	–	10	µA
Data Output					
L output current (V_L = 0.4 V, open drain)	I_L	0.5	–	–	mA
H leakage current (V_H = V_{DD}, open drain)	I_H	–	–	10	µA
Input capacitance	C_I	–	–	10	pF
Test pin	T	open or on V_{SS}			
Clock frequency	f_C	–	20	–	kHz
Pulse Duration					
Reset time	t_{RE}	9	–	–	µs
Answer to reset (RST)	t_{d6}	20	50	–	µs
CLK (count, H level)	t_H	10	–	–	µs
CLK (count, L level)	t_L	10	–	–	µs
Write time (f = 20 kHz)	t_W	5	–	–	ms
Erase time (f = 20 kHz)	t_E	5	–	–	ms
AC Characteristics					
Setup time (D/CLK)	t_{d1}	4	–	–	µs
Setup time (CLK/RST)	t_{d3}	4	–	–	µs
Setup time (RST/CLK)	t_{d4}	4	–	–	µs
Hold time (D/CLK)	t_{d5}	4	–	–	µs
Delay time (CLK/D)	t_{d2}	6	–	–	µs
Rise time (I/O, CLK, RST)	t_R	–	–	1	µs
Fall time (I/O, CLK, RST)	t_F	–	–	1	µs



Wire-Bonded Module M2.2

Wafer Size: 5”
Stepping Size: 2290 x 3220 µm

Scribe Line: 80 µm
Pad Size: 110 x 110 µm^2



Chip Dimensions