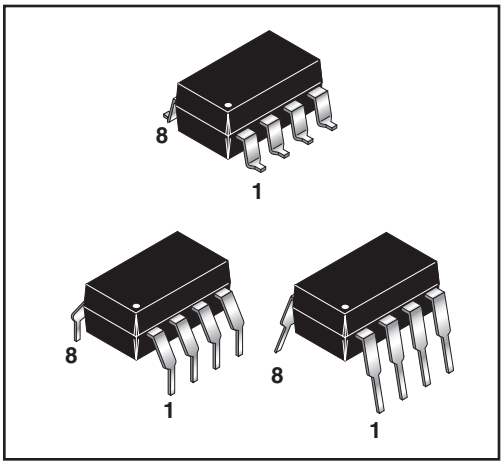
AC/DC TO LOGIC INTERFACE OPTOCOUPLER

HCPL-3700

DESCRIPTION

The HCPL-3700 voltage/current threshold detection optocoupler consists of an AlGaAs LED connected to a threshold sensing input buffer IC which are optically coupled to a high gain darlington output. The input buffer chip is capable of controlling threshold levels over a wide range of input voltages with a single resistor. The output is TTL and CMOS compatible.



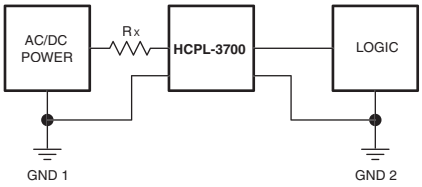
FEATURES

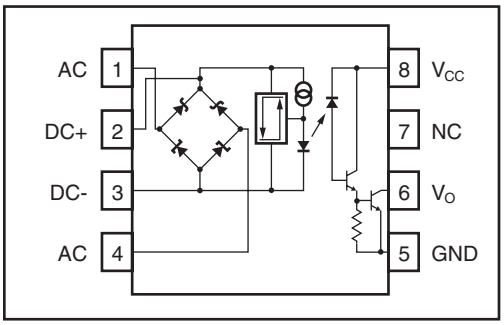
- AC or DC input
- Programmable sense voltage
- Logic level compatibility
- Threshold guaranteed over temperature (0°C to 70°C)
- Optoplanar™ construction for high common mode immunity
- UL recognized (file # E90700)

TRUTH TABLE
(Positive Logic)

Input	Output
H	L
L	H

A 0.1 µF bypass capacitor must be connected between pins 8 and 5.





APPLICATIONS

- Low voltage detection
- 5 V to 240 V AC/DC voltage sensing
- Relay contact monitor
- Current sensing
- Microprocessor Interface
- Industrial controls

ABSOLUTE MAXIMUM RATINGS (No derating required up to 70°C)

Parameter			Symbol	Value	Units
Storage Temperature			T_{STG}	-55 to +125	°C
Operating Temperature			T_{OPR}	-40 to +85	°C
Lead Solder Temperature			T_{SOL}	260 for 10 sec	°C
EMITTER	Average		I_{IN}	50 (MAX)	mA
Input Current	Surge	3 ms, 120 Hz Pulse Rate		140 (MAX)	
	Transient	10 µs, 120 Hz Pulse Rate		500 (MAX)	
Input Voltage (Pins 2-3)			V_{IN}	-0.5 (MIN)	V
Input Power Dissipation		(Note 1)	P_{IN}	230 (MAX)	mW
Total Package Power Dissipation		(Note 2)	P_T	305 (MAX)	mW
DETECTOR					
Output Current	(Average)	(Note 3)	I_O	30 (MAX)	mA
Supply Voltage	(Pins 8-5)		V_{CC}	-0.5 to 20	V
Output Voltage	(Pins 6-5)		V_O	-0.5 to 20	V
Output Power Dissipation		(Note 4)	P_O	210 (MAX)	mW

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C Unless otherwise specified)

Parameter		Test Conditions	Symbol	Min	Typ	Max	Unit
Input Threshold Current		(V_{IN} = V_{TH+}, V_{CC} = 4.5 V)	I_{TH+}	1.96	2.4	3.11	mA
		(V_O = 0.4 V, $I_O \geq$ 4.2 mA) (Note 5)	I_{TH-}	1.00	1.2	1.62	mA
Input Threshold Voltage	DC (Pins 2,3)	(V_{IN} = V_2 - V_3, Pins 1 & 4 Open) (V_{CC} = 4.5 V, V_O = 0.4 V) (Note 5) ($I_O \geq$ 4.2 mA)	V_{TH+}	3.35	3.8	4.05	V
		(V_{IN} = V_2 - V_3, Pins 1 & 4 Open) (V_{CC} = 4.5 V, V_O = 2.4 V) (Note 5) ($I_O \geq$ 100 µA)	V_{TH-}	2.01	2.5	2.86	V
	AC (Pins 1,4)	$\lvert V_{IN} \rvert$ = $\lvert V_1$ - $V_4 \rvert$ (Pins 2 & 3 Open) (V_{CC} = 4.5 V, V_O = 0.4 V) (Note 5) ($I_O \geq$ 4.2 mA)	V_{TH+}	4.23	5.0	5.50	V
		$\lvert V_{IN} \rvert$ = $\lvert V_1$ - $V_4 \rvert$ (Pins 2 & 3 Open) (V_{CC} = 4.5 V, V_O = 2.4 V) (Note 5) ($I_O \leq$ 100 µA)	V_{TH-}	2.87	3.7	4.20	V
Hysteresis		(I_{HYS} = I_{TH+} - I_{TH-})	I_{HYS}		1.2		mA
		(V_{HYS} = V_{TH+} - V_{TH-})	V_{HYS}		1.3		V
Input Clamp Voltage		(V_{IHC1} = V_2 - V_3, V_3 = GND) (I_{IN} = 10 mA, Pins 1 & 4 Connected to Pin 3)	V_{IHC1}	5.4	6.3	6.6	V
		(V_{IHC2} = $\lvert V_1$ - $V_4 \rvert$) ($\lvert I_{IN} \rvert$ = 10 mA) (Pins 2 & 3 Open)	V_{IHC2}	6.1	7.0	7.3	V
		(V_{IHC3} = V_2 - V_3, V_3 = GND) (I_{IN} = 15 mA; Pins 1 & 4 Open)	V_{IHC3}		12.5	13.4	V
		(V_{ILC} = V_2 - V_3, V_3 = GND) (I_{IN} = -10 mA)	V_{ILC}		-0.75		V
Input Current		(V_{IN} = V_2 - V_3 = 5.0 V) (Pins 1 & 4 Open)	I_{IN}	3.0	3.7	4.4	mA
Bridge Diode Forward Voltage		(I_{IN} = 3 mA)	$V_{D1,2}$		0.65		V
		(I_{IN} = 3 mA)	$V_{D3,4}$		0.65		V
Logic Low Output Voltage		(V_{CC} = 4.5 V; I_{OL} = 4.2 mA) (Note 5)	V_{OL}		0.04	0.4	V
Logic High Output Current		(Note 5) (V_{OH} = V_{CC} = 18 V)	I_{OH}			100	µA
Logic Low Supply Current		(V_2 - V_3 = 5.0 V; V_O = Open) (V_{CC} = 5 V)	I_{CCL}		1.0	4	mA
Logic High Supply Current		(V_{CC} = 18 V; V_O = Open)	I_{CCH}		0.01	4	µA
Input Capacitance		(f = 1 MHz; V_{IN} = 0V) (Pins 2 & 3, Pins 1 & 4 Open)	C_{IN}		50		pF

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	2	18	V
Operating Temperature	T_A	0	70	°C
Operating Frequency	f	0	4	kHz

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5 V Unless otherwise specified)

AC Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
Propagation Delay Time (to Output Low Level)	(R_L = 4.7 kΩ, C_L = 30 pF) (Note 6)	T_{PHL}		6.0	15	µs
Propagation Delay Time (to Output High Level)	(R_L = 4.7 kΩ, C_L = 30 pF) (Note 6)	T_{PLH}		25.0	40	µs
Output Rise Time (10-90%)	(R_L = 4.7 kΩ, C_L = 30 pF)	t_r		45		µs
Output Fall Time (90-10%)	(R_L = 4.7 kΩ, C_L = 30 pF)	t_f		0.5		µs
Common Mode Transient Immunity (at Output High Level)	(I_{IN} = 0 mA, R_L = 4.7 kΩ) ($V_{O\ min}$ = 2.0 V, V_{CM} = 1400 V) (Notes 7,8)	$\|CM_H\|$		4000		V/µs
Common Mode Transient Immunity (at Output Low Level)	(I_N = 3.11 mA,R_L = 4.7 kΩ) ($V_{O\ max}$ = 0.8 V, V_{CM} = 140 V) (Notes 7,8)	$\|CM_L\|$		600		V/µs

PACKAGE CHARACTERISTICS (T_A = 0°C to 70°C Unless otherwise specified)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
Withstand Insulation Voltage	(Relative humidity < 50%) (T_A = 25°C, t = 1 min) (Notes 9,10)	V_{ISO}	2500			V_{RMS}
Resistance (input to output)	(Note 9) (V_{IO} = 500 Vdc)	R_{I-O}		10^{12}		Ω
Capacitance (input to output)	(f = 1 MHz, V_{IO} = 0 Vdc)	C_{I-O}		0.6		pF

NOTES

1. Derate linearly above 70°C free-air temperature at a rate of 1.8 mW/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 2.5 mW/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.6 mA/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 1.9 mW/°C.
5. Logic low output level at pin 6 occurs when $V_{IN} \geq V_{TH+}$ and when $V_{IN} > V_{TH-}$ once V_{IN} exceeds V_{TH+}. Logic high output level at pin 6 occurs when $V_{IN} \leq V_{TH-}$ and when $V_{IN} < V_{TH+}$ once V_{IN} decreases below V_{TH-}.
6. T_{PHL} propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 µs rise time) to the 1.5 V level on the leading edge of the output pulse. T_{PLH} propagation delay is measured on the trailing edges of the input and output pulse. (Refer to Fig. 9)
7. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM}, to assure that the output will remain in a logic high state (i.e., $V_O > 2.0$ V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., $V_O < 0.8$ V). (Refer to Fig.10)
8. In applications where dV_{cm}/dt may exceed 50,000 V/µs (Such as static discharge), a series resistor, R_{CC}, should be included to protect the detector chip from destructive surge currents. The recommended value for R_{CC} is 240 V per volt of allowable drop in V_{CC} (between pin 8 and V_{CC}) with a minimum value of 240 Ω.
9. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
10. The 2500 V_{RMS}/1 min. capability is validated by a 3.0 kV_{RMS}/1 sec. dielectric voltage withstand test.
11. AC voltage is instantaneous voltage for V_{TH+} & V_{TH-}.
12. All typicals at $T_A = 25°C$, $V_{CC} = 5$ V unless otherwise specified.

TYPICAL PERFORMANCE CURVES

Fig. 1 Logic Low Supply Current vs. Operating Supply Voltage

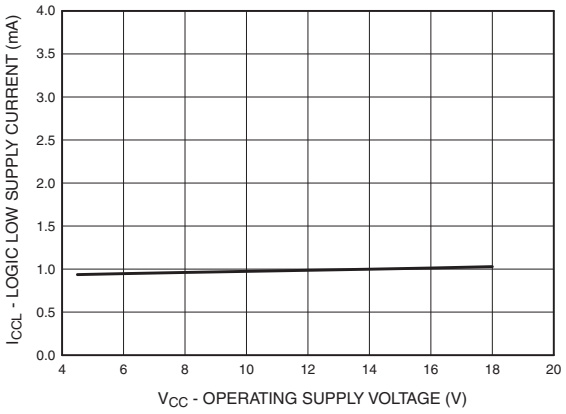


Fig. 2 Input Current vs. Input Voltage

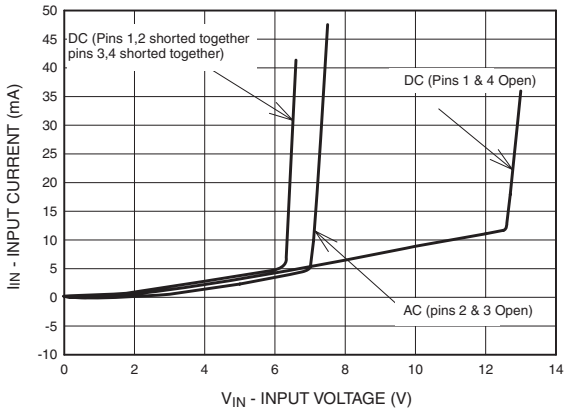


Fig. 3 Input Current/Low Level Output Voltage vs. Temperature

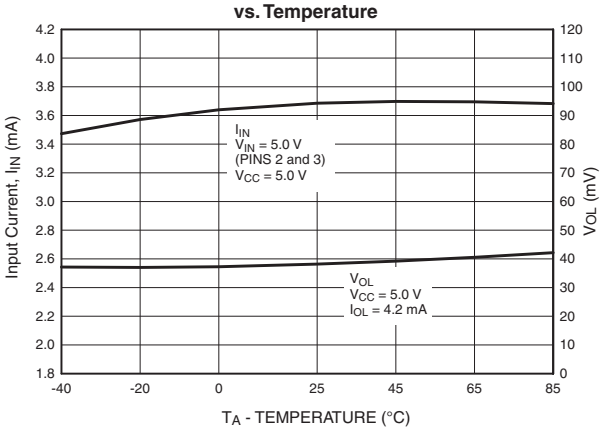


Fig. 4 Current Threshold/Voltage Threshold vs. Temperature

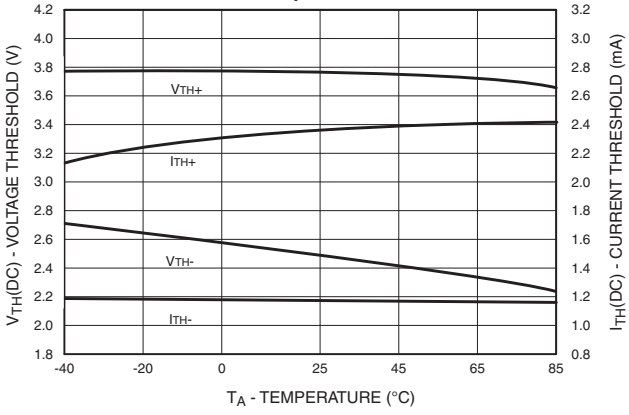


Fig. 5 Propagation Delay vs. Temperature

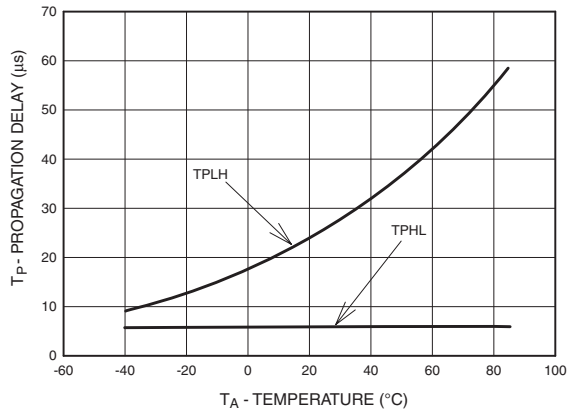


Fig. 6 Rise and Fall Time vs. Temperature

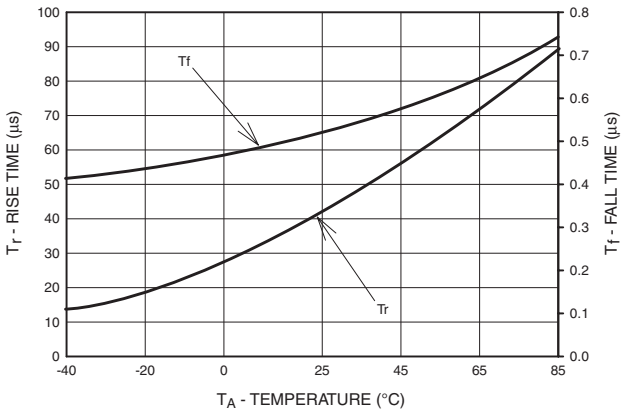


Fig. 7 Logic High Supply Current vs. Temperature

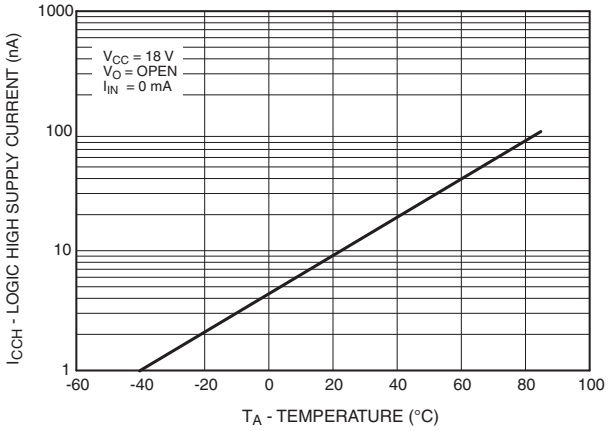
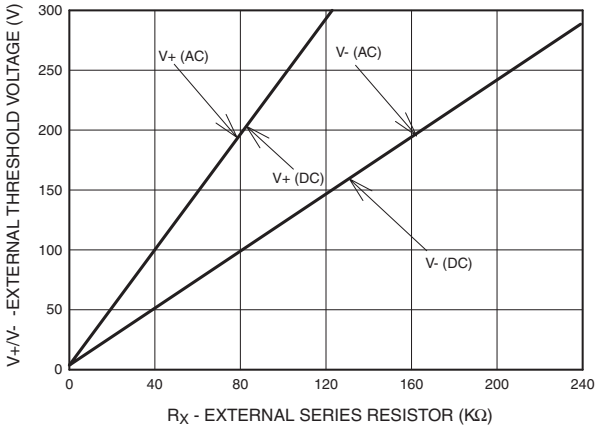


Fig. 8 External Threshold Characteristics V+/V- vs. Rx



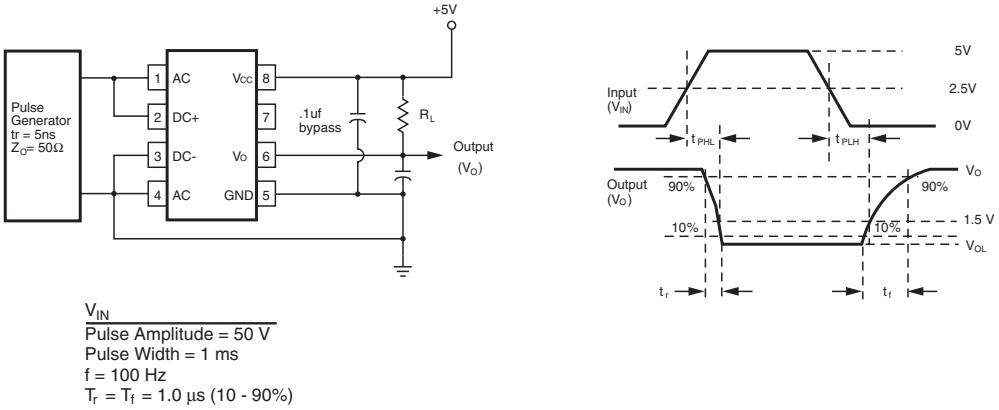


Fig. 9. Switching Test Circuit

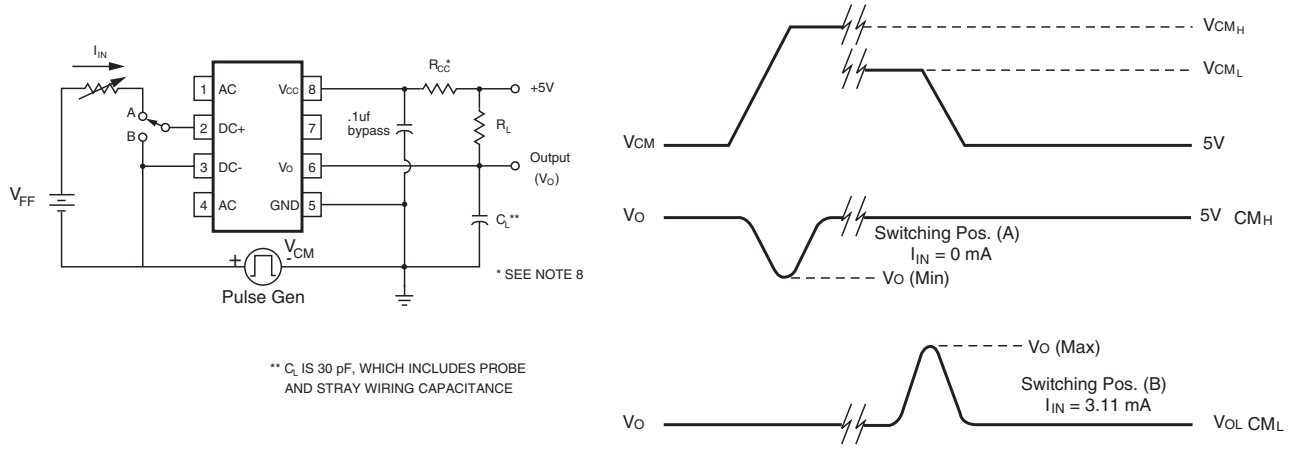
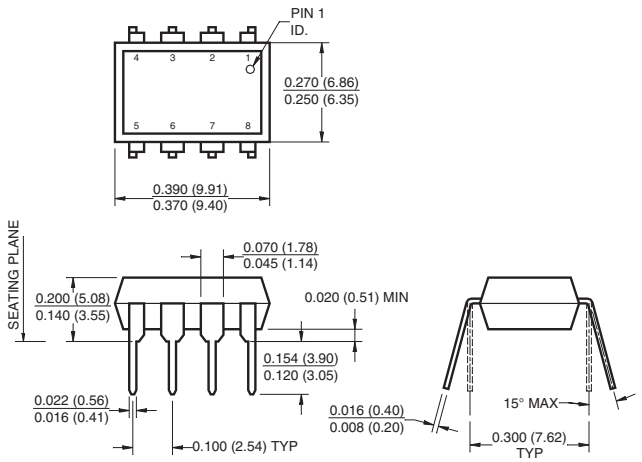
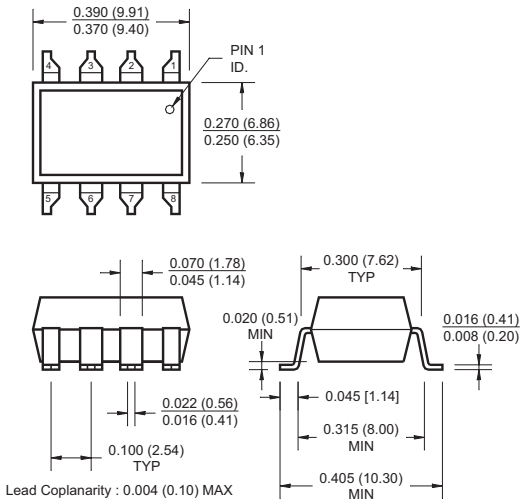


Fig. 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

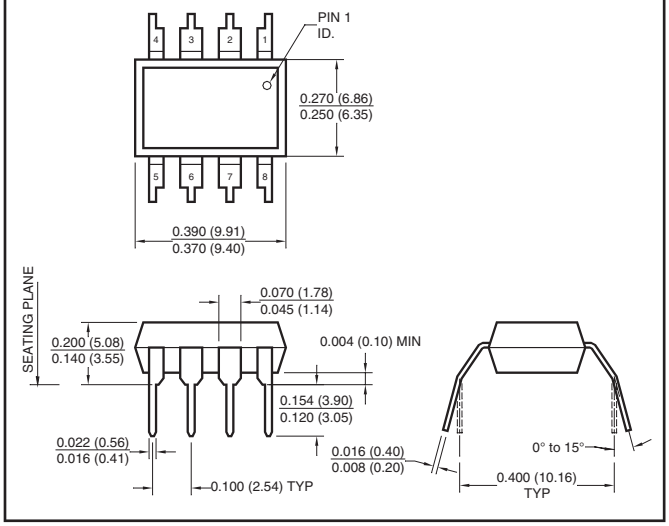
Package Dimensions (Through Hole)



Package Dimensions (Surface Mount)



Package Dimensions (0.4"Lead Spacing)

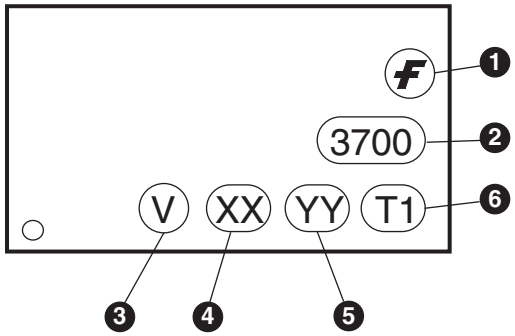


NOTE
All dimensions are in inches (millimeters)

ORDERING INFORMATION

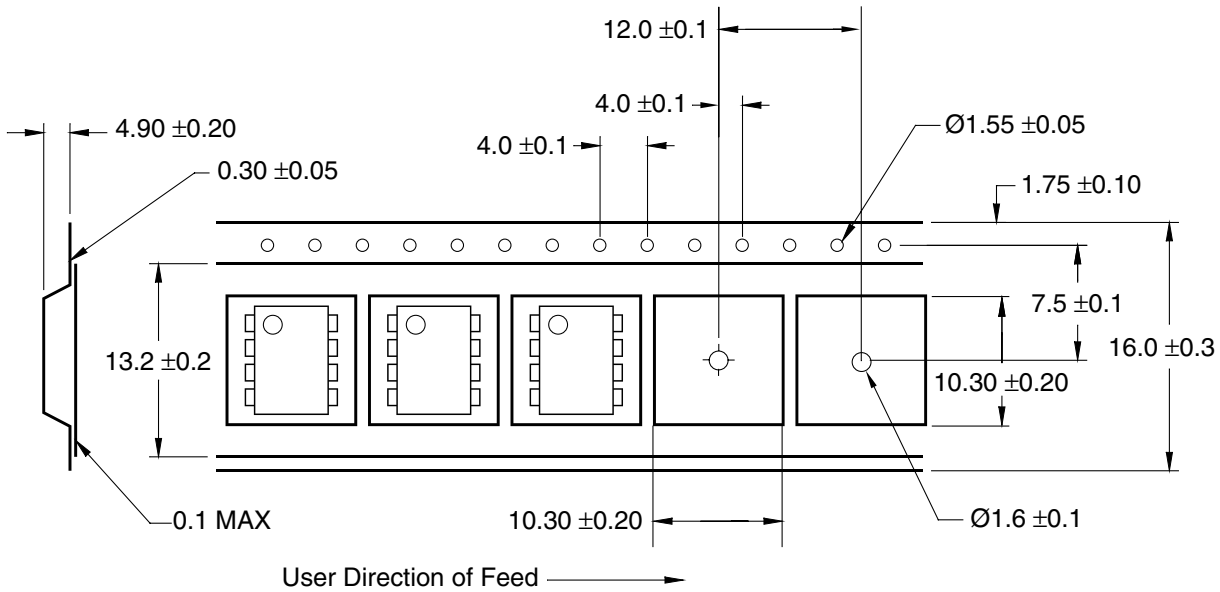
Option	Order Entry Identifier	Description
S	.S	Surface Mount Lead Bend
SD	.SD	Surface Mount; Tape and reel
W	.W	0.4” Lead Spacing

MARKING INFORMATION

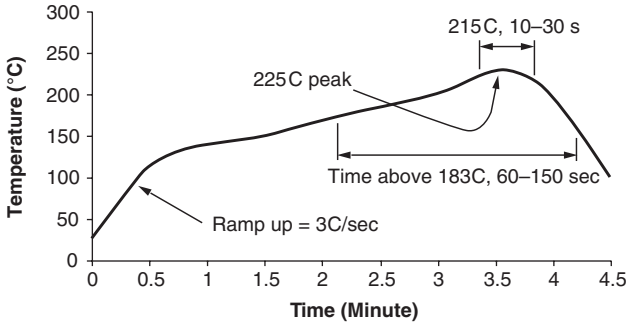


Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	Two digit year code, e.g., ‘03’
5	Two digit work week ranging from ‘01’ to ‘53’
6	Assembly package code

QT Carrier Tape Specifications ("D" Taping Orientation)



Reflow Profile



- Peak reflow temperature: 225C (package surface temperature)
- Time of temperature higher than 183C for 60–150 seconds
- One time soldering reflow is recommended

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.