HARRIS Semiconductor

NOT RECOMMENDED FOR NEW DESIGNS
See HS-1840ARH

HS-1840RH

Rad-Hard 16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection

September 1997

Features

- Radiation Environment
  - Gamma Rate ($\dot{\gamma}$) 1 x 10^8 RAD(Si)/s
  - Gamma Dose (γ) 2 x 10^5 RAD(Si)
- Low Power Consumption
- Fast Access Time 1000ns
- High Analog Input Impedance 500MΩ During Power Loss (Open)
- Dielectrically Isolated Device Islands
- Excellent In Hi-Rel Redundant Systems
- Break-Before-Make Switching
- No Latch-Up

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HS1-1840RH-Q	-55 to 125	28 Ld CERDIP	
HS1-1840RH-8	-55 to 125	28 Ld CERDIP	
HS1-1840RH/Proto	-55 to 125	28 Ld CERDIP	
HS1-1840RH/Sample	25	28 Ld CERDIP	
HS9-1840RH-Q	-55 to 125	28 Ld FP	
HS9-1840RH-8	-55 to 125	28 Ld FP	
HS9-1840RH/Proto	-55 to 125	28 Ld FP	
HS9-1840RH/Sample	25	28 Ld FP	

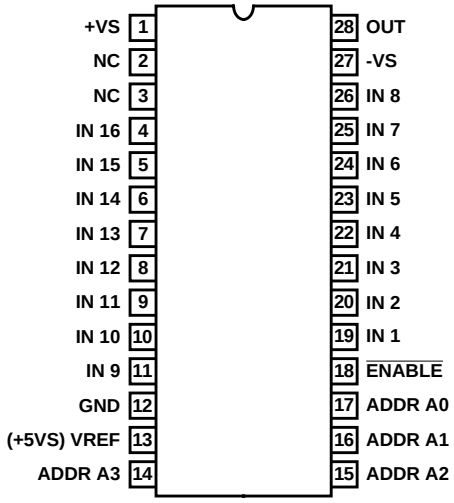
Description

The HS-1840RH is a radiation hardened, monolithic 16 channel multiplexer constructed with the Harris Linear Dielectric Isolation CMOS process. It is designed to provide a high input impedance to the analog source if device power fails (open) or the analog signal voltage inadvertently exceeds the supply rails during powered operation. Excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. More significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. All digital inputs have electrostatic discharge protection.

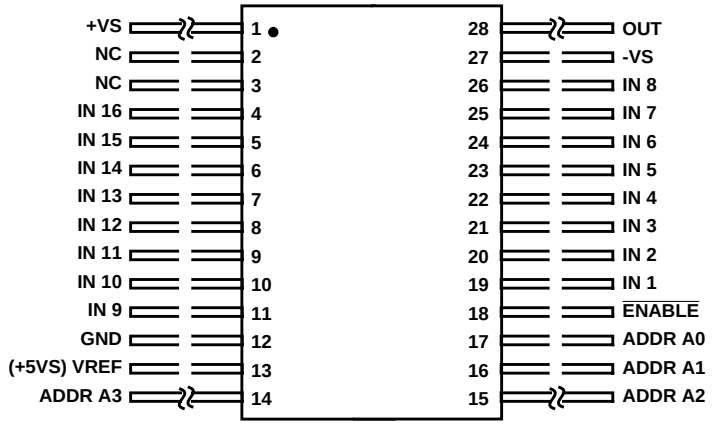
The HS-1840RH has been specifically designed to meet exposure to radiation environments. It is available in a 28 lead Ceramic Sidebraze dual-in-line package and 28 lead Ceramic Flatpack. It is guaranteed operational from -55^{o}C to +125^{o}C.

Pinouts

HS1-1840RH 28 LEAD SIDEBRAZE CERDIP CASE OUTLINE GDIP1-T28, COMPLIANT TO MIL-STD-1835 PACKAGE
TOP VIEW



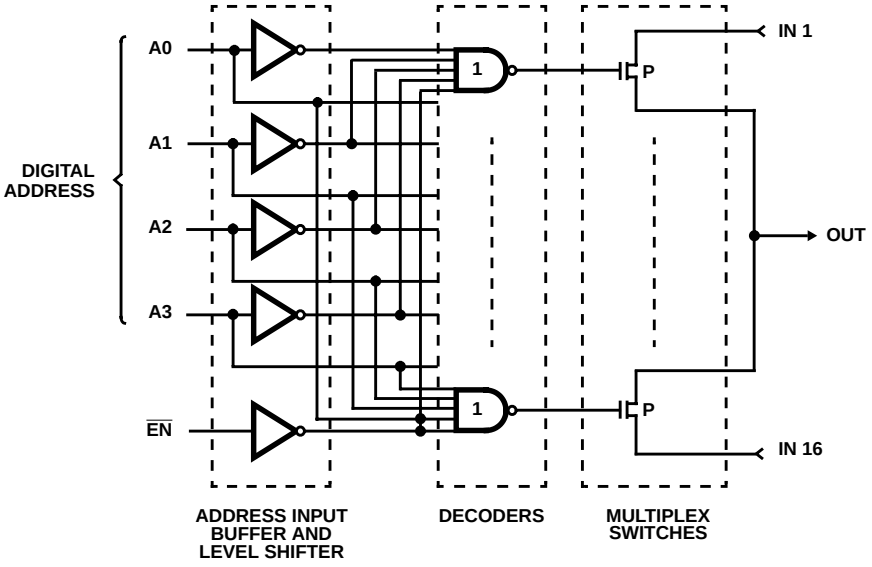
HS9-1840RH 28 LEAD CERAMIC SIDEBRAZE CASE FLATPACK OUTLINE CDFP3-F28, COMPLIANT TO MIL-STD-1835 PACKAGE
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3992.1
Spec Number 518022

Functional Diagram



Truth Table

A3	A2	A1	A0	$\overline{EN}$	"ON" CHANNEL
X	X	X	X	H	None
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

Absolute Maximum Ratings

Supply Voltage Between Pins 1 and 27 . . . . . +40V
+VSUPPLY to Ground . . . . . +20V
-VSUPPLY to Ground . . . . . -20V
VREF to Ground . . . . . +20V
Analog Input Overvoltage
+VS . . . . . +25V (Power On/Off)
-VS . . . . . -25V (Power On/Off)
Digital Input Overvoltage
+VEN, +VA . . . . . VREF +4V
-VEN, -VA . . . . . GND -4V
Continuous Current 10mA
Storage Temperature Range . . . . . -65^oC to $+150^oC$
Junction Temperature . . . . . $+175^oC$
Lead Temperature (Soldering 10s) . . . . . $+275^oC$

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
Sidebraze Package	$83.1^oC/W$	$19.1^oC/W$
Flatpack Package	$49.1^oC/W$	$16.5^oC/W$

Total Power Dissipation (Note)
Sidebraze CerDIP Package 1600mW
Ceramic Flatpack Package 1400mW
ESD Classification . . . . . Class 1

NOTE: For DIP Derate $20.4mW/^oC$ above $T_A = +95^oC$
For Flatpack Derate $18.5mW/^oC$ above $T_A = +95^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (±VSUPPLY) . . . . . ±15V
Operating Temperature Range . . . . . -55^oC to $+125^oC$
VREF (Pin 13) . . . . . +5V
Logic Low Level (VAL) . . . . . +0.8V
Logic High Level (VAH) . . . . . +4.0V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, VREF = +5V, VAH = +4.0V, VAL = 0.8V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Analog Signal Range	VS		7, 8A, 8B	-55^oC, $+25^oC$, $+125^oC$	-5	+15	V
Input Leakage Current, Address, or Enable Pins	IAH IAL	Measure Inputs Sequentially Ground All Unused Pins	1, 2, 3	-55^oC, $+25^oC$, $+125^oC$	-1000	1000	nA
Leakage Current Into the Source Terminal of an "Off" Switch	+IS(OFF)	VS = +10V, All Unused Inputs and Output = -10V, VEN = 4V	1	$+25^oC$	-10	10	nA
			2, 3	$+125^oC$,-55^oC	-100	100	nA
	-IS(OFF)	VS = -10V, All Unused Inputs, Output = +10V, VEN = 4V	1	$+25^oC$	-10	10	nA
			2, 3	$+125^oC$, -55^oC	-100	100	nA
Leakage Current into the Source Terminal of an "Off" Switch With Power "Off"	+IS(OFF) Power Off	V+, V-, VREF, A0, A1, A2, A3,A4, EN = GND, Unused Inputs Tied to GND, VS = +25V	1	$+25^oC$	-50	50	nA
			2, 3	$+125^oC$, -55^oC	-100	100	nA
Leakage Current Into the Source Terminal of an "Off" Switch With Overvoltage Applied	+IS(OFF) Overvoltage	VS = +25V, VD = 0V, VEN = 4V All Unused Inputs Tied to GND	1, 2, 3	-55^oC, $+25^oC$, $+125^oC$	-1000	1000	nA
	-IS(OFF) Overvoltage	VS = -25V, VD = 0V, VEN = 4V All Unused Inputs Tied to GND	1, 2, 3	-55^oC, $+25^oC$, $+125^oC$	-1000	1000	nA
Leakage Current Into the Drain Terminal of an "Off" Switch	+ID(OFF)	VD = +10V, VEN = 4V All Unused Inputs = -10V	1	$+25^oC$	-10	10	nA
			2, 3	$+125^oC$, -55^oC	-100	100	nA
	-ID(OFF)	VD = -10V, VEN = 4V All Unused Inputs = +10V	1	$+25^oC$	-10	10	nA
			2, 3	$+125^oC$, -55^oC	-100	100	nA
Leakage Current Into the Drain Terminal of an "Off" Switch With Overvoltage Applied	+ID(OFF) Overvoltage	VS = +25V, Measure VD, VEN = 4V, All Unused Inputs to GND	1, 2, 3	-55^oC, $+25^oC$, $+125^oC$	-1000	1000	nA
	-ID(OFF) Overvoltage	VS = -25V, Measure VD, All Unused Inputs to GND	1, 2, 3	-55^oC, $+25^oC$, $+125^oC$	-1000	1000	nA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, VREF = +5V, VAH = +4.0V, VAL = 0.8V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Leakage Current from an "On" Driver into the Switch (Drain & Source)	+ID(ON)	VS = +10V, VD = +10V, VEN = 0.8V All Unused Inputs = -10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-100	100	nA
	-ID(ON)	VS = -10V, VD = -10V, VEN = 0.8V, All Unused Inputs = +10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-100	100	nA
Switch On Resistance	+15V R(ON)	VS = +15V, ID = -1mA, VEN = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	50	1000	Ω
	-5V R(ON)	VS = -5V, ID = +1mA, VEN = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	50	4000	Ω
	+5V R(ON)	VS = +5V, ID = -1mA, VEN = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	50	2500	Ω
Positive Supply Current	I(+)	VEN = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	mA
Negative Supply Current	I(-)	VEN = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	-0.5	-	mA
Positive Standby Supply Current	+ISBY	VEN = 4.0V	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	mA
Negative Standby Supply Current	-ISBY	VEN = 4.0V	1, 2, 3	-55°C, +25°C, +125°C	-0.5	-	mA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, VREF = +5V, VAH = +4.0V, VAL = 0.8V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	TD	RL = 1000Ω, CL = 50pF	9	+25°C	25	-	ns
			10, 11	+125°C, -55°C	5	-	ns
Propagation Delay Times: Address Inputs to I/O Channels	TON(A), TOFF(A)	RL = 10kΩ, CL = 50pF	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	1000	ns
Enable to I/O	TON(EN), TOFF(EN)	RL = 1000Ω, CL = 50pF	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized At: V- = -15V, V+ = +15V, VREF = +5V, VAH = +4.0V, VAL = 0.8V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Address Input	CA	+VS = -VS = 0V, f = 1MHz	1	+25°C	-	7	pF
Capacitance Channel Input	CS(OFF)	+VS = -VS = 0V, f = 1MHz	1	+25°C	-	5	pF
Capacitance Channel Output	CD(OFF) TOFF(EN)	+VS = -VS = 0V, f = 1MHz	1	+25°C	-	50	pF
Off Isolation	VISO	VEN = 4.0V, f = 200kHz, CL = 7pF, RL = 1kΩ, VS = 3.0VRMS	1	+25°C	45	-	dB

NOTE: 1. The parameters listed in Table 3 are controlled via design or process parameters and not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. POST 200K RAD(Si) ELECTRICAL CHARACTERISTICS

Tested, per MIL-STD-883. Unless Otherwise Specified: V- = -15V, V+ = +15V, VREF = +5V, VAH = +4.5V, VAL = 0.5V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Leakage Current, Address, or Enable Pins	IAH IAL	Measure Inputs Sequentially, Ground All Unused Pins	1	+25°C	-1000	1000	nA
Leakage Current Into the Source Terminal of an “Off” Switch	+IS(OFF)	VS = +10V, All Unused Inputs and Output = -10V, VEN = 4.5V	1	+25°C	-100	100	nA
	-IS(OFF)	VS = -10V, All Unused Inputs and Output = +10V, VEN = 4.5V	1	+25°C	-100	100	nA
Leakage Current into the Source Terminal of an “Off” Switch With Power “Off”	+IS(OFF) Power Off	V+, V-, VREF, A0, A1, A2, A3, A4, EN = GND, Unused Inputs Tied to GND, VS = +25V	1	+25°C	-100	100	nA
Leakage Current Into the Source Terminal of an “Off” Switch With Overvoltage Applied	+IS(OFF) Overvoltage	VS = +25V, VD = 0V, VEN = 4.5V All Unused Inputs Tied to GND	1	+25°C	-1500	1500	nA
	-IS(OFF) Overvoltage	VS = -25V, VD = 0V, VEN = 4.5V All Unused Inputs Tied to GND	1	+25°C	-1500	1500	nA
Leakage Current Into the Drain Terminal of an “Off” Switch	+ID(OFF)	VD = +10V, VEN = 4.5V All Unused Inputs = -10V	1	+25°C	-100	100	nA
	-ID(OFF)	VD = -10V, VEN = 4.5V All Unused Inputs = +10V	1	+25°C	-100	100	nA
Leakage Current Into the Drain Terminal of an “Off” Switch With Overvoltage Applied	+ID(OFF) Overvoltage	VS = +25V, Measure VD, VEN = 4.5V All Unused Inputs to GND	1	+25°C	-1000	1000	nA
	-ID(OFF) Overvoltage	VS = -25V, Measure VD, VEN = 4.5V All Unused Inputs to GND	1	+25°C	-1000	1000	nA
Leakage Current from an “On” Driver into the Switch (Drain & Source)	+ID(ON)	VS = +10V, VD = +10V, VEN = 0.5V All Unused Inputs = -10V	1	+25°C	-100	100	nA
	-ID(ON)	VS = -10V, VD = -10V, VEN = 0.5V All Unused Inputs = +10V	1	+25°C	-100	100	nA
Switch On Resistance	+15V R(ON)	VS = +15V, ID = -1mA, VEN = 0.5V	1	+25°C	50	1000	Ω
	-5V R(ON)	VS = -5V, ID = +1mA, VEN = 0.5V	1	+25°C	50	4000	Ω
	+5V R(ON)	VS = +5V, ID = -1mA, VEN = 0.5V	1	+25°C	50	2500	Ω
Positive Supply Current	I(+)	VEN = 0.5V	1	+25°C	-	0.50	mA
Negative Supply Current	I(-)	VEN = 0.5V	1	+25°C	-0.50	-	mA
Positive Standby Supply Current	+I(SBY)	VEN = 4.5V	1	+25°C	-	0.50	mA
Negative Standby Supply Current	-I(SBY)	VEN = 4.5V	1	+25°C	-0.50	-	mA
Make-Before-Break Time Delay	TD	RL = 1000Ω, CL = 50pf	9	+25°C	5	-	ns
Propagation Delay Times: Address Inputs to I/O Channels	TON (A) TOFF (A)	RL = 10KΩ, CL = 50pf	9	+25°C	-	3000	ns
Enable to I/O	TON (EN) TOFF (EN)	RL = 1000Ω, CL = 50pf	9	+25°C	-	3000	ns

TABLE 5. DC POST BURN-IN DELTA ELECTRICAL CHARACTERISTICS

Guaranteed, per MIL-STD-883, Method 1019. Unless Otherwise Specified: V- = -15V, V+ = +15V, VREF = +5V, VAH = +4.0V, VAL = 0.8V

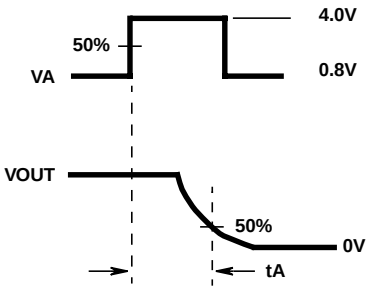
PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Leakage Current, Address, or Enable Pins	IAH IAL	Measure Inputs Sequentially, Ground All Unused Pins	1	+25°C	-100	100	nA
Leakage Current Into the Source Terminal of an “Off” Switch	+IS(OFF)	VS = +10V, All Unused Inputs & Output = -10V, VEN = 4.0V	1	+25°C	-20	20	nA
	-IS(OFF)	VS = -10V, All Unused Inputs & Output = +10V, VEN = 4.0V	1	+25°C	-20	20	nA
Leakage Current Into the Drain Terminal of an “Off” Switch	+ID(OFF)	VD = +10V, VEN = 4.0V All Unused Inputs = -10V	1	+25°C	-20	20	nA
	-ID(OFF)	VD = -10V, VEN = 4.0V All Unused Inputs = +10V	1	+25°C	-20	20	nA
Leakage Current from an “On” Driver into the Switch (Drain & Source)	+ ID(ON)	VS = +10V, VD = +10V, VEN = 0.8V All Unused Inputs = -10V	1	+25°C	-20	20	nA
	-ID(ON)	VS = -10V, VD = -10V, VEN = 0.8V All Unused Inputs = +10V	1	+25°C	-20	20	nA
Switch On Resistance	+15V R(ON)	VS = +15V, ID = -1mA, VEN = 0.8V	1	+25°C	-150	150	Ω
	-5V R(ON)	VS = -5V, ID = +1mA, VEN = 0.8V	1	+25°C	-250	250	Ω
Positive Supply Current	I(+)	VEN = 0.8V	1	+25°C	-50	50	µA
Negative Supply Current	I(-)	VEN = 0.8V	1	+25°C	-50	50	µA
Positive Standby Supply Current	+ISBY	VEN = 4.0V	1	+25°C	-50	50	µA
Negative Standby Supply Current	-ISBY	VEN = 4.0V	1	+25°C	-50	50	µA

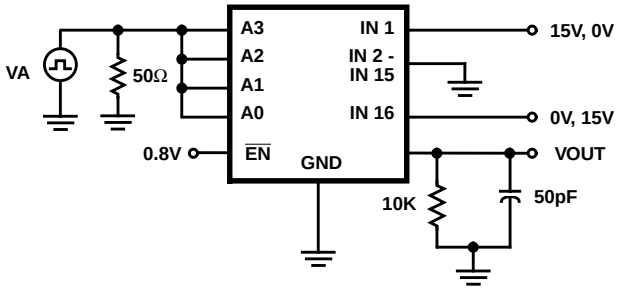
TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1	1
Interim Test		100%/5004	1	N/A
PDA		100%/5004	1	1
Final Test		100%/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3	N/A
	Others	Samples/5005	1, 7	N/A
Group C		Samples/5005	N/A	1, 2, 3
Group D		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7	1, 7

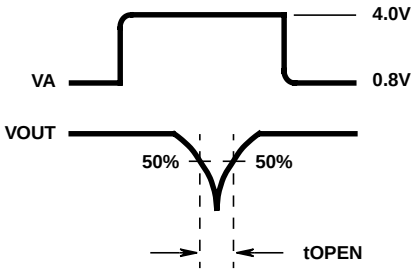
Performance Characteristics and Test Circuits

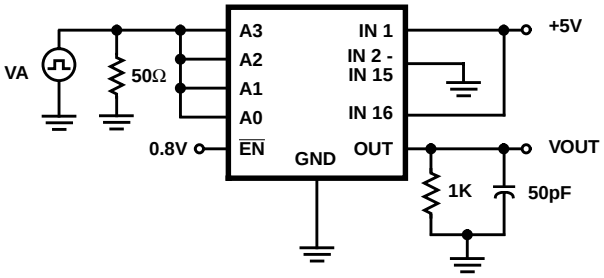
ACCESS TIME vs LOGIC LEVEL (HIGH)



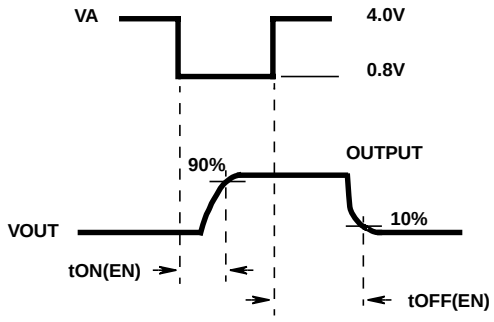


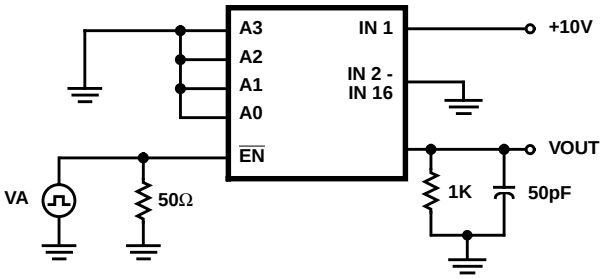
BREAK-BEFORE-MAKE DELAY (tOPEN)



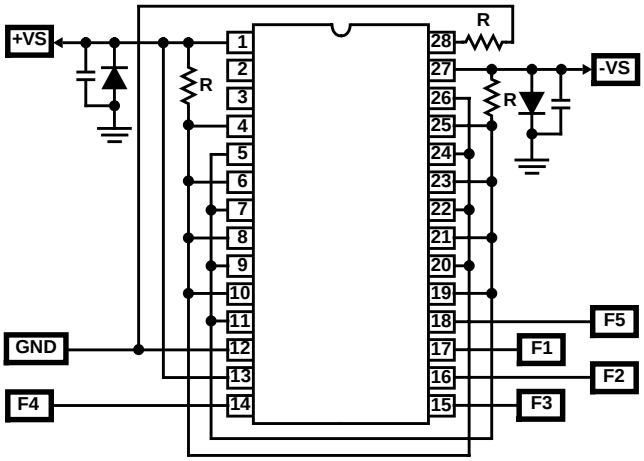


ENABLE DELAY (tON(EN), tOFF(EN))





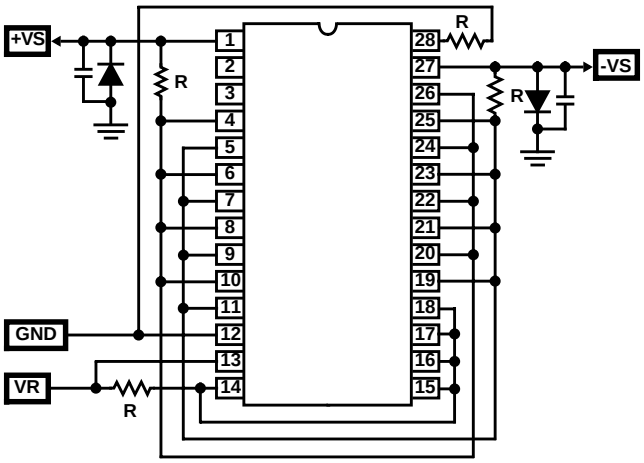
Burn-In/Life Test Circuits



DYNAMIC BURN-IN AND LIFE TEST CIRCUIT

NOTES:

VS+ = +15.5V ±0.5V, VS- = -15.5V ±0.5V
R = 1kΩ ±5%
C1 = C2 = 0.01µF ±10%, 1 each per socket, minimum
D1 = D2 = 1N4002, 1 each per board, minimum
Input Signals: square wave, 50% duty cycle, 0V to 15V peak ±10%
F1 = 100kHz; F2 = F1/2; F3 = F1/4; F4 = F1/8; F5 = F1/16



STATIC BURN-IN TEST CIRCUIT

NOTES:

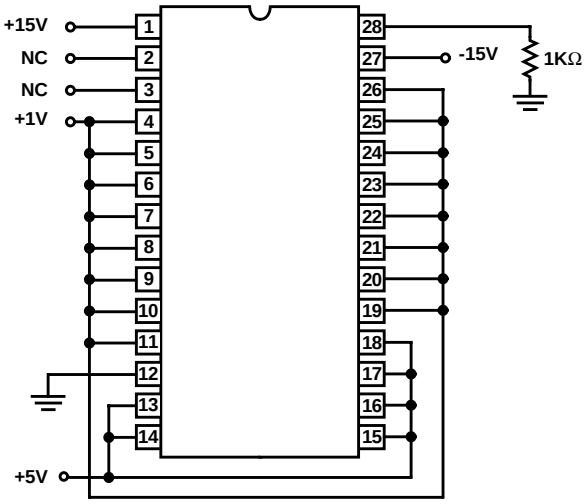
R = 1kΩ ±5%, $^1/_4$W
C1 = C2 = 0.01µF minimum, 1 each per socket, minimum
VS+ = 15.5V ±0.5V, VS- = -15.5V ±0.5V, VR = 15.5 ±0.5V

NOTES:

1. The above test circuits are utilized for all package types.
2. The Dynamic Test Circuit is utilized for all life testing.

Irradiation Circuit

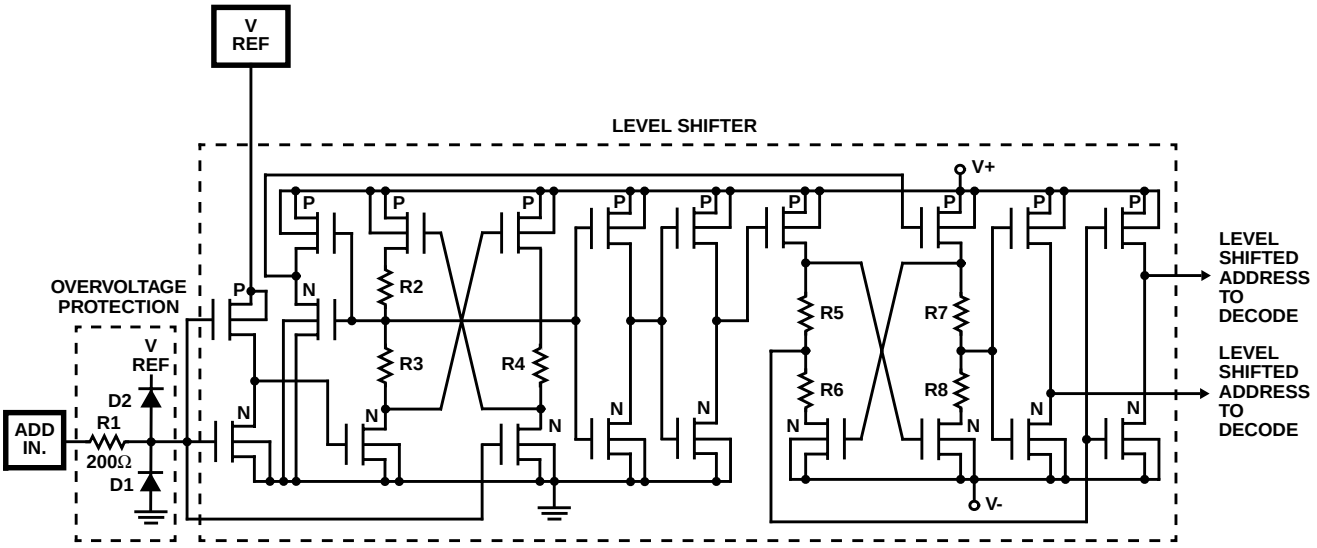
HS-1840RH 28 LEAD DIP



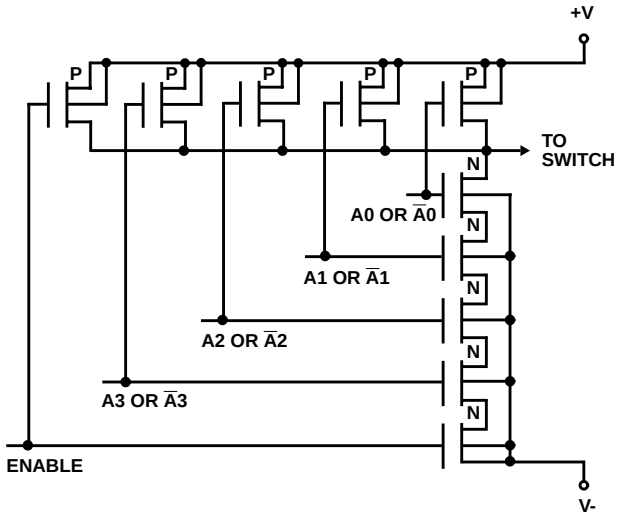
NOTE: All irradiation testing is performed in the 28 lead CerDIP package.

Schematic Diagrams

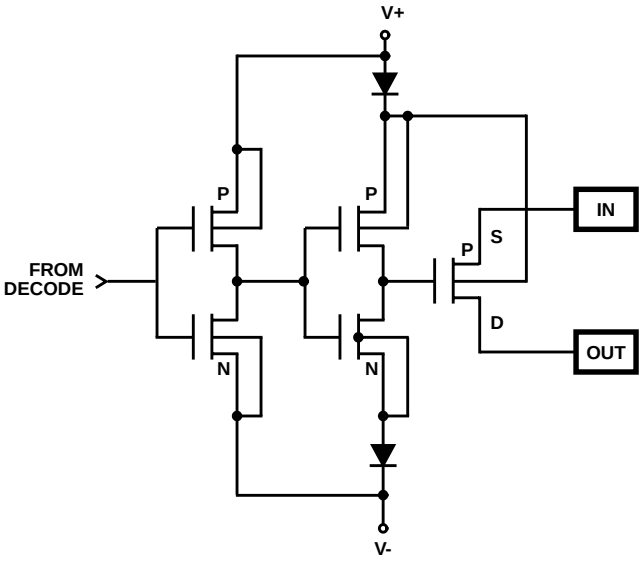
ADDRESS INPUT BUFFER AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEX SWITCH



Harris - Space Level Product Flow

SEM - Traceable to Diffusion Method 2018, Modified

This device does not meet MIL-STD-883 Method 2018.3 Class S minimum metal step coverage of 50%. The metal does meet the intent of the Class S requirement by meeting the current density requirement of <2E5 A/cm^2. Calculation based on continuous current of 10mA. Data can be provided upon request.

Wafer Lot Acceptance Method 5007

Internal Visual Inspection (Note 1)

Gamma Radiation Assurance Tests Method 1019

100% Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Notes 1, 2)

Temperature Cycling Method 1010 Condition C

Constant Acceleration Method 2001 Y1 30KG

Particle Impact Noise Detection Method 2020, Condition A 20G

Marking and Serialization

X-Ray Inspection Method 2012

Initial Electrical Tests (T0)

Static Burn-In 72 Hour, +125^{o}C (Min) Method 1015 Condition A

Room Temperature Electrical Tests (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Dynamic Burn-In 240 Hours at +125^{o}C or equivalent Method 1015 Condition A

Electrical Tests Subgroups 1, 7, 9 (T2)

Burn-In Delta Calculation (T0 - T2)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Electrical Test +125^{o}C, -55^{o}C

Alternate Group A Inspection Method 5005

Fine and Gross Leak Tests Method 1014

Customer Source Inspection (Note 2)

Group B Inspection (Notes 2, 4) Method 5005

Group D Inspection (Notes 2, 4) Method 5005

External Visual Inspection Method 2009

Data Package Generation (Note 3)

NOTES:

1. Visual Inspection is performed to MIL-STD-883 Method 2010, Condition A.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A) -55^{o}C, +25^{o}C, +125^{o}C
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data, (Table 5 Parameters only)
   +25^{o}C Initial Test
   +25^{o}C Interim Test 1
   +25^{o}C Interim Test 2
   +25^{o}C Delta Over Burn-In
4. Group B data package contains Attributes Data and Variables Data, (Table 5 Parameters only). Group D data package contains Attributes only.

Harris -8 Product Flow

Internal Visual Inspection, Alternate Condition B (Note 1)

Gamma Radiation Assurance Tests Method 1019

Customer Pre-Cap Visual Inspection (Notes 1, 2)

Temperature Cycling Method 1010 Condition C (50 Cycles)

Constant Acceleration Method 2001 Y1 30kG

Fine and Gross Leak Tests Method 1014

Marking

Initial Electrical Tests (T0)

Dynamic Burn-In 160 Hours, +125^{o}C Method 1015 or Equivalent Condition D

Electrical Tests Subgroups 1, 7, 9 (T1) Method 5004

PDA Calculation 5% Subgroups 1, 7 Method 5004

Electrical Test +125^{o}C, -55^{o}C Method 5004

Alternate Group A Inspection Method 5005

Customer Source Inspection (Note 2)

Group B Inspection (Notes 2, 4) Method 5005 (Optional)

Group C Inspection (Notes 2, 4) Method 5005 (Optional)

Group D Inspection (Notes 2, 4) Method 5005 (Optional)

External Visual Inspection Method 2009

Data Package Generation (Note 3)

NOTES:

1. Visual inspection is performed to MIL-STD-883 Method 2010, Alternate Condition B.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data Package Contents:
   Test Attributes (including Group A) -55^{o}C, +25^{o}C, +125^{o}C
   Radiation Testing Certificate of Conformance
4. Group B, C and D data package contains Attributes Data only.

Metallization Topology

DIE DIMENSIONS:
110 x 159 x 11mils

METALLIZATION:
Type: Al
Thickness: 12.5kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Eutectic
Temperature: Sidebrazed CerDIP - 460°C (Max)
Flatpack - 460°C (Max)

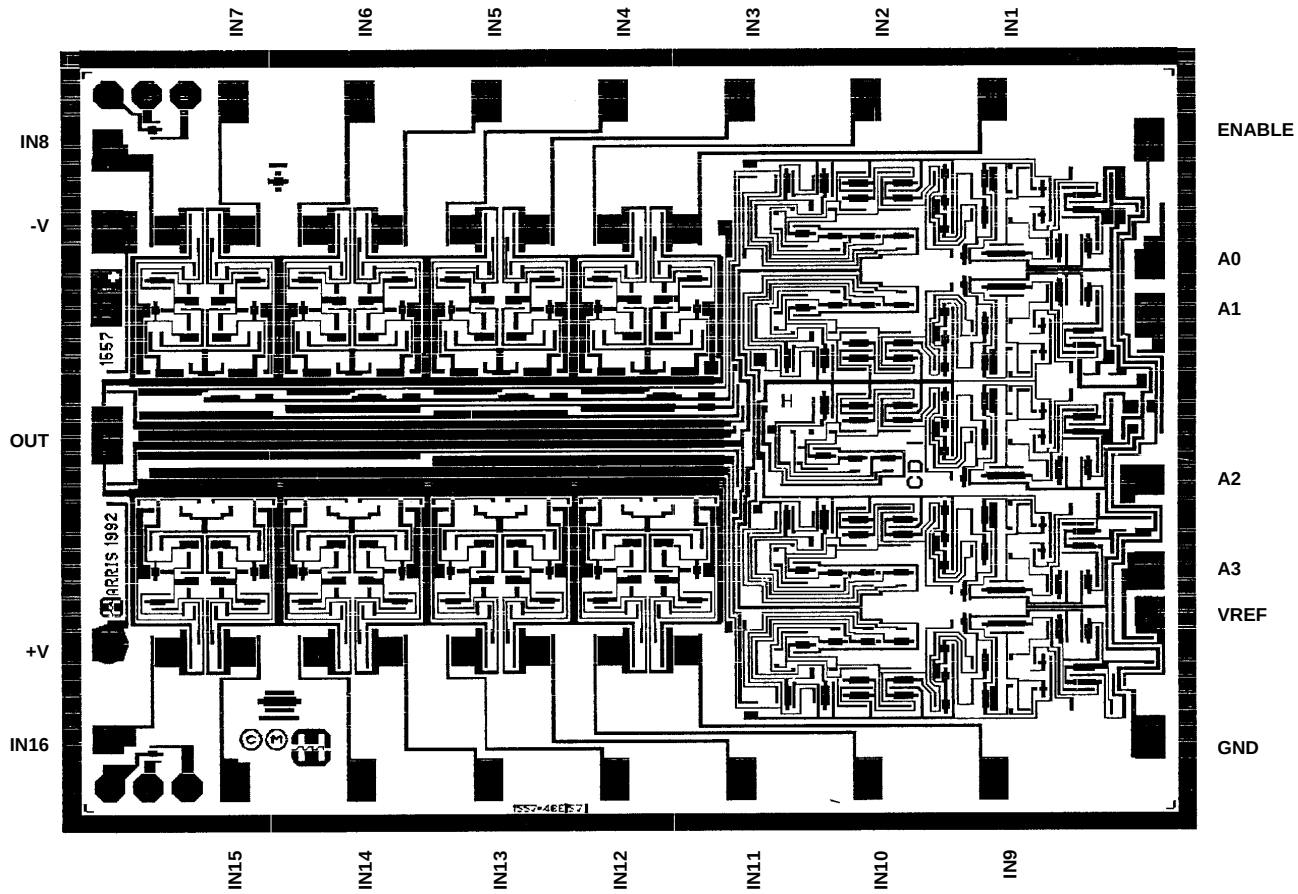
WORST CASE CURRENT DENSITY: Modified SEM

LEAD TEMPERATURE (10s Soldering): <275°C

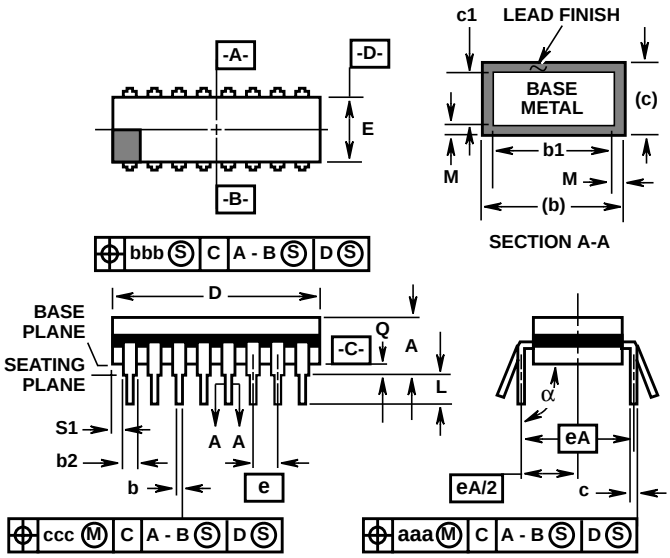
PROCESS: CMOS-DI

Metallization Mask Layout

HS-1840RH



Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



NOTES:

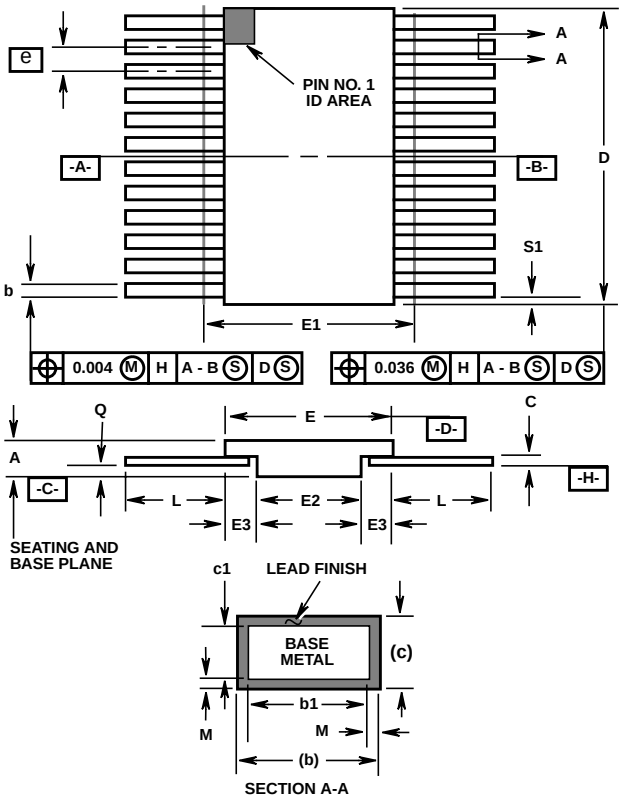
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	28		28		8

Rev. 0 4/94

Ceramic Metal Seal Flatpack Packages (Flatpack)



K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B)
28 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.740	-	18.80	3
E	0.460	0.520	11.68	13.21	-
E1	-	0.550	-	13.97	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	28		28		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.