Features

- Master and Slave Operation Possible
- Supply Voltage up to 40V
- Operating voltage V_S = 5V to 27V
- Typically 10 µA Supply Current During Sleep Mode
- Typically 40 µA Supply Current in Silent Mode
- Linear Low-drop Voltage Regulator:
  - Normal, Fail-safe, and Silent Mode
    - ATA6628 V_{CC} = 3.3V ±2%
    - ATA6630 V_{CC} = 5.0V ±2%
  - In Sleep Mode V_{CC} is Switched Off
- VCC- Undervoltage Detection (4 ms Reset Time) and Watchdog Reset Logical Combined at Open Drain Output NRES
- High-speed Mode Up to 115 kBaud
- Internal 1:6 Voltage Divider for $V_{Battery}$ Sensing
- Negative Trigger Input for Watchdog
- Boosting the Voltage Regulator Possible with an External NPN Transistor
- LIN Physical Layer According to LIN 2.0, 2.1 and SAEJ2602-2
- Wake-up Capability via LIN-bus, Wake Pin, or KI_15 Pin
- INH Output to Control an External Voltage Regulator or to Switch off the Master Pull Up Resistor
- Bus Pin is Overtemperature and Short-circuit Protected versus GND and Battery
- Adjustable Watchdog Time via External Resistor
- Advanced EMC and ESD Performance
- Fulfills the OEM “Hardware Requirements for LIN in Automotive Applications Rev.1.1”
- Interference and Damage Protection According ISO7637
- Package: QFN 5 mm × 5 mm with 20 Pins

LIN Bus Transceiver with 3.3V (5V) Regulator and Watchdog

ATA6628
ATA6630

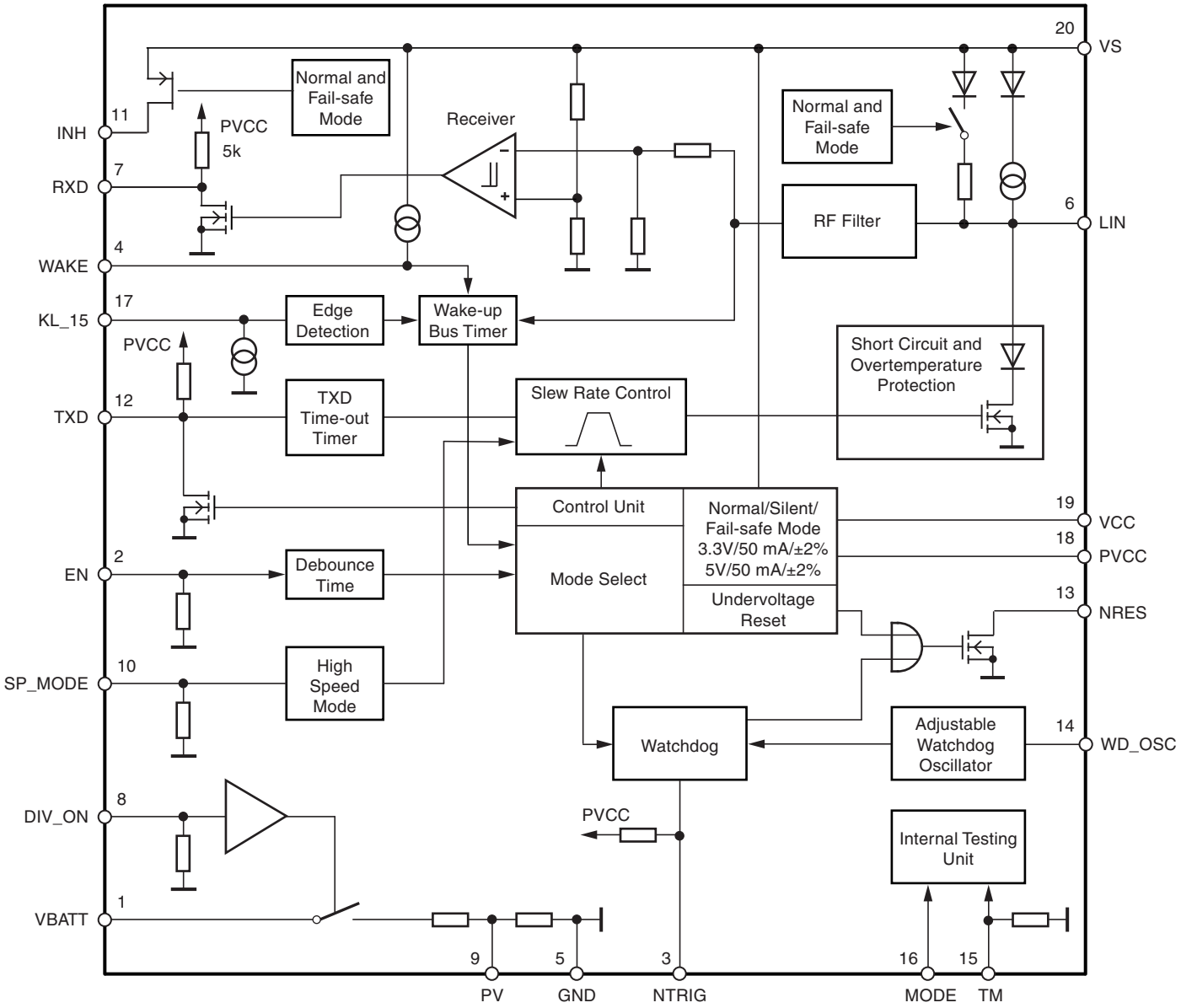
Preliminary

1. Description

The ATA6628 is a fully integrated LIN transceiver, which complies with the LIN 2.0, 2.1 and SAEJ2602-2 specifications. It has a low-drop voltage regulator for 3.3V/50 mA output and a window watchdog. The ATA6630 has the same functionality as the ATA6628; however, it uses a 5V/50 mA regulator. The voltage regulator is able to source 50 mA, but the output current can be boosted by using an external NPN transistor. This chip combination makes it possible to develop inexpensive, simple, yet powerful slave and master nodes for LIN-bus systems. ATA6628/ATA6630 are designed to handle the low-speed data communication in vehicles, e.g., in convenience electronics. Improved slope control at the LIN-driver ensures secure data communication up to 20 kBaud. Sleep Mode and Silent Mode guarantee very low current consumption.

9117E–AUTO–07/10

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN20

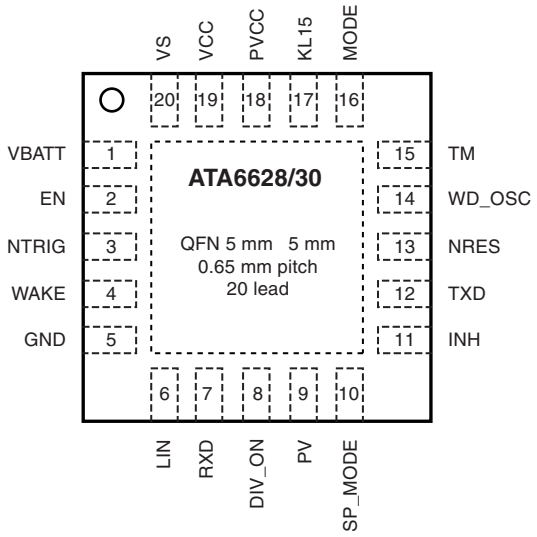


Table 2-1. Pin Description

Pin	Symbol	Function
1	VBATT	Battery supply for the voltage divider
2	EN	Enables the device into Normal Mode
3	NTRIG	Low-level watchdog trigger input from microcontroller; if not needed, connect to PVCC
4	WAKE	High-voltage input for local wake-up request; if not needed, connect to VS
5	GND	System ground
6	LIN	LIN-bus line input/output
7	RXD	Receive data output
8	DIV_ON	Input to switch on the internal voltage divider, active high
9	PV	Voltage divider output
10	SP_MODE	Input to switch the transceiver in High-speed Mode, active high
11	INH	Battery related High-side switch
12	TXD	Transmit data input; active low output (strong pull down) after a local wake up request
13	NRES	Output undervoltage and watchdog reset (open drain)
14	WD_OSC	External resistor for adjustable watchdog timing; if not needed, connect to GND
15	TM	For factory testing only (tie to ground)
16	MODE	Low watchdog is on; high watchdog is off
17	KL_15	Ignition detection (edge sensitive)
18	PVCC	3.3V/5V regulator sense input pin, connect to VCC
19	VCC	3.3V/5V regulator output/driver pin, connect to PVCC
20	VS	Battery supply
Backside		Heat slug is connected to GND

3. Functional Description

3.1 Physical Layer Compatibility

Since the LIN physical layer is independent from higher LIN layers (e.g., the LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes, which, according to older versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3), are without any restrictions.

3.2 Supply Pin (VS)

The LIN operating voltage is V_S = 5V to 27V. An undervoltage detection is implemented to disable data transmission if V_S falls below VS_{th} in order to avoid false bus messages. After switching on VS, the IC starts in Fail-safe Mode, and the voltage regulator is switched on (i.e., 3.3V/5V/50 mA output capability).

The supply current is typically 10 µA in Sleep Mode and 40 µA in Silent Mode.

3.3 Ground Pin (GND)

The ATA6628/ATA6630 does not affect the LIN Bus in the event of GND disconnection. It is able to handle a ground shift up to 11.5% of VS. The mandatory system ground is pin 5.

3.4 Voltage Regulator Output Pin (VCC)

The internal 3.3V/5V voltage regulator is capable of driving loads up to 50 mA. It is able to supply the microcontroller and other ICs on the PCB and is protected against overloads by means of current limitation and overtemperature shut-down. Furthermore, the output voltage is monitored and will cause a reset signal at the NRES output pin if it drops below a defined threshold V_{thun}. To boost up the maximum load current, an external NPN transistor may be used, with its base connected to the VCC pin and its emitter connected to PVCC.

3.5 Voltage Regulator Sense Pin (PVCC)

The PVCC is the sense input pin of the 3.3V/5V voltage regulator. For normal applications (i.e., when only using the internal output transistor), this pin must be connected to the VCC pin. If an external boosting transistor is used, the PVCC pin must be connected to the output of this transistor, i.e., its emitter terminal.

3.6 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown and an internal pull-up resistor compliant with the LIN 2.x specification are implemented. The allowed voltage range is between –27V and +40V. Reverse currents from the LIN bus to VS are suppressed, even in the event of GND shifts or battery disconnection. LIN receiver thresholds are compatible with the LIN protocol specification. The fall time from recessive to dominant bus state and the rise time from dominant to recessive bus state are slope controlled.

3.7 Input/Output Pin (TXD)

In Normal Mode the TXD pin is the microcontroller interface used to control the state of the LIN output. TXD must be pulled to ground in order to have a low LIN-bus. If TXD is high or not connected (internal pull-up resistor), the LIN output transistor is turned off, and the bus is in recessive state. During Fail-safe Mode, this pin is used as output and is signalling the fail-safe source. It is current-limited to < 8 mA.

3.8 TXD Dominant Time-out Function

The TXD input has an internal pull-up resistor. An internal timer prevents the bus line from being driven permanently in dominant state. If TXD is forced to low for longer than t_{DOM} > 27 ms, the LIN-bus driver is switched to recessive state. Nevertheless, when switching to Sleep Mode, the actual level at the TXD pin is relevant.

To reactivate the LIN bus driver, switch TXD to high (> 10 µs).

3.9 Output Pin (RXD)

This output pin reports the state of the LIN-bus to the microcontroller. LIN high (recessive state) is reported by a high level at RXD; LIN low (dominant state) is reported by a low level at RXD. The output has an internal pull-up resistor with typically 5 kΩ to PVCC. The AC characteristics can be defined with an external load capacitor of 20 pF.

The output is short-circuit protected. RXD is switched off in Unpowered Mode (i.e., V_S = 0V).

During Fail-safe Mode it is signalling the fail-safe source.

3.10 Enable Input Pin (EN)

The Enable Input pin controls the operation mode of the device. If EN is high, the circuit is in Normal Mode, with transmission paths from TXD to LIN and from LIN to RXD both active. The VCC voltage regulator operates with 3.3V/5V/50 mA output capability.

If EN is switched to low while TXD is still high, the device is forced to Silent Mode. No data transmission is then possible, and the current consumption is reduced to I_{VS} typ. 40 µA. The VCC regulator has its full functionality.

If EN is switched to low while TXD is low, the device is forced to Sleep Mode. No data transmission is possible, and the voltage regulator is switched off.

3.11 Wake Input Pin (WAKE)

The WAKE Input pin is a high-voltage input used to wake up the device from Sleep Mode or Silent Mode. It is usually connected to an external switch in the application to generate a local wake-up. A pull-up current source, typically 10 µA, is implemented.

If a local wake-up is not needed in the application, connect the WAKE pin directly to the VS pin.

3.12 Mode Input Pin (MODE)

Connect the MODE pin directly or via an external resistor to GND for normal watchdog operation. To debug the software of the connected microcontroller, connect MODE pin to PVCC and the watchdog is switched off.

Note: If you do not use the watchdog, connect pin MODE directly to PVCC.

3.13 TM Input Pin

The TM pin is used for final production measurements at Atmel®. In normal application, it has to be always connected to GND.

3.14 KL_15 Pin

The KL_15 pin is a high-voltage input used to wake up the device from Sleep or Silent Mode. It is an edge-sensitive pin (low-to-high transition). It is usually connected to ignition to generate a local wake-up in the application when the ignition is switched on. Although KL_15 pin is at high voltage (V_{Batt}), it is possible to switch the IC into Sleep or Silent Mode. Connect the KL_15 pin directly to GND if you do not need it. A debounce timer with a typical Tdb_{Kl_15} of 160 µs is implemented.

The input voltage threshold can be adjusted by varying the external resistor due to the input current I_{KL_15}. To protect this pin against voltage transients, a serial resistor of 47 kΩ and a ceramic capacitor of 100 nF are recommended. With this RC combination you can increase the wake-up time Tw_{KL_15} and, therefore, the sensitivity against transients on the ignition KL_15.

You can also increase the wake-up time using external capacitors with higher values.

3.15 INH Output Pin

The INH Output pin is used to switch an external voltage regulator on during Normal and Fail-safe Mode. The INH Output is a high-side switch, which is switched-off in Sleep and Silent Mode. It is possible to switch off the external 1 kΩ master resistor via the INH pin for master node applications.

3.16 Reset Output Pin (NRES)

The Reset Output pin, an open drain output, switches to low during VCC undervoltage or a watchdog failure.

3.17 WD_OSC Output Pin

The WD_OSC Output pin provides a typical voltage of 1.2V, which supplies an external resistor with values between 34 kΩ and 120 kΩ to adjust the watchdog oscillator time.

If the watchdog is disabled, this voltage is switched off and you can either tie to GND or leave this pin open.

3.18 NTRIG Input Pin

The NTRIG Input pin is the trigger input for the window watchdog. A pull-up resistor is implemented. A negative edge triggers the watchdog. The trigger signal (low) must exceed a minimum time $t_{trigmin}$ to generate a watchdog trigger.

3.19 Wake-up Events from Sleep or Silent Mode

- LIN-bus
- WAKE pin
- EN pin
- KL_15

3.20 DIV_ON Input Pin

The DIV_ON pin is a low voltage input. It is used to switch on or off the internal voltage divider PV output directly with no time limitation (see Table 3-1 on page 7). It is switched on if DIV_ON is high or it is switched off if DIV_ON is low. In Sleep Mode the DIV_ON functionality is disabled and PV is off. An internal pull-down resistor is implemented.

3.21 VBATT Input Pin

The VBATT is a high voltage input pin to supply the internal voltage divider. In an application with battery voltage monitoring, this pin is connected to $V_{Battery}$ via a 47Ω resistor in series and a 10 nF capacitor to GND (see Figure 9-2 on page 31). The the divider ratio is 1:6.

3.22 PV Output Pin

For applications with battery monitoring, this pin is directly connected to the ADC of a microcontroller. For buffering the ADC input an external capacitor might be needed. This pin guarantees a voltage and temperature stable output of a $V_{Battery}$ ratio. The PV output pin is controlled by the DIV_ON input pin.

Table 3-1. Table of Voltage Divider

Mode of Operation	Input DiV_ON	Voltage Divider Output PV
Fail-safe/Normal/ High-speed/Silent	0	Off
	1	On
Sleep	0	Off
	1	Off

3.23 SP_MODE Input Pin

The SP_MODE pin is a low-voltage input. High-speed Mode of the transceiver can be activated via a high level during Normal Mode. Return to LIN 2.x Transceiver Mode with slope control is possible if you switch the SP_MODE pin to low.

4. Modes of Operation

Figure 4-1. Modes of Operation

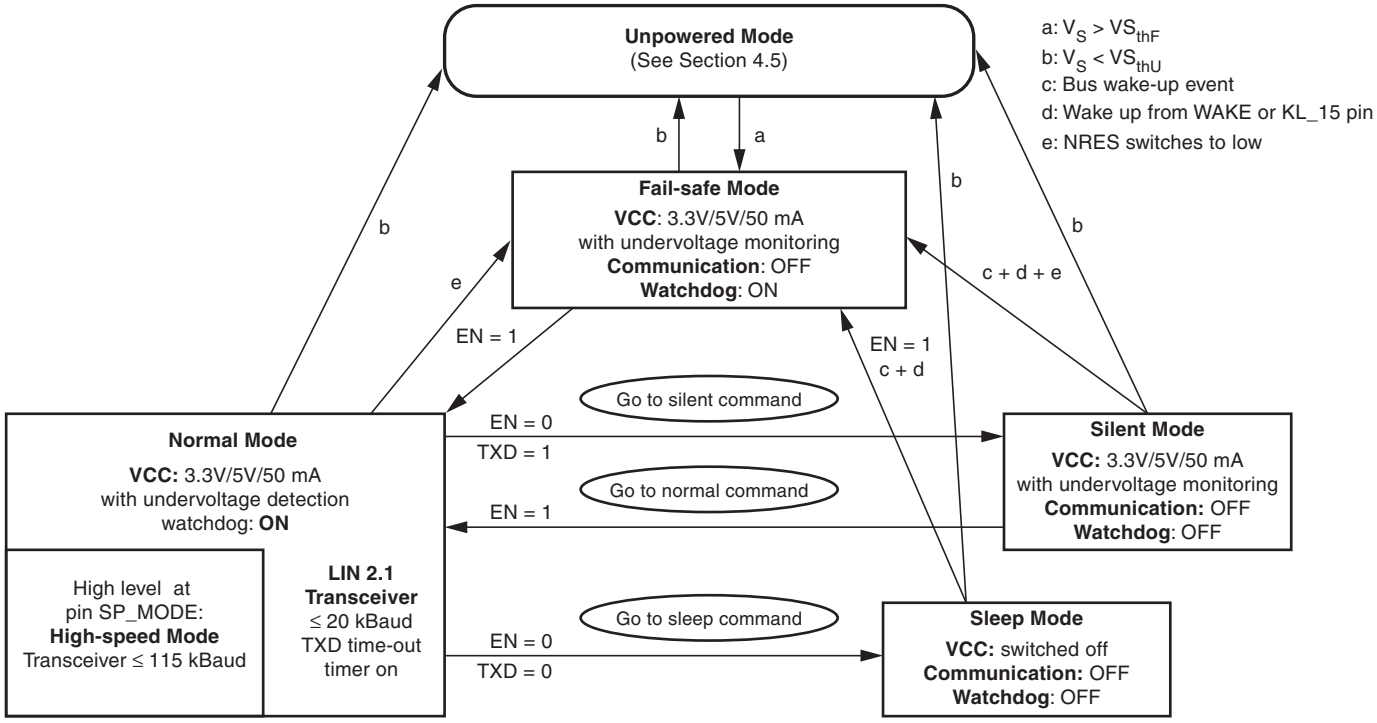


Table 4-1. Table of Modes

Mode of Operation	Transceiver	Pin LIN	V_{CC}	Pin Mode	Watchdog	Pin WD_OSC	Pin INH
Unpowered	Off	Recessive	On	GND	On	On	Off
Fail-safe	Off	Recessive	3.3V/5V	GND	On	1.23V	On
Normal/ High-speed	On	TXD depending	3.3V/5V	GND	On	1.23V	On
Silent	Off	Recessive	3.3V/5V	GND	Off	0V	Off
Sleep	Off	Recessive	0V	GND	Off	0V	Off

4.1 Normal Mode

This is the normal transmitting and receiving mode. The voltage regulator is active and can source up to 50 mA. The undervoltage detection is activated. The watchdog needs a trigger signal from NTRIG to avoid resets at NRES. If NRES is switched to low, the IC changes its state to Fail-safe Mode.

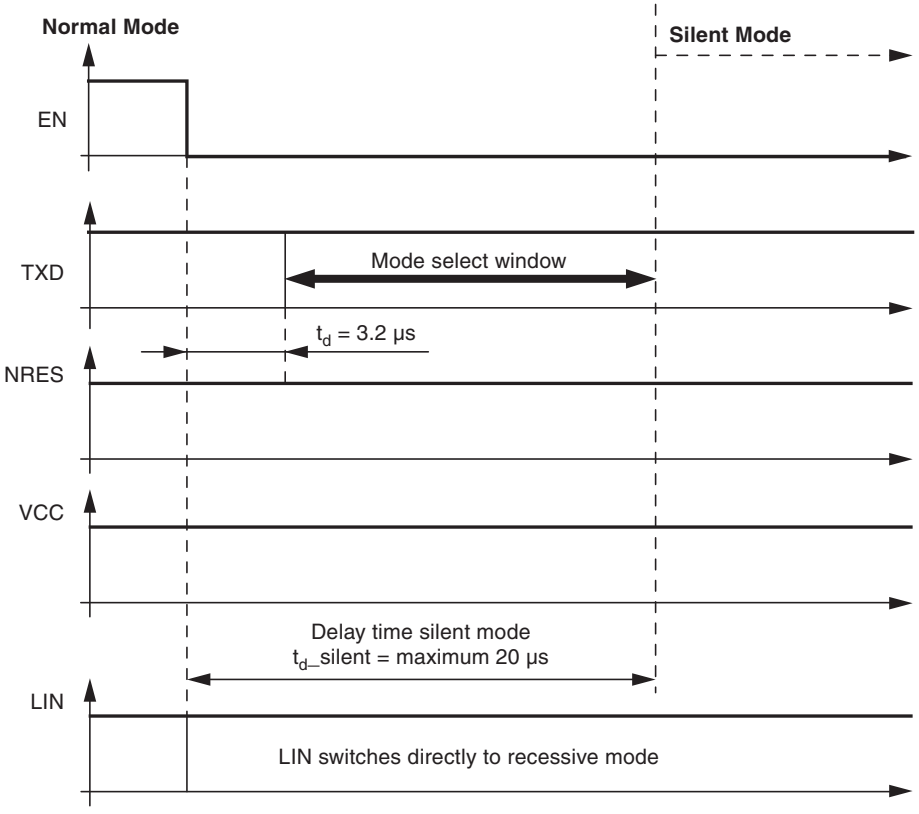
4.2 Silent Mode

A falling edge at EN when TXD is high switches the IC into Silent Mode. The TXD Signal has to be logic high during the Mode Select window (see Figure 4-2 on page 9). The transmission path is disabled in Silent Mode. The INH output is switched off and the voltage divider is enabled. The overall supply current from V_{Batt} is a combination of the $I_{VSsi} = 40\ \mu A$ plus the VCC regulator output current I_{VCC}.

The 3.3V/5V regulator with 2% tolerance can source up to 50 mA. The internal slave termination between the LIN pin and the VS pin is disabled in Silent Mode to minimize the current consumption in the event that the LIN pin is short-circuited to GND. Only a weak pull-up current (typically 10 µA) between the LIN pin and the VS pin is present. Silent Mode can be activated independently from the actual level on the LIN, WAKE, or KL_15 pins. If an undervoltage condition occurs, NRES is switched to low, and the IC changes its state to Fail-safe Mode.

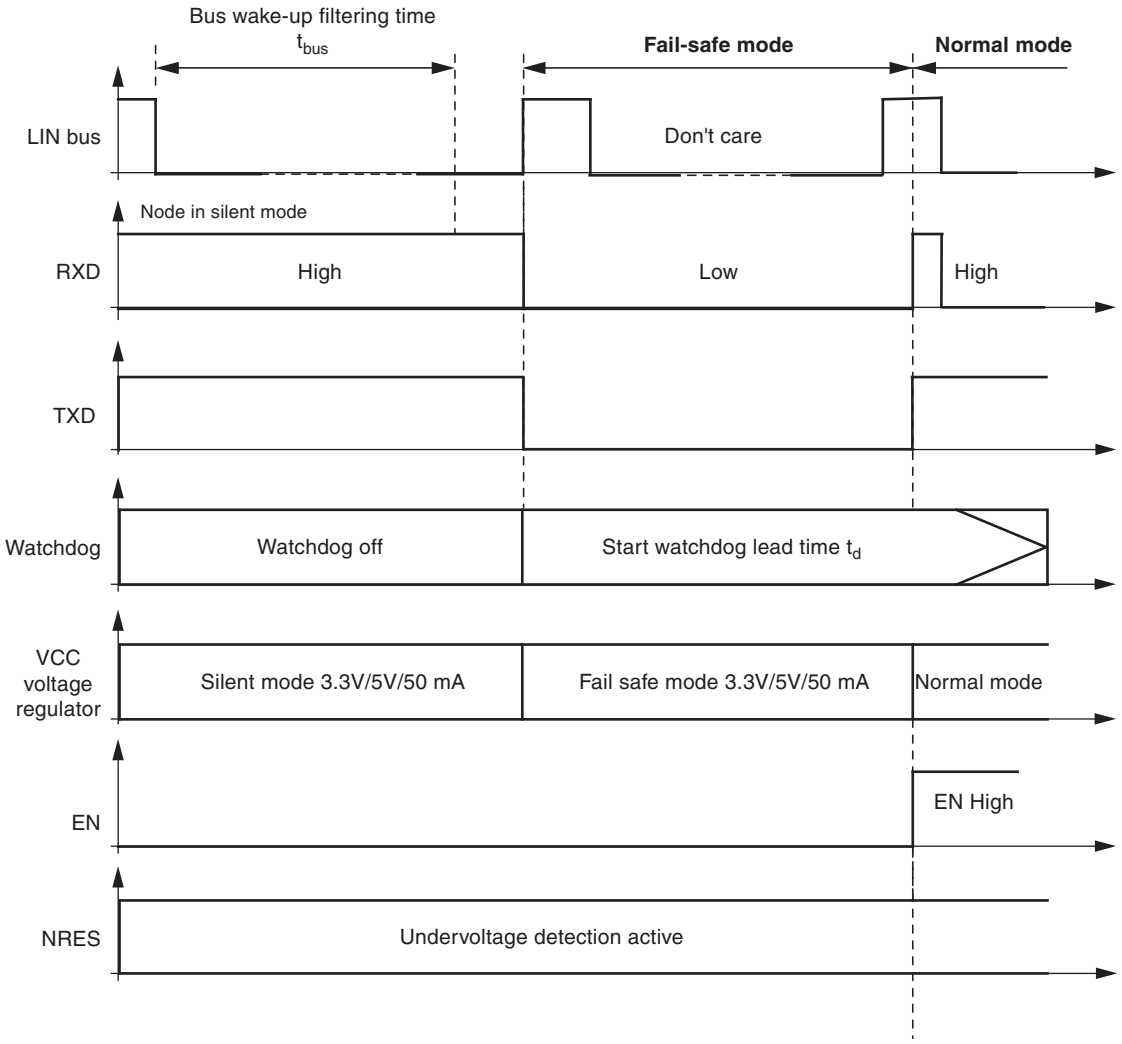
A voltage less than the LIN Pre_Wake detection VLINL at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer.

Figure 4-2. Switch to Silent Mode



A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (t_{bus}) and the following rising edge at the LIN pin (see Figure 4-3 on page 10) result in a remote wake-up request which is only possible if TXD is high. The device switches from Silent Mode to Fail-safe Mode. The internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at the RXD pin to interrupt the microcontroller (see Figure 4-3 on page 10). EN high can be used to switch directly to Normal Mode.

Figure 4-3. LIN Wake-up from Silent Mode



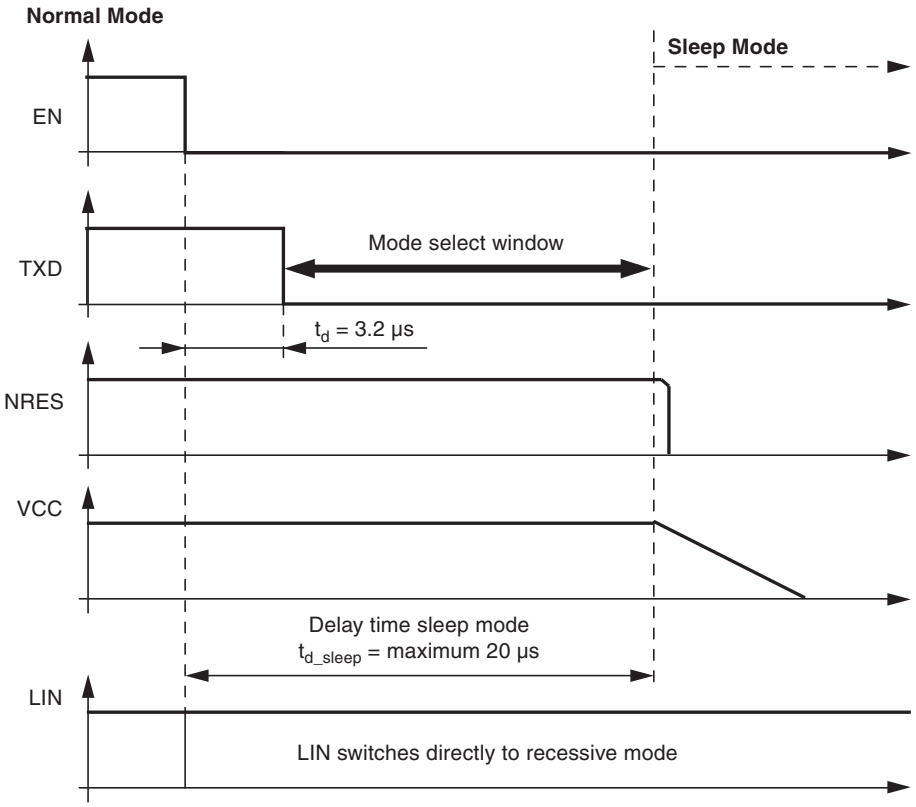
4.3 Sleep Mode

A falling edge at EN when TXD is low switches the IC into Sleep Mode. The TXD Signal has to be logic low during the Mode Select window (Figure 4-4 on page 11). In order to avoid any influence to the LIN-pin during switching into sleep mode it is possible to switch the EN up to 3.2 µs earlier to Low than the TXD. Therefore, the best an easiest way are two falling edges at TXD and EN at the same time. The transmission path is disabled in Sleep Mode. The supply current $I_{VSsleep}$ from V_{Batt} is typically 10 µA.

The INH output, the PV output and the VCC regulator are switched off. NRES and RXD are low. The internal slave termination between the LIN pin and VS pin is disabled to minimize the current consumption in the event that the LIN pin is short-circuited to GND. Only a weak pull-up current (typically 10 µA) between the LIN pin and the VS pin is present. Sleep Mode can be activated independently from the current level on the LIN, WAKE, or KL_15 pin.

A voltage less than the LIN Pre_Wake detection VLINL at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer.

Figure 4-4. Switch to Sleep Mode

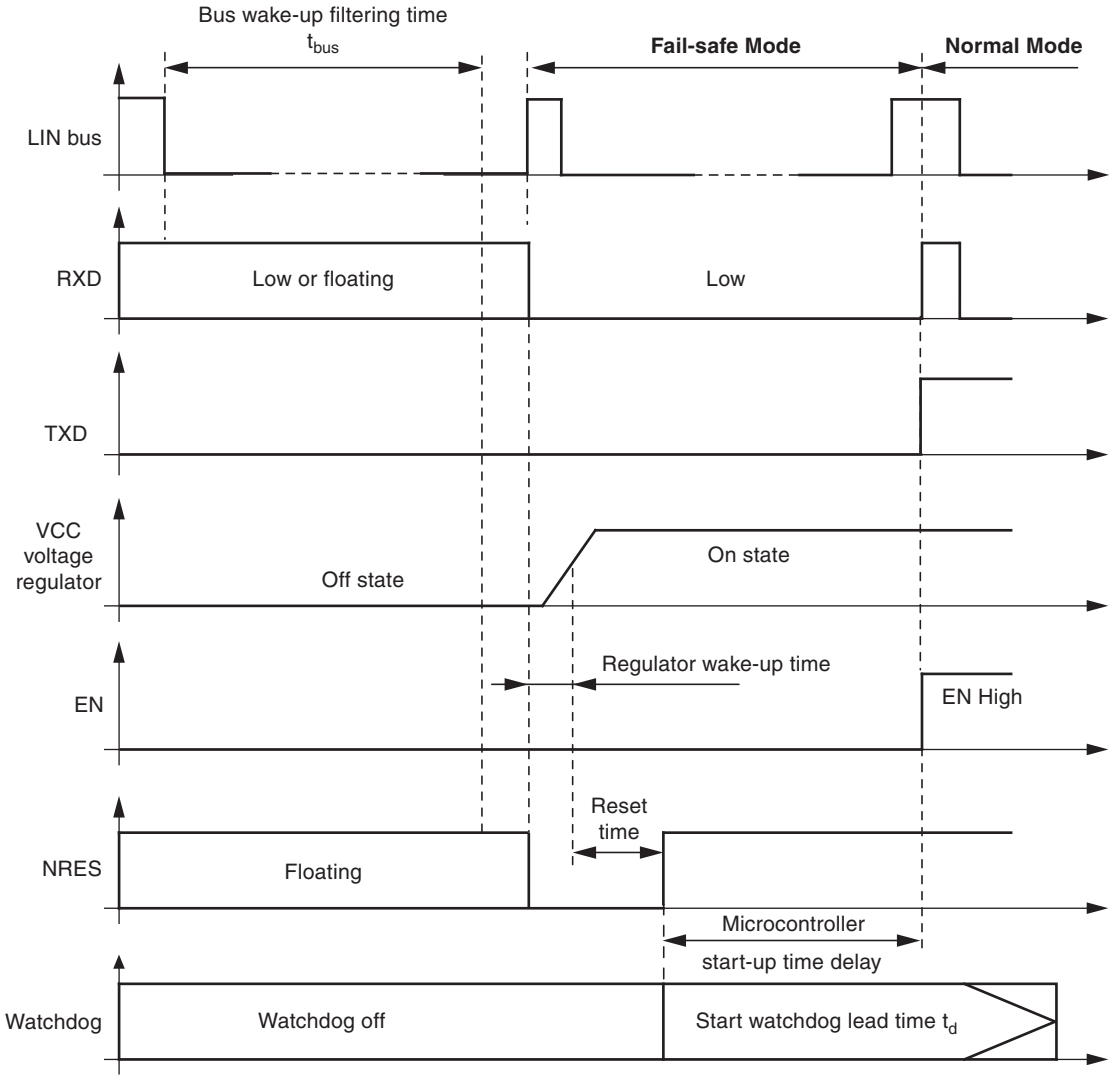


A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (t_{bus}) and a rising edge at pin LIN result in a remote wake-up request. The device switches from Sleep Mode to Fail-safe Mode.

The VCC regulator is activated, and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at the RXD pin to interrupt the microcontroller (see Figure 4-5 on page 12).

EN high can be used to switch directly from Sleep/Silent to Fail-safe Mode. If EN is still high after VCC ramp up and undervoltage reset time, the IC switches to the Normal Mode.

Figure 4-5. LIN Wake Up from Sleep Mode



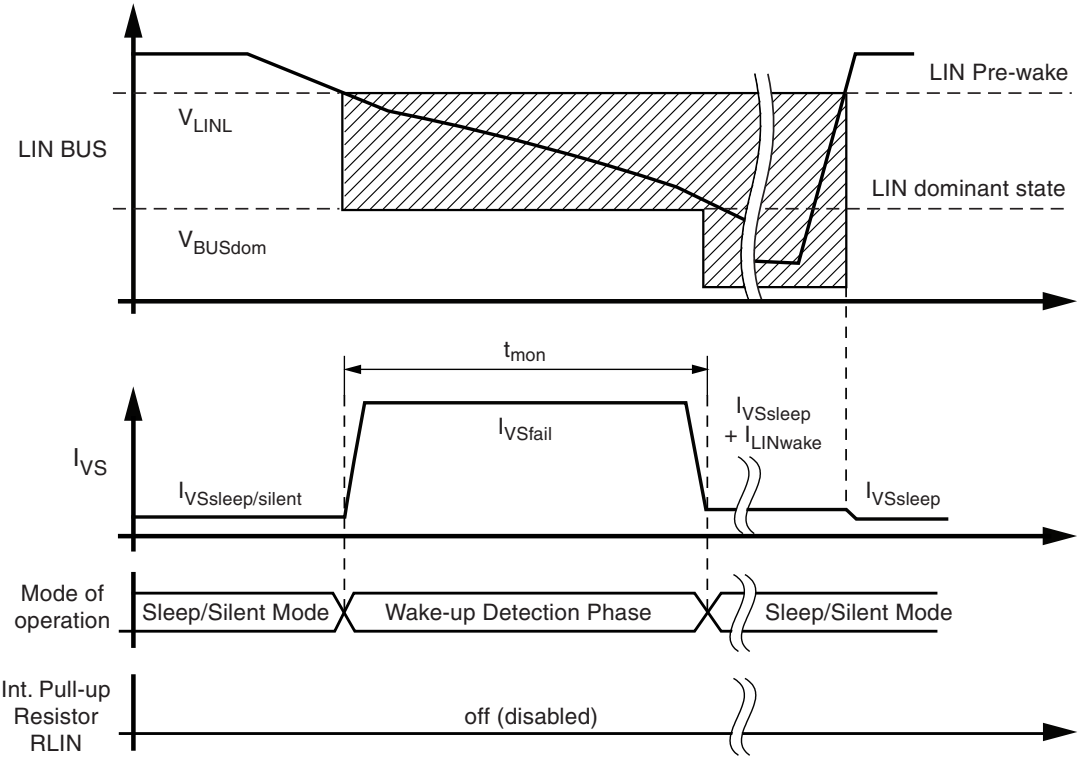
4.4 Sleep or Silent Mode: Behavior at a Floating LIN-bus or a Short Circuited LIN to GND

In Sleep or in Silent Mode the device has a very low current consumption even during short-circuits or floating conditions on the bus. A floating bus can arise if the Master pull-up resistor is missing, e.g., if it is switched off when the LIN- Master is in sleep mode or even if the power supply of the Master node is switched off.

In order to minimize the current consumption I_{VS} in sleep or silent mode during voltage levels at the LIN-pin below the LIN pre-wake threshold, the receiver is activated only for a specific time tmon. If t_{mon} elapses while the voltage at the bus is lower than Pre-wake detection low (V_{LINL}) and higher than the LIN dominant level, the receiver is switched off again and the circuit changes back to sleep respectively Silent Mode. The current consumption is then the result of $I_{VSsleep}$ or $I_{VSsilent}$ plus $I_{LINwake}$. If a dominant state is reached on the bus no wake-up will occur. Even if the voltage rises above the Pre-wake detection high (V_{LINH}), the IC will stay in sleep respectively silent mode (see Figure 4-6).

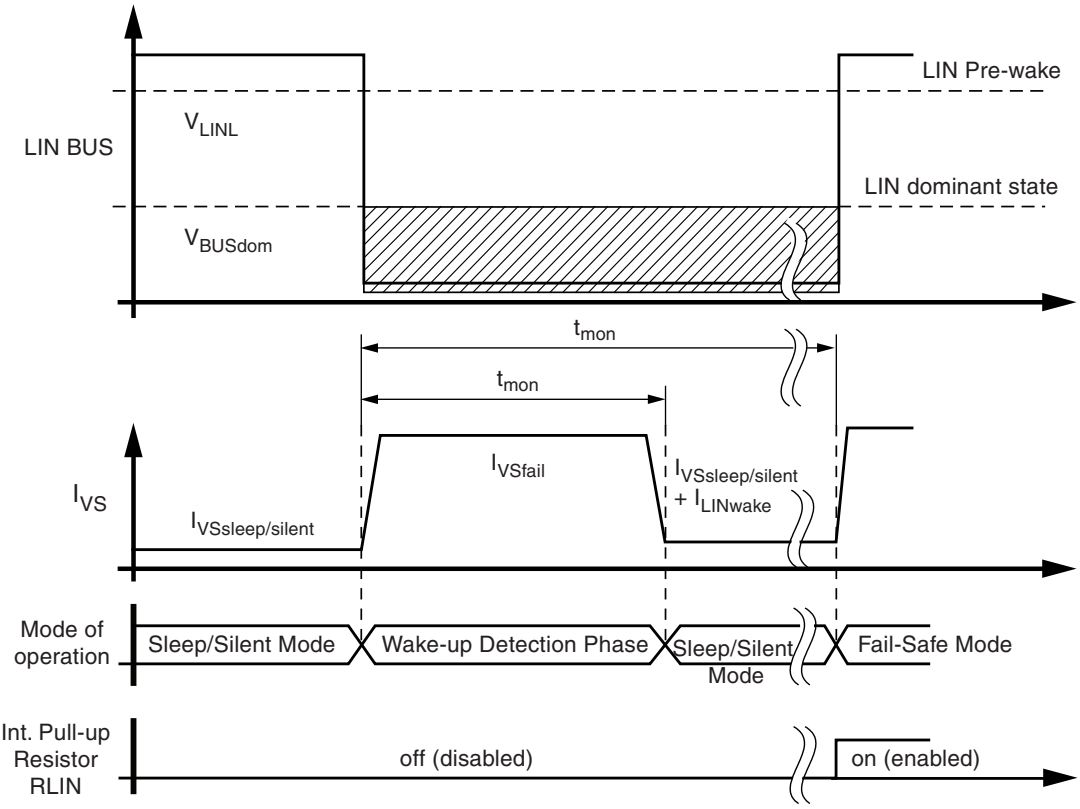
This means the LIN-bus must be above the Pre-wake detection threshold V_{LINH} for a few micro-seconds before a new LIN wake-up is possible.

Figure 4-6. Floating LIN-bus During Sleep or Silent Mode



If the ATA6628/ATA6630 is in Sleep or Silent Mode and the voltage level at the LIN-bus is in dominant state ($V_{LIN} < V_{BUSdom}$) for a time period exceeding t_{mon} (during a short circuit at LIN, for example), the IC switches back to Sleep Mode respectively Silent Mode. The V_S current consumption then consists of $I_{VSsleep}$ or $I_{VSsilent}$ plus $I_{LINWAKE}$. After a positive edge at pin LIN the IC switches directly to Fail-safe Mode (see Figure 4-7 on page 14).

Figure 4-7. Short Circuit to GND on the LIN bus During Sleep- or Silent Mode



4.5 Fail-safe Mode

The device automatically switches to Fail-safe Mode at system power-up. The voltage regulator is switched on (V_{CC} = 3.3V/5V/2%/50 mA) (see Figure 5-1 on page 19). The NRES output switches to low for t_{res} = 4 ms and gives a reset to the microcontroller. LIN communication is switched off. The IC stays in this mode until EN is switched to high. The IC then changes to Normal Mode. A power down of V_{Batt} ($V_S < VS_{thU}$) during Silent or Sleep Mode switches the IC into Fail-safe Mode after power up. A low at NRES switches into Fail-safe Mode directly. During Fail-safe Mode, the TXD pin is an output and signals the fail-safe source. The watchdog is switched on.

The LIN SBC can operate in different Modes, like Normal, Silent, or Sleep Mode. The functionality of these modes is described in Table 4-2.

Table 4-2. TXD, RXD Depending from Operation Modes

Different Modes	TXD	RXD
Fail-safe Mode	Signalling fail-safe sources (see Table 4-3 and Table 4-4)	
Normal Mode	Follows data transmission	
Silent Mode	High	High

A wake-up event from either Silent or Sleep Mode will be signalled to the microcontroller using the two pins RXD and TXD. The coding is shown in Table 4-3.

A wake-up event will lead the IC to the Fail-safe Mode.

Table 4-3. Signalling Fail-safe Sources

Fail-safe Sources	TXD	RXD
LIN wake-up (pin LIN)	Low	Low
Local wake-up (at pin Wake, pin KL15)	Low	High
VS_{th} (battery) undervoltage detection	High	Low

Table 4-4. Signalling in Fail-safe Mode after Reset (NRES was Low), Shows the Reset Source at TXD and RXD Pins

Fail-safe Sources	TXD	RXD
VCC undervoltage at NRES	High	Low
Watchdog reset at NRES	High	High

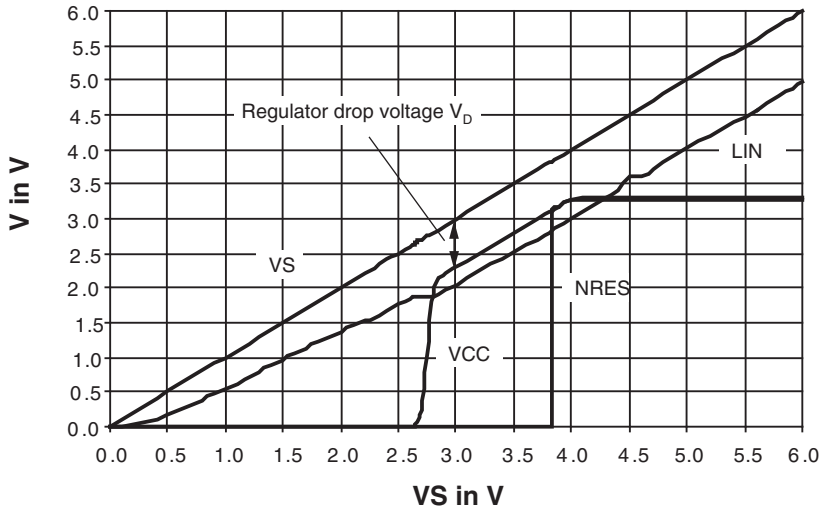
4.6 Unpowered Mode

If you connect battery voltage to the application circuit, the voltage at the VS pin increases according to the block capacitor (see Figure 5-1 on page 19). After VS is higher than the VS undervoltage threshold VS_{th}, the IC mode changes from Unpowered Mode to Fail-safe Mode. The VCC output voltage reaches its nominal value after t_{VCC}. This time, t_{VCC}, depends on the VCC capacitor and the load.

The NRES is low for the reset time delay t_{reset}. During this time, t_{reset}, no mode change is possible.

IF VS drops below VS_{th}, then the IC switches to Unpowered Mode. The behavior of VCC, NRES and LIN is shown in Figure 4-8. The watchdog needs to be triggered.

Figure 4-8. VCC versus VS for the VCC = 3.3V Regulator



4.7 High-speed Mode

If SP_MODE pin is high and the IC is in Normal Mode, the slew rate control is switched off. The slope time of the LIN falling edge is $t_{S\_Fall} < 2$ µs. The slope time of the LIN rising edge strongly depends on the LIN capacitive and resistive load. To achieve a high baud rate it is recommended to use a small resistor (500Ω) and a low capacitor. This allows very fast data transmission up to 115 kBaud, e.g., for electronic control (ECU) tests and microcontroller program or data download. In this mode superior EMC performance is not guaranteed.

5. Wake-up Scenarios from Silent or Sleep Mode

5.1 Remote Wake-up via Dominant Bus State

A voltage less than the LIN Pre_Wake detection V_{LINL} at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer.

A falling edge at the LIN pin followed by a dominant bus level V_{BUSdom} maintained for a certain time period (t_{BUS}) and a rising edge at pin LIN result in a remote wake-up request. A remote wake-up from Silent Mode is only possible if TXD is high. The device switches from Silent or Sleep Mode to Fail-safe Mode. The VCC voltage regulator is/remains activated, the INH pin is switched to high, and the internal slave termination resistor is switched on. The remote wake-up request is indicated by a low level at the RXD pin to generate an interrupt for the microcontroller and a strong pull down at TXD.

5.2 Local Wake-up via Pin WAKE

A falling edge at the WAKE pin followed by a low level maintained for a certain time period (t_{WAKE}) results in a local wake-up request. The device switches to Fail-safe Mode. The internal slave termination resistor is switched on. The local wake-up request is indicated by a low level at the TXD pin to generate an interrupt for the microcontroller. When the Wake pin is low, it is possible to switch to Silent or Sleep Mode via pin EN. In this case, the wake-up signal has to be switched to high > 10 µs before the negative edge at WAKE starts a new local wake-up request.

5.3 Local Wake-up via Pin KL_15

A positive edge at pin KL_15 followed by a high voltage level for a certain time period (> t_{KL_15}) results in a local wake-up request. The device switches into the Fail-safe Mode. The internal slave termination resistor is switched on. The extra long wake-up time ensures that no transients at KL_15 create a wake-up. The local wake-up request is indicated by a low level at the TXD pin to generate an interrupt for the microcontroller. During high-level voltage at pin KL_15, it is possible to switch to Silent or Sleep Mode via pin EN. In this case, the wake-up signal has to be switched to low > 250 µs before the positive edge at KL_15 starts a new local wake-up request. With external RC combination, the time is even longer.

5.4 Wake-up Source Recognition

The device can distinguish between different wake-up sources (see Table 4-4 on page 15).

The wake-up source can be read on the TXD and RXD pin in Fail-safe Mode. These flags are immediately reset if the microcontroller sets the EN pin to high (see Figure 4-3 on page 10 and Figure 4-5 on page 12) and the IC is in Normal mode.

5.5 Fail-safe Features

- During a short-circuit at LIN to $V_{Battery}$, the output limits the output current to I_{BUS_lim}. Due to the power dissipation, the chip temperature exceeds T_{LINoff}, and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. RXD stays on high because LIN is high. During LIN overtemperature switch-off, the VCC regulator works independently.
- During a short-circuit from LIN to GND the IC can be switched into Sleep or Silent Mode and even in this case the current consumption is lower than 45 µA in Sleep Mode and lower than 80 µA in Silent Mode. If the short-circuit disappears, the IC starts with a remote wake-up.
- Sleep or Silent Mode: During a floating condition on the bus the IC switches back to Sleep Mode/Silent Mode automatically and thereby the current consumption is lower than 45 µA/80 µA.
- The reverse current is < 2 µA at the LIN pin during loss of V_{Batt}. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.
- During a short circuit at VCC, the output limits the output current to I_{VCClim}. Because of undervoltage, NRES switches to low and sends a reset to the microcontroller if NRES is connected to the microcontroller. The IC switches into Fail-safe Mode. If the chip temperature exceeds the value T_{VCCoff}, the VCC output switches off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. Because of the Fail-safe Mode, the VCC voltage will switch on again although EN is switched off from the microcontroller. The microcontroller can start with its normal operation.
- EN pin provides a pull-down resistor to force the transceiver into recessive mode if EN is disconnected.
- RXD pin is set floating if V_{Batt} is disconnected.
- TXD pin provides a pull-up resistor to force the transceiver into recessive mode if TXD is disconnected.
- If TXD is short-circuited to GND, it is possible to switch to Sleep Mode via ENABLE
- If the WD_OSC pin has a short-circuit to GND and the NTRIG Signal has a period time > 27 ms a reset is guaranteed.
- If the resistor at the WD_OSC pin is disconnected and the NTRIG Signal has a period time < 46 ms a reset is guaranteed.
- If there is no NTRIG signal and a short-circuit at WD_OSC to GND the NRES switches to low after 90 ms. For an open circuit (no resistor) at WD_OSC it switches to low after 390 ms.

5.6 Voltage Regulator

The voltage regulator needs an external capacitor for compensation and for smoothing the disturbances from the microcontroller. It is recommended to use an electrolythic capacitor with C > 1.8 µF and a ceramic capacitor with C = 100 nF. The values of these capacitors can be varied by the customer, depending on the application.

The main power dissipation of the IC is created from the VCC output current I_{VCC}, which is needed for the application. In Figure 5-2 on page 19 the safe operating area of the ATA6628/ATA6630 is shown.

Figure 5-1. VCC Voltage Regulator: Ramp-up and Undervoltage Detection

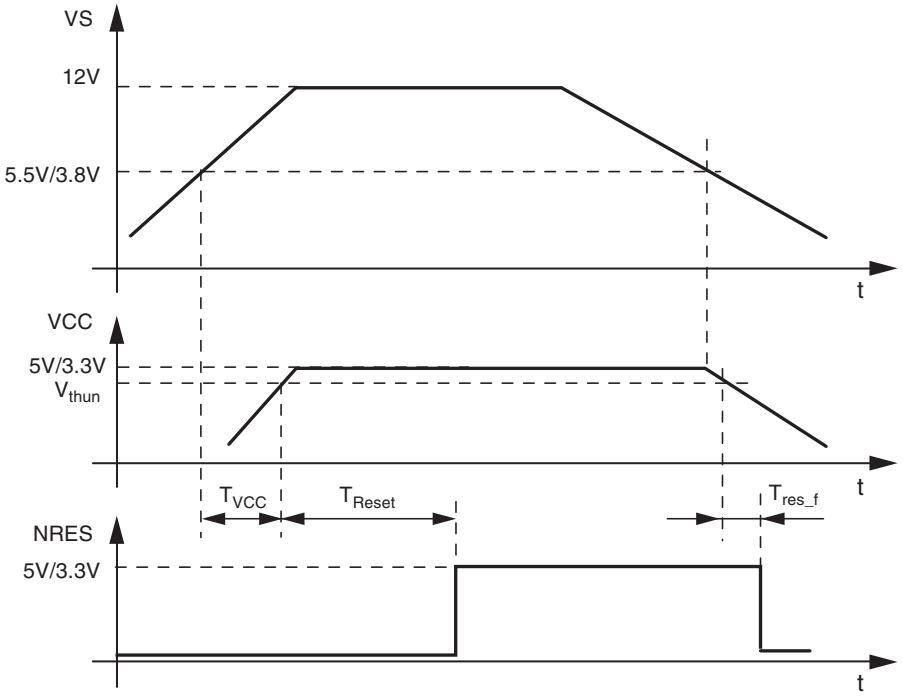
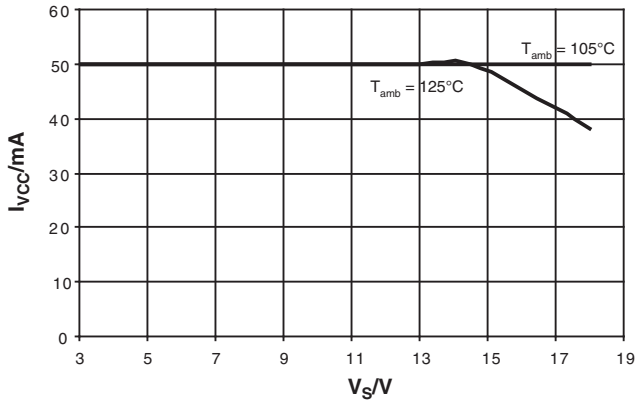


Figure 5-2. Power Dissipation: Safe Operating Area versus VCC Output Current and Supply Voltage V_S at Different Ambient Temperatures Due to R_{thja} = 35 K/W



For microcontroller programming, it may be necessary to supply the VCC output via an external power supply while the V_S Pin of the system basis chip is disconnected. This behavior is no problem for the system basis chip.

6. Watchdog

The watchdog anticipates a trigger signal from the microcontroller at the NTRIG (negative edge) input within a time window of T_{wd}. The trigger signal must exceed a minimum time $t_{trigmin}$ > 200 ns. If a triggering signal is not received, a reset signal will be generated at output NRES. The timing basis of the watchdog is provided by the internal oscillator. Its time period, T_{osc}, is adjustable via the external resistor R_{wd_osc} (34 kΩ to 120 kΩ).

During Silent or Sleep Mode the watchdog is switched off to reduce current consumption.

The minimum time for the first watchdog pulse is required after the undervoltage reset at NRES disappears. It is defined as lead time t_d. After wake up from Sleep or Silent Mode, the lead time t_d starts with the negative edge of the RXD output.

6.1 Typical Timing Sequence with R_{WD_OSC} = 51 kΩ

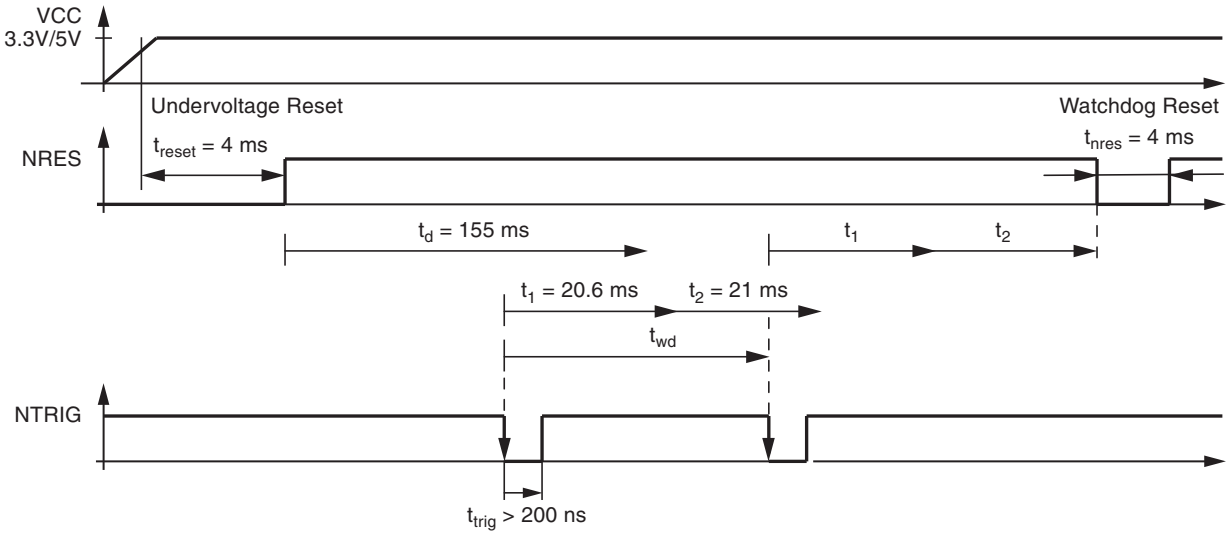
The trigger signal T_{wd} is adjustable between 20 ms and 64 ms using the external resistor R_{WD_OSC}.

For example, with an external resistor of R_{WD_OSC} = 51 kΩ ±1%, the typical parameters of the watchdog are as follows:

$t_{osc} = 0.405 \times R_{WD\_OSC} - 0.0004 \times (R_{WD\_OSC})^2$ (R_{WD_OSC} in kΩ; t_{osc} in µs)
t_{OSC} = 19.6 µs due to 51 kΩ
$t_d = 7895 \times$ 19.6 µs = 155 ms
$t_1 = 1053 \times$ 19.6 µs = 20.6 ms
$t_2 = 1105 \times$ 19.6 µs = 21.6 ms
t_{nres} = constant = 4 ms

After ramping up the battery voltage, the 5V regulator is switched on. The reset output NRES stays low for the time t_{reset} (typically 4 ms), then it switches to high, and the watchdog waits for the trigger sequence from the microcontroller. The lead time, t_d, follows the reset and is t_d = 155 ms. In this time, the first watchdog pulse from the microcontroller is required. If the trigger pulse NTRIG occurs during this time, the time t_1 starts immediately. If no trigger signal occurs during the time t_d, a watchdog reset with t_{NRES} = 4 ms will reset the microcontroller after t_d = 155 ms. The times t_1 and t_2 have a fixed relationship. A triggering signal from the microcontroller is anticipated within the time frame of t_2 = 21.6 ms. To avoid false triggering from glitches, the trigger pulse must be longer than $t_{TRIG,min}$ > 200 ns. This slope serves to restart the watchdog sequence. If the triggering signal fails in this open window t_2, the NRES output will be drawn to ground. A triggering signal during the closed window t_1 immediately switches NRES to low.

Figure 6-1. Timing Sequence with R_{WD_OSC} = 51 kΩ



6.2 Worst Case Calculation with R_{WD_OSC} = 51 kΩ

The internal oscillator has a tolerance of 20%. This means that t_1 and t_2 can also vary by 20%. The worst case calculation for the watchdog period t_{wd} is calculated as follows.

The ideal watchdog time t_{wd} is between the maximum t_1 and the minimum t_1 plus the minimum t_2.

$t_{1,min} = 0.8 \times t_1 = 16.5$ ms, $t_{1,max} = 1.2 \times t_1 = 24.8$ ms
$t_{2,min} = 0.8 \times t_2 = 17.3$ ms, $t_{2,max} = 1.2 \times t_2 = 26$ ms

$t_{wdmax} = t_{1min} + t_{2min} = 16.5$ ms + 17.3 ms = 33.8 ms
$t_{wdmin} = t_{1max} = 24.8$ ms

t_{wd} = 29.3 ms ±4.5 ms (±15%)

A microcontroller with an oscillator tolerance of ±15% is sufficient to supply the trigger inputs correctly.

Table 6-1. Typical Watchdog Timings

R_{WD_OSC} kΩ	Oscillator Period t_{osc}/µs	Lead Time t_d/ms	Closed Window t_1/ms	Open Window t_2/ms	Trigger Period from Microcontroller t_{wd}/ms	Reset Time t_{nres}/ms
34	13.3	105	14.0	14.7	19.9	4
51	19.61	154.8	20.64	21.67	29.32	4
91	33.54	264.80	35.32	37.06	50.14	4
120	42.84	338.22	45.11	47.34	64.05	4

7. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage V_S	V_S	–0.3		+40	V
Pulse time ≤ 500 ms T_a = 25°C Output current I_{VCC} ≤ 50 mA	V_S			+40	V
Pulse time ≤ 2 min T_a = 25°C Output current I_{VCC} ≤ 50 mA	V_S			27	V
WAKE (with 2.7 kΩ serial resistor) KL_15 (with 47 kΩ/100 nF) VBATT (with 47Ω/10 nF) DC voltage Transient voltage due to ISO7637 (coupling 1 nF)		 –1 –150		 +40 +100	 V V
INH - DC voltage		–0.3		V_S + 0.3	V
LIN, VBATT - DC voltage		–27		+40	V
Logic pins (RxD, TxD, EN, NRES, NTRIG, WD_OSC, MODE, TM, DIV_ON, SP_MODE, PV)		–0.3		VCC + 0.5V	V
Output current NRES	I_{NRES}			+2	mA
PVCC DC voltage VCC DC voltage		–0.3 –0.3		+5.5 +6.5	V V
ESD according to IBEE LIN EMC Test Spec. 1.0 following IEC 61000-4-2 - Pin VS, LIN to GND - Pin WAKE (2.7 kΩ, serial resistor) to GND - Pin VBATT (10 nF) to GND		±6			KV
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002) MIL-STD-883 (M3015.7)		±3			KV
CDM ESD STM 5.3.1		±750			V
MM ESD EIA/JESD22-A115 ESD STM5.2 AEC-Q100 (002)		±200			V
ESD HBM following STM5.1 with 1.5 kΩ 100 pF - Pin VS, LIN, WAKE to GND		±6			KV
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_s	–55		+150	°C

8. Thermal Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction to heat slug	R_{thjc}			10	K/W
Thermal resistance junction to ambient, where heat slug is soldered to PCB according to Jedec	R_{thja}		35		K/W
Thermal shutdown of VCC regulator		150	165	170	°C
Thermal shutdown of LIN output		150	165	170	°C
Thermal shutdown hysteresis			10		°C

9. Electrical Characteristics

5V < V_S < 27V, –40°C < T_j < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**VS Pin**								
1.1	Nominal DC voltage range		VS	V_S	5		27	V	A
1.2	Supply current in Sleep Mode	Sleep Mode $V_{LIN} > V_S - 0.5V$ V_S < 14V	VS	$I_{VSsleep}$	3	10	14	µA	A
		Sleep Mode, V_{LIN} = 0V Bus shorted to GND V_S < 14V	VS	$I_{VSsleep\_short}$	6	17	30	µA	A
1.3	Supply current in Silent Mode	Bus recessive V_S < 14V (T_j = 25°C) Without load at VCC	VS	I_{VSsi}	20	35	45	µA	A
		Bus recessive V_S < 14V (T_j = 125°C) Without load at VCC	VS	I_{VSsi}	25	40	50	µA	A
		Silent Mode V_S < 14V Bus shorted to GND Without load at VCC	VS	I_{VSsi_short}	25	50	80	µA	A
1.4	Supply current in Normal Mode	Bus recessive V_S < 14V Without load at VCC	VS	I_{VSrec}	0.3		0.8	mA	A
1.5	Supply current in Normal Mode	Bus recessive V_S < 14V V_{CC} load current 50 mA	VS	I_{VSdom}	50		53	mA	A
1.6	Supply current in Fail-safe Mode	Bus recessive, RXD is low V_S < 14V Without load at VCC for ATA6628 for ATA6630	 VS VS	 I_{VSfail} I_{VSfail}		 1.0 1.5	 1.5 2.0	 mA mA	 A A
1.7	VS undervoltage threshold	Switch to Unpowered Mode	VS	V_{SthU}	4	4.2	4.4	V	A
		Switch to Fail-safe Mode	VS	V_{SthF}	4.3	4.5	4.9	V	A
1.8	VS undervoltage threshold hysteresis		VS	V_{Sth_hys}		0.3		V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2	**RXD Output Pin**								
2.1	Low-level output sink current	Normal Mode V_{LIN} = 0V V_{RXD} = 0.4V	RXD	I_{RXD}	1.3	2.5	8	mA	A
2.2	Low-level output voltage	I_{RXD} = 1 mA	RXD	V_{RXDL}			0.4	V	A
2.3	Internal resistor to PVCC		RXD	R_{RXD}	3	5	7	kΩ	A
3	**TXD Input/Output Pin**								
3.1	Low-level voltage input		TXD	V_{TXDL}	–0.3		+0.8	V	A
3.2	High-level voltage input		TXD	V_{TXDH}	2		V_{CC} + 0.3V	V	A
3.3	Pull-up resistor	V_{TXD} = 0V	TXD	R_{TXD}	125	250	400	kΩ	A
3.4	High-level leakage current	V_{TXD} = V_{CC}	TXD	I_{TXD}	–3		+3	µA	A
3.5	Low-level output sink current	Fail-safe Mode, wake up V_{LIN} = V_S V_{WAKE} = 0V V_{TXD} = 0.4V	TXD	$I_{TXDwake}$	2	2.5	8	mA	A
4	**EN Input Pin**								
4.1	Low-level voltage input		EN	V_{ENL}	–0.3		+0.8	V	A
4.2	High-level voltage input		EN	V_{ENH}	2		V_{CC} + 0.3V	V	A
4.3	Pull-down resistor	V_{EN} = V_{CC}	EN	R_{EN}	50	125	200	kΩ	A
4.4	Low-level input current	V_{EN} = 0V	EN	I_{EN}	–3		+3	µA	A
5	**NTRIG Watchdog Input Pin**								
5.1	Low-level voltage input		NTRIG	V_{NTRIGL}	–0.3		+0.8	V	A
5.2	High-level voltage input		NTRIG	V_{NTRIGH}	2		V_{CC} + 0.3V	V	A
5.3	Pull-up resistor	V_{NTRIG} = 0V	NTRIG	R_{NTRIG}	125	250	400	kΩ	A
5.4	High-level leakage current	V_{NTRIG} = V_{CC}	NTRIG	I_{NTRIG}	–3		+3	µA	A
6	**Mode Input Pin**								
6.1	Low-level voltage input		MODE	V_{MODEL}	–0.3		+0.8	V	A
6.2	High-level voltage input		MODE	V_{MODEH}	2		V_{CC} + 0.3V	V	A
6.3	High-level leakage current	V_{MODE} = V_{CC} or V_{MODE} = 0V	MODE	I_{MODE}	–3		+3	µA	A
7	**INH Output Pin**								
7.1	High-level voltage	I_{INH} = –15 mA	INH	V_{INHH}	V_S – 0.75		V_S	V	A
7.2	Switch-on resistance between VS and INH		INH	R_{INH}		30	50	Ω	A
7.3	Leakage current	Sleep Mode V_{INH} = 0V/27V, VS = 27V	INH	I_{INHL}	–3		+3	µA	A
8	**LIN Bus Driver**								
8.1	Driver recessive output voltage	Load1/Load2	LIN	V_{BUSrec}	0.9 × V_S		V_S	V	A
8.2	Driver dominant voltage	V_{VS} = 7V R_{load} = 500 Ω	LIN	$V_{\_LoSUP}$			1.2	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.3	Driver dominant voltage	V_{VS} = 18V R_{load} = 500 Ω	LIN	$V_{\_HiSUP}$			2	V	A
8.4	Driver dominant voltage	V_{VS} = 7.0V R_{load} = 1000 Ω	LIN	$V_{\_LoSUP\_1k}$	0.6			V	A
8.5	Driver dominant voltage	V_{VS} = 18V R_{load} = 1000 Ω	LIN	$V_{\_HiSUP\_1k}$	0.8			V	A
8.6	Pull-up resistor to VS	The serial diode is mandatory	LIN	R_{LIN}	20	30	47	kΩ	A
8.7	Voltage drop at the serial diodes	In pull-up path with R_{slave} $I_{SerDiode}$ = 10 mA	LIN	$V_{SerDiode}$	0.4		1.0	V	D
8.8	LIN current limitation V_{BUS} = V_{Batt_max}		LIN	I_{BUS_LIM}	70	120	200	mA	A
8.9	Input leakage current at the receiver including pull-up resistor as specified	Input leakage current Driver off V_{BUS} = 0V V_{Batt} = 12V	LIN	$I_{BUS\_PAS\_dom}$	–1	–0.35		mA	A
8.10	Leakage current LIN recessive	Driver off 8V < V_{Batt} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{Batt}$	LIN	$I_{BUS\_PAS\_rec}$		10	20	µA	A
8.11	Leakage current at GND loss, control unit disconnected from ground. Loss of local ground must not affect communication in the residual network.	GND_{Device} = V_S V_{Batt} = 12V 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_gnd}$	–10	+0.5	+10	µA	A
8.12	Leakage current at loss of battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	V_{Batt} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_bat}$		0.1	2	µA	A
8.13	Capacitance on pin LIN to GND		LIN	C_{LIN}			20	pF	D
9	**LIN Bus Receiver**								
9.1	Center of receiver threshold	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2	LIN	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	A
9.2	Receiver dominant state	V_{EN} = V_{CC}	LIN	V_{BUSdom}			0.4 × V_S	V	A
9.3	Receiver recessive state	V_{EN} = V_{CC}	LIN	V_{BUSrec}	0.6 × V_S			V	A
9.4	Receiver input hysteresis	V_{hys} = V_{th_rec} – V_{th_dom}	LIN	V_{BUShys}	0.028 × V_S	0.1 × V_S	0.175 × V_S	V	A
9.5	Pre_Wake detection LIN High-level input voltage		LIN	V_{LINH}	V_S – 2V		V_S + 0.3V	V	A
9.6	Pre_Wake detection LIN Low-level input voltage	Activates the LIN receiver	LIN	V_{LINL}	–27		V_S – 3.3V	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10	**Internal Timers**								
10.1	Dominant time for wake-up via LIN bus	V_{LIN} = 0V	LIN	t_{bus}	30	90	150	µs	A
10.2	Time delay for mode change from Fail-safe into Normal Mode via EN pin	$V_{EN} = V_{CC}$	EN	t_{norm}	5	15	20	µs	A
10.3	Time delay for mode change from Normal Mode to Sleep Mode via EN pin	V_{EN} = 0V	EN	t_{sleep}	2	7	12	µs	A
10.4	TXD dominant time-out time	V_{TXD} = 0V	TXD	t_{dom}	27	55	70	ms	A
10.5	Time delay for mode change from Silent Mode into Normal Mode via EN	$V_{EN} = V_{CC}$	EN	t_{s_n}	5	15	40	µs	A
10.6	Monitoring time for wake-up over LIN bus		LIN	t_{mon}	6	10	15	ms	A
	LIN Bus Driver AC Parameter with Different Bus Loads Load 1 (small): 1 nF, 1 kΩ; Load 2 (large): 10 nF, 500Ω; R_{RXD} = 5 kΩ; C_{RXD} = 20 pF; Load 3 (medium): 6.8 nF, 660Ω characterized on samples; 10.7 and 10.8 specifies the timing parameters for proper operation of 20 Kbit/s, 10.9 and 10.10 at 10.4 Kbit/s								
10.7	Duty cycle 1	$TH_{Rec(max)} = 0.744 \times V_S$ $TH_{Dom(max)} = 0.581 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 50 µs $D1 = t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN	D1	0.396				A
10.8	Duty cycle 2	$TH_{Rec(min)} = 0.422 \times V_S$ $TH_{Dom(min)} = 0.284 \times V_S$ V_S = 7.6V to 18V t_{Bit} = 50 µs $D2 = t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN	D2			0.581		A
10.9	Duty cycle 3	$TH_{Rec(max)} = 0.778 \times V_S$ $TH_{Dom(max)} = 0.616 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 96 µs $D3 = t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN	D3	0.417				A
10.10	Duty cycle 4	$TH_{Rec(min)} = 0.389 \times V_S$ $TH_{Dom(min)} = 0.251 \times V_S$ V_S = 7.6V to 18V t_{Bit} = 96 µs $D4 = t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN	D4			0.590		A
10.11	Slope time falling and rising edge at LIN	V_S = 7.0V to 18V	LIN	t_{SLOPE_fall} t_{SLOPE_rise}	3.5		22.5	µs	A
11	**Receiver Electrical AC Parameters of the LIN Physical Layer, LIN Receiver, RXD Load Conditions (C_{RXD}): 20 pF**								
11.1	Propagation delay of receiver (Figure 9-1)	V_S = 7.0V to 18V $t_{rx\_pd} = \max(t_{rx\_pdr}, t_{rx\_pdf})$	RXD	t_{rx_pd}			6	µs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	V_S = 7.0V to 18V $t_{rx\_sym} = t_{rx\_pdr} - t_{rx\_pdf}$	RXD	t_{rx_sym}	–2		+2	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
12	**NRES Open Drain Output Pin**								
12.1	Low-level output voltage	$V_S \geq 5.5V$ I_{NRES} = 1 mA	NRES	V_{NRESL}			0.14	V	A
12.2	Low-level output low	10 kΩ to 5V V_{CC} = 0V	NRES	V_{NRESLL}			0.14	V	A
12.3	Undervoltage reset time	$V_S \geq 5.5V$ C_{NRES} = 20 pF	NRES	t_{reset}	2	4	6	ms	A
12.4	Reset debounce time for falling edge	$V_S \geq 5.5V$ C_{NRES} = 20 pF	NRES	t_{res_f}	1.5		10	µs	A
12.5	Switch off leakage current	V_{NRES} = 5.5V	NRES		–3		+3	µA	A
13	**Watchdog Oscillator**								
13.1	Voltage at WD_OSC in Normal or Fail-safe Mode	I_{WD_OSC} = –200 µA $V_{VS} \geq 4V$	WD_OSC	V_{WD_OSC}	1.13	1.23	1.33	V	A
13.2	Possible values of resistor	Resistor ±1%	WD_OSC	R_{OSC}	34		120	kΩ	A
13.3	Oscillator period	R_{OSC} = 34 kΩ		t_{OSC}	10.65	13.3	15.97	µs	A
13.4	Oscillator period	R_{OSC} = 51 kΩ		t_{OSC}	15.68	19.6	23.52	µs	A
13.5	Oscillator period	R_{OSC} = 91 kΩ		t_{OSC}	26.83	33.5	40.24	µs	A
13.6	Oscillator period	R_{OSC} = 120 kΩ		t_{OSC}	34.2	42.8	51.4	µs	A
14	**Watchdog Timing Relative to t_{osc}**								
14.1	Watchdog lead time after Reset			t_d		7895		cycles	A
14.2	Watchdog closed window			t_1		1053		cycles	A
14.3	Watchdog open window			t_2		1105		cycles	A
14.4	Watchdog reset time NRES		NRES	t_{nres}	3.2	4	4.8	ms	A
15	**KL_15 Pin**								
15.1	High-level input voltage R_V = 47 kΩ	Positive edge initializes a wake-up	KL_15	V_{KL_15H}	4		V_S + 0.3V	V	A
15.2	Low-level input voltage R_V = 47 kΩ		KL_15	V_{KL_15L}	–1		+2	V	A
15.3	KL_15 pull-down current	V_S < 27V V_{KL_15} = 27V	KL_15	I_{KL_15}		50	60	µA	A
15.4	Internal debounce time	Without external capacitor	KL_15	Tdb_{KL_15}	80	160	250	µs	A
15.5	KL_15 wake-up time	R_V = 47 kΩ , C = 100 nF	KL_15	Tw_{KL_15}	0.4	2	4.5	ms	C
16	**WAKE Pin**								
16.1	High-level input voltage		WAKE	V_{WAKEH}	V_S – 1V		V_S + 0.3V	V	A
16.2	Low-level input voltage	Initializes a wake-up signal	WAKE	V_{WAKEL}	–1		V_S – 3.3V	V	A
16.3	WAKE pull-up current	V_S < 27V, V_{WAKE} = 0V	WAKE	I_{WAKE}	–30	–10		µA	A
16.4	High-level leakage current	V_S = 27V, V_{WAKE} = 27V	WAKE	I_{WAKEL}	–5		+5	µA	A
16.5	Time of low pulse for wake-up via WAKE pin	V_{WAKE} = 0V	WAKE	I_{WAKEL}	30	70	150	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
17	**VCC Voltage Regulator ATA6628 in Normal/Fail-safe and Silent Mode, VCC and PVCC Short-circuited**								
17.1	Output voltage VCC	4V < V_S < 18V (0 mA to 50 mA)	VCC	VCC_{nor}	3.234		3.366	V	A
17.2	Output voltage VCC at low VS	3V < V_S < 4V	VCC	VCC_{low}	$V_S - V_D$		3.366	V	A
17.3	Regulator drop voltage	V_S > 3V, I_{VCC} = –15 mA	VS, VCC	V_D			200	mV	A
17.4	Regulator drop voltage	V_S > 3V, I_{VCC} = –50 mA	VS, VCC	V_D		500	700	mV	A
17.5	Line regulation	4V < V_S < 18V	VCC	VCC_{line}		0.1	0.2	%	A
17.6	Load regulation	5 mA < I_{VCC} < 50 mA	VCC	VCC_{load}		0.1	0.5	%	A
17.7	Power supply ripple rejection	10 Hz to 100 kHz C_{VCC} = 10 µF V_S = 14V, I_{VCC} = –15 mA	VCC		50			dB	D
17.8	Output current limitation	V_S > 4V	VCC	I_{VCClim}	–240	–160	–85	mA	A
17.9	Load capacity	0.2Ω < ESR < 5Ω at 100 kHz	VCC	C_{load}	1.8	10		µF	D
17.10	VCC undervoltage threshold	Referred to VCC V_S > 4V	VCC	V_{thunN}	2.8		3.2	V	A
17.11	Hysteresis of undervoltage threshold	Referred to VCC V_S > 4V	VCC	$Vhys_{thun}$		150		mV	A
17.12	Ramp-up time V_S > 4V to V_{CC} = 3.3V	C_{VCC} = 2.2 µF I_{load} = –5 mA at VCC	VCC	T_{VCC}		320	500	µs	A
18	**VCC Voltage Regulator ATA6630 in Normal/Fail-safe and Silent Mode, VCC and PVCC Short-circuited**								
18.1	Output voltage VCC	5.5V < V_S < 18V (0 mA to 50 mA)	VCC	VCC_{nor}	4.9		5.1	V	A
18.2	Output voltage VCC at low VS	4V < V_S < 5.5V	VCC	VCC_{low}	$V_S - V_D$		5.1	V	A
18.3	Regulator drop voltage	V_S > 4V, I_{VCC} = –20 mA	VS, VCC	V_{D1}			250	mV	A
18.4	Regulator drop voltage	V_S > 4V, I_{VCC} = –50 mA	VS, VCC	V_{D2}		400	600	mV	A
18.5	Regulator drop voltage	V_S > 3.3V, I_{VCC} = –15 mA	VS, VCC	V_{D3}			200	mV	A
18.6	Line regulation	5.5V < V_S < 18V	VCC	VCC_{line}		0.1	0.2	%	A
18.7	Load regulation	5 mA < I_{VCC} < 50 mA 100 kHz	VCC	VCC_{load}		0.1	0.5	%	A
18.8	Power supply ripple rejection	10 Hz to 100 kHz C_{VCC} = 10 µF V_S = 14V, I_{VCC} = –15 mA	VCC		50			dB	D
18.9	Output current limitation	VS > 5.5V	VCC	I_{VCClim}	–240	–130	–85	mA	A
18.10	Load capacity	0.2Ω < ESR < 5Ω at 100 kHz	VCC	V_{thunN}	1.8	10		µF	D
18.11	VCC undervoltage threshold	Referred to VCC V_S > 5.5V	VCC	V_{thunN}	4.2		4.8	V	A
18.12	Hysteresis of undervoltage threshold	Referred to VCC V_S > 5.5V	VCC	$Vhys_{thun}$		250		mV	A
18.13	Ramp-up time V_S > 5.5V to V_{CC} = 5V	C_{VCC} = 2.2 µF I_{load} = –5 mA at VCC	VCC	t_{VCC}		370	600	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
19	**DIV_ON Input Pin**								
19.1	Low-level voltage input		DIV_ON	V_{DIV_ON}	–0.3		+0.8	V	A
19.2	High-level voltage input		DIV_ON	V_{DIV_ON}	2		V_{CC} + 0.3	V	A
19.3	Pull-down resistor	$V_{DIV\_ON} = V_{CC}$	DIV_ON	R_{DIV_ON}	125	250	400	kΩ	A
19.4	Low-level input current	V_{DIV_ON} = 0V	DIV_ON	I_{DIV_ON}	–3		+3	µA	A
20	**SP_MODE Input Pin**								
20.1	Low-level voltage input		SP_MODE	V_{SP_MODE}	–0.3		+0.8	V	A
20.2	High-level voltage input		SP_MODE	V_{SP_MODE}	2		V_{CC} + 0.3	V	A
20.3	Pull-down resistor	$V_{SP\_MODE} = V_{CC}$	SP_MODE	R_{SP_MODE}	50	125	200	kΩ	A
20.4	Low-level input current	V_{SP_MODE} = 0V	SP_MODE	I_{SP_MODE}	–3		+3	µA	A
21	**LIN Driver in High-speed Mode(VSP_Mode = VCC)**								
21.1	Transmission Baud rate	V_S = 7V to 18V R_{LIN} = 500Ω, C_{LIN} = 600 pF	LIN	SP	115			kBaud	C
21.2	Slope time LIN falling edge	V_S = 7V to 18V	LIN	t_{SL_fall}		1	2	µs	A
21.3	Slope time LIN rising edge, depending on RC-load	V_S = 14V R_{LIN} = 500Ω, C_{LIN} = 600 pF	LIN	t_{SL_rise}		2	3	µs	A
22	**ATA6628 Voltage Divider**								
22.1	Divider ratio	VS = 5V to 18V	PV			1:6			A
22.2	Divider ratio error				–2		+2	%	A
22.3	Divider temperature drift					3		ppm/°C	C
22.4	VBATT range of divider linearity		VBATT		5		18	V	A
22.5	VBatt input current	VBATT = 14V	VBATT		100		220	µA	A
22.6	Maximum output Voltage at PV	VBATT 18V to 40V	VBATT		3	3.1	3.5	V	A
22.7	Pin capacitance		PV			2		pF	
23	**ATA6630 Voltage Divider**								
23.1	Divider ratio	VS = 5V to 27V	PV			1:6			A
23.2	Divider ratio error				–2		+2	%	A
23.3	Divider temperature drift					3		ppm/°C	C
23.4	VBATT range of divider linearity		VBATT		5		27	V	A
23.5	VBatt input current	VBATT = 14V	VBATT		100		220	µA	A
23.6	Maximum output Voltage at PV	VBATT 27V to 40V	PV		4.4	4.8	5.2	V	A
23.7	Pin capacitance		PV			2		pF	

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 9-1. Definition of Bus Timing Characteristics

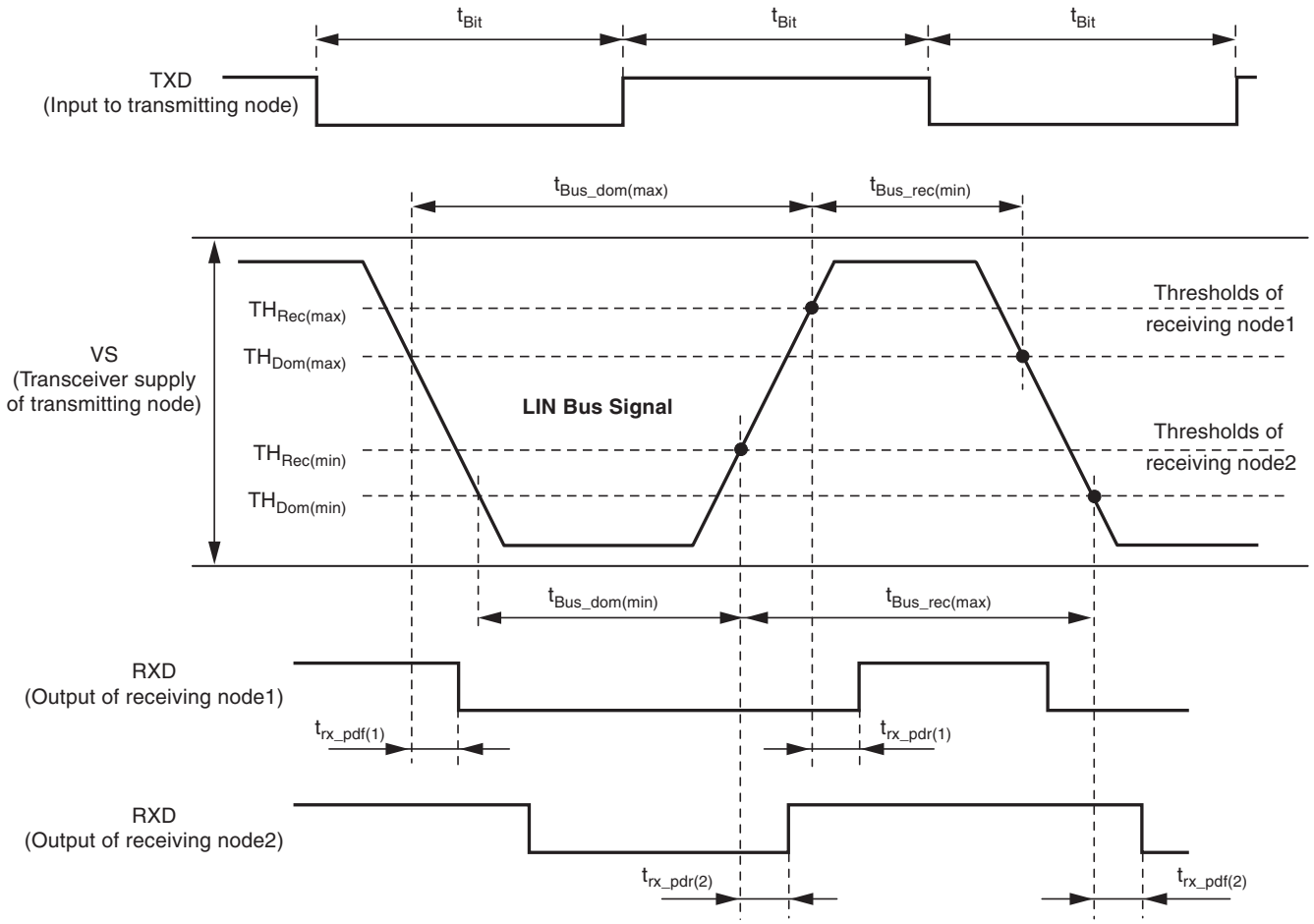


Figure 9-2. Typical Application Circuit

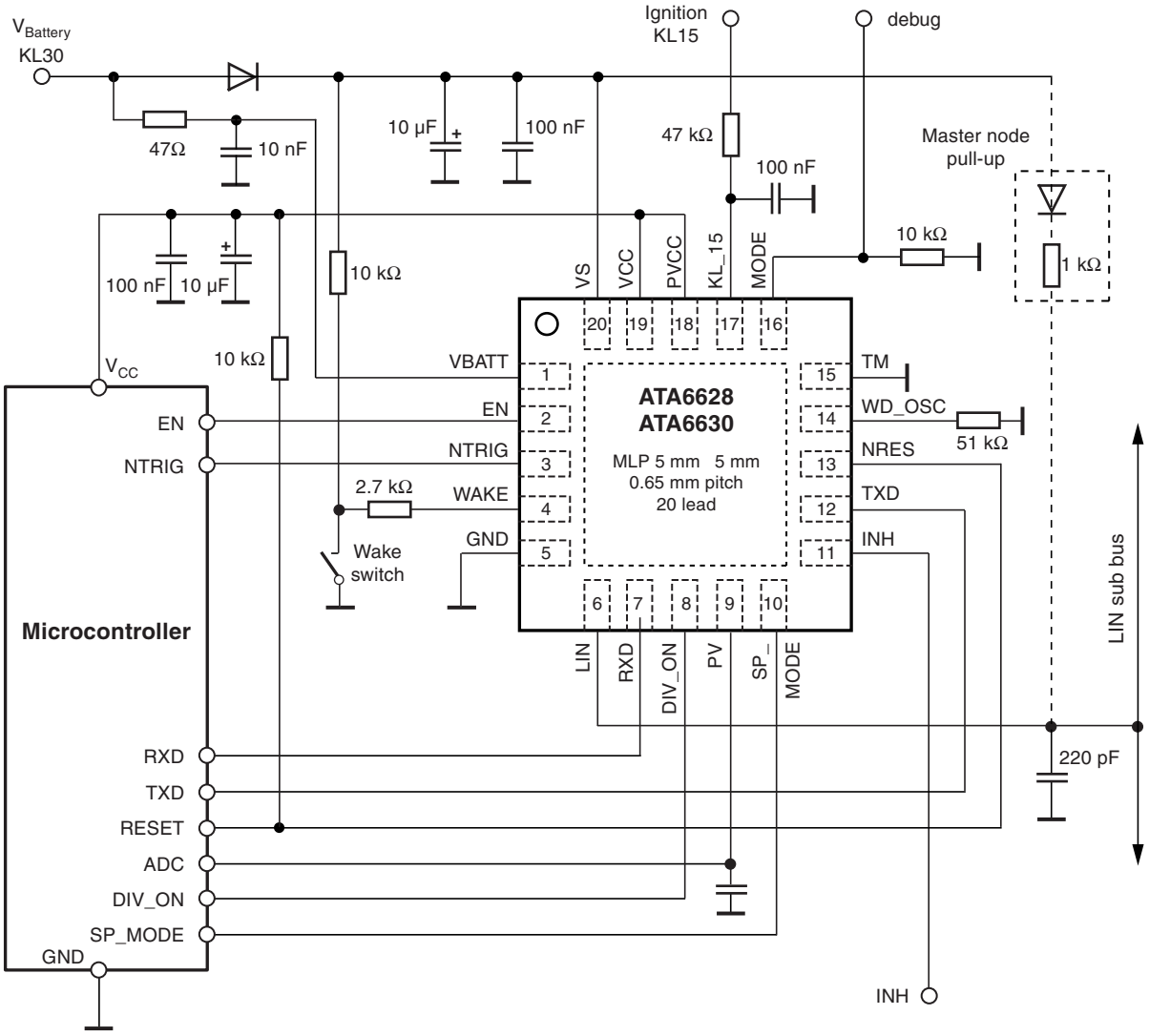
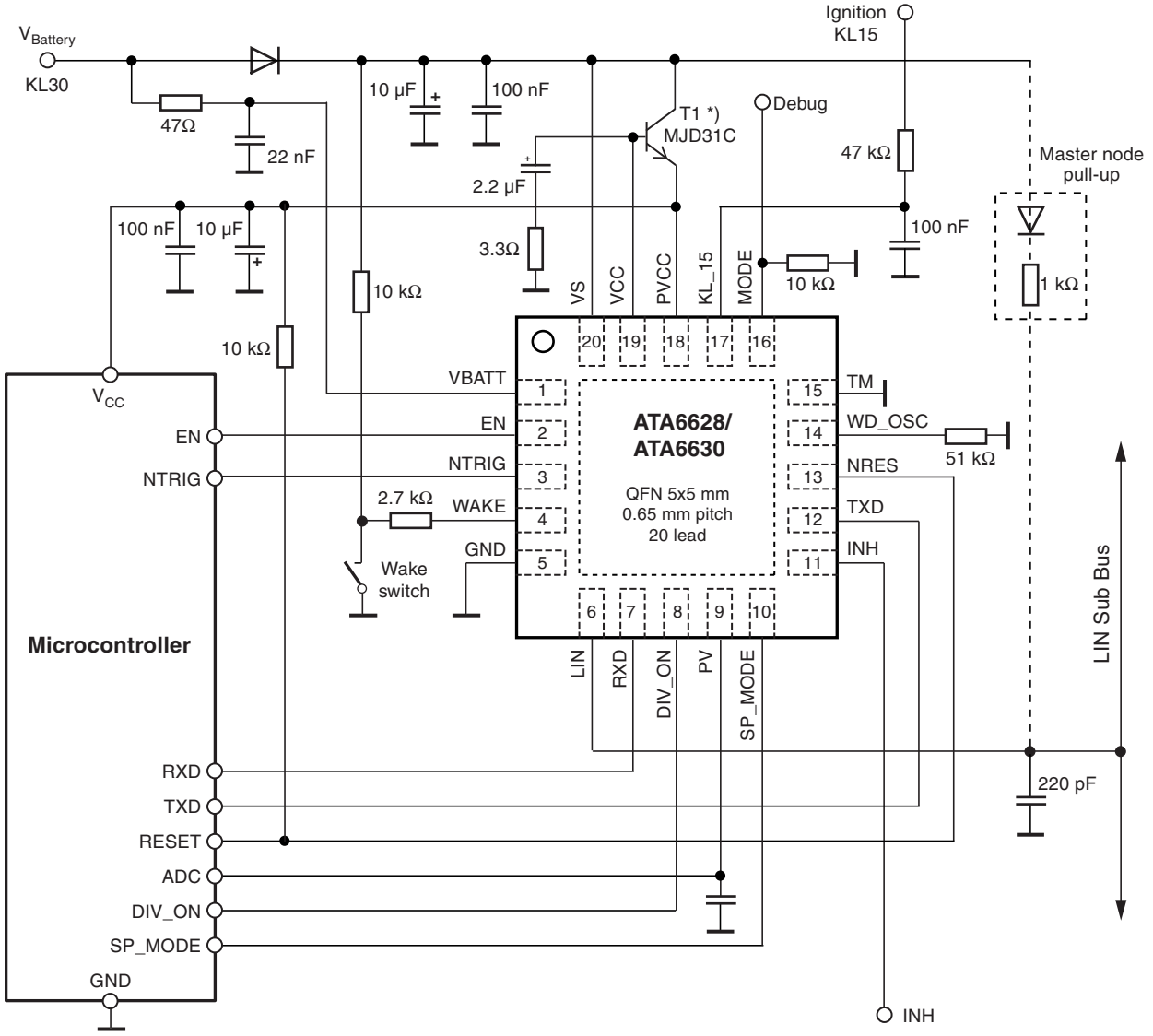
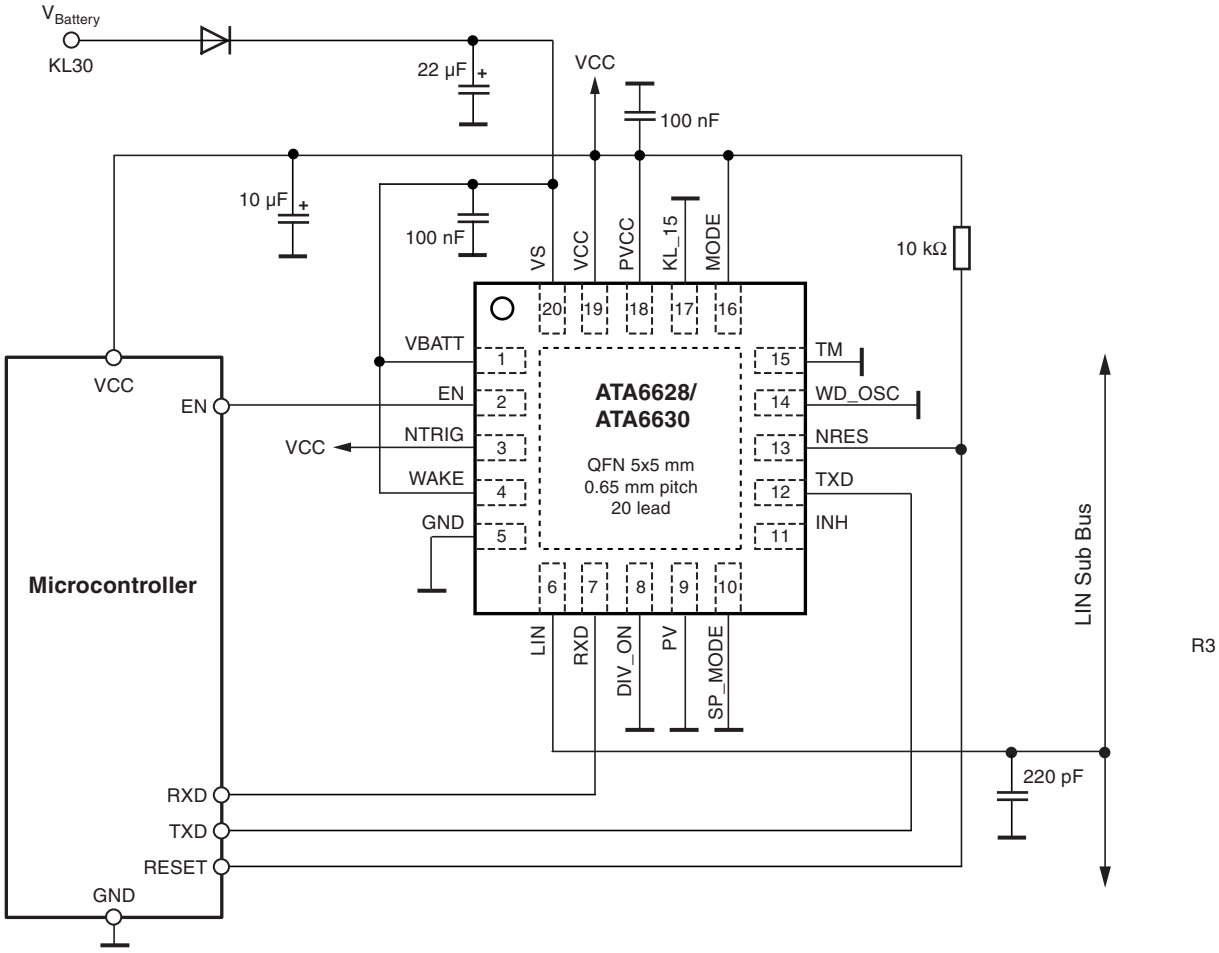


Figure 9-3. Application Circuit with External NPN-Transistor



*) Note that the output voltage PVCC is no longer short-ciruit protected when boosting the output current by an external NPN-transistor.

Figure 9-4. LIN Slave Application with Minimum External Devices



Note: No watchdog, no Battery voltage measurement, no local wake up, INH output not used

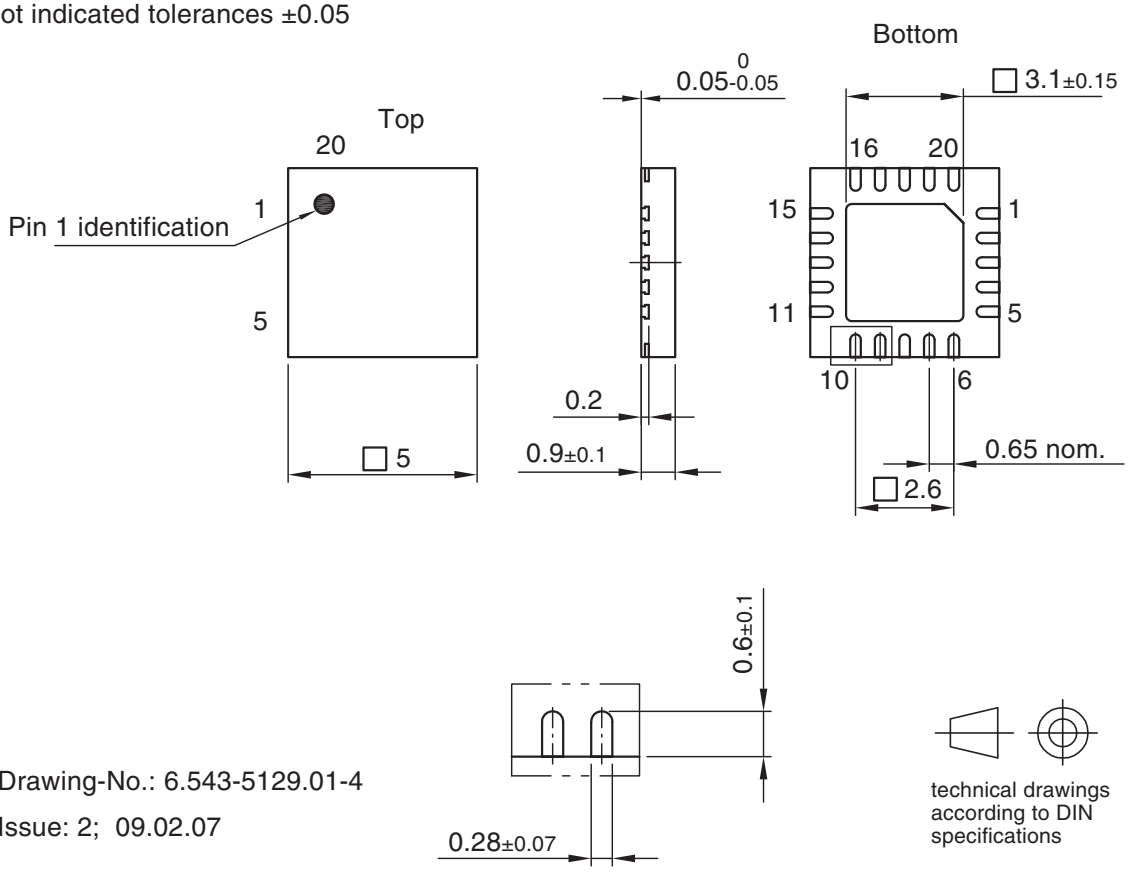
10. Ordering Information

Extended Type Number	Package	Remarks
ATA6628-PGPW	QFN20	3.3V LIN system-basis-chip, Pb-free, 1.5k, taped and reeled
ATA6630-PGPW	QFN20	5V LIN system-basis-chip, Pb-free, 1.5k, taped and reeled
ATA6628-PGQW	QFN20	3.3V LIN system-basis-chip, Pb-free, 6k, taped and reeled
ATA6630-PGQW	QFN20	5V LIN system-basis-chip, Pb-free, 6k, taped and reeled

11. Package Information

Package: VQFN_5 x 5_20L
Exposed pad 3.1 x 3.1
Dimensions in mm

Not indicated tolerances ±0.05



Drawing-No.: 6.543-5129.01-4

Issue: 2; 09.02.07

technical drawings
according to DIN
specifications

12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9117E-AUTO-07/10	• Section 6 “Watchdog” on pages 20 to 21 changed
9117D-AUTO-05/10	• Features on page 1 changed • Pin Description table: row Pin 16 changed • Text under heading 3.3, 3.8, 3.11, 3.12, 4.2, 5.1, 5.5, 6 changed • Figures 4-5, 6-1 changed • Figure 9-1 heading changed • Figures 9-2 and 9-3 added • Abs.Max.Rat.Table -> Parameter text in row “ESD according...” changed • Abs.Max.Rat.Table -> Values in row “ESD HBM following....” changed • El.Char.Table -> rows changed: 1.2, 1.3, 1.6, 1.7, 7.1,10.4, 17.12, 12.1, 12.2, 17.5, 17.6, 17.7, 17.8, 18.6, 18.7, 18.8, 18.9, 18.13, 11.5, 23.5 • El.Char.Table -> row 8.13 added
9117C-AUTO-10/09	• Complete datasheet: “LIN 2.1 specicfication” changed in “LIN 2.0, 2.1 specicfication or “2.x” • Features on page 1 changed • Description text on page 1 changed • Pin Descritption table rows changed: 8, 11, 12 • Sections changed: 3.9, 3.10, 3.15, 3.20, 3.21, 4.1, 4.2, 4.3, 4-7, 5.1, 5.5, 5.6 • New section 4.4 added (the following section numbers automatically changes...) • Table Abs. Max. Ratings: changes in following rows: WAKE, INH - DC voltage, ESD HBM following STM5.1 • Table El. Characteristics: changes in folloring rows: 1.2, 1.3, 7.2, 8.7, 8.11, 8.12, 13.1, 15.5, 17.9, 18.10, 21 to 23.7 new rows 10.6, 12.5, 18.8 added (the following counting changed) row 20.5 deleted • Figure heading changed: 4-7 • Figures changed: 1-1, 4-3, 4-4, 4-5, 4-6, 4-7, 9-2 • Table headings changed: 3-1

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