

AS1110

Data Sheet

Constant-Current, 16-Channel LED Driver with Diagnostics

1 General Description

The AS1110 is designed to drive up to 16 LEDs through a fast serial interface and features 16 output constant current drivers and an on-chip diagnostic read-back function.

The high clock-frequency (up to 50MHz), adjustable output current, and flexible serial interface makes the device perfectly suited for high-volume transmission applications.

Output current is adjustable (up to 100mA/channel) using an external resistor (R_{EXT}).

The serial interface with Schmitt trigger inputs includes an integrated shift register. Additionally, an internal data register stores the currently displayed data.

The device features integrated diagnostics for over-temperature, open-LED, and shorted-LED conditions. Integrated registers store global fault status information during load as well as the detailed temperature/open-LED/shorted-LED diagnostics results.

The AS1110 also features a low-current diagnostic mode to minimize display flicker during fault testing.

The AS1110 is available in a 24-pin SSOP and the 28-pin QFN (5x5mm) package.

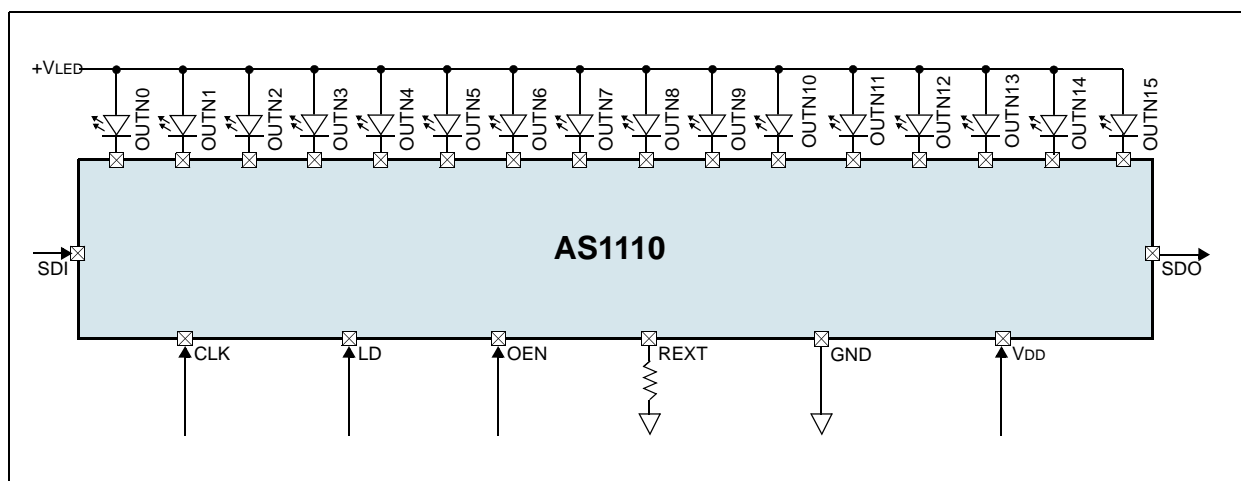
2 Key Features

- 16 Constant-Current Output Channels
- Excellent Output Current Accuracy
 - Between Channels: $\leq \pm 3\%$
 - Between Devices: $\leq \pm 6\%$
- Output Current Per Channel: 0.5 to 100mA
- Controlled In-Rush Current
- Over-Temperature, Open-LED, Shorted-LED Diagnostic Functions
- Low-Current Test Mode
- Global Fault Monitoring
- Low Shutdown Mode Current: 10 μ A
- Fast Serial Interface: 50MHz
- Cascaded Configuration
- Extremely Fast Output Drivers Suitable for PWM
- 24-pin SSOP and 28-pin QFN (5x5mm) Package

3 Applications

The device is ideal for fixed- or slow-rolling displays using static or multiplexed LED matrix and dimming functions, large LED matrix displays, mixed LED display and switch monitoring, displays in elevators, public transports (underground, trains, buses, taxis, airplanes, etc.), large displays in stadiums and public areas, price indicators in retail stores, promotional panels, bar-graph displays, industrial controller displays, white good panels, emergency light indicators, and traffic signs.

Figure 1. Main Diagram and Pin Assignments



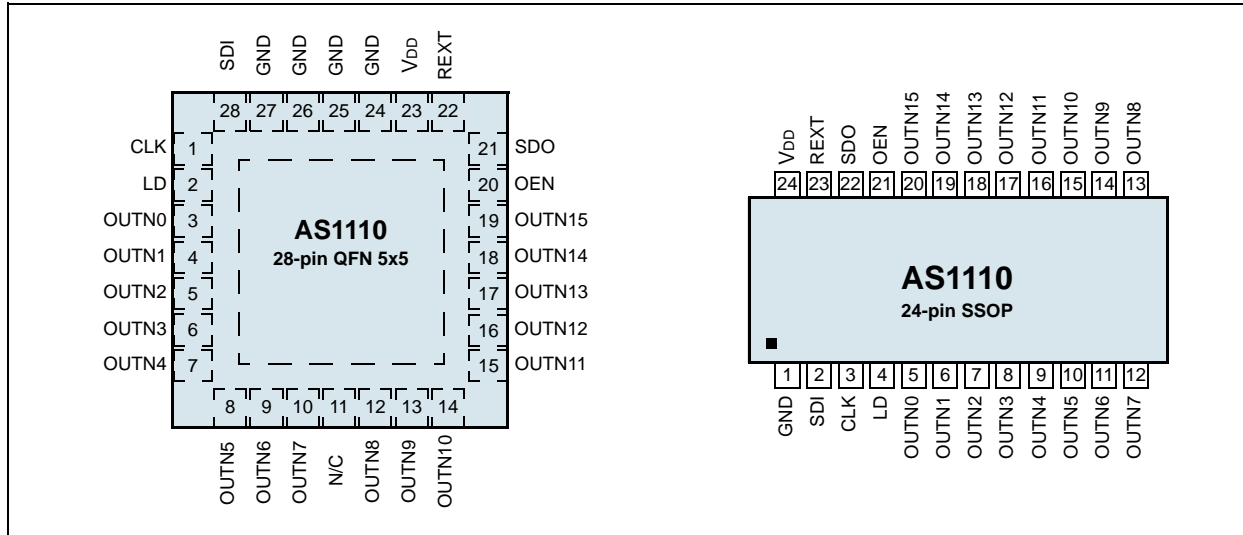
Contents

1	General Description	1
2	Key Features	1
3	Applications	1
4	Pinout	3
	Pin Assignments	3
	Pin Descriptions	3
5	Absolute Maximum Ratings	4
6	Electrical Characteristics	5
	Switching Characteristics	6
7	Typical Operating Characteristics	7
8	Detailed Description	8
	Serial Interface	9
	Timing Diagrams	9
	Error-Detection Mode	11
	Global Error Mode	11
	Error Detection Functions	12
	Open-LED Detection	12
	Shorted-LED	12
	Overtemperature	12
	Detailed Error Reports	13
	Detailed Temperature Warning Report	13
	Detailed Open-LED Error Report	14
	Detailed Shorted-LED Error Report	15
	Low-Current Diagnostic Mode	15
	Shutdown Mode	16
9	Application Information	17
	Error Detection	17
	Error Detection On-The-Fly	17
	Error Detection with Low-Current Diagnosis Mode	17
	Cascading Devices	18
	Constant Current	19
	Adjusting Output Current	19
	Package Power Dissipation	19
	Delayed Outputs	19
	Switching-Noise Reduction	19
	Load Supply Voltage	19
10	Package Drawings and Markings	21
11	Ordering Information	23

4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number		Pin Name	Description
SSOP	QFN		
1	24:27	GND	Ground
2	28	SDI	Serial Data Input
3	1	CLK	Serial Data Clock. The rising edge of the CLK signal is used to clock data into and out of the AS1110 shift register. In error mode, the rising edge of the CLK signal is used to switch error modes.
4	2	LD	Serial Data Load
5:20	3:10 12:19	OUTN0:15	Output Current Drivers. These pins are used as LED drivers or for input sense for diagnostic modes. Data is transferred to the data register at the rising edge of these pins.
21	20	OEN	Output Enable. The active-low pin OEN signal can always enable output drivers to sink current independent of the AS1110 mode. 0 = Output drivers are enabled. 1 = Output drivers are disabled.
22	21	SDO	Serial Data Output. In normal mode SDO is latched out 8.5 clock cycles after SDI is latched in. In global error detection mode this pin indicates the occurrence of a global error. 0 = Global error mode returned an error. 1 = No errors.
23	22	REXT	External Resistor Connection. This pin connects through the external resistor (REXT) to GND, to setup the load current.
24	23	V _{DD}	Positive Supply Voltage
-	11	N/C	Not connected

5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Section 6 Electrical Characteristics on page 5](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Min	Max	Units	Comments
V _{DD} to GND		0	7	V	
Input Voltage		-0.4	V _{DD} +0.4	V	
Output Voltage		-0.4	15	V	
GND Pin Current			2000	mA	24-pin SSOP package
			2800	mA	28-pin QFN (5x5mm) package
Thermal Resistance Θ_{JA}			88	°C/W	on PCB, 24-pin SSOP package
			23	°C/W	on PCB, 28-pin QFN (5x5mm) package
Ambient Temperature		-40	+85	°C	
Storage Temperature		-55	150	°C	
Humidity		5	86	%	Non-condensing
Electrostatic Discharge	Digital Outputs		2000	V	Norm: MIL 833 E method 3015
	All Other Pins		2000		
Latch-Up Immunity		-100 - (I _{NOM} x 0.5)	+100 + I _{NOM}	mA	EIA/JESD78
Package Body Temperature			+260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices". The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

$V_{DD} = +3.0$ to $+5.5V$, $T_{AMB} = -40$ to $+85^{\circ}C$ (unless otherwise specified).

Table 3. Electrical Characteristics

Symbol	Parameter		Condition	Min	Typ	Max	Unit
V _{DD}	Supply Voltage			3.0		5.5	V
V _{DS}	Output Voltage		OUTN0:15	0		15.0	V
I _{OUT}	Output Current		OUTN0:15	0.5		100	mA
I _{OH}			SDO			-1.0	
I _{OL}			SDO			1.0	
V _{IH}	Input Voltage	High Level	CLK, OEN, LD, SDI	0.7 x V _{DD}		V _{DD} + 0.3	V
V _{IL}		Low Level		-0.3		0.3 x V _{DD}	
I _{DS(OFF)}	Output Leakage Current		OEN = 1, V _{DS} = 15.0V			0.5	μA
V _{OL}	Output Voltage	SDO	I _{OL} = +1.0mA			0.4	V
V _{OH}			I _{OH} = -1.0mA	V _{DD} - 0.4V			
I _{AV(LC1)}	Device-to-Device Average Output Current from OUTN0 to OUTN15		V _{DS} = 0.5V, V _{DD} = Const., R _{EXT} = 744Ω	24.5		26	mA
ΔI _{AV(LC1)}	Current Skew (Between Channels)		I _{OUT} = 25.26mA, V _{DS} ≥ 0.5V, V _{DD} = Const., R _{EXT} = 744Ω		±1	±3	%
I _{AV(LC2)}	Device-to-Device Average Output Current from OUTN0 to OUTN15		V _{DS} = 0.6V, V _{DD} > 3.3V, R _{EXT} = 372Ω	49.50		51.55	mA
ΔI _{AV(LC2)}	Current Skew (Between Channels)		I _{OUT} = 50.52mA, V _{DS} ≥ 0.6V, V _{DD} = Const., R _{EXT} = 372Ω		±1	±2	%
I _{AV(LC3)}	Device-to-Device Average Output Current from OUTN0 to OUTN15		V _{DS} = 0.8V, V _{DD} = 5.0V, R _{EXT} = 186Ω	98		104	mA
ΔI _{AV(LC3)}	Current Skew (Between Channels)		I _{OUT} = 90mA, V _{DS} ≥ 0.8V, V _{DD} = Const., R _{EXT} = 186Ω		±1	±2	%
I _{LC}	Low-Current Diagnosis Mode		V _{DS} = 0.8V, V _{DD} = 5.0V	0.4	0.6	0.8	mA
I _{PD}	Power Down Supply Current		V _{DS} = 0.8V, V _{DD} = 5.0V, R _{EXT} = 372Ω, OUTN0:15 = On		10	20	μA
%/ΔV _{DS}	Output Current vs. Output Voltage Regulation		V _{DS} within 1.0 and 3.0V		±0.1		%/V
%/ΔV _{DD}	Output Current vs. Supply Voltage Regulation		V _{DD} within 3.0 and 5.0V		±1		%/V
R _{IN(UP)}	Pullup Resistance		OEN	250	500	800	kΩ
R _{IN(DOWN)}	Pulldown Resistance		LD	250	500	800	kΩ
V _{THL}	Error Detection Threshold Voltage			0.25	0.3	0.45	V
V _{THH}	Error Detection Threshold Voltage		V _{DD} = 3.0V	1.2	1.3	1.4	V
			V _{DD} = 5.0V	2.0	2.2	2.4	
T _{OV1}	Overtemperature Threshold Flag				150		°C

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	
IDD(OFF)0	Supply Current	Off	REXT = Open, OUTN0:15 = Off		2.7	6	mA
IDD(OFF)1			REXT = 744Ω, OUTN0:15 = Off		4.3	8	
IDD(OFF)2			REXT = 372Ω, OUTN0:15 = Off		5.4	9	
IDD(OFF)3		On	REXT = 186Ω, OUTN0:15 = Off		9.3	13	
IDD(ON)1		REXT = 744Ω, OUTN0:15 = On		6.2	11		
IDD(ON)2		REXT = 372Ω, OUTN0:15 = On		10.5	15		
IDD(ON)3		REXT = 186Ω, OUTN0:15 = On		19.5	26		

Switching Characteristics

$V_{DD} = 3.0$ to $5.5V$, $V_{DS} = 0.8V$, $V_{IH} = V_{DD}$, $V_{IL} = GND$, $R_{EXT} = 372\Omega$, $V_{LOAD} = 4.0V$, $R_{LOAD} = 64\Omega$, $C_{LOAD} = 10pF$; guaranteed by design.

Table 4. Switching Characteristics for $V_{DD} = 5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tp1	Propagation Delay Time (Without Staggered Output Delay)	CLK - SDO		5	10	ns
tp2		LD - OUTNn		100	200	
tp3		OEN - OUTNn		100	200	
tp4	Propagation Delay Time				10	ns
tw(CLK)	Pulse Width	CLK	15			ns
tw(L)		LD	15			
tw(OE)		OEN (@I _{OUT} < 60mA)	200			
tr*	CLK Rise Time				500	ns
tf*	CLK Fall Time				500	ns
tor	Output Rise Time of V _{OUT} (Turn Off)			100	200	ns
tof	Output Fall Time of V _{OUT} (Turn On)			100	300	ns
tsu(D)	Setup Time for SDI		5			ns
th(D)	Hold Time for SDI		5			ns
tsu(L)	Setup Time for LD		5			ns
th(L)	Hold Time for LD		5			ns
tTESTING	OEN Time for Error Detection		2000			ns
tSTAG	Staggered Output Delay			20	40	ns
tsu(OE)	Output Enable Setup Time		20			ns
tGSW(ERROR)	Global Error Switching Setup Time		10			ns
tsu(ERROR)	Global Error Detection Setup Time		10			ns
tp(I/O)	Propagation Delay Global Error Flag				5	ns
tSW(ERROR)	Switching Time Global Error Flag				10	ns
fCLK	Maximum Clock Frequency (Cascade Operation)		30	50		MHz
tp3,ON	Low-Current Test Mode Propagation Delay Time	Turn ON		3	5	μs
tp3,OFF		Turn OFF		0.05	0.1	μs
tREXT2,1	External Resistor Reaction Time	Change from REXT1 = 372Ω, IOUT1 = 50.52mA to REXT2 = 37.2kΩ, IOUT2 < 1mA		0.5	1	μs
tREXT2,1	External Resistor Reaction Time	Change from REXT1 = 37.2kΩ, IOUT1 = 0.5mA to REXT2 = 372Ω, IOUT2 > 25mA		0.5	1	μs

* If multiple AS1110 devices are cascaded and tr or tf is large, it may be critical to achieve the timing required for data transfer between two cascaded LED drivers.

7 Typical Operating Characteristics

Figure 3. Output Current vs. R_{EXT} , $V_{DD} = 5V$; $V_{DS} = 0.8V$, $T_{AMB} = 25^{\circ}C$

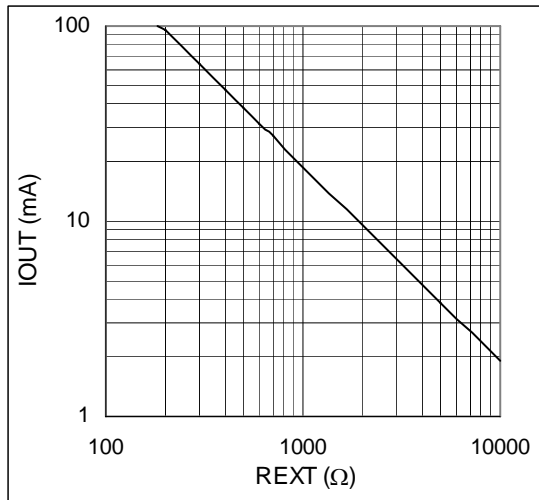


Figure 4. Relative Output Current Error vs. V_{DD} , $I_{OUT}/I_{OUT}@V_{DD}=5V - 1$, $T_{AMB} = 25^{\circ}C$

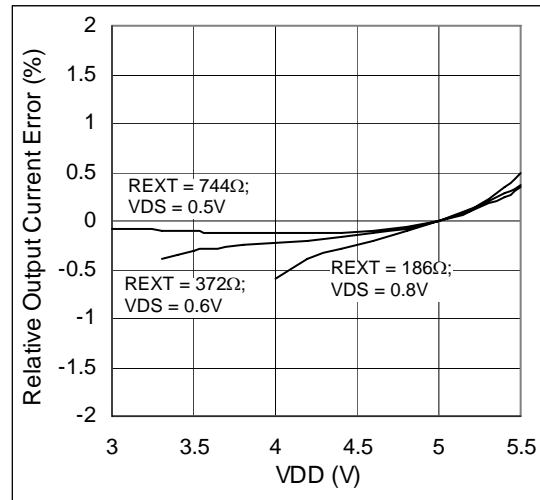


Figure 5. Output Current vs. V_{DS} ; $V_{DD} = 5V$, $T_{AMB} = 25^{\circ}C$

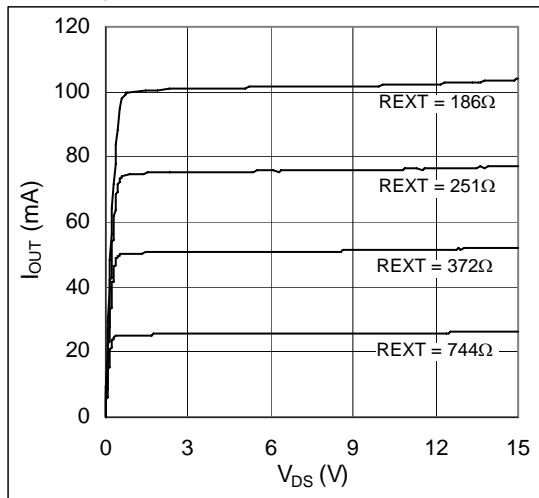
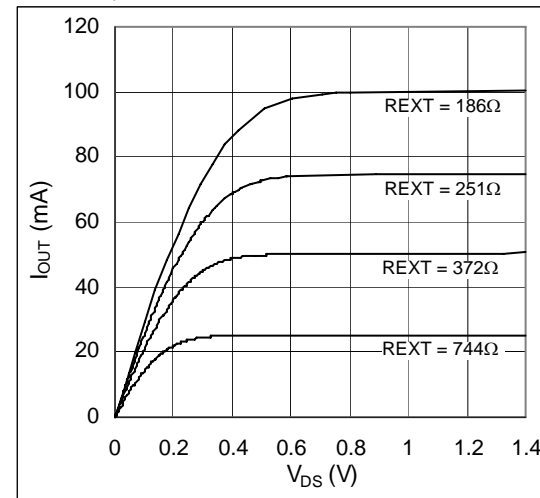


Figure 6. Output Current vs. V_{DS} ; $V_{DD} = 5V$, $T_{AMB} = 25^{\circ}C$



8 Detailed Description

The AS1110 is designed to drive up to 16 LEDs through a fast serial interface and 16 constant-current output drivers. Furthermore, the AS1110 provides diagnostics for detecting open- or shorted-LEDs, as well as over-temperature conditions for LED display systems, especially LED traffic sign applications.

The AS1110 contains an 16-bit shift register and an 16-bit data register, which convert serial input data into parallel output format. At AS1110 output stages, sixteen regulated current sinks are designed to provide uniform and constant current with excellent matching between ports for driving LEDs within a wide range of forward voltage variations. External output current is adjustable from 0.5 to 100mA using an external resistor for flexibility in controlling the brightness intensity of LEDs. The AS1110 guarantees to endure 15V maximum at the outputs.

The serial interface is capable of operating at a minimum of 30 MHz, satisfying the requirements of high-volume data transmission.

Using a multiplexed input/output technique, the AS1110 adds additional functionality to pins SDO, LD and OEN. These pins provide highly useful functions (open- and shorted-LED detection, over-temperature detection), thus reducing pin count. Over-temperature detection will work on-the-run, whereas the open- and shorted-LED detection can be used on-the-run or in low-current diagnostic mode (see page 15).

Figure 7. Block Diagram

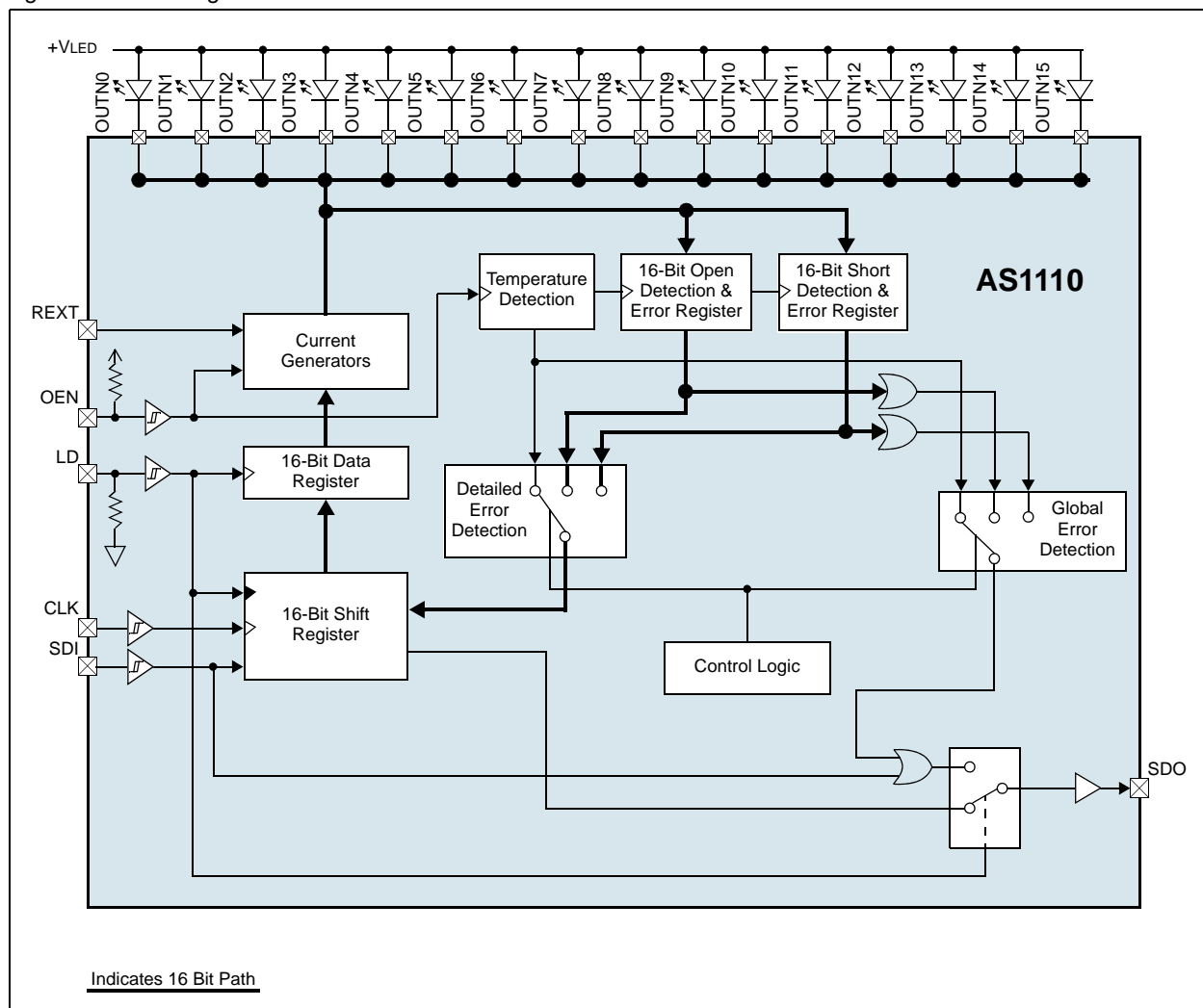


Figure 10. Data Input Timing Diagram

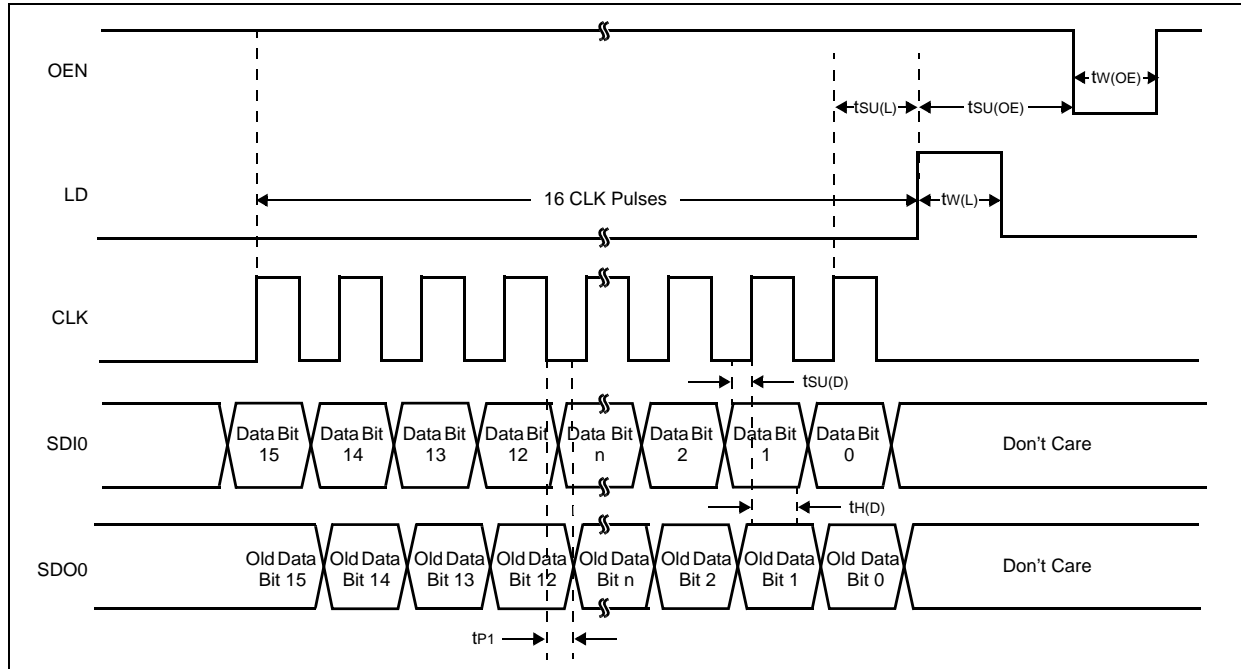


Figure 11. Data Input Example Timing Diagram

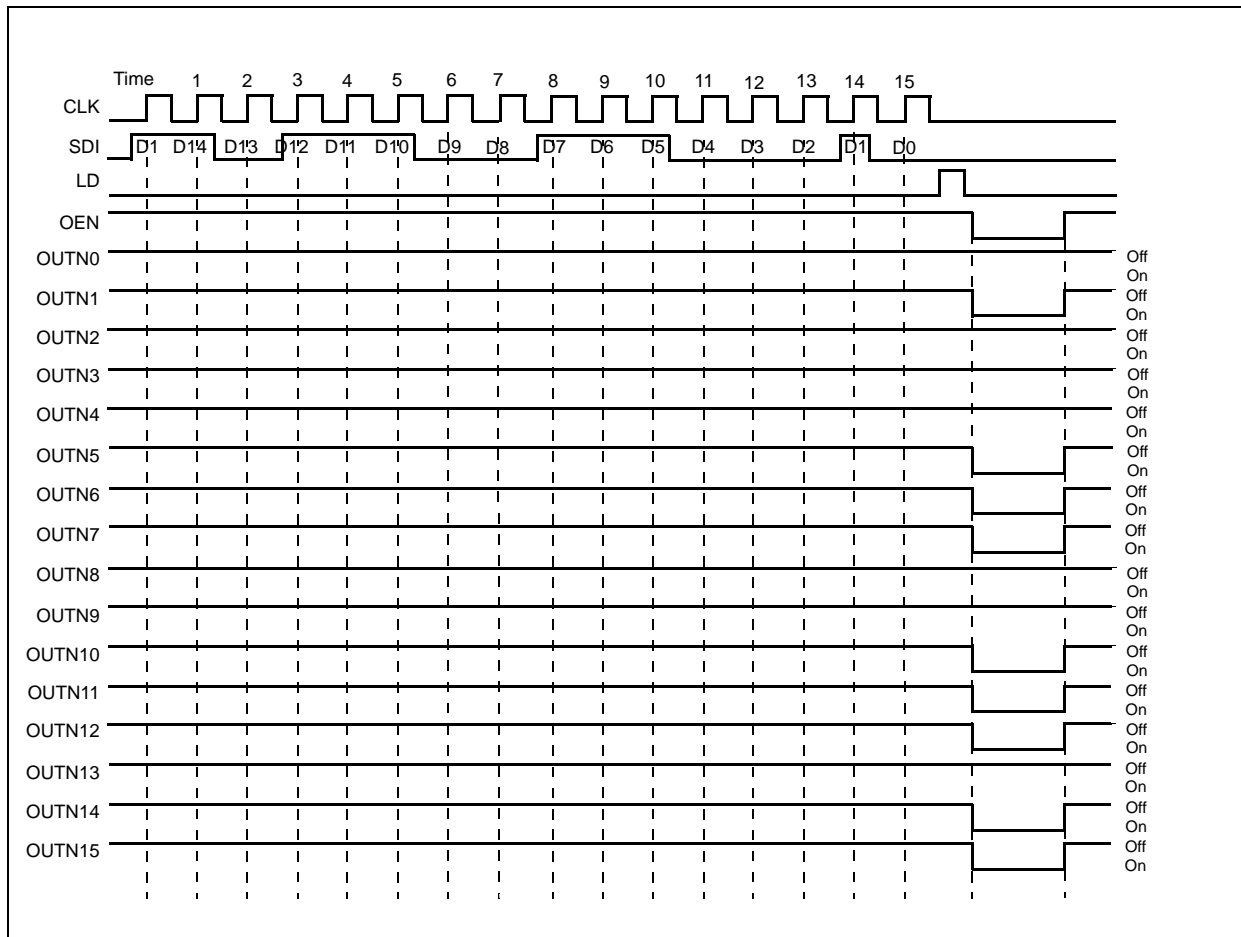
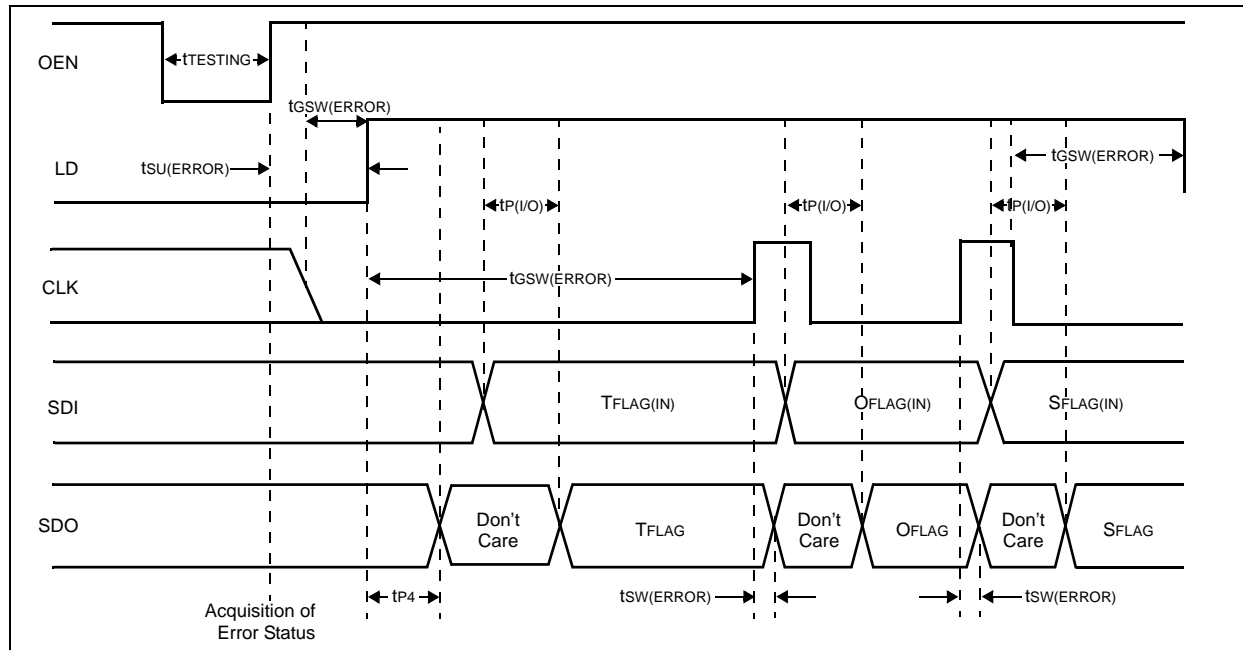


Figure 12. Switching Global Error Mode Timing Diagram



Error-Detection Mode

Acquisition of the error status occurs at the rising edge of OEN. Error-detection mode is started on the rising edge of LD when OEN is high. The CLK signal must be low when entering error detection mode. Error detection for open- and shorted-LEDs can only be performed for LEDs that are switched on during test time. To switch between error-detection modes clock pulses are needed (see Table 5).

Note: To test all LEDs, a test pattern that turns on all LEDs must be input to the AS1110.

Global Error Mode

Global error mode is entered when error-detection mode is started. Clock pulses during this period are used to select between temperature, open-LED, and shorted-LED tests, as well as low-current diagnostic mode and shutdown mode (see Table 5). In global error mode, an error flag (TFLAG, OFLAG, SFLAG) is delivered to pin SDO if any errors are encountered.

Table 5. Global Error Mode Selections

Clock Pulses	Output Port	Error-Detection Mode	Global Error Flag/Shutdown Condition
0	Don't Care	Over-Temperature Detection	TFLAG = SDO = 1: No over-temperature warning. TFLAG = SDO = 0: Over-temperature warning.
1	Enabled	Open-LED Detection	OFLAG = SDO = 1: No open-LED error. OFLAG = SDO = 0: Open-LED error.
2	Enabled	Shorted-LED Detection	SFLAG = SDO = 1: No shorted-LED error. SFLAG = SDO = 0: Shorted-LED error.
3	Don't Care	Low-Current Diagnostic Mode	
4	Don't Care	Shutdown Mode	SDI = 1: Wakeup SDI = 0: Shutdown

Note: For a valid result SDI must be 1 for the first device.

If there are multiple AS1110s in a chain, the error flag will be gated through all devices. To get a valid result at the end of the chain, a logic 1 must be applied to the SDI input of the first device of the chain. If one device produces an error this error will show up after $n \cdot t_{P(I/O)} + t_{SW(ERROR)}$ at pin SDO of the last device in the chain. This means it is not possible to identify which device in the chain produced the error. Therefore, if a global error occurs, the detailed error report can be run to identify which AS1110, or LED produced the error.

Note: When no error has occurred, the detailed error report can be skipped, setting LD and subsequently OEN low.

Error Detection Functions

Open-LED Detection

The AS1110 open-LED detection is based on the comparison between V_{DS} and V_{THL} . The open LED status is acquired at the rising edge of OEN and stored internally. While detecting open-LEDs the output port must be turned on. Open LED detection can be started with 1 clock pulse during error detection mode while the output port is turned on.

Note: LEDs which are turned off at test time cannot be tested and will be shown as a logic 1 in the detailed error report.

Table 6. Open LED Detection Modes

Output Port State	Effective Output Point Conditions	Detected Open-LED Error Status Code	Meaning
On	$V_{DS} < V_{THL}$	0	Open Circuit
On	$V_{DS} > V_{THL}$	1	Normal

Shorted-LED

The AS1110 shorted-LED detection is based on the comparison between V_{DS} and V_{THH} . The shortened LED status is acquired at the rising edge of OEN and stored internally. While detecting shorted-LEDs the output port must be turned on. Shorted-LED detection can be started with 2 clock pulses during error detection mode while the output port is turned on.

For valid results, the voltage at OUTN0:OUTN15 must be lower than V_{THH} under low-current diagnostic mode operating conditions. This can be achieved by reducing the V_{LED} voltage or by adding additional diodes, resistors or LED's.

Note: LEDs which are turned off at test time cannot be tested and will be shown as a logic 1 in the detailed error report.

Table 7. Shorted LED Detection Modes

Output Port State	Effective Output Point Conditions	Detected Shorted-LED Error Status Code	Meaning
On	$V_{DS} > V_{THH}$	0	Short Circuit
On	$V_{DS} < V_{THH}$	1	Normal

Overtemperature

Thermal protection for the AS1110 is provided by continuously monitoring the device's core temperature. The overtemperature status is acquired at the rising edge of OEN and stored internally.

Table 8. Overtemperature Modes

Output Port State	Effective Output Point Conditions	Detected Overtemperature Status Code	Meaning
Don't Care	Temperature $> T_{OV1}$	0	Overtemperature Condition
Don't Care	Temperature $< T_{OV1}$	1	Normal

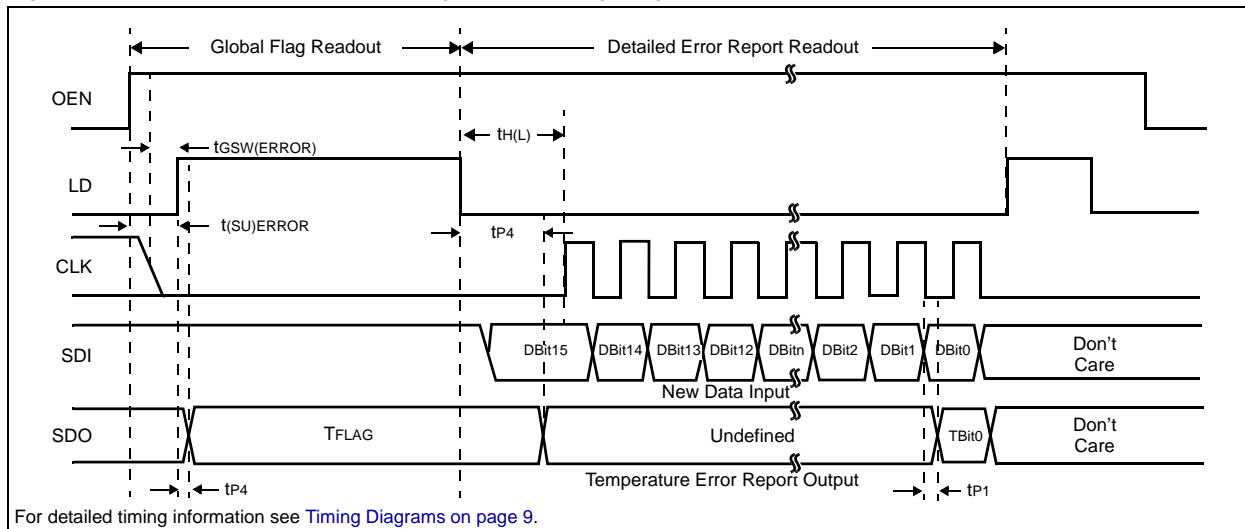
Detailed Error Reports

The detailed error report can be read out after global error mode has been run. At the falling edge of LD, the detailed error report of the selected test is latched into the shift register and can be clocked out with $n \cdot 16$ clock cycles (n is the number of AS1110s in a chain) via pin SDO. At the same time new data can be written into the shift register, which is loaded on the next rising edge of pin LD. This pattern is shown at the output drivers, at the falling edge of OEN.

Detailed Temperature Warning Report

The detailed temperature warning report can be read out immediately after global error mode has been run. SDI must be 1 for the first device. Bit0 of the 16bit data word represents the temperature flag of the chip.

Figure 13. Detailed Temperature Warning Report Timing Diagram



Detailed Temperature Warning Report Example

Consider a case where four AS1110s are cascaded in one chain. The detailed error report lists the temperatures for each device in the chain:

IC1:[70°] IC2:[85°] IC3:[170°] IC4:[60°]

In this case, IC3 is overheated and will generate a global error, and therefore $4 \cdot 16$ clock cycles are needed to write out the detailed temperature warning report, and optionally read in new data. The detailed temperature warning report would look like this:

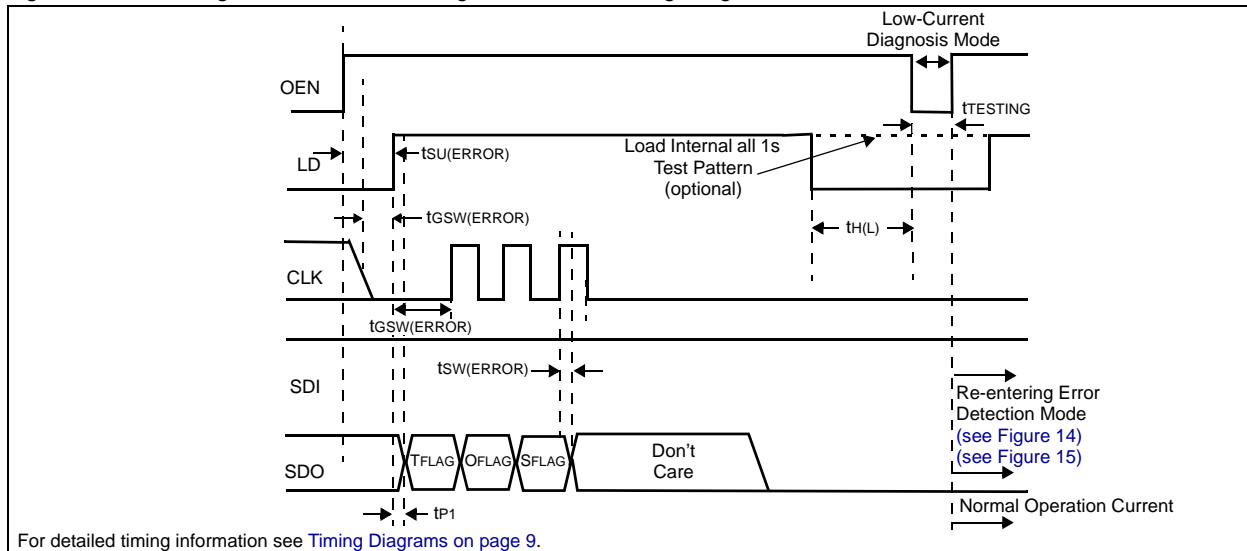
XXXXXXXXXXXXXXXXX1 XXXXXXXXXXXXXXXXXXXX1 XXXXXXXXXXXXXXXXXXXX0 XXXXXXXXXXXXXXXXXXXX1

The 0 in the detailed temperature warning report indicates that IC3 is the device with the over-temperature condition.

Note: In an actual report there are no spaces in the output.

On the next falling edge of OEN, current is reduced to I_{LC} . With the next rising edge of OEN the current will immediately increase to normal levels and the detailed error report can be read out entering error-detection mode.

Figure 16. Switching into Low-Current Diagnostic Mode Timing Diagram



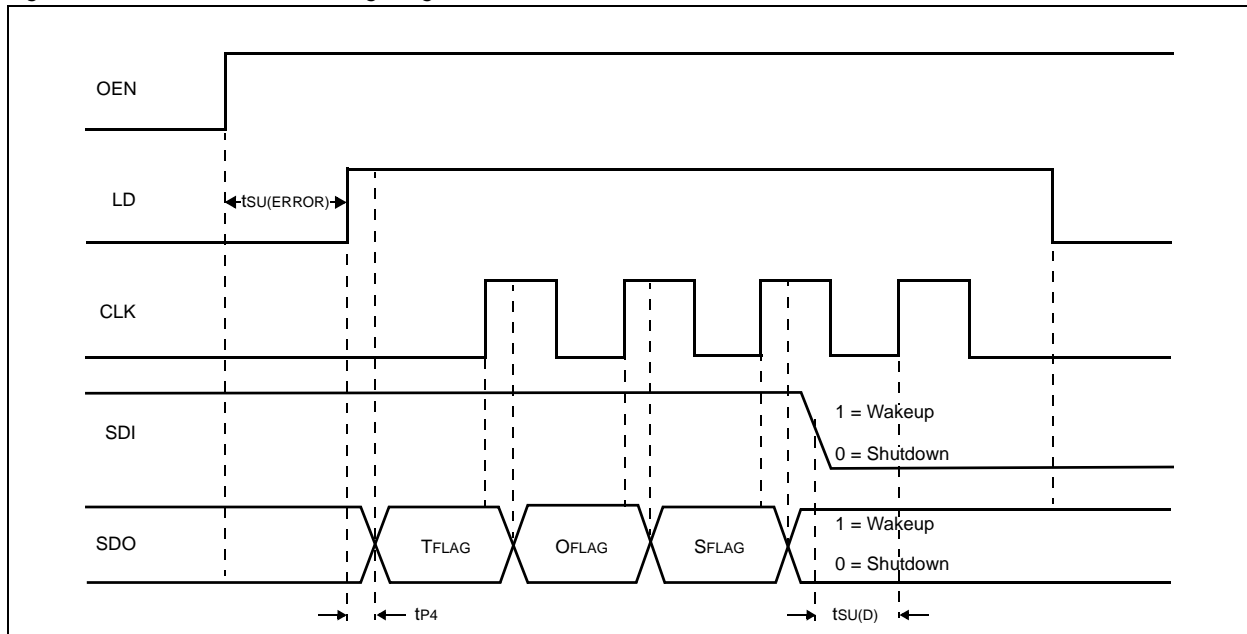
Shutdown Mode

The AS1110 features a shutdown mode which can be entered via 4 clock pulses during error-detection mode. To enable the shutdown mode a 0 must be placed at SDI after the rising edge of the 3rd clock pulse.

To disable shutdown mode a 1 must be placed at SDI after the 3rd clock pulse. The shutdown/wakeup information will be latched through if multiple AS1110 devices are in a chain. At the rising edge of the 4th clock pulse the shutdown bit will be read out and the AS1110 will shutdown or wakeup.

Note: In shutdown mode the supply current drops down to $<10\mu\text{A}$.

Figure 17. Shutdown Mode Timing Diagram



9 Application Information

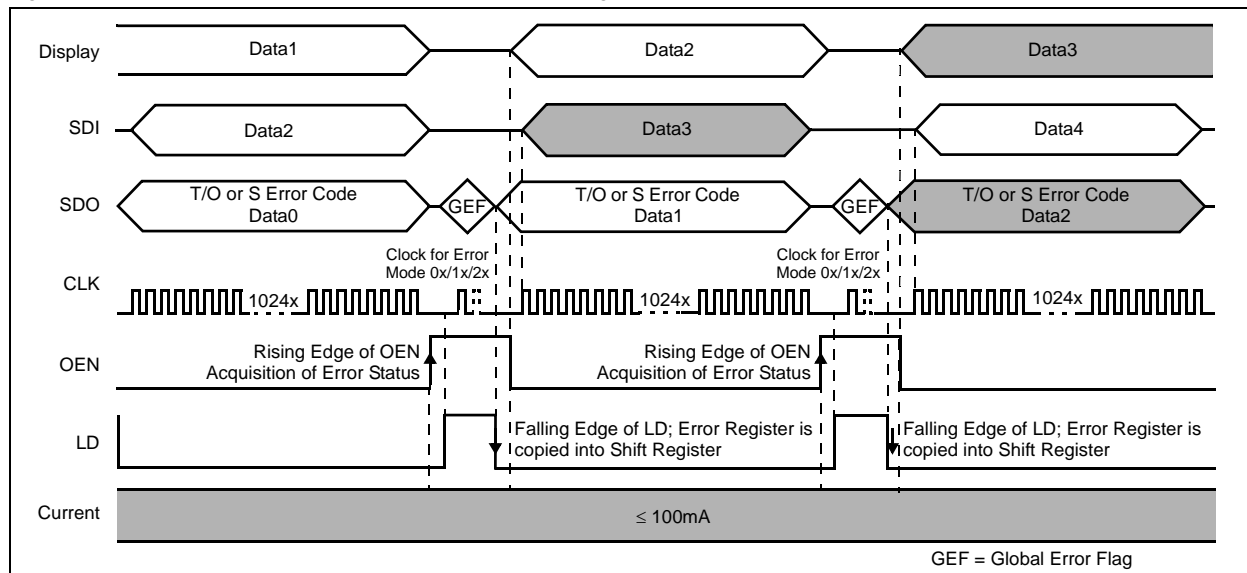
Error Detection

The AS1110 features two types of error detection. The error detection can be used on-the-fly, for active LEDs, without any delay, or by entering into low-current diagnosis mode.

Error Detection On-The-Fly

Error detection on-the-fly will output the status of active LEDs during operation. Without choosing an error mode this will output the temperature flag at every input/output cycle. Triggering one clock pulse for open or two clock pulses for short detection during error detection mode outputs the detailed open- or short-error report with the next input/output cycle (see Figure 18). LEDs turned off at test time are not tested and will show a logic "1" at the detailed error report.

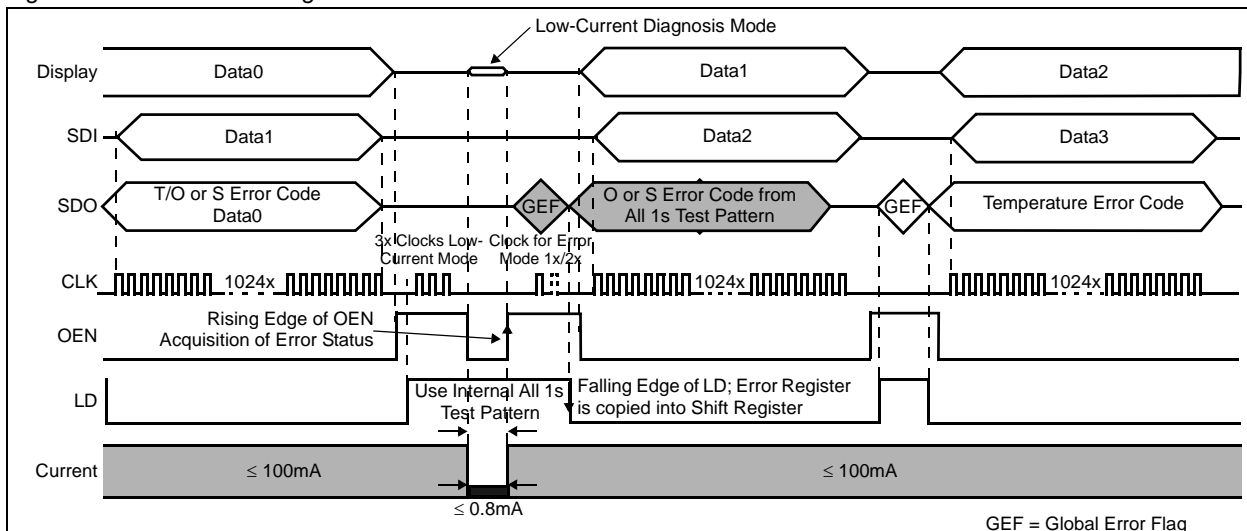
Figure 18. Normal Operation with Error Detection During Operation – 64 Cascaded AS1110s



Error Detection with Low-Current Diagnosis Mode

This unique feature of the AS1110 uses an internal all 1s test pattern for a flicker free diagnosis of all LEDs. This error detection mode can be started at the end of each input cycle (see Figure 19).

Figure 19. Low-Current Diagnosis Mode with Internal All 1s Test Pattern – 64 Cascaded AS1110s



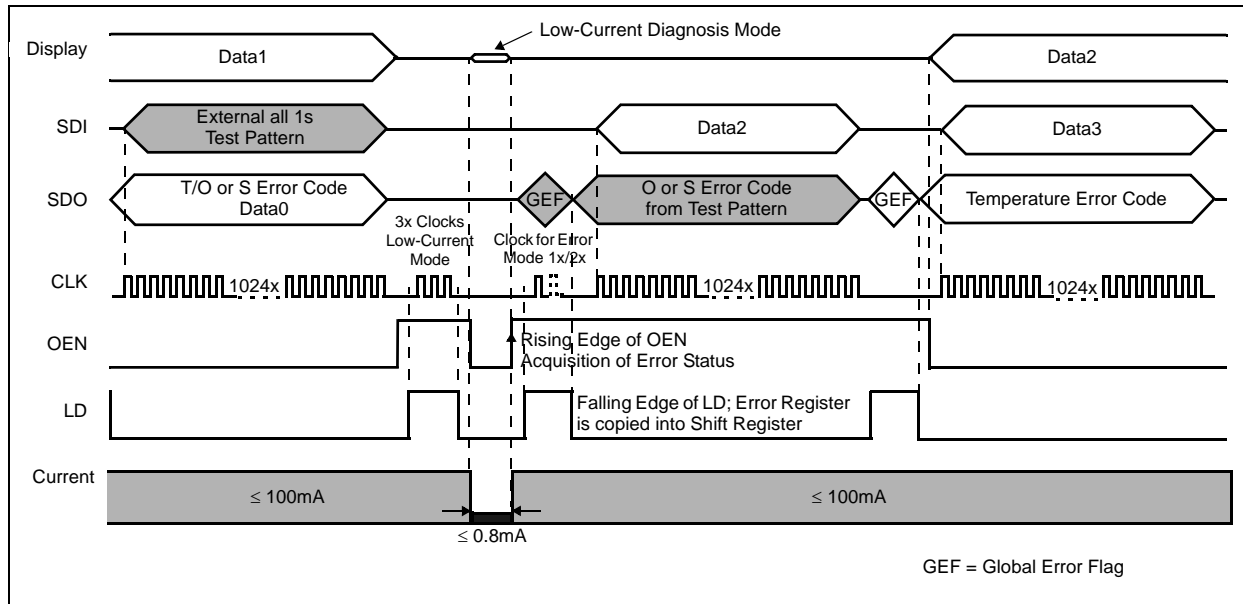
The last pattern written into the shift register will be saved before starting low-current diagnosis mode and can be displayed immediately after the test has been performed.

Low-current diagnostic mode is started with 3 clock pulses during error detection mode. Then OEN should be enabled for $\geq 2\mu\text{s}$ for testing. With the rising edge of OEN the LED test is stopped, and while LD is high the desired error mode can be selected with the corresponding clock pulses. After LD and OEN go low again the previously saved pattern can be displayed at the outputs.

With the next data input the detailed error code will be clocked out at pin SDO.

Note: See Figure 20 for use of an external test pattern.

Figure 20. Low-Current Diagnosis Mode with External Test Pattern – 64 Cascaded AS1110s

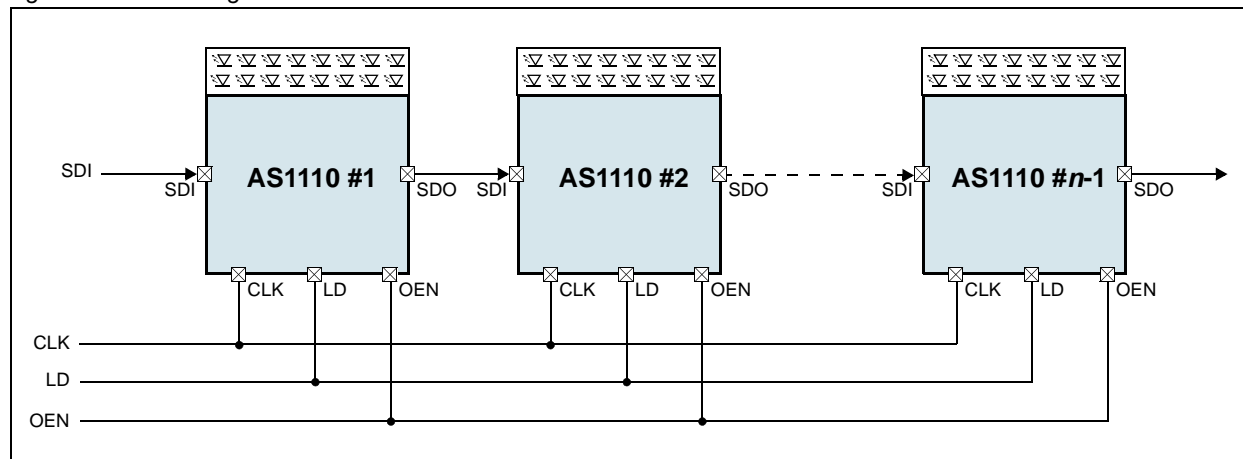


Cascading Devices

To cascade multiple AS1110 devices, pin SDO must be connected to pin SDI of the next AS1110 (see Figure 21). At each rising edge of CLK the LSB of the shift register will be written into the shift register SDI of the next AS1110 in the chain.

Note: When n AS1110 devices are in one chain, $n \cdot 16$ clock pulses are needed to latch-in the input data.

Figure 21. Cascading AS1110 Devices



Constant Current

In LED display applications, the AS1110 provides virtually no current variations from channel-to-channel and from AS1110-to-AS1110. This is mostly due to 2 factors:

- While $I_{OUT} \geq 10\text{mA}$, the maximum current skew is less than $\pm 3\%$ between channels and less than $\pm 6\%$ between AS1110 devices.
- In the saturation region, the characteristic curve of the output stage is flat (see Figure 5 on page 7). Thus, the output current can be kept constant regardless of the variations of LED forward voltages (V_F).

Adjusting Output Current

The AS1110 scales up the reference current (I_{REF}) set by external resistor (R_{EXT}) to sink a current (I_{OUT}) at each output port. As shown in Figure 3 on page 7 the output current in the saturation region is extremely flat so that it is possible to define it as target current ($I_{OUT\ TARGET}$). $I_{OUT\ TARGET}$ can be calculated by:

$$V_{REXT} = 1.253\text{V} \quad (\text{EQ 1})$$

$$I_{REF} = V_{REXT}/R_{EXT} \text{ (if the other end of } R_{EXT} \text{ is connected to ground)} \quad (\text{EQ 2})$$

$$I_{OUT\ TARGET} = I_{REF} * 15 = (1.253\text{V}/R_{EXT}) * 15 \quad (\text{EQ 3})$$

Where:

R_{EXT} is the resistance of the external resistor connected to pin R_{EXT} .

V_{REXT} is the voltage on pin R_{EXT} .

The magnitude of current (as a function of R_{EXT}) is around 50.52mA at 372 Ω and 25.26mA at 744 Ω . Figure 3 on page 7 shows the relationship curve between the $I_{OUT\ TARGET}$ of each channel and the corresponding external resistor (R_{EXT}).

Package Power Dissipation

The maximum allowable package power dissipation (P_D) is determined as:

$$P_{D(MAX)} = (T_J - T_{AMB})/R_{TH(J-A)} \quad (\text{EQ 4})$$

When 16 output channels are turned on simultaneously, the actual package power dissipation is:

$$P_{D(ACT)} = (I_{DD} * V_{DD}) + (I_{OUT} * \text{Duty} * V_{DS} * 16) \quad (\text{EQ 5})$$

Therefore, to keep $P_{D(ACT)} \leq P_{D(MAX)}$, the maximum allowed output current as a function of duty cycle is:

$$I_{OUT} = \{[(T_J - T_{AMB})/R_{TH(J-A)}] - (I_{DD} * V_{DD})\} / V_{DS} / \text{Duty} / 16 \quad (\text{EQ 6})$$

Where:

$T_J = 150^\circ\text{C}$

Delayed Outputs

The AS1110 has graduated delay circuits between outputs. These delay circuits can be found between $OUTN_n$ and constant current block.

The fixed delay time is 20 ns (typ) where $OUTN_0$ has no delay, $OUTN_1$ has 20ns delay, $OUTN_2$ has 40ns delay ... $OUTN_{15}$ has 300ns delay. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on (see Figure 10 on page 10)

Switching-Noise Reduction

LED drivers are frequently used in switch-mode applications which normally exhibit switching noise due to parasitic inductance on the PCB.

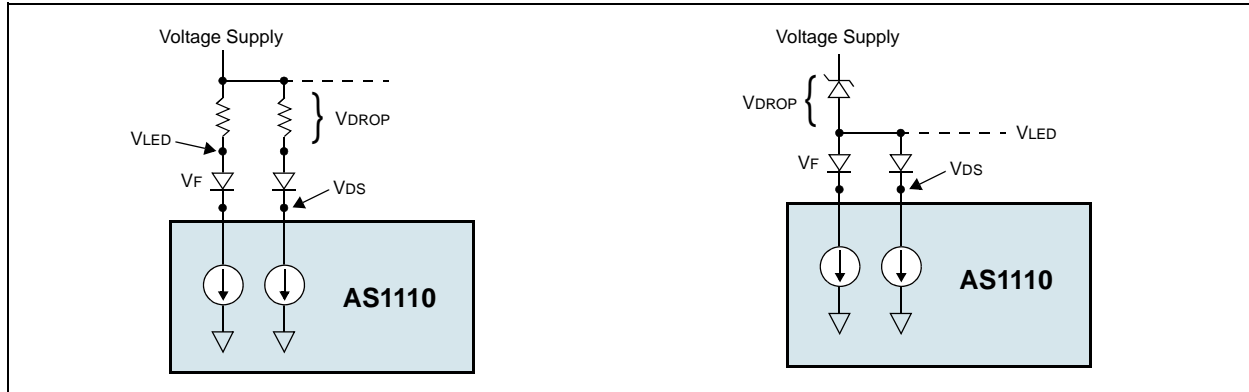
Load Supply Voltage

Considering the package power dissipation limits (see EQ 4:6), the AS1110 should be operated within the range of $V_{DS} = 0.4$ to 1.0V.

For example, if V_{LED} is higher than 5V, V_{DS} may be so high that $P_{D(ACT)} > P_{D(MAX)}$ where $V_{DS} = V_{LED} - V_F$. In this case, the lowest possible supply voltage or a voltage reducer (V_{DROP}) should be used. The voltage reducer allows $V_{DS} = (V_{LED} - V_F) - V_{DROP}$.

Note: Resistors or zener diodes can be used as a voltage reducer as shown in Figure 22.

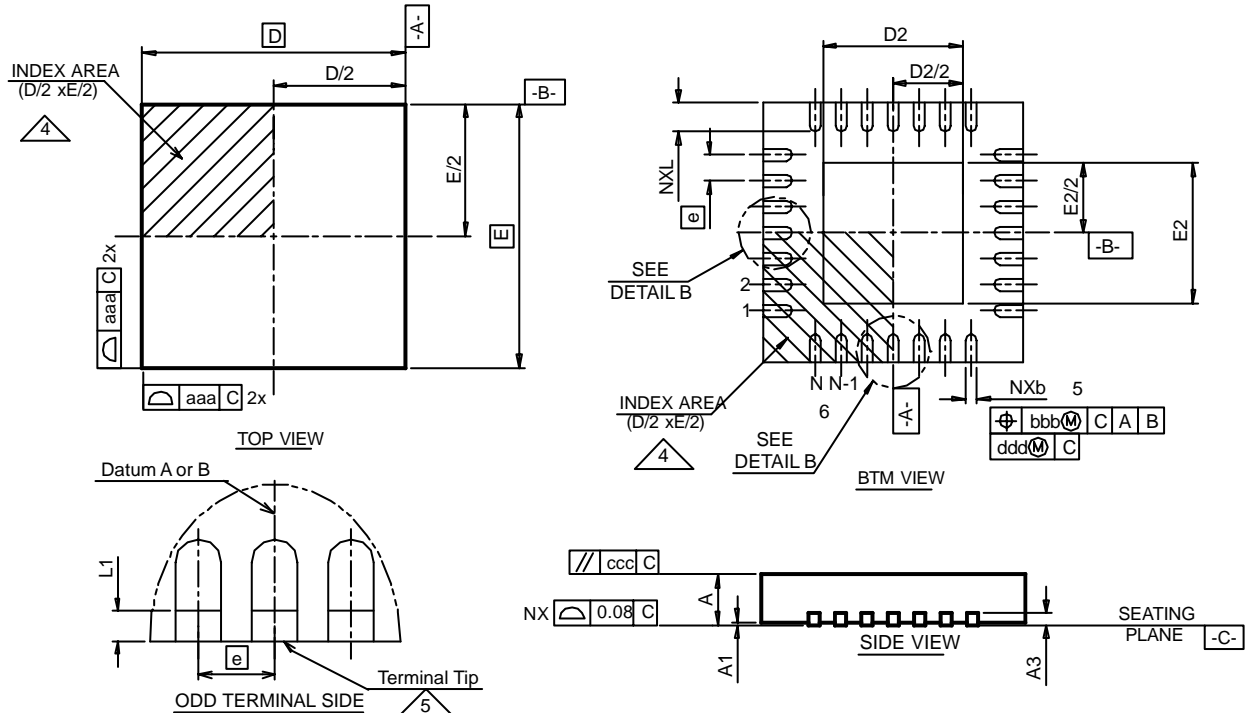
Figure 22. Voltage Reducer using Resistor (Left) and Zener Diode (Right)



10 Package Drawings and Markings

The AS1110 is available in a 28-pin QFN (5x5mm) package and a 24-pin SSOP package.

Figure 23. 28-pin QFN (5x5mm) Package



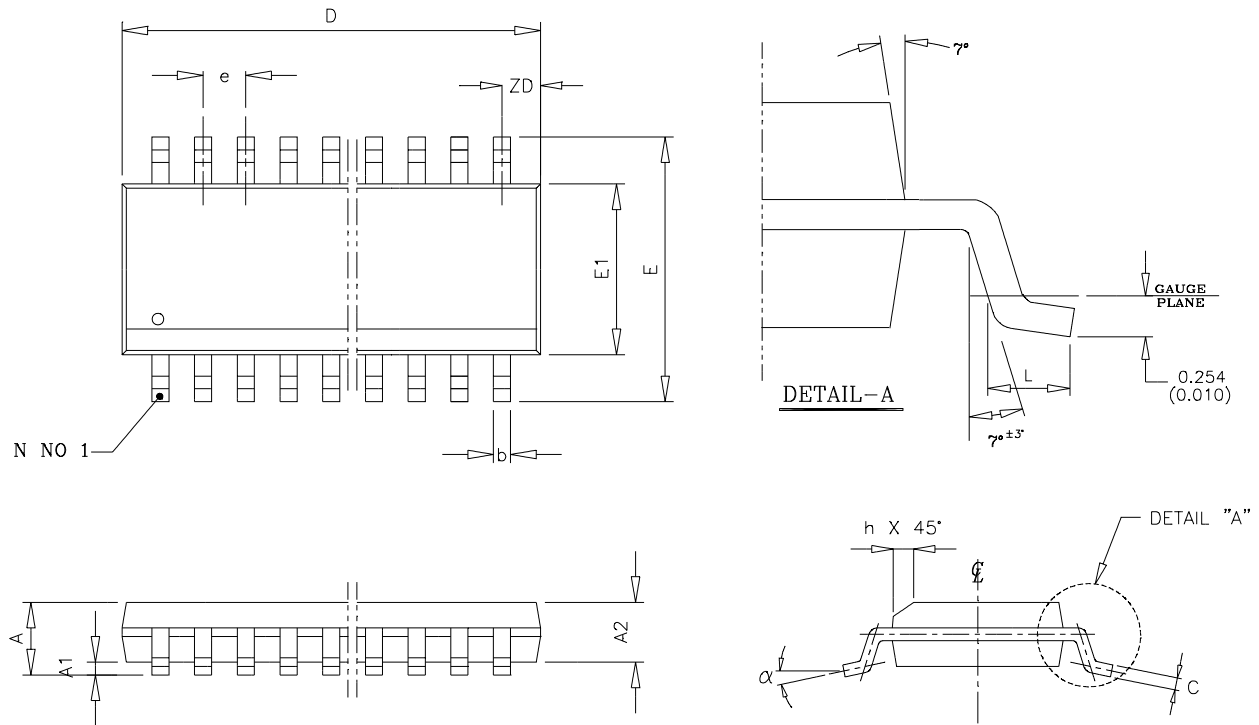
Symbol	Min	Typ	Max	Notes
A	0.70	0.75	0.80	1, 2
A1	0.00	0.02	0.05	1, 2
A3		0.20 REF		1, 2
L	0.45	0.55	0.65	1, 2
L1	0.03		0.15	1, 2
aaa		0.15		1, 2
bbb		0.10		1, 2
ccc		0.10		1, 2
ddd		0.05		1, 2
eee		0.08		1, 2
ggg		0.10		1, 2

Symbol	Min	Typ	Max	Notes
D BSC		5.00		1, 2
E BSC		5.00		1, 2
D2	3.00	3.15	3.25	1, 2
E2	3.00	3.15	3.25	1, 2
K	0.20			1, 2
b	0.18	0.25	0.30	1, 2, 5
e		0.50		
N		28		1, 2
ND		7		1, 2, 5
NE		7		1, 2, 5

Notes: Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters; angles in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to *JEDEC 95 SPP-012*. Details of terminal #1 identifier are optional but must be located within the zone indicated. The terminal #1 identifier may be either a mold or marked feature.
5. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30mm from terminal tip. If one end of the terminal has the optional radius, the b dimension should not be measured in that radius area.
6. Dimensions ND and NE refer to the number of terminals on each D and E side, respectively.

Figure 24. 24-pin SSOP Package



Symbol	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.37	1.57
b	0.20	0.30
C	0.19	0.25
D	8.55	8.74
E	5.79	6.20
E1	3.81	3.99
e	0.635 BSC	
h	0.22	0.49
L	0.40	1.27
θ	0°	8°

11 Ordering Information

The device is available as the standard products shown in [Table 9](#).

Table 9. Ordering Information

Type	Description	Delivery Form	Package
AS1110-BSSU	Constant-Current, 16-Channel LED Driver with Diagnostics	Tubes	24-pin SSOP
AS1110-BSST	Constant-Current, 16-Channel LED Driver with Diagnostics	Tape and Reel	24-pin SSOP
AS1110-BQFR	Constant-Current, 16-Channel LED Driver with Diagnostics	Tray	28-pin QFN (5x5mm)
AS1110-BQFT	Constant-Current, 16-Channel LED Driver with Diagnostics	Tape and Reel	28-pin QFN (5x5mm)

Copyrights

Copyright © 1997-2007, austriamicrosystems AG, Schloss Premstaetten, 8141 Unterpremstaetten, Austria-Europe. Trademarks Registered ®. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

All products and companies mentioned are trademarks or registered trademarks of their respective companies.

Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.



Contact Information

Headquarters

austriamicrosystems AG
A-8141 Schloss Premstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

<http://www.austriamicrosystems.com/contact>