National Semiconductor

MICROCIRCUIT DATA SHEET

MNLMH6624-X REV 1A0

Original Creation Date: 07/28/03
Last Update Date: 08/20/03
Last Major Revision Date: 08/19/03

ULTRA LOW NOISE WIDEBAND OP AMP

General Description

The LMH6624 combines a wide bandwidth (1.5GHz GBW) with very low input noise (092nV/SqRtHz, 2.3pA/SqRtHz) and ultra low dc errors (100uV Vos, ±0.1uV/ C drift) to provide a very precise operational amplifier with wide dynamic-range. This enables the user to achieve closed-loop gains of greater than 10.

The LMH6624's traditional voltage feedback topology provides the following benefits: balanced inputs, low offsets voltage and offset current, very low offset drift, 81dB open-loop gain, 95dB common mode rejection ratio, and 88dB power supply rejection ratio.

The LMH6624 operates from ±2.5V to ±6V in dual supply mode and from +5V to +12V in single supply configuration. The LMH6624 is stable for closed-loop gain of Av ≤ -10 or +10 ≤AV. LMH6624 is offered in SQT23-5 and SIOC-8 packages.

Industry Part Number

LMH6624

NS Part Numbers

LMH6624J-QML
LMH6624J-QMLV
LMH6624WG-QML
LMH6624WG-QMLV

Prime Die

LMH6624A

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 1.5GHz gain-bandwidth product
- 0,92nV/SqRtHz input voltage noise
- 800uV input offset voltage
- 350V/us slew rate
- 400V/us slew rate (Av = 10)
- -65dBc HD2 @ f = 10MHZ, Rl = 100 Ohms
- -80dBc HD3 @ f = 10MHZ, Rl = 100 Ohms
- ±2.5V to ±6V Supply voltage range (dual supply)
- ±5V to ±12V Supply voltage range (single supply)
- Improved replacement for the CLC425

CONTROLLING DOCUMENT:

LMH6624J-QML	5962-0254401QPA
LMH6624J-QMLV	5962-0254401VPA
LMH6624WG-QML	5962-0254401QZA
LMH6624WG-QMLV	5962-0254401VZA

Applications

- Instrumentation sense amplifiers
- Ultrasound pre-amps
- Magnetic tape & disk pre-amps
- Wide band active filters
- Professional audio systems
- Opto-electronics
- Medical diagnostic systems

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vs)	±6 Vdc
Common Mode Input Voltage (Vcm)	V+ - V-
Differential Input Voltage (Vin)	±1.2V
Maximum Power Dissipation (Pd) (Note 2)	1.0W
Lead Temperature (Soldering, 10 seconds)	+300 C
Junction Temperature (Tj)	+175 C
Storage Temperature Range	-65 C ≤ Ta ≤ +150 C
Thermal Resistance	
ThetaJa	
Junction-to-ambient	
CERAMIC DIP	
(Still Air Flow)	130 C/W
(500LF/Min Air Flow)	70 C/W
CERAMIC SOIC	
(Still Air Flow)	180 C/W
(500LF/Min Air Flow)	115 C/W
ThetaJC	
CERAMIC DIP	17 C/W
CERAMIC SOIC	20 C/W
Package Weight (Typical)	
CERAMIC DIP	1090mg
CERAMIC SOIC	220mg
ESD Tolerance (Note 3)	
ESD Rating	2000 V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated within the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) / ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100 pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vs)	±5Vdc
Ambient Operating Temperature Range (TA)	-55 C ≤ Ta ≤ +125 C

Electrical Characteristics

DC PARAMETERS: Static and DC Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5 Vdc, Av = +20, load resistance (Rl = 100 Ohms), feedback resistance (Rf) = 500 Ohms, and gain setting resistance (Rg) = 26.1 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iin	Input Bias Current				-20	+20	uA	1, 2, 3
Vio	Input Offset Voltage				-0.8	+0.8	mV	1
					-1	+1	mV	2, 3
Is	Supply Current	Rl = infinite				16	mA	1, 2
						18	mA	3
PSRR	Power Supply Rejection Ratio	+Vs = +4.0V to +5.0V, -Vs = -4.0V to -5.0V			75		dB	1, 2, 3
AOL	Open Loop Gain				77		dB	4
					72		dB	5, 6

AC PARAMETERS: Frequency Domain Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±5 Vdc, Av = +20, load resistance (Rl = 100 Ohms), feedback resistance (Rf) = 500 Ohms, and gain setting resistance (Rg) = 26.1 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SSBW	Small Signal Bandwidth	-3 dB bandwidth, Vout < 0.4 Vpp	2		75		MHz	9
GFP	Gain Flatness Peaking Low	0.1 MHz to 30 MHz, Vout ≤ 0.4 Vpp	2			0.7	dB	9
GFR	Gain Flatness Rolloff	0.1 MHz to 30 MHz, Vout ≤ 0.4 Vpp	2			1.0	dB	9

AC PARAMETERS: Distortion and Noise Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±5 Vdc, Av = +20, load resistance (Rl = 100 Ohms), feedback resistance (Rf) = 500 Ohms, and gain setting resistance (Rg) = 26.1 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

HD2	2nd Harmonic Distortion	1 Vpp at 10 MHz	2			-48	dBc	9
HD3	3rd Harmonic Distortion	1 Vpp at 10 MHz	2			-65	dBc	9

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: "Deltas not required on B-Level product. Deltas required for S-Level product at Group B5 ONLY, or as specified on the Internal Processing Instructions (IPI), (Note 3).

Iin	Input Bias Current		1		-0.2	+0.2	uA	1
Vio	Input Offset Voltage		1		-0.1	0.1	mV	1
Is	Supply Current		1		-1	+1	mA	1

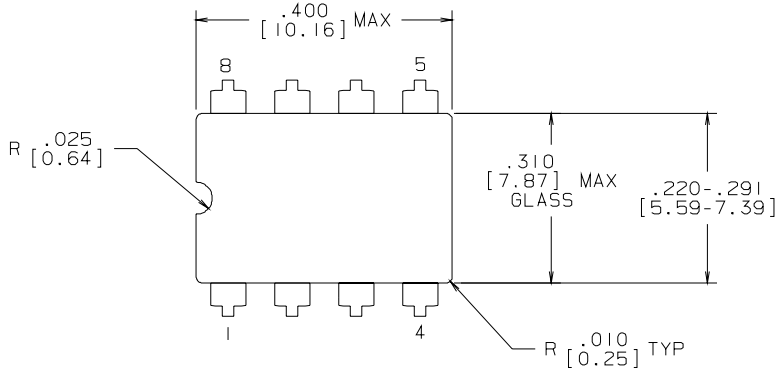
Note 1: If not tested, shall be guaranteed to the limits specified in table I herein.
Note 2: Group A testing only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as convential current flow out of a device terminal.

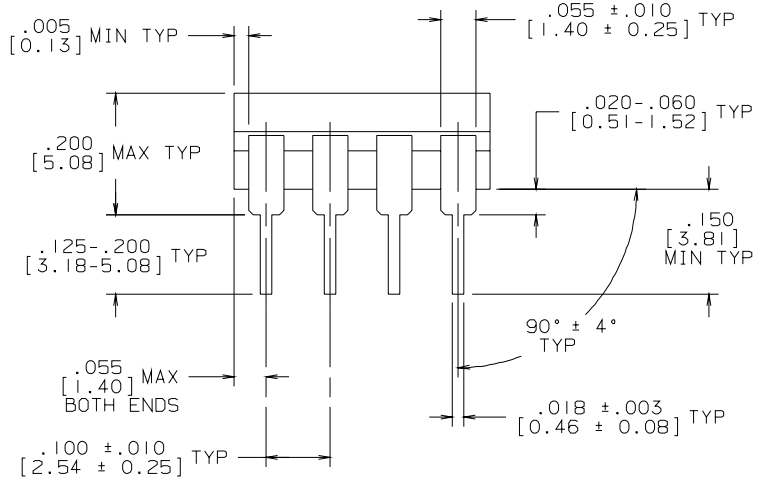
Graphics and Diagrams

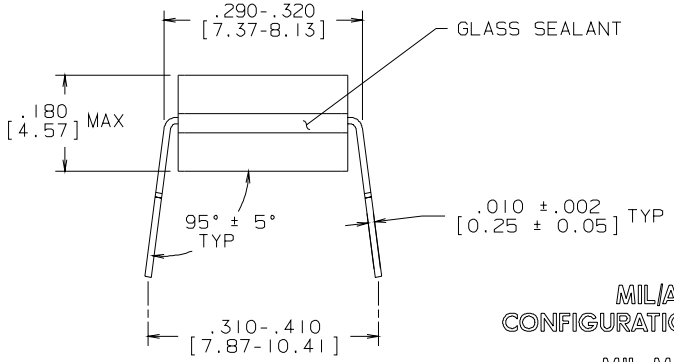
GRAPHICS#	DESCRIPTION
06402HRA2	CERAMIC SOIC (WG), 10 LEAD (B/I CKT)
07089HRA2	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000479A	CERDIP (J), 8 LEAD (PIN OUT)
P000483A	CERAMIC SOIC (WG), 10 LEAD (PIN OUT)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

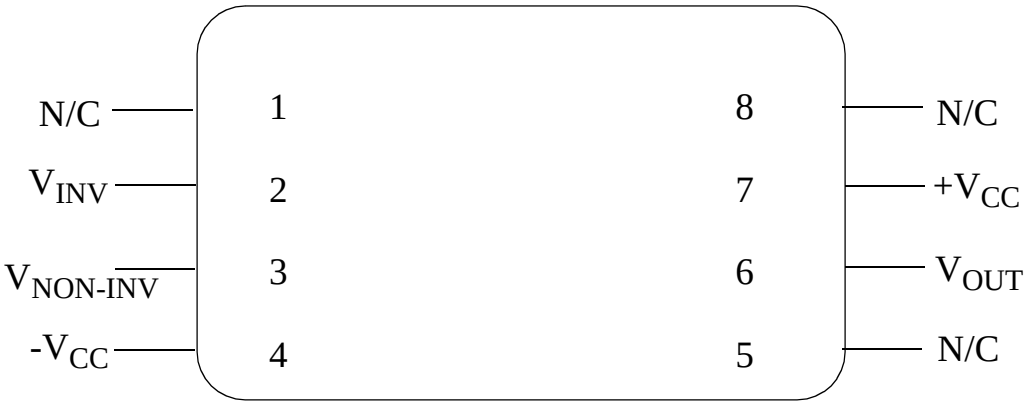
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LMH6624J

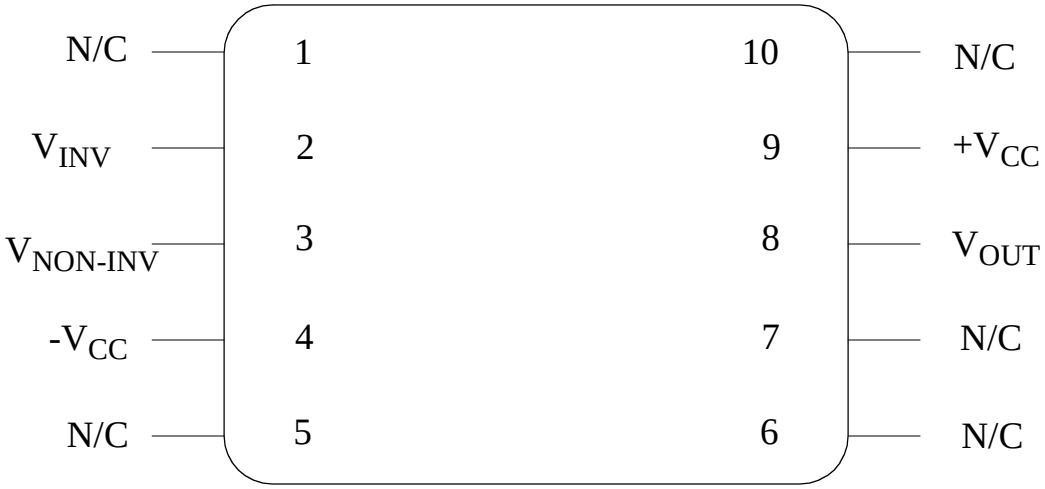
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000479A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LMH6624WG

10 - LEAD CERAMIC SOIC

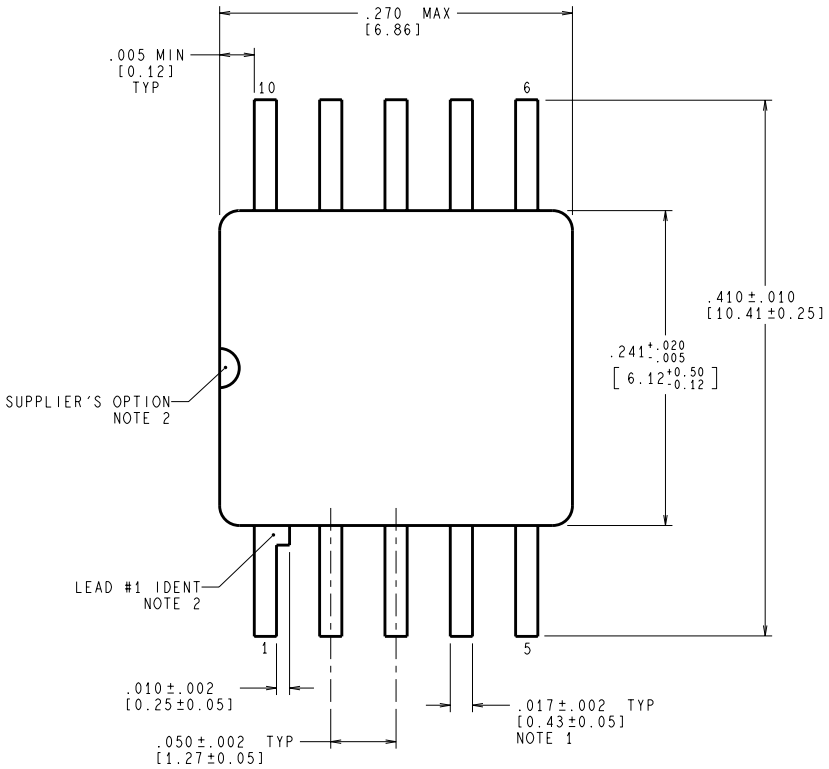
CONNECTION DIAGRAM

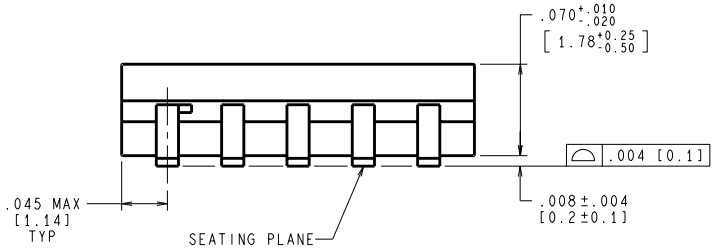
TOP VIEW

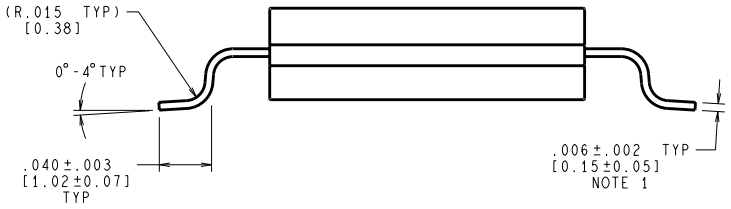
P000483A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK,
10 LEAD,
GULL WING

PROJECTION INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0004195	08/20/03	Rose Malone	Initial MDS Release: MNLMH6624-X, Rev. 0A0
1A0	M0004262	08/20/03	Rose Malone	Update MDS: MNLMH6624-X, Rev. 0A0 to MNLMH6624-X, Rev. 1A0. Changed Subgroups in AC Electrical Section from 4 to 9 for parameters SSBW, GFP, GFR, HD2, HD3.