FAIRCHILD SEMICONDUCTOR™

February 2001
Revised August 2001

74VCX32373
Low Voltage 32-Bit Transparent Latch with 3.6V Tolerant Inputs and Outputs (Preliminary)

General Description

The VCX32373 contains thirty-two non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear to be transparent to the data when the Latch enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state.

The 74VCX32373 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74VCX32373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD} (I_n to O_n)
  - 3.0 ns max for 3.0V to 3.6V V_{CC}
  - 3.4 ns max for 2.3V to 2.7V V_{CC}
  - 6.8 ns max for 1.65V to 1.95V V_{CC}
- Power-off high impedance inputs and outputs
- Support live insertion and withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
  - ±24 mA @ 3.0V V_{CC}
  - ±18 mA @ 2.3V V_{CC}
  - ±6 mA @ 1.65V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

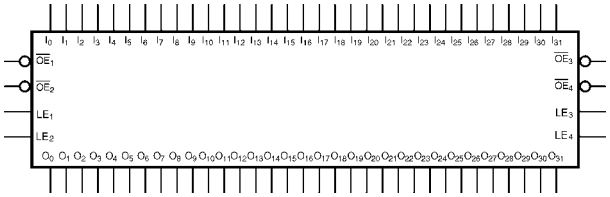
Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Ordering Number	Package Number	Package Description
74VCX32373GX (Note 2)	BGA96A	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]

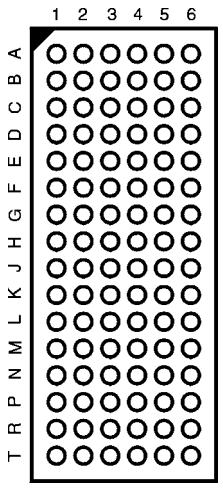
Note 2: BGA package available in Tape and Reel only.

Logic Symbol



Connection Diagram

Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
LE_n	Latch Enable Input
I_0–I_{31}	Inputs
O_0–O_{31}	Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_1	O_0	$\overline{OE}_1$	LE_1	I_0	I_1
B	O_3	O_2	GND	GND	I_2	I_3
C	O_5	O_4	V_{CC}	V_{CC}	I_4	I_5
D	O_7	O_6	GND	GND	I_6	I_7
E	O_9	O_8	GND	GND	I_8	I_9
F	O_{11}	O_{10}	V_{CC}	V_{CC}	I_{10}	I_{11}
G	O_{13}	O_{12}	GND	GND	I_{12}	I_{13}
H	O_{14}	O_{15}	$\overline{OE}_2$	LE_2	I_{15}	I_{14}
J	O_{17}	O_{16}	$\overline{OE}_3$	LE_3	I_{16}	I_{17}
K	O_{19}	O_{18}	GND	GND	I_{18}	I_{19}
L	O_{21}	O_{20}	V_{CC}	V_{CC}	I_{20}	I_{21}
M	O_{23}	O_{22}	GND	GND	I_{22}	I_{23}
N	O_{25}	O_{24}	GND	GND	I_{24}	I_{25}
P	O_{27}	O_{26}	V_{CC}	V_{CC}	I_{26}	I_{27}
R	O_{29}	O_{28}	GND	GND	I_{28}	I_{29}
T	O_{30}	O_{31}	$\overline{OE}_4$	LE_4	I_{31}	I_{30}

Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

Inputs			Outputs
LE_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)

Inputs			Outputs
LE_3	$\overline{OE}_3$	I_{16}–I_{23}	O_{16}–O_{23}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

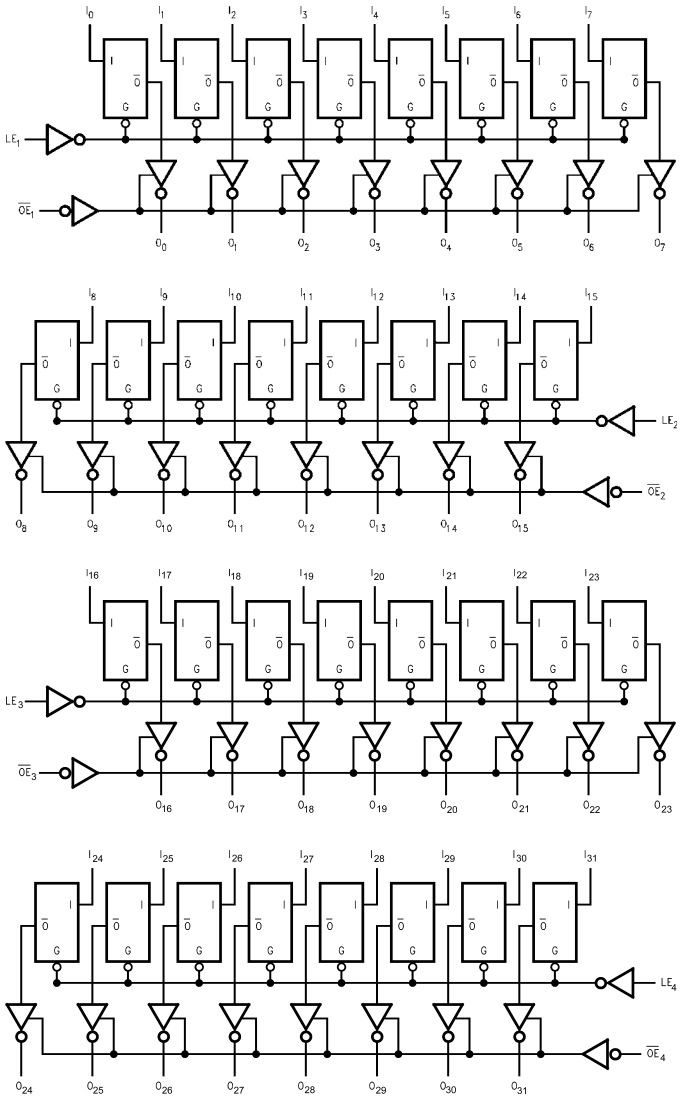
Inputs			Outputs
LE_4	$\overline{OE}_4$	I_{24}–I_{31}	O_{24}–O_{31}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

Z = High Impedance
O_0 = Previous O_0 before HIGH-to-LOW of Latch Enable

Functional Description

The 74VCX32373 contains thirty-two edge D-type latches with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 32-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the I_n enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its I input changes. When LE_n is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition on LE_n. The 3-STATE outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 3)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATED	−0.5V to +4.6V
Outputs Active (Note 4)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK}) V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 5)

Power Supply	
Operating	1.65V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	−0.3V to +3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in "OFF" State	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	±24 mA
V_{CC} = 2.3V to 2.7V	±18 mA
V_{CC} = 1.65V to 2.3V	±6 mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics ($2.7V < V_{CC} \leq 3.6V$)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 18 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6V	2.7–3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 3.6V V_I = V_{IH} or V_{IL}	2.7–3.6		±10	µA
I_{OFF}	Power-OFF Leakage Current	0 ≤ (V_I, V_O) ≤ 3.6V	0		10	µA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	µA
		V_{CC} ≤ (V_I, V_O) ≤ 3.6V (Note 6)	2.7–3.6		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		750	µA

Note 6: Outputs disabled or 3-STATE only.

DC Electrical Characteristics ($2.3V \le V_{CC} \le 2.7V$)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.6		V
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100 µA	2.3 – 2.7	V_{CC} – 0.2		V
		I_{OH} = –6 mA	2.3	2.0		V
		I_{OH} = –12 mA	2.3	1.8		V
		I_{OH} = –18 mA	2.3	1.7		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.3 – 2.7		0.2	V
		I_{OL} = 12 mA	2.3		0.4	V
		I_{OL} = 18 mA	2.3		0.6	V
I_I	Input Leakage Current	$0 \le V_I \le 3.6V$	2.3 – 2.7		±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0 \le V_O \le 3.6V$ $V_I = V_{IH}$ or V_{IL}	2.3 – 2.7		±10	µA
I_{OFF}	Power-OFF Leakage Current	$0 \le (V_I, V_O) \le 3.6V$	0		10	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 2.7		20	µA
		$V_{CC} \le (V_I, V_O) \le 3.6V$ (Note 7)	2.3 – 2.7		±20	µA

Note 7: Outputs disabled or 3-STATE only.

DC Electrical Characteristics ($1.65V \le V_{CC} < 2.3V$)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 2.3	$0.65 \times V_{CC}$		V
V_{IL}	LOW Level Input Voltage		1.65 - 2.3		$0.35 \times V_{CC}$	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100 µA	1.65 - 2.3	V_{CC} – 0.2		V
		I_{OH} = –6 mA	1.65	1.25		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	1.65 - 2.3		0.2	V
		I_{OL} = 6 mA	1.65		0.3	V
I_I	Input Leakage Current	$0 \le V_I \le 3.6V$	1.65 - 2.3		±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0 \le V_O \le 3.6V$ $V_I = V_{IH}$ or V_{IL}	1.65 - 2.3		±10	µA
I_{OFF}	Power-OFF Leakage Current	$0 \le (V_I, V_O) \le 3.6V$	0		10	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	1.65 - 2.3		20	µA
		$V_{CC} \le (V_I, V_O) \le 3.6V$ (Note 8)	1.65 – 2.3		±20	µA

Note 8: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 9)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 30$ pF, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay I_n to O_n	0.8	3.0	1.0	3.4	1.5	6.8	ns
t_{PHL}, t_{PLH}	Propagation Delay LE to O_n	0.8	3.0	1.0	3.9	1.5	7.8	ns
t_{PZL}, t_{PZH}	Output Enable Time	0.8	3.5	1.0	4.6	1.5	9.2	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	0.8	3.5	1.0	3.8	1.5	6.8	ns
t_S	Setup Time	1.5		1.5		2.5		ns
t_H	Hold Time	1.0		1.0		1.0		ns
t_W	Pulse Width	1.5		1.5		4.0		ns

Note 9: For $C_L = 50$pF, add approximately 300 ps to the AC maximum specification.

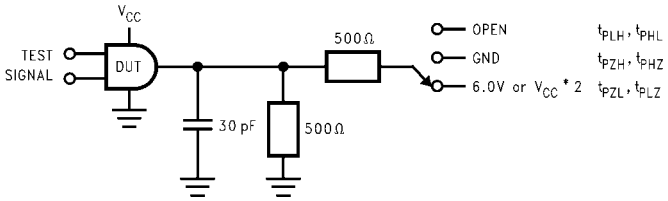
Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	−0.25	V
			2.5	−0.6	
			3.3	−0.8	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$ Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 1.8V$, 2.5V or 3.3V, $V_I = 0V$ or V_{CC}	6	pF
C_{OUT}	Output Capacitance	$V_I = 0V$ or V_{CC}, $V_{CC} = 1.8V$, 2.5V or 3.3V	7	pF
C_{PD}	Power Dissipation Capacitance	$V_I = 0V$ or V_{CC}, f = 10 MHz, $V_{CC} = 1.8V$, 2.5V or 3.3V	20	pF

AC Loading and Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V; V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V; 1.8V ± 0.15V
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit

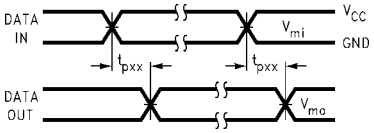


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

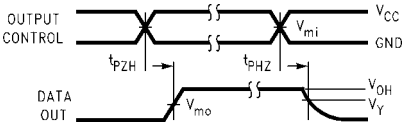


FIGURE 3. 3-STATE Output HIGH Enable and Disable Times for Low Voltage Logic

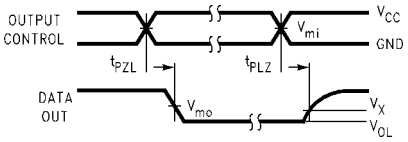


FIGURE 4. 3-STATE Output LOW Enable and Disable Times for Low Voltage Logic

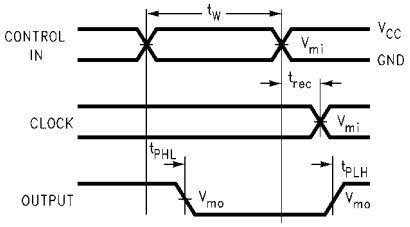


FIGURE 5. Propagation Delay, Pulse Width and t_{rec} Waveforms

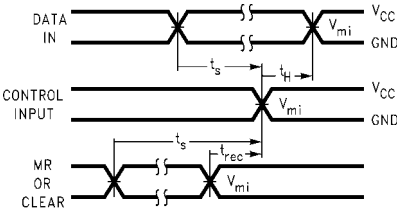
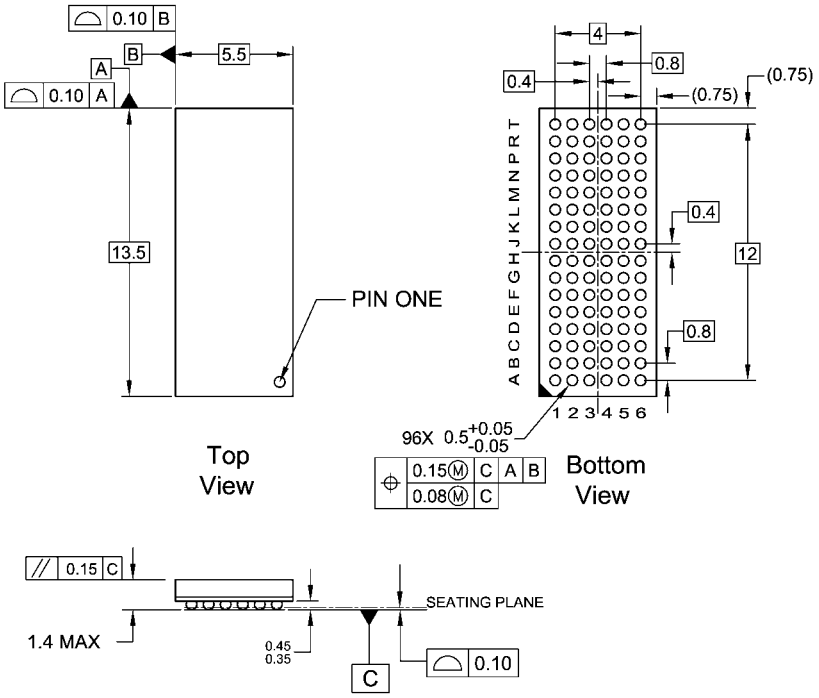


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	**2.5V ± 0.2V**	**1.8V ± 0.15V**
V_{mi}	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} +0.3V	V_{OL} +0.15V	V_{OL} +0.15V
V_Y	V_{OH} −0.3V	V_{OH} −0.15V	V_{OH} −0.15V

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA96ArevE

96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA96A

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