

## 74VCX16244

### Low Voltage 16-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs

#### General Description

The VCX16244 contains sixteen non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The 74VCX16244 is designed for low voltage (1.2V to 3.6V)  $V_{CC}$  applications with I/O capability up to 3.6V.

The 74VCX16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

- 1.2V to 3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- $t_{PD}$ 
  - 2.5 ns max for 3.0V to 3.6V  $V_{CC}$
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Static Drive ( $I_{OH}/I_{OL}$ )
  - $\pm 24$  mA @ 3.0V  $V_{CC}$
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

**Note 1:** To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

#### Ordering Code:

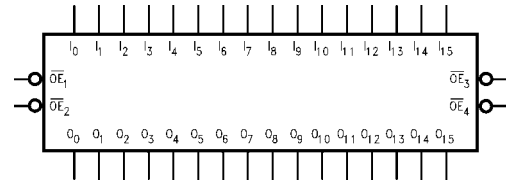
Order Number	Package Number	Package Description
74VCX16244G (Note 2)(Note 3)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74VCX16244MTD (Note 3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

**Note 2:** Ordering Code "G" indicates Tray.

**Note 3:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

74VCX16244 Low Voltage 16-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs

### Logic Symbol

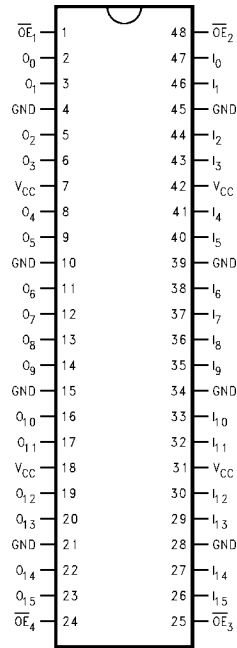


### Pin Descriptions

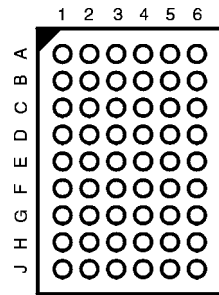
Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	Outputs
NC	No Connect

### Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

### FBGA Pin Assignments

	1	2	3	4	5	6
<b>A</b>	$O_0$	NC	$\overline{OE}_1$	$\overline{OE}_2$	NC	$I_0$
<b>B</b>	$O_2$	$O_1$	NC	NC	$I_1$	$I_2$
<b>C</b>	$O_4$	$O_3$	$V_{CC}$	$V_{CC}$	$I_3$	$I_4$
<b>D</b>	$O_6$	$O_5$	GND	GND	$I_5$	$I_6$
<b>E</b>	$O_8$	$O_7$	GND	GND	$I_7$	$I_8$
<b>F</b>	$O_{10}$	$O_9$	GND	GND	$I_9$	$I_{10}$
<b>G</b>	$O_{12}$	$O_{11}$	$V_{CC}$	$V_{CC}$	$I_{11}$	$I_{12}$
<b>H</b>	$O_{14}$	$O_{13}$	NC	NC	$I_{13}$	$I_{14}$
<b>J</b>	$O_{15}$	NC	$\overline{OE}_4$	$\overline{OE}_3$	NC	$I_{15}$

### Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$I_0-I_3$	$O_0-O_3$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	$I_8-I_{11}$	$O_8-O_{11}$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	$I_4-I_7$	$O_4-O_7$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	$I_{12}-I_{15}$	$O_{12}-O_{15}$
L	L	L
L	H	H
H	X	Z

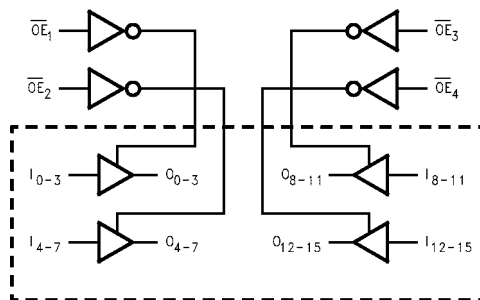
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial (HIGH or LOW, inputs may not float)  
 Z = High Impedance

## Functional Description

The 74VCX16244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE out-

puts are controlled by an Output Enable ( $\overline{OE}_n$ ) input. When  $\overline{OE}_n$  is LOW, the outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

## Logic Diagram



**Absolute Maximum Ratings** (Note 4)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_I$ )	-0.5V to +4.6V
Output Voltage ( $V_O$ )	
Outputs 3-STATED	-0.5V to +4.6V
Outputs Active (Note 5)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current	
( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or GND Current per	
Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

**Recommended Operating Conditions** (Note 6)

Power Supply	
Operating	1.2V to 3.6V
Input Voltage	-0.3V to +3.6V
Output Voltage ( $V_O$ )	
Output in Active States	0.0V to $V_{CC}$
Output in 3-State	0.0V to 3.6V
Output Current in $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to 3.6V	$\pm 24$ mA
$V_{CC} = 2.3V$ to 2.7V	$\pm 18$ mA
$V_{CC} = 1.65V$ to 2.3V	$\pm 6$ mA
$V_{CC} = 1.4V$ to 1.6V	$\pm 2$ mA
$V_{CC} = 1.2V$	$\pm 100$ $\mu$ A
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

**Note 4:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 5:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 6:** Floating or unused inputs must be held HIGH or LOW.

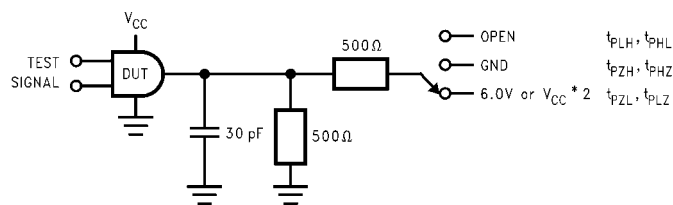
**DC Electrical Characteristics**

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	$0.65 \times V_{CC}$		
			1.4 - 1.6	$0.65 \times V_{CC}$		
			1.2	$0.65 \times V_{CC}$		
$V_{IL}$	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		$0.35 \times V_{CC}$	
			1.4 - 1.6		$0.35 \times V_{CC}$	
			1.2		$0.05 \times V_{CC}$	
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -12$ mA $I_{OH} = -18$ mA $I_{OH} = -24$ mA	2.7 - 3.6	$V_{CC} - 0.2$		V
			2.7	2.2		
			3.0	2.4		
			3.0	2.2		
		$I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA $I_{OH} = -12$ mA $I_{OH} = -18$ mA	2.3 - 2.7	$V_{CC} - 0.2$		
			2.3	2.0		
			2.3	1.8		
			2.3	1.7		
		$I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA	1.65 - 2.3	$V_{CC} - 0.2$		
			1.65	1.25		
		$I_{OH} = -100 \mu A$ $I_{OH} = -2$ mA	1.4 - 1.6	$V_{CC} - 0.2$		
			1.4	1.05		
		$I_{OH} = -100 \mu A$	1.2	$V_{CC} - 0.2$		

DC Electrical Characteristics (Continued)							
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Max	Units	
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	2.7 - 3.6		0.2	V	
		I <sub>OL</sub> = 12 mA	2.7		0.4		
		I <sub>OL</sub> = 18 mA	3.0		0.4		
		I <sub>OL</sub> = 24 mA	3.0		0.55		
		I <sub>OL</sub> = 100 μA	2.3 - 2.7		0.2		
		I <sub>OL</sub> = 12 mA	2.3		0.4		
		I <sub>OL</sub> = 18 mA	2.3		0.6		
		I <sub>OL</sub> = 100 μA	1.65 - 2.3		0.2		
		I <sub>OL</sub> = 6 mA	1.65		0.3		
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 3.6V	1.2 - 3.6		±5.0	μA	
		I <sub>OZ</sub>	3-STATE Output Leakage	0 ≤ V <sub>O</sub> ≤ 3.6V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	1.2 - 3.6		±10.0
I <sub>OFF1</sub>	Power-OFF Leakage Current	0 ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V	0		10.0	μA	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	1.2 - 3.6		20.0	μA	
		V <sub>CC</sub> ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V (Note 7)	1.2 - 3.6		±20.0		
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V	2.7 - 3.6		750	μA	
<b>Note 7:</b> Outputs disabled or 3-STATE only.							
AC Electrical Characteristics (Note 8)							
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Figure Number
				Min	Max		
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	0.8	2.5	ns	Figures 1, 2
			2.5 ± 0.2	1.0	3.0		
			1.8 ± 0.15	1.5	6.0		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2kΩ	1.5 ± 0.1	1.0	12.0	ns	Figures 5, 6
1.2	1.5	30.0					
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.1		
			1.8 ± 0.15	1.5	8.2		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2kΩ	1.5 ± 0.1	1.0	16.4	ns	Figures 5, 7, 8
1.2	1.5	41.0					
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	3.8		
			1.8 ± 0.15	1.5	6.8		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2kΩ	1.5 ± 0.1	1.0	13.6	ns	Figures 5, 7, 8
1.2	1.5	34.0					
t <sub>OSSL</sub> t <sub>OSLH</sub>	Output to Output Skew (Note 9)	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2kΩ	1.5 ± 0.1		1.5	ns	
1.2		1.5					
<b>Note 8:</b> For C <sub>L</sub> = 50pF, add approximately 300 ps to the AC maximum specification.							
<b>Note 9:</b> Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t <sub>OSSL</sub> ) or LOW-to-HIGH (t <sub>OSLH</sub> ).							

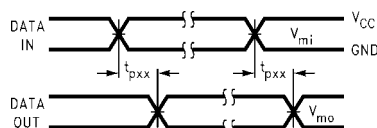
Dynamic Switching Characteristics					
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C	Units
				Typical	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8	-0.25	V
			2.5	-0.6	
			3.3	-0.8	
V <sub>OHV</sub>	Quiet Output Dynamic Valley V <sub>OH</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	
Capacitance					
Symbol	Parameter	Conditions	T <sub>A</sub> = +25°C		Units
			Typical		
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 1.8, 2.5V or 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	6.0		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	7.0		pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz, V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	20.0		pF

**AC Loading and Waveforms ( $V_{CC}$  3.3V ± 0.3V to 1.8V ± 0.15V)**

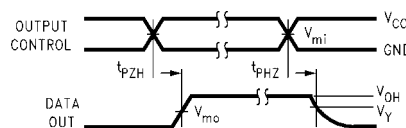


TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ ; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V; 1.8V \pm 0.15V$
$t_{PZH}, t_{PHZ}$	GND

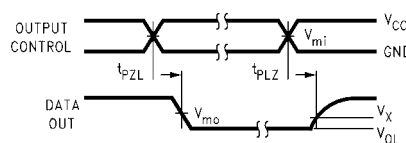
**FIGURE 1. AC Test Circuit**



**FIGURE 2. Waveform for Inverting and Non-Inverting Functions**



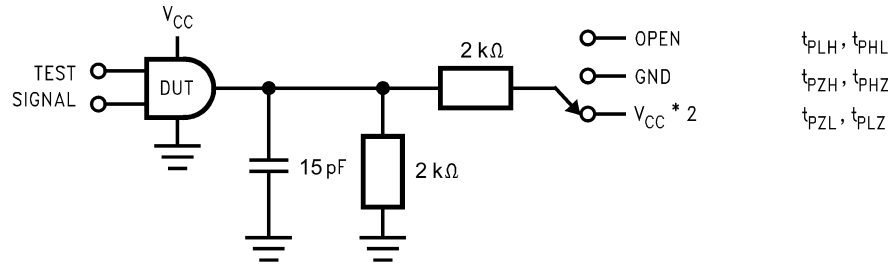
**FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**



**FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic**

Symbol	$V_{CC}$		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
$V_{mi}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_Y$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

AC Loading and Waveforms ( $V_{CC} 1.5 \pm 0.1V$  to  $1.2V$ )



TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	$V_{CC} \times 2$ at $V_{CC} = 1.5 \pm 0.1V$
$t_{PZH}, t_{PHZ}$	GND

FIGURE 5. AC Test Circuit

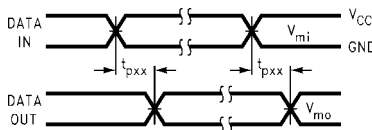


FIGURE 6. Waveform for Inverting and Non-Inverting Functions

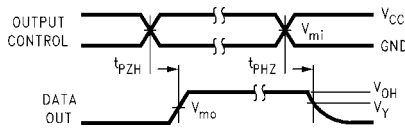


FIGURE 7. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

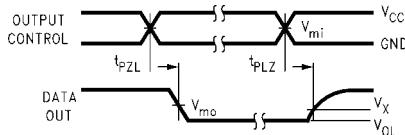
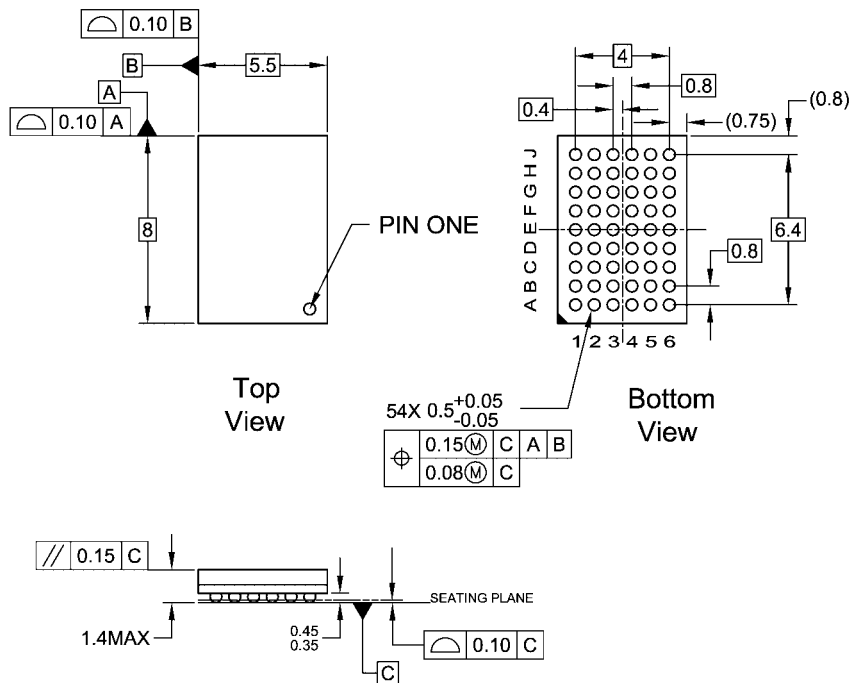


FIGURE 8. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	$V_{CC}$
	$1.5V \pm 0.1V$
$V_{mi}$	$V_{CC}/2$
$V_{mo}$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.1V$
$V_Y$	$V_{OH} - 0.1V$



**Physical Dimensions** inches (millimeters) unless otherwise noted



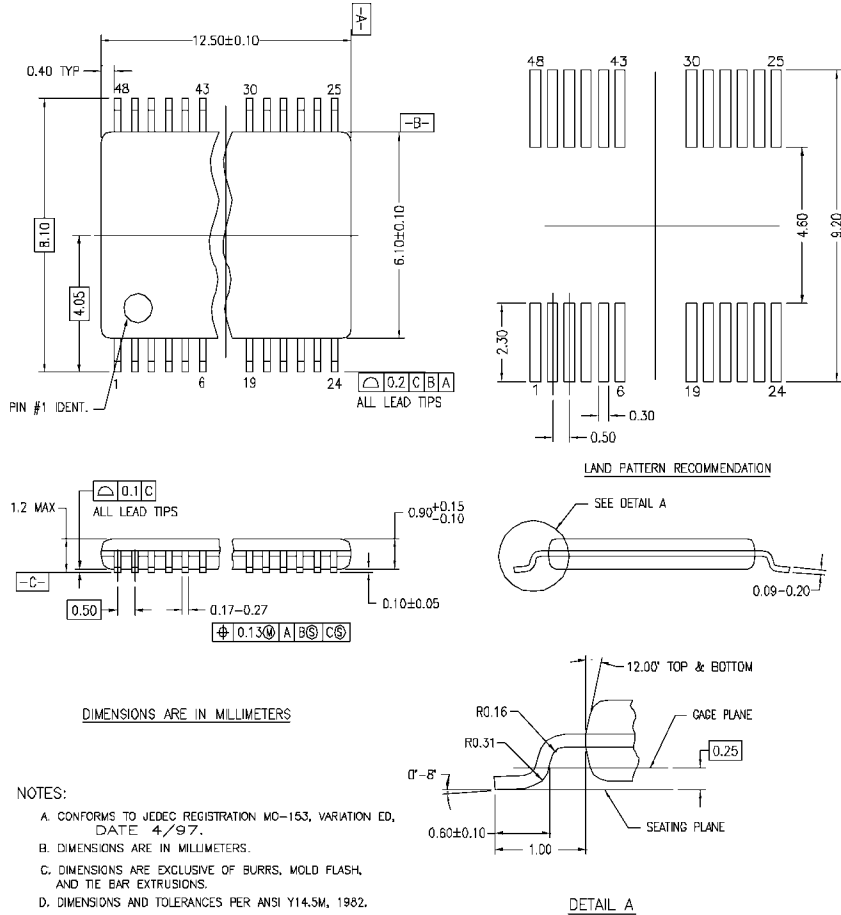
**NOTES:**

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide  
Package Number BGA54A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



MTD48REV C

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)