# CY7C1480V33
# CY7C1482V33
# CY7C1486V33

# 72-Mbit (2 M × 36/4 M × 18/1 M × 72) Pipelined Sync SRAM

## Features

- Supports bus operation up to 250 MHz
- Available speed grades are 250, 200, and 167 MHz
- Registered inputs and outputs for pipelined operation
- 3.3V core power supply
- 2.5V/3.3V I/O operation
- Fast clock-to-output times
  - 3.0 ns (for 250 MHz device)
- Provide high performance 3-1-1-1 access rate
- User selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed writes
- Asynchronous output enable
- Single cycle chip deselect
- CY7C1480V33, CY7C1482V33 available in JEDEC-standard Pb-free 100-pin TQFP, Pb-free and non-Pb-free 165-ball FBGA package. CY7C1486V33 available in Pb-free and non-Pb-free 209-ball FBGA package
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- "ZZ" Sleep Mode option

## Functional Description[1]

The CY7C1480V33/CY7C1482V33/CY7C1486V33 SRAM integrates 2 M × 36/4 M × 18/1 M × 72 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE}_1$), depth-expansion Chip Enables ($CE_2$ and $\overline{CE}_3$), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{BW}_X$, and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at the rising edge of the clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ($\overline{ADV}$).

Address, data inputs, and write controls are registered on-chip to initiate a self timed write cycle.This part supports byte write operations (see Pin Definitions on page 8 and Truth Table on page 11 for further details). Write cycles can be one to two or four bytes wide as controlled by the byte write control inputs. $\overline{GW}$ when active LOW causes all bytes to be written.

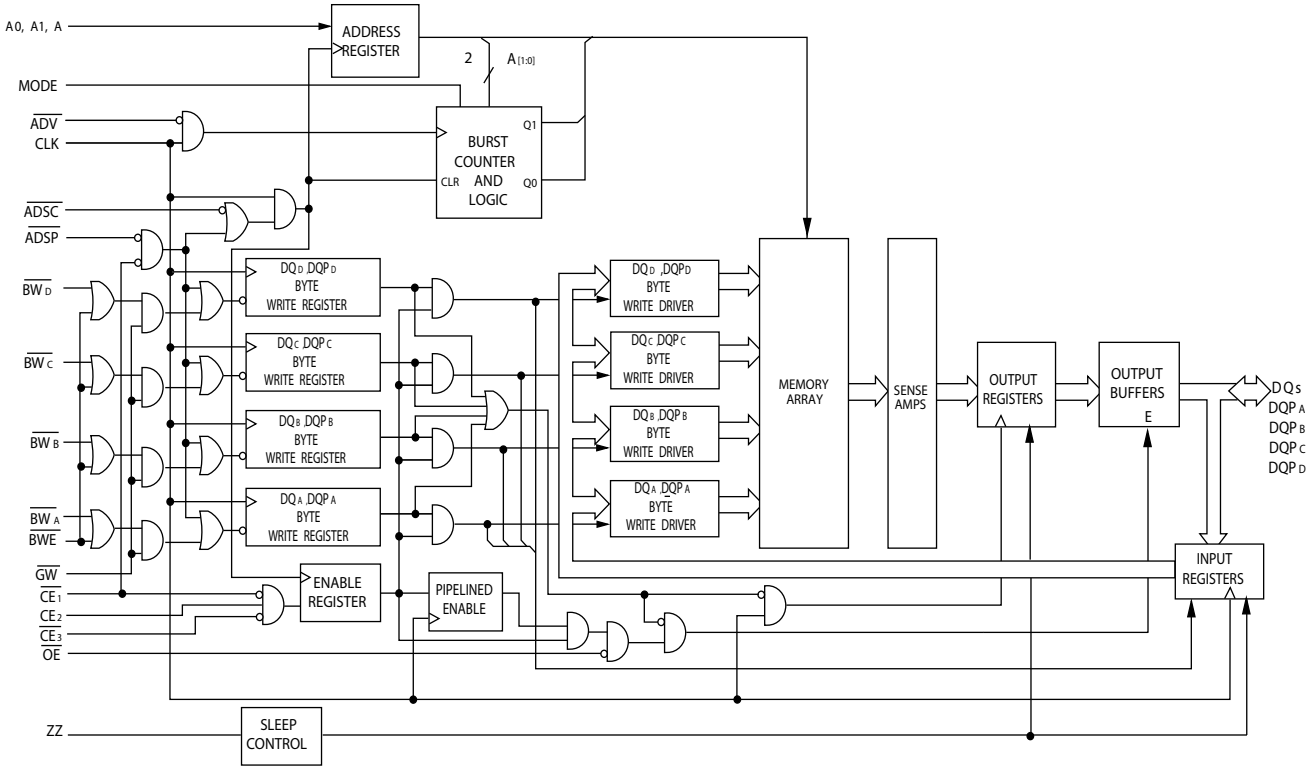
The CY7C1480V33/CY7C1482V33/CY7C1486V33 operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC standard JESD8-5 compatible.

## Selection Guide

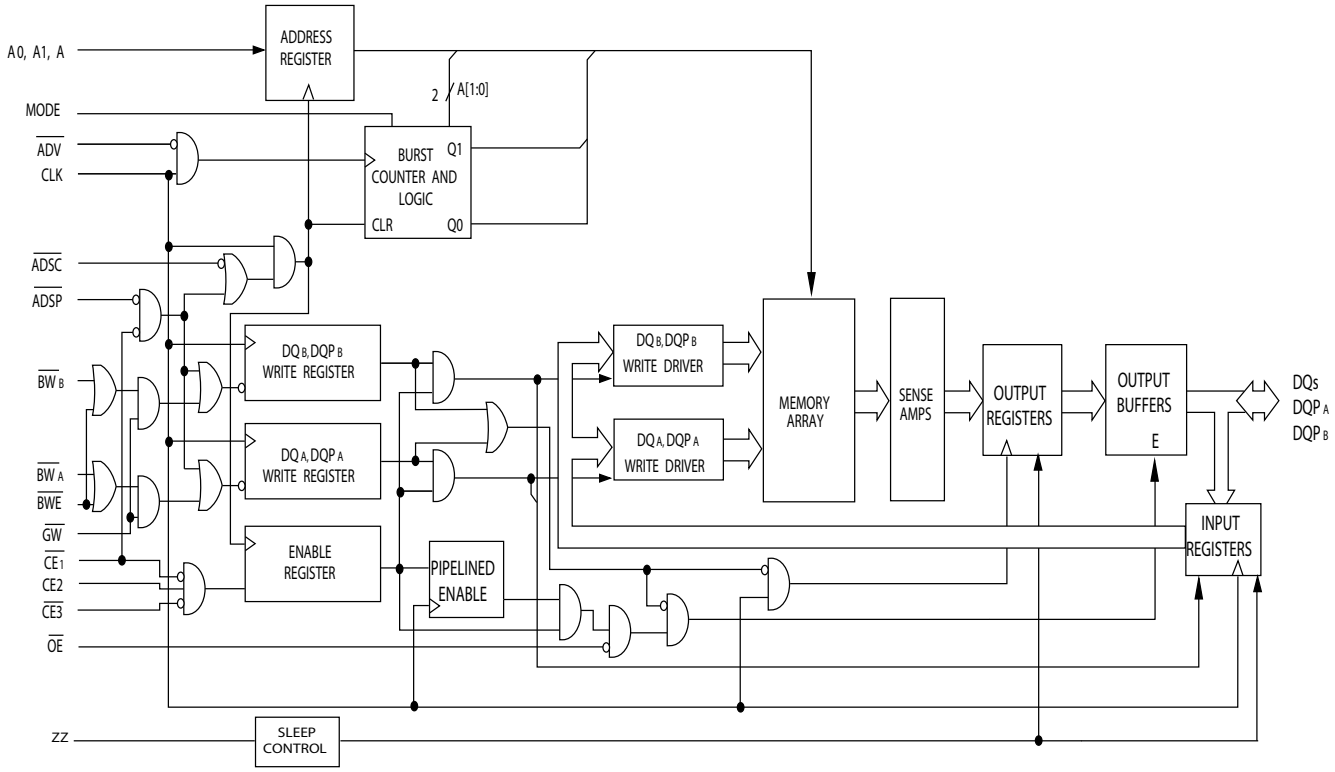
| | 250 MHz | 200 MHz | 167 MHz | Unit |
|---|---|---|---|---|
| Maximum Access Time | 3.0 | 3.0 | 3.4 | ns |
| Maximum Operating Current | 500 | 500 | 450 | mA |
| Maximum CMOS Standby Current | 120 | 120 | 120 | mA |

**Note**
1. For best practices recommendations, please refer to the Cypress application note AN1064, SRAM System Guidelines.

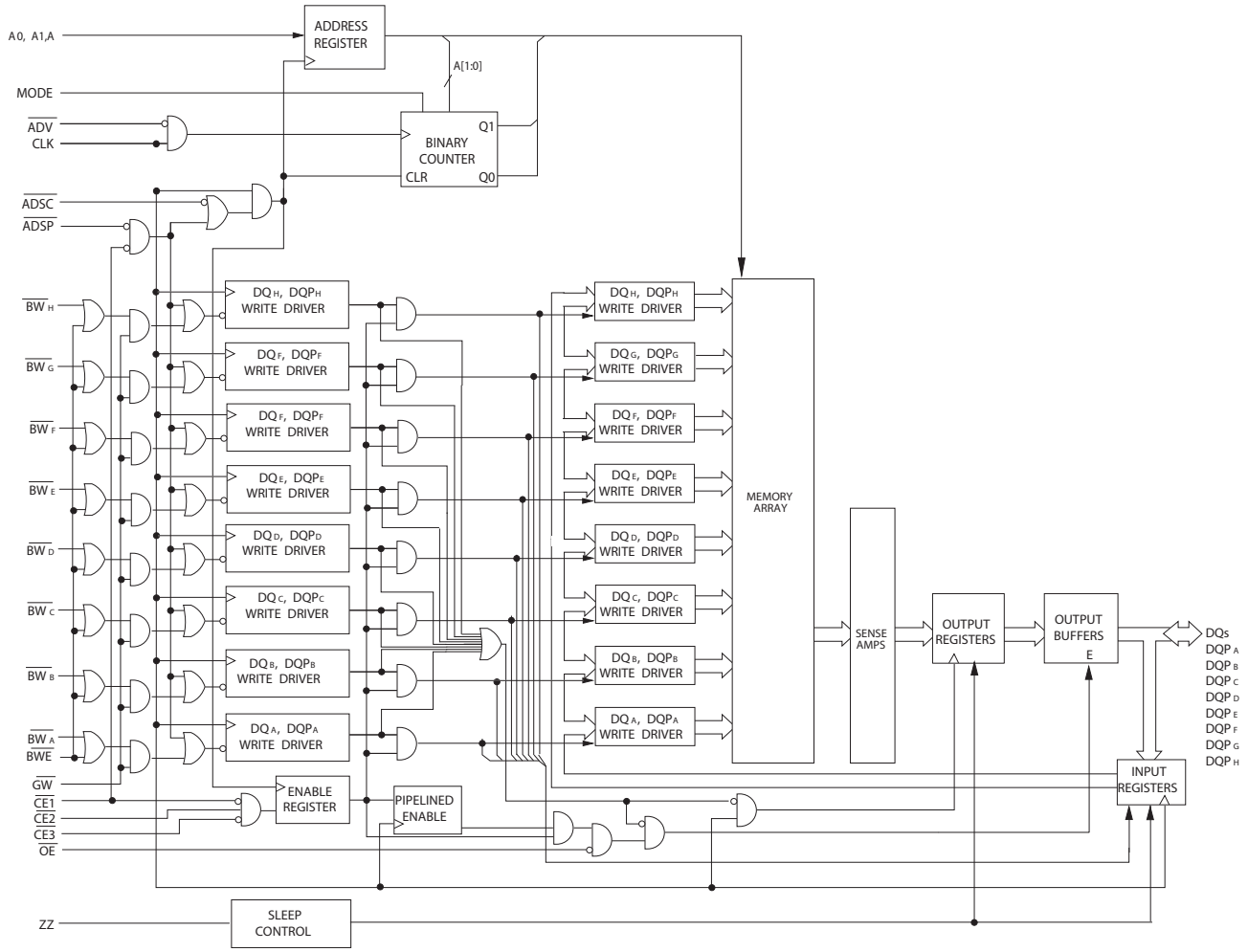
## Logic Block Diagram – CY7C1480V33 (2 M × 36)




## Logic Block Diagram – CY7C1482V33 (4 M × 18)



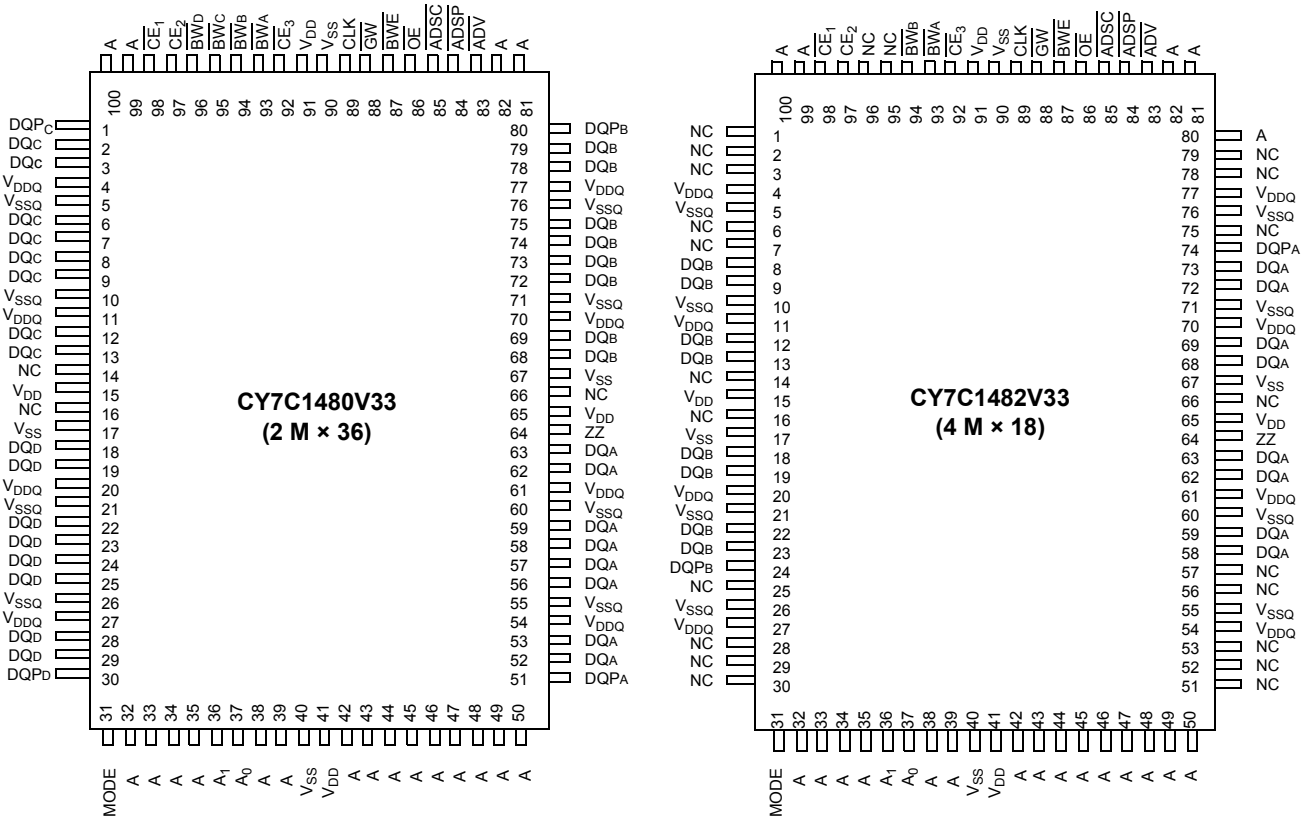
## Logic Block Diagram – CY7C1486V33 (1 M × 72)



## Contents

## Pin Configurations

### 100-pin TQFP Pinout



## Pin Configurations (continued)

### 165-ball FBGA (15 × 17 × 1.4 mm) Pinout

### CY7C1480V33 (2 M × 36)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | NC/288M | A | $\overline{CE}_1$ | $\overline{BW}_C$ | $\overline{BW}_B$ | $\overline{CE}_3$ | $\overline{BWE}$ | $\overline{ADSC}$ | $\overline{ADV}$ | A | NC |
| **B** | NC/144M | A | CE2 | $\overline{BW}_D$ | $\overline{BW}_A$ | CLK | $\overline{GW}$ | $\overline{OE}$ | $\overline{ADSP}$ | A | NC/576M |
| **C** | $DQP_C$ | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC/1G | $DQP_B$ |
| **D** | $DQ_C$ | $DQ_C$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_B$ | $DQ_B$ |
| **E** | $DQ_C$ | $DQ_C$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_B$ | $DQ_B$ |
| **F** | $DQ_C$ | $DQ_C$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_B$ | $DQ_B$ |
| **G** | $DQ_C$ | $DQ_C$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_B$ | $DQ_B$ |
| **H** | NC | NC | NC | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | NC | NC | ZZ |
| **J** | $DQ_D$ | $DQ_D$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_A$ | $DQ_A$ |
| **K** | $DQ_D$ | $DQ_D$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_A$ | $DQ_A$ |
| **L** | $DQ_D$ | $DQ_D$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_A$ | $DQ_A$ |
| **M** | $DQ_D$ | $DQ_D$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_A$ | $DQ_A$ |
| **N** | $DQP_D$ | NC | $V_{DDQ}$ | $V_{SS}$ | NC | A | NC | $V_{SS}$ | $V_{DDQ}$ | NC | $DQP_A$ |
| **P** | NC | A | A | A | TDI | A1 | TDO | A | A | A | A |
| **R** | MODE | A | A | A | TMS | A0 | TCK | A | A | A | A |

### CY7C1482V33 (4 M × 18)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | NC/288M | A | $\overline{CE}_1$ | $\overline{BW}_B$ | NC | $\overline{CE}_3$ | $\overline{BWE}$ | $\overline{ADSC}$ | $\overline{ADV}$ | A | A |
| **B** | NC/144M | A | CE2 | NC | $\overline{BW}_A$ | CLK | $\overline{GW}$ | $\overline{OE}$ | $\overline{ADSP}$ | A | NC/576M |
| **C** | NC | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC/1G | $DQP_A$ |
| **D** | NC | $DQ_B$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_A$ |
| **E** | NC | $DQ_B$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_A$ |
| **F** | NC | $DQ_B$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_A$ |
| **G** | NC | $DQ_B$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_A$ |
| **H** | NC | NC | NC | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | NC | NC | ZZ |
| **J** | $DQ_B$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_A$ | NC |
| **K** | $DQ_B$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_A$ | NC |
| **L** | $DQ_B$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_A$ | NC |
| **M** | $DQ_B$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_A$ | NC |
| **N** | $DQP_B$ | NC | $V_{DDQ}$ | $V_{SS}$ | NC | A | NC | $V_{SS}$ | $V_{DDQ}$ | NC | NC |
| **P** | NC | A | A | A | TDI | A1 | TDO | A | A | A | A |
| **R** | MODE | A | A | A | TMS | A0 | TCK | A | A | A | A |

## Pin Configurations (continued)

### 209-ball FBGA (14 × 22 × 1.76 mm) Pinout

### CY7C1486V33 (1 M × 72)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $DQ_G$ | $DQ_G$ | A | $CE_2$ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{CE_3}$ | A | $DQ_B$ | $DQ_B$ |
| **B** | $DQ_G$ | $DQ_G$ | $\overline{BWS_C}$ | $\overline{BWS_G}$ | NC/288M | $\overline{BWE}$ | A | $\overline{BWS_B}$ | $\overline{BWS_F}$ | $DQ_B$ | $DQ_B$ |
| **C** | $DQ_G$ | $DQ_G$ | $\overline{BWS_H}$ | $\overline{BWS_D}$ | NC/144M | $\overline{CE_1}$ | NC/576M | $\overline{BWS_E}$ | $\overline{BWS_A}$ | $DQ_B$ | $DQ_B$ |
| **D** | $DQ_G$ | $DQ_G$ | $V_{SS}$ | NC | NC/1G | $\overline{OE}$ | $\overline{GW}$ | NC | $V_{SS}$ | $DQ_B$ | $DQ_B$ |
| **E** | $DQP_G$ | $DQP_C$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $DQP_F$ | $DQP_B$ |
| **F** | $DQ_C$ | $DQ_C$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $DQ_F$ | $DQ_F$ |
| **G** | $DQ_C$ | $DQ_C$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $DQ_F$ | $DQ_F$ |
| **H** | $DQ_C$ | $DQ_C$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $DQ_F$ | $DQ_F$ |
| **J** | $DQ_C$ | $DQ_C$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $DQ_F$ | $DQ_F$ |
| **K** | NC | NC | CLK | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | NC | NC |
| **L** | $DQ_H$ | $DQ_H$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $DQ_A$ | $DQ_A$ |
| **M** | $DQ_H$ | $DQ_H$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $DQ_A$ | $DQ_A$ |
| **N** | $DQ_H$ | $DQ_H$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $DQ_A$ | $DQ_A$ |
| **P** | $DQ_H$ | $DQ_H$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | ZZ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $DQ_A$ | $DQ_A$ |
| **R** | $DQP_D$ | $DQP_H$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $DQP_A$ | $DQP_E$ |
| **T** | $DQ_D$ | $DQ_D$ | $V_{SS}$ | NC | NC | MODE | NC | NC | $V_{SS}$ | $DQ_E$ | $DQ_E$ |
| **U** | $DQ_D$ | $DQ_D$ | A | A | A | A | A | A | A | $DQ_E$ | $DQ_E$ |
| **V** | $DQ_D$ | $DQ_D$ | A | A | A | A1 | A | A | A | $DQ_E$ | $DQ_E$ |
| **W** | $DQ_D$ | $DQ_D$ | TMS | TDI | A | A0 | A | TDO | TCK | $DQ_E$ | $DQ_E$ |

## Pin Definitions

| Pin Name | I/O | Description |
|---|---|---|
| $A_0$, $A_1$, A | Input-Synchronous | **Address Inputs Used to Select One of the Address Locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, $CE_2$, and $\overline{CE}_3$ are sampled active. A1: A0 are fed to the two-bit counter. |
| $\overline{BW}_A$,$\overline{BW}_B$,$\overline{BW}_C$,$\overline{BW}_D$, $\overline{BW}_E$,$\overline{BW}_F$,$\overline{BW}_G$,$\overline{BW}_H$ | Input-Synchronous | **Byte Write Select Inputs, Active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK. |
| $\overline{GW}$ | Input-Synchronous | **Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW}_X$ and $\overline{BWE}$). |
| $\overline{BWE}$ | Input-Synchronous | **Byte Write Enable Input, Active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write. |
| CLK | Input-Clock | **Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW during a burst operation. |
| $\overline{CE}_1$ | Input-Synchronous | **Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $CE_2$ and $\overline{CE}_3$ to select or deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded. |
| $CE_2$ | Input-Synchronous | **Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device. $CE_2$ is sampled only when a new external address is loaded. |
| $\overline{CE}_3$ | Input-Synchronous | **Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $CE_2$ to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded. |
| $\overline{OE}$ | Input-Asynchronous | **Output Enable, Asynchronous Input, Active LOW**. Controls the direction of the IO pins. When LOW, the IO pins behave as outputs. When deasserted HIGH, IO pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state. |
| $\overline{ADV}$ | Input-Synchronous | **Advance Input Signal, Sampled on the Rising Edge of CLK, Active LOW**. When asserted, it automatically increments the address in a burst cycle. |
| $\overline{ADSP}$ | Input-Synchronous | **Address Strobe from Processor, Sampled on the Rising Edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH. |
| $\overline{ADSC}$ | Input-Synchronous | **Address Strobe from Controller, Sampled on the Rising Edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. |
| ZZ | Input-Asynchronous | **ZZ "Sleep" Input, Active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down. |
| DQs, DQPs | I/O-Synchronous | **Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and $DQP_X$ are placed in a tri-state condition. |
| $V_{DD}$ | Power Supply | **Power supply inputs to the core of the device**. |
| $V_{SS}$ | Ground | **Ground for the core of the device**. |
| $V_{SSQ}$[2] | IO Ground | **Ground for the I/O circuitry**. |
| $V_{DDQ}$ | IO Power Supply | **Power supply for the I/O circuitry**. |

**Note**
2. Applicable for TQFP package. For BGA package $V_{SS}$ serves as ground for the core and the IO circuitry.

## Pin Definitions (continued)

| Pin Name | I/O | Description |
|---|---|---|
| MODE | Input Static | **Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to $V_{DD}$ or left floating selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode Pin has an internal pull up. |
| TDO | JTAG Serial Output Synchronous | **Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not used, this pin must be disconnected. This pin is not available on TQFP packages. |
| TDI | JTAG Serial Input Synchronous | **Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to $V_{DD}$. This pin is not available on TQFP packages. |
| TMS | JTAG Serial Input Synchronous | **Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to $V_{DD}$. This pin is not available on TQFP packages. |
| TCK | JTAG Clock | **Clock input to the JTAG circuitry**. If the JTAG feature is not used, this pin must be connected to $V_{SS}$. This pin is not available on TQFP packages. |
| NC | – | **No Connects**. Not internally connected to the die. 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die. |

## Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ($t_{CO}$) is 3.0 ns (250 MHz device).

The CY7C1480V33/CY7C1482V33/CY7C1486V33 supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte Write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select ($BW_X$) inputs. A Global Write Enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($CE_1$, $CE_2$, $CE_3$) and an asynchronous Output Enable (OE) provide easy bank selection and output tri-state control. ADSP is ignored if $CE_1$ is HIGH.

### Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2) $CE_1$, $CE_2$, $CE_3$ are all asserted active, and (3) the write signals (GW, BWE) are all deasserted HIGH. ADSP is ignored if $CE_1$ is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the Address Register while being presented to the memory array. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 3.0 ns (250-MHz device) if OE is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the OE signal. Consecutive single read cycles are supported. After the SRAM is deselected at clock rise by the chip select and either ADSP or ADSC signals, its output tri-states immediately.

### Single Write Accesses Initiated by ADSP

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2) $CE_1$, $CE_2$, $CE_3$ are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The write signals (GW, BWE, and $BW_X$) and ADV inputs are ignored during this first cycle.

ADSP triggered write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the DQs inputs is written into the corresponding address location in the memory array. If GW is HIGH, then the write operation is controlled by BWE and $BW_X$ signals.

The CY7C1480V33/CY7C1482V33/CY7C1486V33 provides byte write capability that is described in the Truth Table for Read/Write on page 12. Asserting the Byte Write Enable input (BWE) with the selected Byte Write ($BW_X$) input, will selectively write to only the desired bytes. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because CY7C1480V33/CY7C1482V33/CY7C1486V33 is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQs inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a Write cycle is detected, regardless of the state of OE.

### Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ Write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3) $\overline{CE_1}$, $CE_2$, $\overline{CE_3}$ are all asserted active, and (4) the appropriate combination of the Write inputs (GW, $\overline{BWE}$, and $\overline{BW_X}$) are asserted active to conduct a Write to the desired byte(s). $\overline{ADSC}$-triggered Write accesses require a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The $\overline{ADV}$ input is ignored during this cycle. If a global Write is conducted, the data presented to the DQs is written into the corresponding address location in the memory core. If a Byte Write is conducted, only the selected bytes are written. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because CY7C1480V33/CY7C1482V33/CY7C1486V33 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQs inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a Write cycle is detected, regardless of the state of $\overline{OE}$.

### Burst Sequences

The CY7C1480V33/CY7C1482V33/CY7C1486V33 provides a two-bit wraparound counter, fed by A1: A0, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both Read and Write burst operations are supported.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected before entering the “sleep” mode. $\overline{CE_1}$, $CE_2$, $\overline{CE_3}$, ADSP, and $\overline{ADSC}$ must remain inactive for the duration of $t_{ZZREC}$ after the ZZ input returns LOW.

## Interleaved Burst Address Table (MODE = Floating or $V_{DD}$)

| First Address A1: A0 | Second Address A1: A0 | Third Address A1: A0 | Fourth Address A1: A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

## Linear Burst Address Table (MODE = GND)

| First Address A1: A0 | Second Address A1: A0 | Third Address A1: A0 | Fourth Address A1: A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 10 | 11 | 00 |
| 10 | 11 | 00 | 01 |
| 11 | 00 | 01 | 10 |

## ZZ Mode Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{DDZZ}$ | Sleep mode standby current | ZZ ≥ $V_{DD}$ – 0.2 V | – | 120 | mA |
| $t_{ZZS}$ | Device operation to ZZ | ZZ ≥ $V_{DD}$ – 0.2 V | – | $2t_{CYC}$ | ns |
| $t_{ZZREC}$ | ZZ recovery time | ZZ ≤ 0.2 V | $2t_{CYC}$ | – | ns |
| $t_{ZZI}$ | ZZ Active to Sleep current | This parameter is sampled | – | $2t_{CYC}$ | ns |
| $t_{RZZI}$ | ZZ Inactive to exit Sleep current | This parameter is sampled | 0 | – | ns |

## Truth Table

The Truth Table for CY7C1480V33, CY7C1482V33, and CY7C1486V33 follows.[3, 4, 5, 6, 7]

| Operation | Add. Used | $\overline{CE_1}$ | $CE_2$ | $\overline{CE_3}$ | ZZ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{WRITE}$ | $\overline{OE}$ | CLK | DQ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Deselect Cycle, Power Down | None | H | X | X | L | X | L | X | X | X | L–H | Tri-State |
| Deselect Cycle, Power Down | None | L | L | X | L | L | X | X | X | X | L–H | Tri-State |
| Deselect Cycle, Power Down | None | L | X | H | L | L | X | X | X | X | L–H | Tri-State |
| Deselect Cycle, Power Down | None | L | L | X | L | H | L | X | X | X | L–H | Tri-State |
| Deselect Cycle, Power Down | None | L | X | H | L | H | L | X | X | X | L–H | Tri-State |
| Sleep Mode, Power Down | None | X | X | X | H | X | X | X | X | X | X | Tri-State |
| READ Cycle, Begin Burst | External | L | H | L | L | L | X | X | X | L | L–H | Q |
| READ Cycle, Begin Burst | External | L | H | L | L | L | X | X | X | H | L–H | Tri-State |
| WRITE Cycle, Begin Burst | External | L | H | L | L | H | L | X | L | X | L–H | D |
| READ Cycle, Begin Burst | External | L | H | L | L | H | L | X | H | L | L–H | Q |
| READ Cycle, Begin Burst | External | L | H | L | L | H | L | X | H | H | L–H | Tri-State |
| READ Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | L | L–H | Q |
| READ Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | H | L–H | Tri-State |
| READ Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | L | L–H | Q |
| READ Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | H | L–H | Tri-State |
| WRITE Cycle, Continue Burst | Next | X | X | X | L | H | H | L | L | X | L–H | D |
| WRITE Cycle, Continue Burst | Next | H | X | X | L | X | H | L | L | X | L–H | D |
| READ Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | L | L–H | Q |
| READ Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | H | L–H | Tri-State |
| READ Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | L | L–H | Q |
| READ Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | H | L–H | Tri-State |
| WRITE Cycle,Suspend Burst | Current | X | X | X | L | H | H | H | L | X | L–H | D |
| WRITE Cycle,Suspend Burst | Current | H | X | X | L | X | H | H | L | X | L–H | D |

**Notes**
3. X = “Don't Care.” H = Logic HIGH, L = Logic LOW.
4. $\overline{WRITE}$ = L when any one or more Byte Write enable signals and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
5. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
6. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the ADSP or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH before the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a “don't care” for the remainder of the write cycle.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are Tri-State when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

## Truth Table for Read/Write

The following is a Truth Table for Read/Write for the CY7C1480V33.[8]

| Function | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BW_D}$ | $\overline{BW_C}$ | $\overline{BW_B}$ | $\overline{BW_A}$ |
|---|---|---|---|---|---|---|
| Read | H | H | X | X | X | X |
| Read | H | L | H | H | H | H |
| Write Byte A – ($DQ_A$ and $DQP_A$) | H | L | H | H | H | L |
| Write Byte B – ($DQ_B$ and $DQP_B$) | H | L | H | H | L | H |
| Write Bytes B, A | H | L | H | H | L | L |
| Write Byte C – ($DQ_C$ and $DQP_C$) | H | L | H | L | H | H |
| Write Bytes C, A | H | L | H | L | H | L |
| Write Bytes C, B | H | L | H | L | L | H |
| Write Bytes C, B, A | H | L | H | L | L | L |
| Write Byte D – ($DQ_D$ and $DQP_D$) | H | L | L | H | H | H |
| Write Bytes D, A | H | L | L | H | H | L |
| Write Bytes D, B | H | L | L | H | L | H |
| Write Bytes D, B, A | H | L | L | H | L | L |
| Write Bytes D, C | H | L | L | L | H | H |
| Write Bytes D, C, A | H | L | L | L | H | L |
| Write Bytes D, C, B | H | L | L | L | L | H |
| Write All Bytes | H | L | L | L | L | L |
| Write All Bytes | L | X | X | X | X | X |

## Truth Table for Read/Write

The following is a Truth Table for Read/Write for the CY7C1482V33.[8]

| Function | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BW_B}$ | $\overline{BW_A}$ |
|---|---|---|---|---|
| Read | H | H | X | X |
| Read | H | L | H | H |
| Write Byte A – ($DQ_A$ and $DQP_A$) | H | L | H | L |
| Write Byte B – ($DQ_B$ and $DQP_B$) | H | L | L | H |
| Write Bytes B, A | H | L | L | L |
| Write All Bytes | H | L | L | L |
| Write All Bytes | L | X | X | X |

**Note**
8. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.

## Truth Table for Read/Write

The following is a Truth Table for Read/Write for the CY7C1486V33.[9]

| Function | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BW_X}$ |
|---|---|---|---|
| Read | H | H | X |
| Read | H | L | All $\overline{BW}$ = H |
| Write Byte x – ($DQ_x$ and $DQP_x$) | H | L | L |
| Write All Bytes | H | L | All $\overline{BW}$ = L |
| Write All Bytes | L | X | X |

**Note**

9. $\overline{BW}$x represents any byte write signal $\overline{BW}$[0..7].To enable any byte write $\overline{BW}$x, a Logic LOW signal should be applied at clock rise. Any number of bye writes can be enabled at the same time for any given write.

## IEEE 1149.1 Serial Boundary Scan (JTAG)

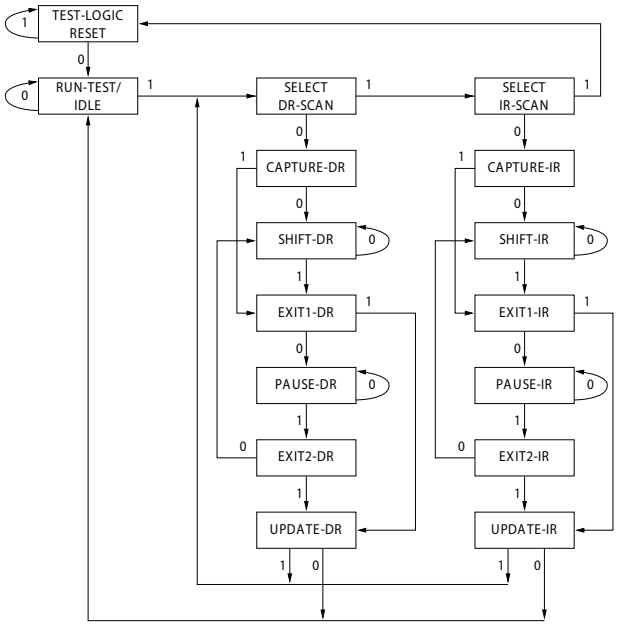
The CY7C1480V33/CY7C1482V33/CY7C1486V33 incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1480V33/CY7C1482V33/CY7C1486V33 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, tie TCK LOW ($V_{SS}$) to prevent device clocking. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to $V_{DD}$ through a pull up resistor. TDO must be left unconnected. At power up, the device comes up in a reset state, which will not interfere with the operation of the device.

## TAP Controller State Diagram




The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

### Test Access Port (TAP)

*Test Clock (TCK)*

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

*Test Mode Select (TMS)*

The TMS input gives commands to the TAP controller and is sampled on the rising edge of TCK. You can leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

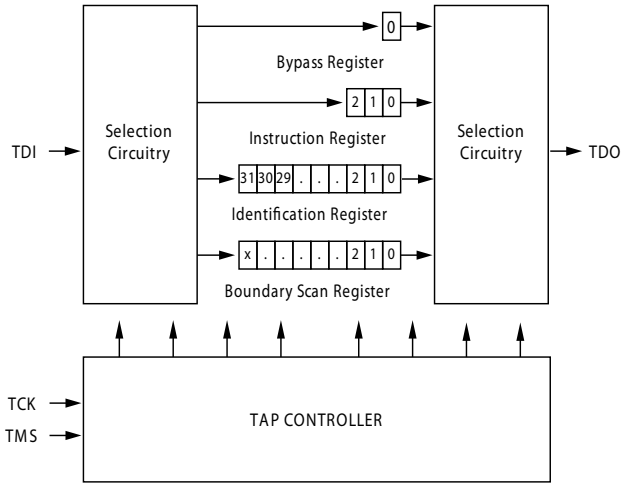
*Test Data-In (TDI)*

The TDI ball serially inputs information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information about loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See TAP Controller Block Diagram.)

*Test Data-Out (TDO)*

The TDO output ball serially clocks data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See TAP Controller State Diagram.)

## TAP Controller Block Diagram




### Performing a TAP Reset

Perform a RESET by forcing TMS HIGH ($V_{DD}$) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

### TAP Registers

Registers are connected between the TDI and TDO balls and enable data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

*Instruction Register*

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 14. At power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to enable fault isolation of the board-level serial test data path.

*Bypass Register*

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This enables data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ($V_{SS}$) when the BYPASS instruction is executed.

*Boundary Scan Register*

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. The ×36 configuration has a 73-bit-long register, and the ×18 configuration has a 54-bit-long register.

The boundary scan register is loaded with the contents of the RAM IO ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

*Identification (ID) Register*

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 17.

## TAP Instruction Set

*Overview*

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in Identification Codes on page 18. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the IO buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the IO ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

*EXTEST*

EXTEST is a mandatory 1149.1 instruction, which is to be executed whenever the instruction register is loaded with all zeros. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-zero instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High Z state.

*IDCODE*

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and enables the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register at power up or whenever the TAP controller is in a test logic reset state.

*SAMPLE Z*

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High Z state.

*SAMPLE/PRELOAD*

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

Be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output may undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that may be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller’s capture setup plus hold time ($t_{CS}$ plus $t_{CH}$).

The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

After the data is captured, the data can be shifted out by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that because the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction has the same effect as the Pause-DR command.

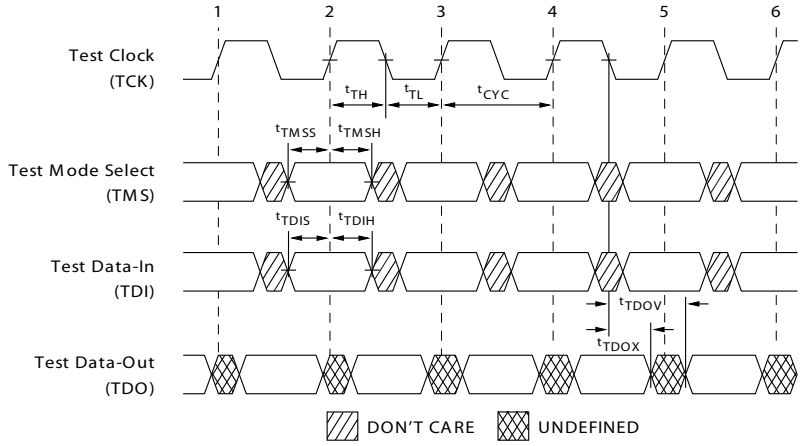
*BYPASS*

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

*Reserved*

These instructions are not implemented but are reserved for future use. Do not use these instructions.

## TAP Timing




## TAP AC Switching Characteristics

Over the Operating Range[10, 11]

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| **Clock** | | | | |
| $t_{TCYC}$ | TCK Clock Cycle Time | 50 | – | ns |
| $t_{TF}$ | TCK Clock Frequency | – | 20 | MHz |
| $t_{TH}$ | TCK Clock HIGH Time | 20 | – | ns |
| $t_{TL}$ | TCK Clock LOW Time | 20 | – | ns |
| **Output Times** | | | | |
| $t_{TDOV}$ | TCK Clock LOW to TDO Valid | – | 10 | ns |
| $t_{TDOX}$ | TCK Clock LOW to TDO Invalid | 0 | – | ns |
| **Setup Times** | | | | |
| $t_{TMSS}$ | TMS Setup to TCK Clock Rise | 5 | – | ns |
| $t_{TDIS}$ | TDI Setup to TCK Clock Rise | 5 | – | ns |
| $t_{CS}$ | Capture Setup to TCK Rise | 5 | – | ns |
| **Hold Times** | | | | |
| $t_{TMSH}$ | TMS Hold after TCK Clock Rise | 5 | – | ns |
| $t_{TDIH}$ | TDI Hold after Clock Rise | 5 | – | ns |
| $t_{CH}$ | Capture Hold after Clock Rise | 5 | – | ns |

**Notes**

10. $t_{CS}$ and $t_{CH}$ refer to the setup and hold time requirements of latching data from the boundary scan register.
11. Test conditions are specified using the load in TAP AC Test Conditions. $t_R/t_F$ = 1 ns.

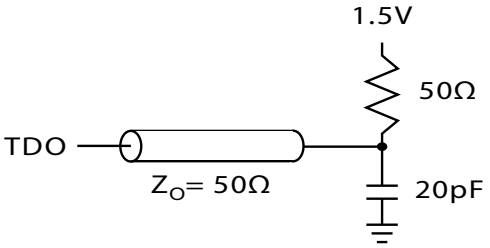
## 3.3 V TAP AC Test Conditions

Input pulse levels ..... $V_{SS}$ to 3.3 V
Input rise and fall times ..... 1 ns
Input timing reference levels ..... 1.5 V
Output reference levels ..... 1.5 V
Test load termination supply voltage ..... 1.5 V

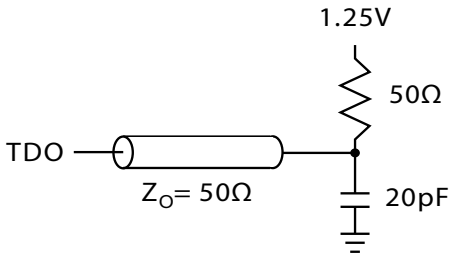
## 2.5 V TAP AC Test Conditions

Input pulse levels ..... $V_{SS}$ to 2.5 V
Input rise and fall time ..... 1 ns
Input timing reference levels ..... 1.25 V
Output reference levels ..... 1.25 V
Test load termination supply voltage ..... 1.25 V

## 3.3 V TAP AC Output Load Equivalent




## 2.5 V TAP AC Output Load Equivalent




## TAP DC Electrical Characteristics and Operating Conditions

(0 °C < $T_A$ < +70 °C; $V_{DD}$ = 3.135 to 3.6 V unless otherwise noted)[12]

| Parameter | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH1}$ | Output HIGH Voltage | $I_{OH}$ = –4.0 mA, $V_{DDQ}$ = 3.3 V | | 2.4 | – | V |
| | | $I_{OH}$ = –1.0 mA, $V_{DDQ}$ = 2.5 V | | 2.0 | – | V |
| $V_{OH2}$ | Output HIGH Voltage | $I_{OH}$ = –100 µA | $V_{DDQ}$ = 3.3 V | 2.9 | – | V |
| | | | $V_{DDQ}$ = 2.5 V | 2.1 | – | V |
| $V_{OL1}$ | Output LOW Voltage | $I_{OL}$ = 8.0 mA | $V_{DDQ}$ = 3.3 V | – | 0.4 | V |
| | | $I_{OL}$ = 1.0 mA | $V_{DDQ}$ = 2.5 V | – | 0.4 | V |
| $V_{OL2}$ | Output LOW Voltage | $I_{OL}$ = 100 µA | $V_{DDQ}$ = 3.3 V | – | 0.2 | V |
| | | | $V_{DDQ}$ = 2.5 V | – | 0.2 | V |
| $V_{IH}$ | Input HIGH Voltage | | $V_{DDQ}$ = 3.3 V | 2.0 | $V_{DD}$ + 0.3 | V |
| | | | $V_{DDQ}$ = 2.5 V | 1.7 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | $V_{DDQ}$ = 3.3 V | –0.3 | 0.8 | V |
| | | | $V_{DDQ}$ = 2.5 V | –0.3 | 0.7 | V |
| $I_X$ | Input Load Current | GND ≤ $V_{IN}$ ≤ $V_{DDQ}$ | | –5 | 5 | µA |

## Identification Register Definitions

| Instruction Field | CY7C1480V33 (2 M × 36) | CY7C1482V33 (4 M × 18) | CY7C1486V33 (1 M × 72) | Description |
|---|---|---|---|---|
| Revision Number (31:29) | 000 | 000 | 000 | Describes the version number |
| Device Depth (28:24) | 01011 | 01011 | 01011 | Reserved for internal use |
| Architecture/Memory Type(23:18) | 000000 | 000000 | 000000 | Defines memory type and architecture |
| Bus Width/Density(17:12) | 100100 | 010100 | 110100 | Defines width and density |
| Cypress JEDEC ID Code (11:1) | 00000110100 | 00000110100 | 00000110100 | Enables unique identification of SRAM vendor |
| ID Register Presence Indicator (0) | 1 | 1 | 1 | Indicates the presence of an ID register |

**Notes**
12. All voltages referenced to $V_{SS}$ (GND).

## Scan Register Sizes

| Register Name | Bit Size (× 36) | Bit Size (× 18) | Bit Size (× 72) |
|---|---|---|---|
| Instruction | 3 | 3 | 3 |
| Bypass | 1 | 1 | 1 |
| ID | 32 | 32 | 32 |
| Boundary Scan Order – 165-ball FBGA | 73 | 54 | – |
| Boundary Scan Order – 209-ball BGA | – | – | 112 |

## Identification Codes

| Instruction | Code | Description |
|---|---|---|
| EXTEST | 000 | Captures the IO ring contents. |
| IDCODE | 001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations. |
| SAMPLE Z | 010 | Captures IO ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state. |
| RESERVED | 011 | Do Not Use: This instruction is reserved for future use. |
| SAMPLE/PRELOAD | 100 | Captures IO ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. |
| RESERVED | 101 | Do Not Use: This instruction is reserved for future use. |
| RESERVED | 110 | Do Not Use: This instruction is reserved for future use. |
| BYPASS | 111 | Places the bypass register between TDI and TDO. This operation does not affect SRAM operations. |

## Boundary Scan Exit Order (2 M × 36)

| Bit # | 165-ball ID | Bit # | 165-ball ID | Bit # | 165-ball ID | Bit # | 165-ball ID |
|---|---|---|---|---|---|---|---|
| 1 | C1 | 21 | R3 | 41 | L10 | 61 | B8 |
| 2 | D1 | 22 | P2 | 42 | K11 | 62 | A7 |
| 3 | E1 | 23 | R4 | 43 | J11 | 63 | B7 |
| 4 | D2 | 24 | P6 | 44 | K10 | 64 | B6 |
| 5 | E2 | 25 | R6 | 45 | J10 | 65 | A6 |
| 6 | F1 | 26 | N6 | 46 | H11 | 66 | B5 |
| 7 | G1 | 27 | P11 | 47 | G11 | 67 | A5 |
| 8 | F2 | 28 | R8 | 48 | F11 | 68 | A4 |
| 9 | G2 | 29 | P3 | 49 | E11 | 69 | B4 |
| 10 | J1 | 30 | P4 | 50 | D10 | 70 | B3 |
| 11 | K1 | 31 | P8 | 51 | D11 | 71 | A3 |
| 12 | L1 | 32 | P9 | 52 | C11 | 72 | A2 |
| 13 | J2 | 33 | P10 | 53 | G10 | 73 | B2 |
| 14 | M1 | 34 | R9 | 54 | F10 | | |
| 15 | N1 | 35 | R10 | 55 | E10 | | |
| 16 | K2 | 36 | R11 | 56 | A10 | | |
| 17 | L2 | 37 | N11 | 57 | B10 | | |
| 18 | M2 | 38 | M11 | 58 | A9 | | |
| 19 | R1 | 39 | L11 | 59 | B9 | | |
| 20 | R2 | 40 | M10 | 60 | A8 | | |

## Boundary Scan Exit Order (4 M × 18)

| Bit # | 165-ball ID | Bit # | 165-ball ID | Bit # | 165-ball ID |
|---|---|---|---|---|---|
| 1 | D2 | 19 | R8 | 37 | C11 |
| 2 | E2 | 20 | P3 | 38 | A11 |
| 3 | F2 | 21 | P4 | 39 | A10 |
| 4 | G2 | 22 | P8 | 40 | B10 |
| 5 | J1 | 23 | P9 | 41 | A9 |
| 6 | K1 | 24 | P10 | 42 | B9 |
| 7 | L1 | 25 | R9 | 43 | A8 |
| 8 | M1 | 26 | R10 | 44 | B8 |
| 9 | N1 | 27 | R11 | 45 | A7 |
| 10 | R1 | 28 | M10 | 46 | B7 |
| 11 | R2 | 29 | L10 | 47 | B6 |
| 12 | R3 | 30 | K10 | 48 | A6 |
| 13 | P2 | 31 | J10 | 49 | B5 |
| 14 | R4 | 32 | H11 | 50 | A4 |
| 15 | P6 | 33 | G11 | 51 | B3 |
| 16 | R6 | 34 | F11 | 52 | A3 |
| 17 | N6 | 35 | E11 | 53 | A2 |
| 18 | P11 | 36 | D11 | 54 | B2 |

## Boundary Scan Exit Order (1 M × 72)

| Bit # | 209-ball ID | Bit # | 209-ball ID | Bit # | 209-ball ID | Bit # | 209-ball ID |
|---|---|---|---|---|---|---|---|
| 1 | A1 | 29 | T1 | 57 | V10 | 85 | C11 |
| 2 | A2 | 30 | T2 | 58 | U11 | 86 | C10 |
| 3 | B1 | 31 | U1 | 59 | U10 | 87 | B11 |
| 4 | B2 | 32 | U2 | 60 | T11 | 88 | B10 |
| 5 | C1 | 33 | V1 | 61 | T10 | 89 | A11 |
| 6 | C2 | 34 | V2 | 62 | R11 | 90 | A10 |
| 7 | D1 | 35 | W1 | 63 | R10 | 91 | A9 |
| 8 | D2 | 36 | W2 | 64 | P11 | 92 | U8 |
| 9 | E1 | 37 | T6 | 65 | P10 | 93 | A7 |
| 10 | E2 | 38 | V3 | 66 | N11 | 94 | A5 |
| 11 | F1 | 39 | V4 | 67 | N10 | 95 | A6 |
| 12 | F2 | 40 | U4 | 68 | M11 | 96 | D6 |
| 13 | G1 | 41 | W5 | 69 | M10 | 97 | B6 |
| 14 | G2 | 42 | V6 | 70 | L11 | 98 | D7 |
| 15 | H1 | 43 | W6 | 71 | L10 | 99 | K3 |
| 16 | H2 | 44 | U3 | 72 | P6 | 100 | A8 |
| 17 | J1 | 45 | U9 | 73 | J11 | 101 | B4 |
| 18 | J2 | 46 | V5 | 74 | J10 | 102 | B3 |
| 19 | L1 | 47 | U5 | 75 | H11 | 103 | C3 |
| 20 | L2 | 48 | U6 | 76 | H10 | 104 | C4 |
| 21 | M1 | 49 | W7 | 77 | G11 | 105 | C8 |
| 22 | M2 | 50 | V7 | 78 | G10 | 106 | C9 |
| 23 | N1 | 51 | U7 | 79 | F11 | 107 | B9 |
| 24 | N2 | 52 | V8 | 80 | F10 | 108 | B8 |
| 25 | P1 | 53 | V9 | 81 | E10 | 109 | A4 |
| 26 | P2 | 54 | W11 | 82 | E11 | 110 | C6 |
| 27 | R2 | 55 | W10 | 83 | D11 | 111 | B7 |
| 28 | R1 | 56 | V11 | 84 | D10 | 112 | A3 |

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on $V_{DD}$ Relative to GND .....–0.3 V to +4.6 V

Supply Voltage on $V_{DDQ}$ Relative to GND .... –0.3 V to +$V_{DD}$

DC Voltage Applied to Outputs in Tri-State .....–0.5 V to $V_{DDQ}$ + 0.5 V

DC Input Voltage .....–0.5 V to $V_{DD}$ + 0.5 V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001 V (MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0 °C to +70 °C | 3.3 V – 5% / + 10% | 2.5 V – 5% to $V_{DD}$ |
| Industrial | –40 °C to +85 °C | | |

## Electrical Characteristics

Over the Operating Range[13, 14]

| Parameter | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | | 3.135 | 3.6 | V |
| $V_{DDQ}$ | IO Supply Voltage | For 3.3 V IO | | 3.135 | $V_{DD}$ | V |
| | | For 2.5 V IO | | 2.375 | 2.625 | V |
| $V_{OH}$ | Output HIGH Voltage | For 3.3 V IO, $I_{OH}$ = –4.0 mA | | 2.4 | – | V |
| | | For 2.5 V IO, $I_{OH}$ = –1.0 mA | | 2.0 | – | V |
| $V_{OL}$ | Output LOW Voltage | For 3.3 V IO, $I_{OL}$ = 8.0 mA | | – | 0.4 | V |
| | | For 2.5 V IO, $I_{OL}$ = 1.0 mA | | – | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage[13] | For 3.3 V IO | | 2.0 | $V_{DD}$ + 0.3 V | V |
| | | For 2.5 V IO | | 1.7 | $V_{DD}$ + 0.3 V | V |
| $V_{IL}$ | Input LOW Voltage[13] | For 3.3 V IO | | –0.3 | 0.8 | V |
| | | For 2.5 V IO | | –0.3 | 0.7 | V |
| $I_X$ | Input Leakage Current except ZZ and MODE | GND ≤ $V_I$ ≤ $V_{DDQ}$ | | –5 | 5 | µA |
| | Input Current of MODE | Input = $V_{SS}$ | | –30 | – | µA |
| | | Input = $V_{DD}$ | | – | 5 | µA |
| | Input Current of ZZ | Input = $V_{SS}$ | | –5 | – | µA |
| | | Input = $V_{DD}$ | | – | 30 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_I$ ≤ $V_{DDQ}$, Output Disabled | | –5 | 5 | µA |
| $I_{DD}$ | $V_{DD}$ Operating Supply Current | $V_{DD}$ = Max, $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{CYC}$ | 4.0-ns cycle, 250 MHz | – | 500 | mA |
| | | | 5.0-ns cycle, 200 MHz | – | 500 | mA |
| | | | 6.0-ns cycle, 167 MHz | – | 450 | mA |
| $I_{SB1}$ | Automatic CE Power Down Current—TTL Inputs | $V_{DD}$ = Max, Device Deselected, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ = $1/t_{CYC}$ | 4.0-ns cycle, 250 MHz | – | 245 | mA |
| | | | 5.0-ns cycle, 200 MHz | – | 245 | mA |
| | | | 6.0-ns cycle, 167 MHz | – | 245 | mA |
| $I_{SB2}$ | Automatic CE Power Down Current—CMOS Inputs | $V_{DD}$ = Max, Device Deselected, $V_{IN}$ ≤ 0.3 V or $V_{IN}$ ≥ $V_{DDQ}$ – 0.3 V, f = 0 | All speeds | – | 120 | mA |

**Notes**
13. Overshoot: $V_{IH}$(AC) < $V_{DD}$ +1.5V (Pulse width less than $t_{CYC}/2$). Undershoot: $V_{IL}$(AC) > –2V (Pulse width less than $t_{CYC}/2$).
14. Power up: Assumes a linear ramp from 0V to $V_{DD}$(min.) within 200 ms. During this time $V_{IH}$ < $V_{DD}$ and $V_{DDQ}$ ≤ $V_{DD}$.

## Electrical Characteristics (continued)

Over the Operating Range[13, 14]

| Parameter | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SB3}$ | Automatic CE Power Down Current—CMOS Inputs | $V_{DD}$ = Max, Device Deselected, or $V_{IN} \le 0.3$ V or $V_{IN} \ge V_{DDQ} - 0.3$ V, f = $f_{MAX} = 1/t_{CYC}$ | 4.0-ns cycle, 250 MHz | – | 245 | mA |
| | | | 5.0-ns cycle, 200 MHz | – | 245 | mA |
| | | | 6.0-ns cycle, 167 MHz | – | 245 | mA |
| $I_{SB4}$ | Automatic CE Power Down Current—TTL Inputs | $V_{DD}$ = Max, Device Deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, f = 0 | All speeds | – | 135 | mA |

## Capacitance[15]

| Parameter | Description | Test Conditions | 100-pin TQFP Max | 165-ball FBGA Max | 209-ball FBGA Max | Unit |
|---|---|---|---|---|---|---|
| $C_{ADDRESS}$ | Address Input Capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{DD}$ = 3.3 V, $V_{DDQ}$ = 2.5 V | 6 | 6 | 6 | pF |
| $C_{DATA}$ | Data Input Capacitance | | 5 | 5 | 5 | pF |
| $C_{CTRL}$ | Control Input Capacitance | | 8 | 8 | 8 | pF |
| $C_{CLK}$ | Clock Input Capacitance | | 6 | 6 | 6 | pF |
| $C_{I/O}$ | Input/Output Capacitance | | 5 | 5 | 5 | pF |

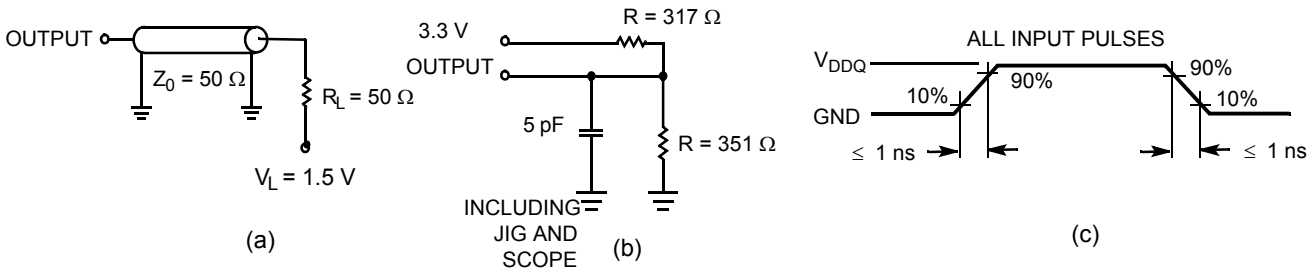
## Thermal Resistance[15]

| Parameter | Description | Test Conditions | 100-pin TQFP Package | 165-ball FBGA Package | 209-ball FBGA Package | Unit |
|---|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51. | 24.63 | 16.3 | 15.2 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 2.28 | 2.1 | 1.7 | °C/W |

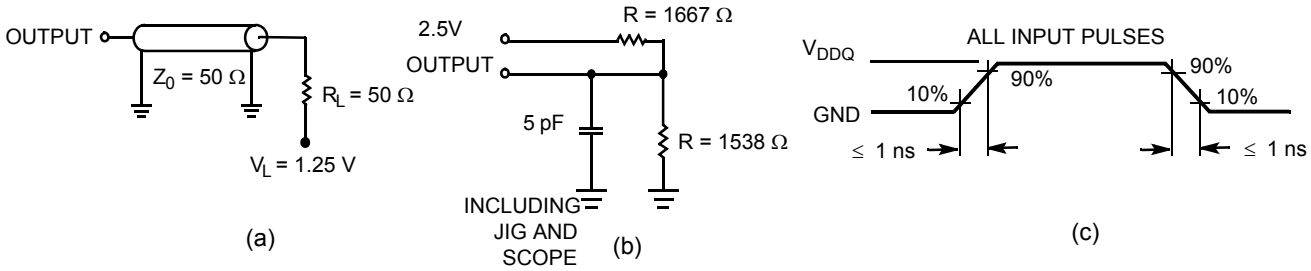
**Note**
15. Tested initially and after any design or process change that may affect these parameters.

## AC Test Loads and Waveforms

### 3.3 V I/O Test Load




### 2.5 V I/O Test Load




## Switching Characteristics

Over the Operating Range[16, 17]

| Parameter | Description | 250 MHz | | 200 MHz | | 167 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{POWER}$ | $V_{DD}$(Typical) to the First Access[18] | 1 | – | 1 | – | 1 | – | ms |
| **Clock** | | | | | | | | |
| $t_{CYC}$ | Clock Cycle Time | 4.0 | – | 5.0 | – | 6.0 | – | ns |
| $t_{CH}$ | Clock HIGH | 2.0 | – | 2.0 | – | 2.4 | – | ns |
| $t_{CL}$ | Clock LOW | 2.0 | – | 2.0 | – | 2.4 | – | ns |
| **Output Times** | | | | | | | | |
| $t_{CO}$ | Data Output Valid After CLK Rise | – | 3.0 | – | 3.0 | – | 3.4 | ns |
| $t_{DOH}$ | Data Output Hold After CLK Rise | 1.3 | – | 1.3 | – | 1.5 | – | ns |
| $t_{CLZ}$ | Clock to Low Z[19, 20, 21] | 1.3 | – | 1.3 | – | 1.5 | – | ns |
| $t_{CHZ}$ | Clock to High Z[19, 20, 21] | – | 3.0 | – | 3.0 | – | 3.4 | ns |
| $t_{OEV}$ | $\overline{OE}$ LOW to Output Valid | – | 3.0 | – | 3.0 | – | 3.4 | ns |
| $t_{OELZ}$ | $\overline{OE}$ LOW to Output Low Z[19, 20, 21] | 0 | – | 0 | – | 0 | – | ns |
| $t_{OEHZ}$ | $\overline{OE}$ HIGH to Output High Z[19, 20, 21] | – | 3.0 | – | 3.0 | – | 3.4 | ns |

**Notes**

16. Timing reference level is 1.5V when $V_{DDQ}$ = 3.3V and is 1.25V when $V_{DDQ}$ = 2.5V.
17. Test conditions shown in (a) of AC Test Loads and Waveforms unless otherwise noted.
18. This part has an internal voltage regulator; $t_{POWER}$ is the time that the power needs to be supplied above $V_{DD}$(minimum) initially before a read or write operation can be initiated.
19. $t_{CHZ}$, $t_{CLZ}$,$t_{OELZ}$, and $t_{OEHZ}$ are specified with AC test conditions shown in part (b) of "AC Test Loads and Waveforms" on page 23. Transition is measured ±200 mV from steady-state voltage.
20. At any possible voltage and temperature, $t_{OEHZ}$ is less than $t_{OELZ}$ and $t_{CHZ}$ is less than $t_{CLZ}$ to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z before Low-Z under the same system conditions.
21. This parameter is sampled and not 100% tested.

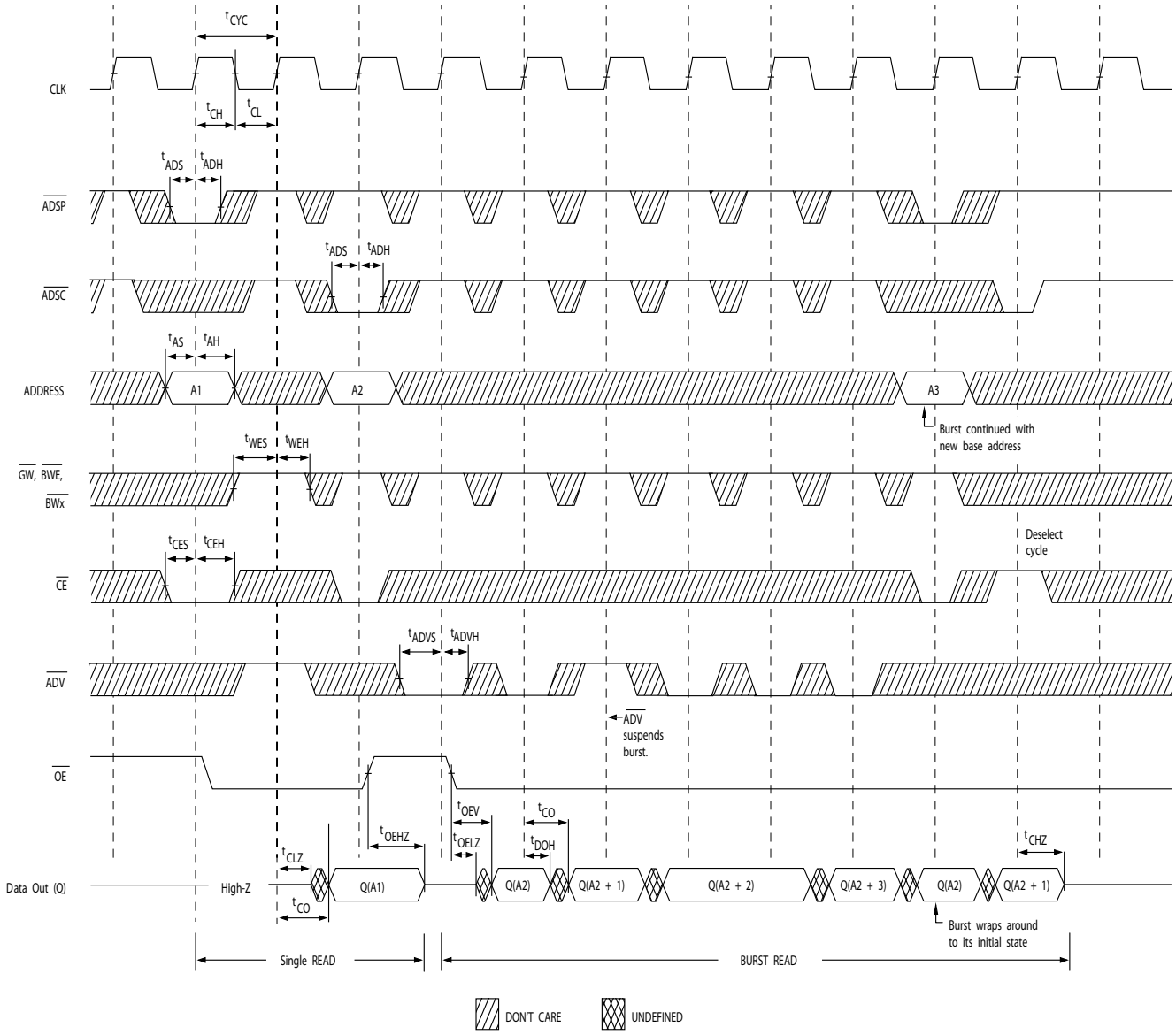
## Switching Characteristics (continued)

Over the Operating Range[16, 17]

| Parameter | Description | 250 MHz | | 200 MHz | | 167 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| **Setup Times** | | | | | | | | |
| $t_{AS}$ | Address Setup Before CLK Rise | 1.4 | – | 1.4 | – | 1.5 | – | ns |
| $t_{ADS}$ | $\overline{ADSC}$, $\overline{ADSP}$ Setup Before CLK Rise | 1.4 | – | 1.4 | – | 1.5 | – | ns |
| $t_{ADVS}$ | $\overline{ADV}$ Setup Before CLK Rise | 1.4 | – | 1.4 | – | 1.5 | – | ns |
| $t_{WES}$ | $\overline{GW}$, $\overline{BWE}$, $\overline{BW}_X$ Setup Before CLK Rise | 1.4 | – | 1.4 | – | 1.5 | – | ns |
| $t_{DS}$ | Data Input Setup Before CLK Rise | 1.4 | – | 1.4 | – | 1.5 | – | ns |
| $t_{CES}$ | Chip Enable Setup Before CLK Rise | 1.4 | – | 1.4 | – | 1.5 | – | ns |
| **Hold Times** | | | | | | | | |
| $t_{AH}$ | Address Hold After CLK Rise | 0.4 | – | 0.4 | – | 0.5 | – | ns |
| $t_{ADH}$ | $\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise | 0.4 | – | 0.4 | – | 0.5 | – | ns |
| $t_{ADVH}$ | $\overline{ADV}$ Hold After CLK Rise | 0.4 | – | 0.4 | – | 0.5 | – | ns |
| $t_{WEH}$ | $\overline{GW}$, $\overline{BWE}$, $\overline{BW}_X$ Hold After CLK Rise | 0.4 | – | 0.4 | – | 0.5 | – | ns |
| $t_{DH}$ | Data Input Hold After CLK Rise | 0.4 | – | 0.4 | – | 0.5 | – | ns |
| $t_{CEH}$ | Chip Enable Hold After CLK Rise | 0.4 | – | 0.4 | – | 0.5 | – | ns |

## Switching Waveforms

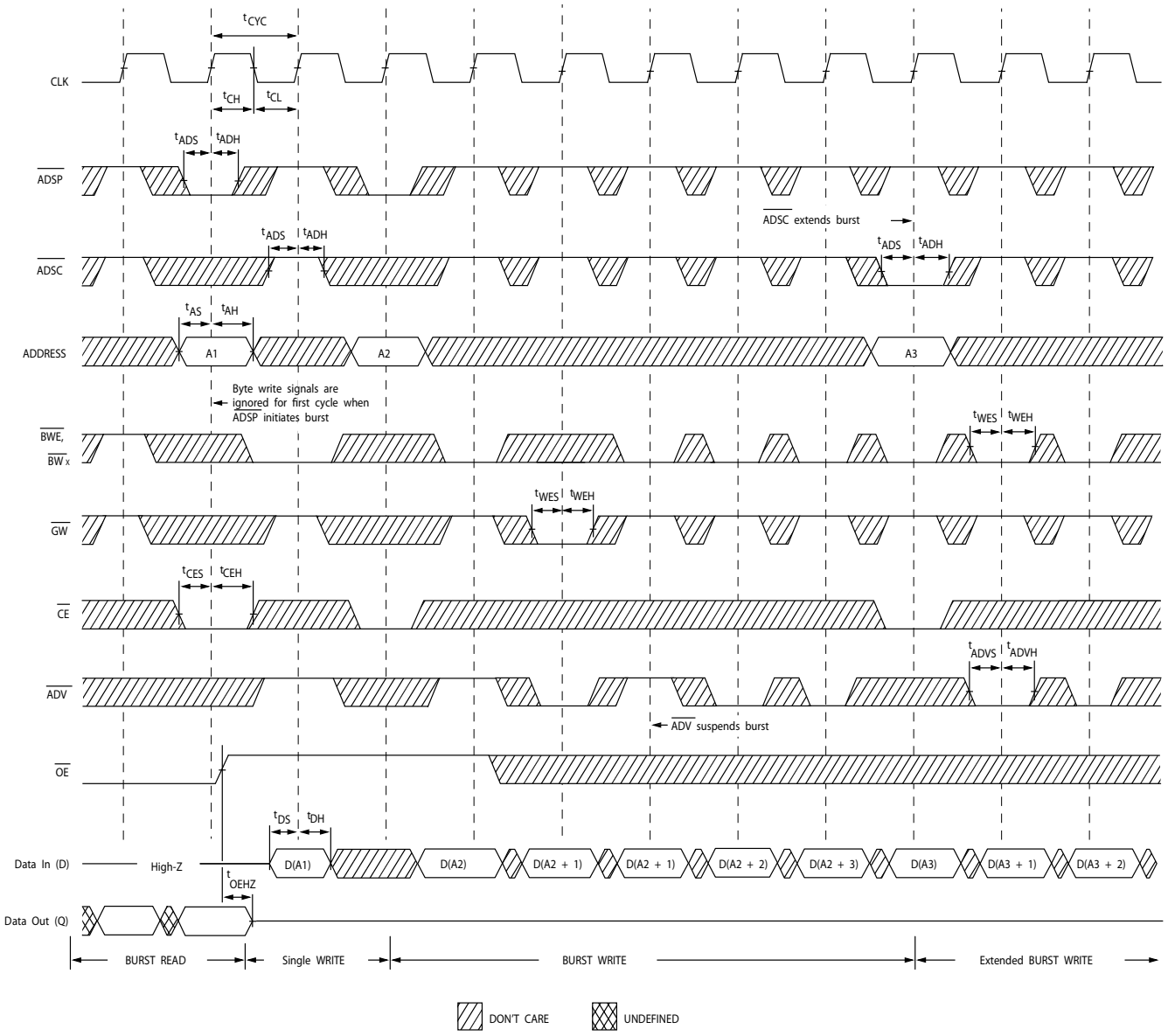
### Read Cycle Timing[22]




**Note**
22. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, $CE_2$ is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH, $CE_2$ is LOW, or $\overline{CE}_3$ is HIGH.

## Switching Waveforms (continued)

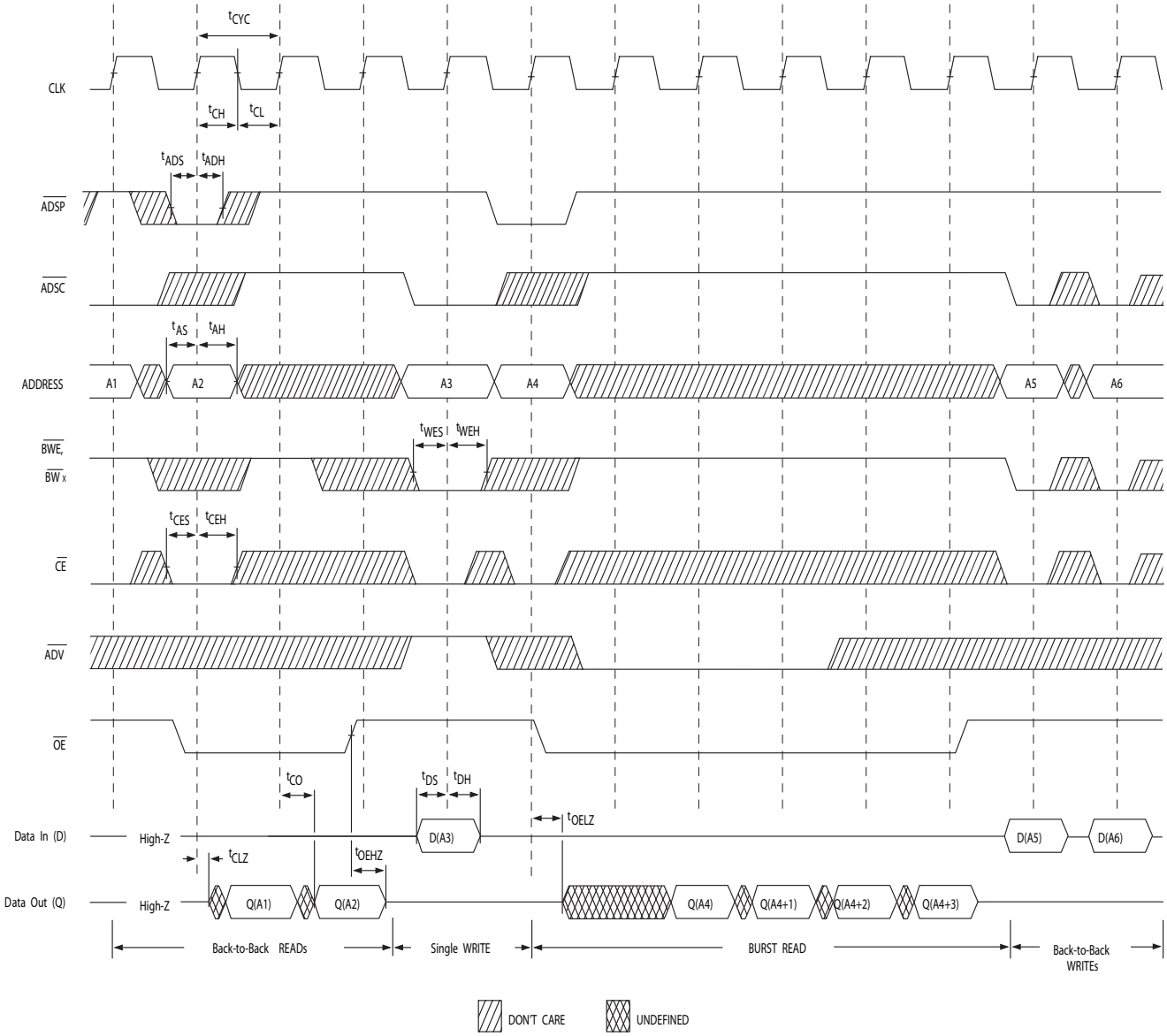
### Write Cycle Timing[23, 24]




**Notes**
23. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, $CE_2$ is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH, $CE_2$ is LOW, or $\overline{CE}_3$ is HIGH.
24. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW, and $\overline{BW}_X$ LOW.

## Switching Waveforms (continued)

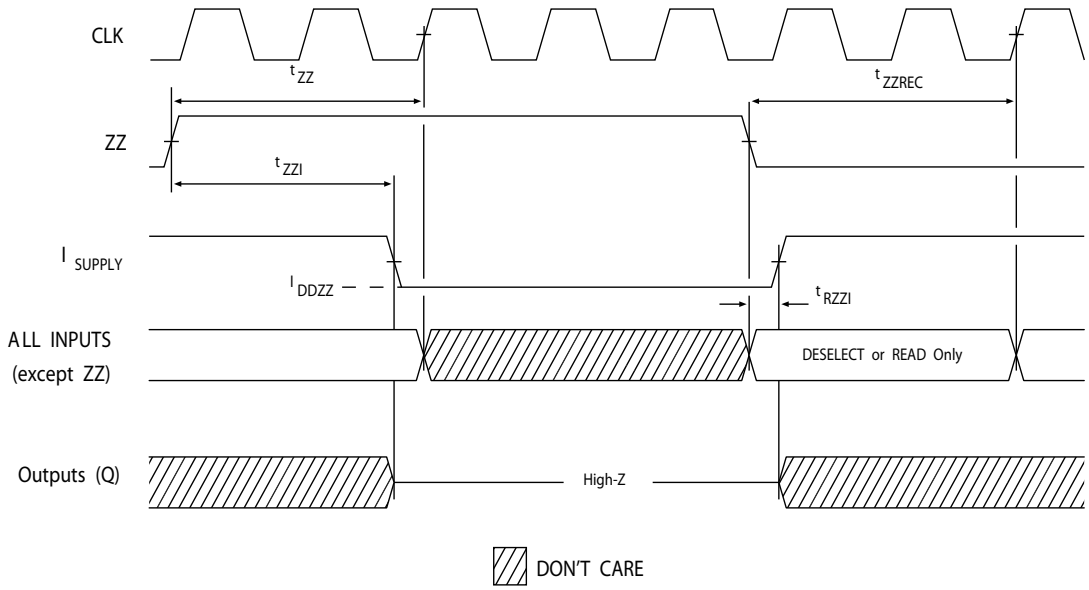
### Read/Write Cycle Timing[25, 26, 27]




**Notes**
25. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, $CE_2$ is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH, $CE_2$ is LOW, or $\overline{CE}_3$ is HIGH.
26. The data bus (Q) remains in high Z following a write cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
27. $\overline{GW}$ is HIGH.

## Switching Waveforms (continued)

### ZZ Mode Timing[28, 29]

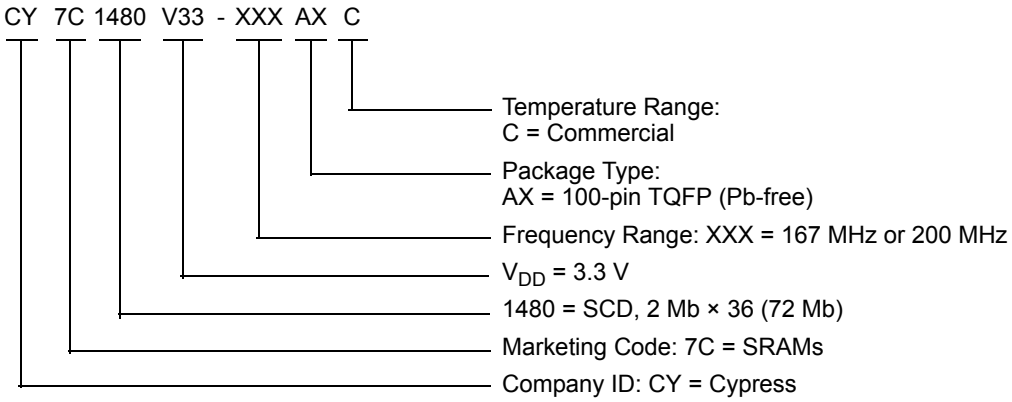



**Notes**
28. Device must be deselected when entering ZZ mode. See Truth Table on page 11 for all possible signal conditions to deselect the device.
29. DQs are in high Z when exiting ZZ sleep mode.

## Ordering Information

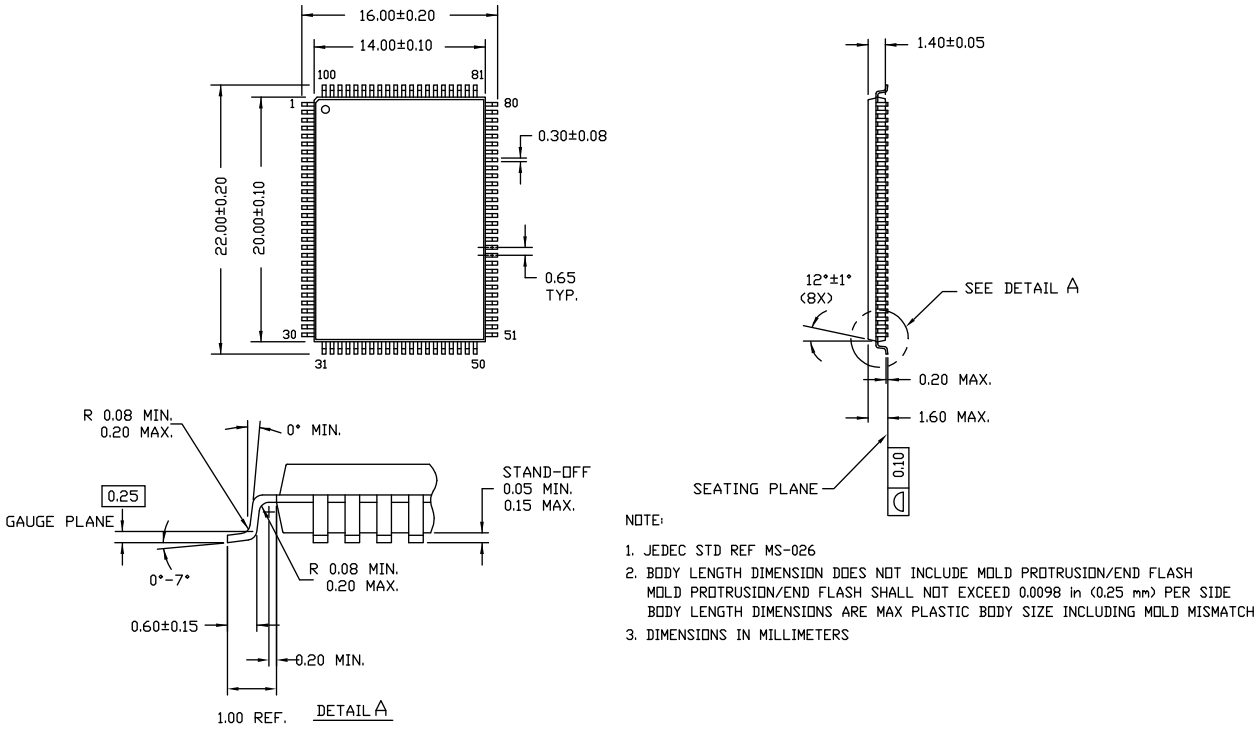
| Speed (MHz) | Ordering Code | Package Diagram | Part and Package Type | Operating Range |
|---|---|---|---|---|
| 167 | CY7C1480V33-167AXC | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Commercial |
| 200 | CY7C1480V33-200AXC | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Commercial |

### Ordering Code Definitions



## Package Diagrams

**Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm), 51-85050**



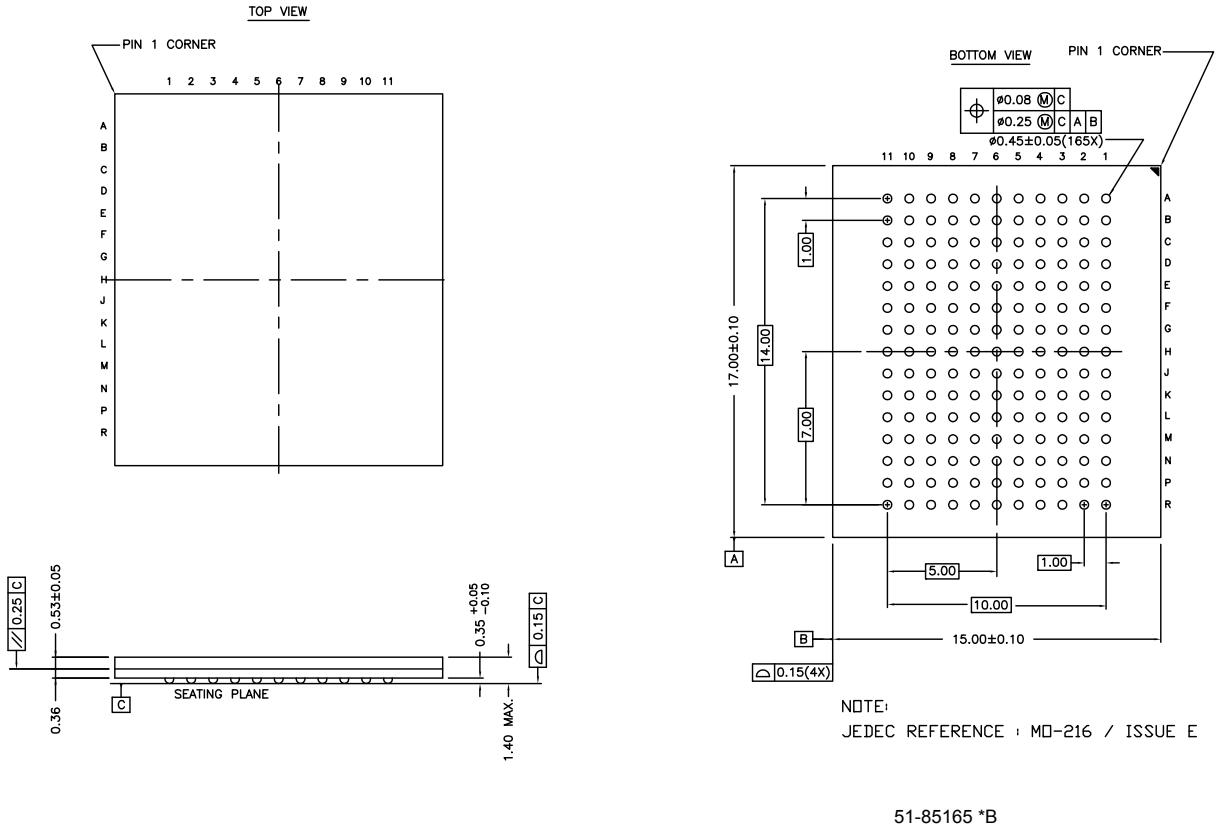

NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *D

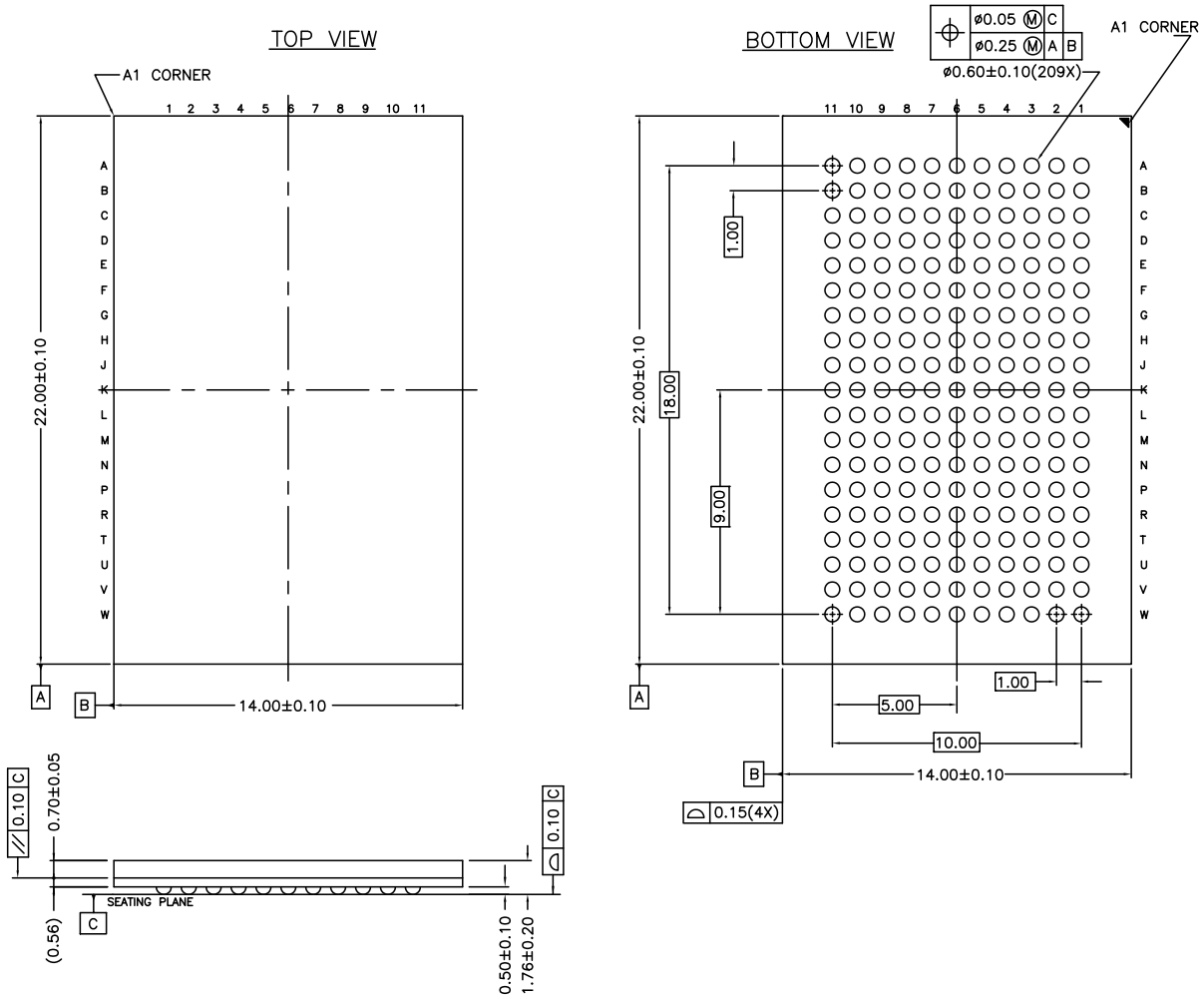
## Package Diagrams (continued)

**Figure 2. 165-Ball FBGA (15 × 17 × 1.4 mm), 51-85165**



## Package Diagrams (continued)

**Figure 3. 209-ball FBGA (14 × 22 × 1.76 mm), 51-85167**




51-85167 *A

## Acronyms

| Acronym | Description |
|---|---|
| BGA | ball grid array |
| CMOS | complementary metal oxide semiconductor |
| FBGA | fine-pitch ball grid array |
| I/O | input/output |
| JTAG | Joint Test Action Group |
| LSB | least significant bit |
| MSB | most significant bit |
| $\overline{OE}$ | output enable |
| SRAM | static random access memory |
| TAP | test access port |
| TCK | test clock |
| TDI | test data-in |
| TDO | test data-out |
| TMS | test mode select |
| TQFP | thin quad flat pack |
| TTL | transistor transistor logic |
| $\overline{WE}$ | write enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celcius |
| µA | micro Amperes |
| mA | milli Amperes |
| mm | milli meter |
| ms | milli seconds |
| MHz | Mega Hertz |
| ns | nano seconds |
| Ω | Ohms |
| % | percent |
| pF | pico Farad |
| V | Volts |
| W | Watts |

## Document History Page

| Document Title: CY7C1480V33/CY7C1482V33/CY7C1486V33, 72-Mbit (2 M × 36/4 M × 18/1 M × 72) Pipelined Sync SRAM<br>Document Number: 38-05283 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| ** | 114670 | 08/06/02 | PKS | New Data Sheet |
| *A | 118281 | 01/21/03 | HGK | Changed $t_{CO}$ from 2.4 to 2.6 ns for 250 MHz<br>Updated features on page 1 for package offering<br>Removed 30-MHz offering<br>Updated Ordering Information<br>Changed Advanced Information to Preliminary |
| *B | 233368 | See ECN | NJY | Changed timing diagrams<br>Changed logic block diagrams<br>Modified Functional Description<br>Modified “Functional Overview” section<br>Added boundary scan order for all packages<br>Included thermal numbers and capacitance values for all packages<br>Included IDD and ISB values<br>Removed 250-MHz speed grade offering and included 225-MHz speed bin<br>Changed package outline for 165FBGA package and 209-ball BGA package<br>Removed 119-BGA package offering |
| *C | 299452 | See ECN | SYT | Removed 225-MHz offering and included 250-MHz speed bin<br>Changed $t_{CYC}$ from 4.4 ns to 4.0 ns for 250-MHz Speed Bin<br>Changed $\Theta_{JA}$ from 16.8 to 24.63 °C/W and $\Theta_{JC}$ from 3.3 to 2.28 °C/W for 100 TQFP Package on Page # 20<br>Added lead-free information for 100-Pin TQFP, 165 FBGA and 209 BGA Packages<br>Added comment of ‘Lead-free BG packages availability’ below the Ordering Information |
| *D | 323080 | See ECN | PCI | Unshaded 200 and 167 MHz speed bin in the AC/DC Table and Selection Guide<br>Address expansion pins/balls in the pinouts for all packages are modified as per JEDEC standard<br>Added Address Expansion pins in the Pin Definitions Table<br>Added Truth Table and Note# 7 for CY7C1486V33 on page# 11<br>Added Industrial Operating Range<br>Modified $V_{OL,}$ $V_{OH}$ test conditions<br>Removed comment of ‘Lead-free BG packages availability’ below the Ordering Information<br>Updated Ordering Information Table |
| *E | 416193 | See ECN | NXR | Converted Preliminary to Final<br>Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court”<br>Changed the description of $I_X$ from Input Load Current to Input Leakage Current on page# 19<br>Changed the $I_X$ current values of MODE on page # 19 from -5 µA and 30 µA to -30 µA and 5 µA<br>Changed the $I_X$ current values of ZZ on page # 19 from -30 µA and 5 µA to -5 µA and 30 µA<br>Changed $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$ on page # 19<br>Replaced Package Name column with Package Diagram in the Ordering Information table<br>Updated the Ordering Information Table |

## Document History Page (continued)

| Document Title: CY7C1480V33/CY7C1482V33/CY7C1486V33, 72-Mbit (2 M × 36/4 M × 18/1 M × 72) Pipelined Sync SRAM<br>Document Number: 38-05283 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| *F | 470723 | See ECN | VKN | Added the Maximum Rating for Supply Voltage on $V_{DDQ}$ Relative to GND<br>Changed $t_{TH}$,$t_{TL}$ from 25 ns to 20 ns and $t_{TDOV}$ from 5 ns to 10 ns in TAP AC Switching Characteristics table<br>Updated the Ordering Information table |
| *G | 486690 | See ECN | VKN | Corrected the typo in the 209-Ball FBGA pinout.<br>(Corrected the ball name H9 to $V_{SS}$ from $V_{SSQ}$). |
| *H | 1026720 | See ECN | VKN | Added footnote #2 related to $V_{SSQ}$ |
| *I | 2898501 | 03/24/2010 | NJY | Removed inactive parts from Ordering Information table; Updated package diagram. |
| *J | 3067398 | 10/20/10 | NJY | The part CY7C1480V33-250AXC found to be in “EOL Prune” state in Oracle PLM is removed from the ordering information table.<br>Added ordering code definitions. |
| *K | 3257192 | 05/14/2011 | NJY | Updated Package Diagrams.<br>Added Acronyms and Units of Measure.<br>Updated in new template. |

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