AN983B/AN983BL
PCI/miniPCI-to-Ethernet LAN Controller

DATASHEET

Rev. 1.8
MAY. 2003

ADMtek.com.tw

Datasheet Revision History

Revision Date	Revision	Description
Oct, 2000	0.1	Draft data sheet for review
Feb, 2001	1.0	First release
Mar, 2001	1.1	Add CSR15.bit28 MRXCK Add CSR18.bit26 PMEP Add CSR18.bit27 PMEPEN
Sep, 2001	1.2	Add 25MHz crystal accuracy Revise PHY registers
Sep, 2001	1.3	Revise product logo of Pin assignment diagram
Sep, 2001	1.4	P.17 MrxD0~D3 P.23 CIOSA : 1 means enable ; 0 means disable P.14 Add LED info to pin diagram
JULY, 2002	1.5	P.25 Offset 80h, DID default value : 0981h P.40 CSR18[25] / PWRS_clr : 1 means PCI_reset rising will clear CR49[1:0]/PWRS
JULY, 2002	1.6	P.85 FIG21, FIG22, FIG23, FIG24 added for MII interface signal timing.
JULY, 2002	1.7	P.45 Unicast registers added
MAY, 2003	1.8	P.69 Modify some error statement about Loop-back Operation of transceiver

Table- 1 Revision History

CONTENTS

FIGURE INDEX

1. GENERAL DESCRIPTIONS

The AN983B is a high performance PCI Fast Ethernet controller with integrated physical layer interface for 10BASE-T and 100BASE-TX application.

The AN983B was designed with advanced CMOS technology to provide glueless 32-bit bus master interface for PCI, boot ROM interface, CSMA/CD protocol for Fast Ethernet, as well as the physical media interface for 100BASE-TX of IEEE802.3u and 10BASE-T of IEEE802.3. The auto-negotiation function is also supported for speed and duplex detection.

The AN983B can be programmed as MAC-only controller. In this mode, it provides the standard MII interface to link to an external PHY. With this mode, it can be connected to the HomePNA PHY to support the HomePNA networking solution or Homeplug Phy(Power-line solution) to support Homeplug networking solution..

The AN983B provides both half-duplex and full-duplex operation, as well as support for full-duplex flow control.

It provides long FIFO buffers for transmission and receiving, and early interrupt mechanism to enhance performance.

The AN983B also supports ACPI and PCI compliant power management function and Magic Packet wake-up event.

2. SYSTEM BLOCK DIAGRAM

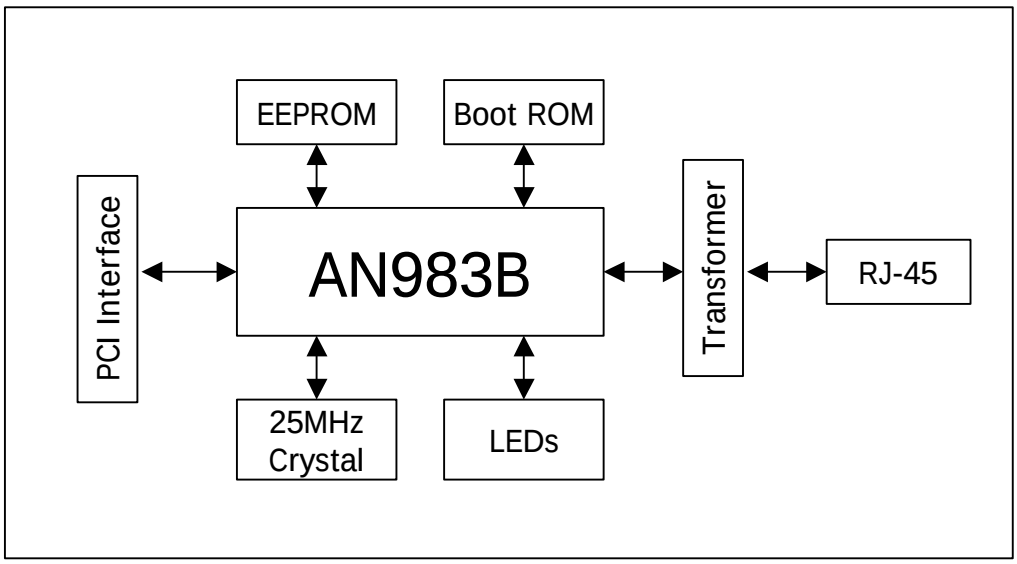


Fig - 1 System diagram of the AN983B

3. FEATURES

INDUSTRY STANDARD

- *IEEE802.3u 100BASE-TX and IEEE802.3 10BASE-T compliant*
- *Support for IEEE802.3x flow control*
- *IEEE802.3u Auto-Negotiation support for 10BASE-T and 100BASE-TX*
- *PCI Specification 2.2 compliant*
- *ACPI and PCI power management Ver.1.1 compliant*
- *Support PC99 wake on LAN*

FIFO

- *Provides two independent long FIFOs with 2k bytes each for transmission and receiving*
- *Pre-fetch up to two transmit packets to minimize inter frame gap (IFG) to 0.96us*
- *Retransmits collided packet without reload from host memory within 64 bytes.*
- *Automatically retransmits FIFO under-run packet with maximum drain threshold until 3 times retry failure and that will not influence the registers and transmit threshold of next packet*

PCI I/F

- *Provides 32-bit PCI bus master data transfer*
- *Supports PCI clock with frequency from 0Hz to 33MHz*
- *Supports network operation with PCI system clock from 20MHz to 33MHz*
- *Provides performance meter, PCI bus master latency timer, for tuning the threshold to enhance the performance*
- *Provides burst transmit packet interrupt and transmit/receive early interrupt to reduce host CPU utilization*
- *Supports memory-read, memory-read-line, memory-read-multiple, memory-write, memory-write-and-invalidate command while being bus master*
- *Supports big or little endian byte ordering*

EEPROM/BOOT ROM I/F

- *Provides write-able Flash ROM and EPROM as boot ROM with size up to 128kB*
- *Provides PCI to access boot ROM by byte, word, or double word*
- *Re-writes Flash boot ROM through I/O port by programming register*

- *Provides serial interface for read/write 93C46/66 EEPROM*
- *Automatically loads device ID, vendor ID, subsystem ID, subsystem vendor ID, Maximum-Latency, and Minimum-Grand from the 64 byte contents of 93C46/66 after PCI reset de-asserted in PCI environment.*

MAC/PHYSICAL

- *Integrates the whole Physical layer functions of 100BASE-TX and 10BASE-T*
- *Provides Full -duplex operation on both 100Mbps and 10Mbps modes*
- *Provides Auto-negotiation (NWAY) function of full/half duplex operation for both 10 and 100 Mbps*
- *Provides transmit wave-shaper, receive filters, and adaptive equalizer*
- *Provides MLT-3 transceiver with DC restoration for Base-line wander compensation*
- *Provides MAC and Transceiver (TXCVR) loop-back modes for diagnostic*
- *Builds in Stream Cipher Scrambler/ De-scrambler and 4B/5B encoder/decoder*
- *Supports external transmit transformer with turn ratio 1:1*
- *Supports external receive transformer with turn ratio 1:1*

LED DISPLAY

- *3 LEDs displays scheme provided:*
  - ***100Mbps(on) or Speed 10(off)***
  - ***Link (keeps on when link ok) or Activity (will be blinking with 10Hz when receiving or transmitting but not collision)***
  - ***FD (keeps on when in Full duplex mode) or Collision (will be blinking with 20Hz when colliding)***

- *4 LEDs displayed scheme provided:*
  - ***100Mbps and Link (keep on when link and 100Mpbs)***
  - ***10Mbps and Link (keep on when link and 10Mpbs)***
  - ***Activity (will be blinking with 10Hz when receiving or transmitting but not collision)***
  - ***FD (keeps on when in Full duplex mode) or Collision (will be blinking with 20Hz when colliding)***

MISCELLANEOUS

- *Provides 128-pin QFP/LQFP packages for PCI/mini-PCI interfaces*
- *3.3V power supply with 5V/3.3V I/O tolerance*

4. BLOCK DIAGRAM

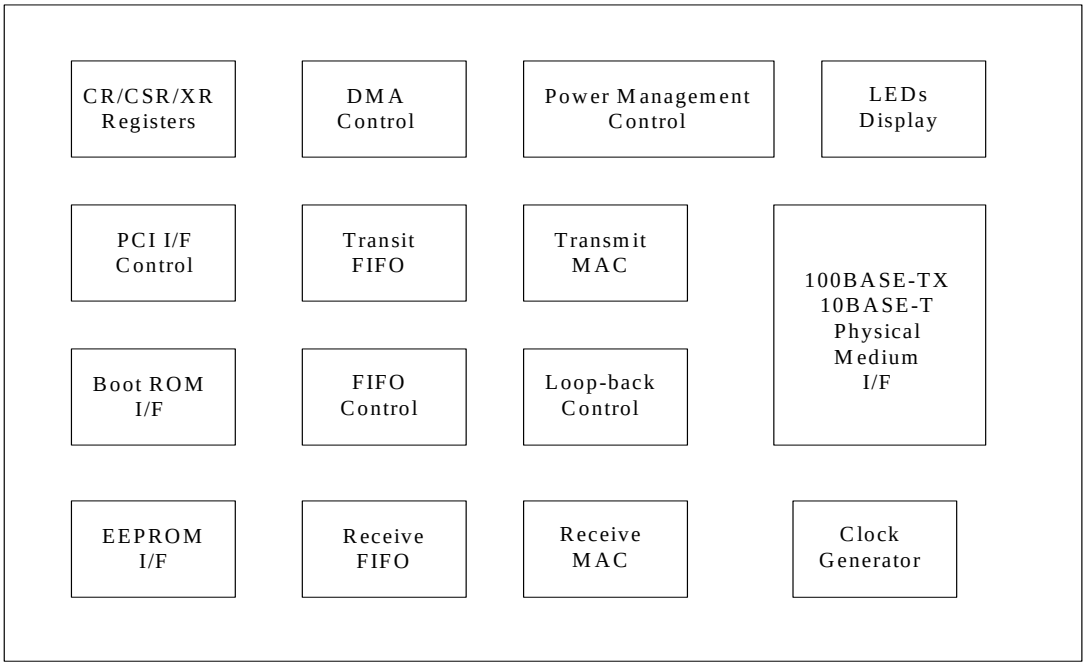


Fig - 2 Block diagram of the AN983B

5. PIN ASSIGNMENT DIAGRAM

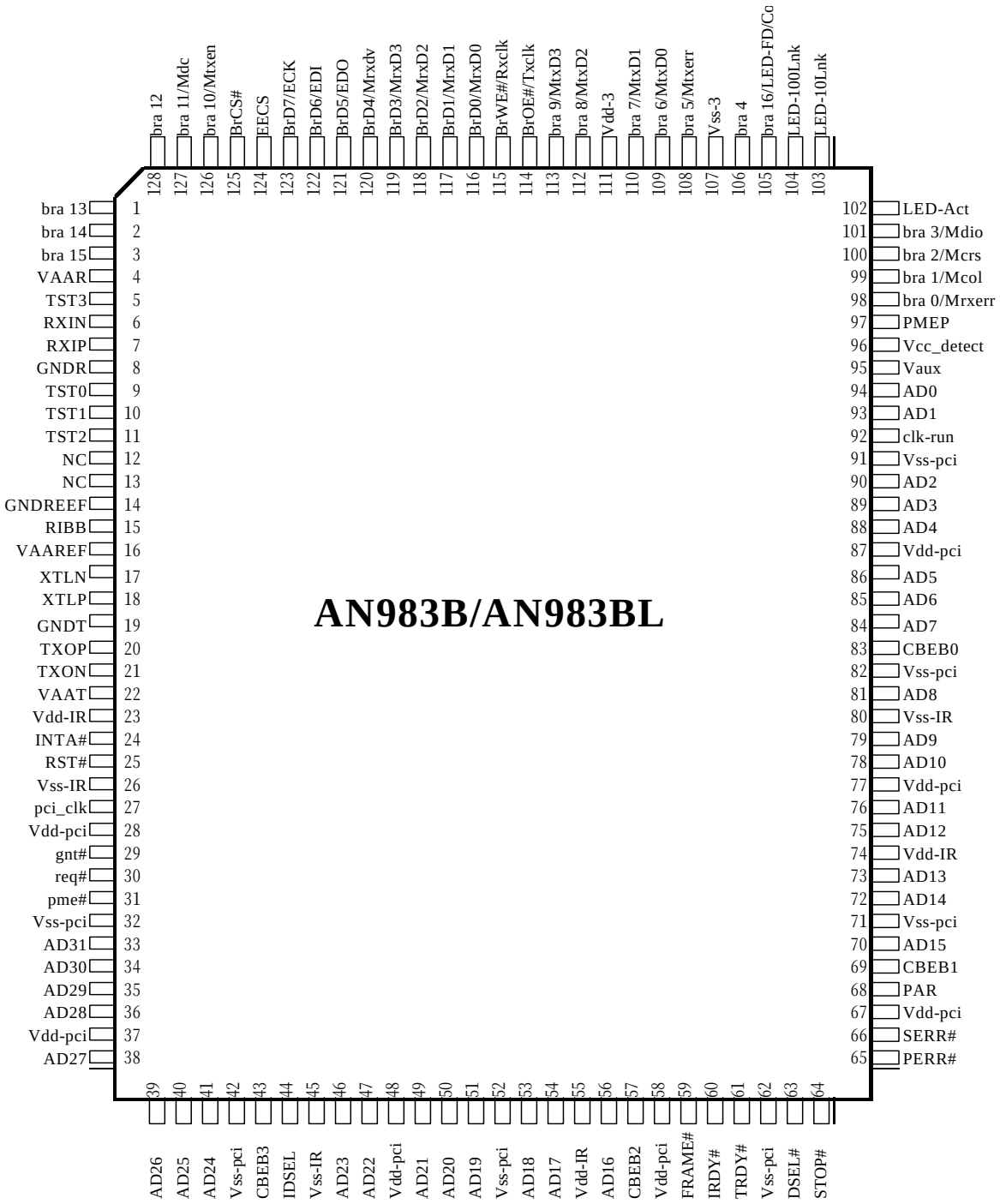


Fig - 3 Pin assignment

6. PIN DESCRIPTION

Pin #	Name	Type	Description
PCI INTERFACE			
24	INTA#	O/D	PCI interrupt request. AN983B asserts this signal when one of the interrupt events occurs.
25	RST#	I	PCI signal to initialize the AN983B. The active reset signal should be sustained at least 100μs to guarantee that the AN983B has completed the initializing activity. During the reset period, all the output pins of AN983B will be set to tri-state and all the O/D pins are floated.
27	PCI-CLK	I	This PCI clock inputs to AN983B for PCI relative circuits as the synchronized timing base with PCI bus. The Bus signals are recognized on rising edge of PCI-CLK. In order to let network operating properly, the frequency range of PCI-CLK is limited between 20MHz and 33MHz when network operating.
29	GNT#	I	PCI Bus Granted. This signal indicates that the PCI bus request of AN983B has been accepted.
30	REQ#	O	PCI Bus Request. Bus master device want to get bus access right
31	PME#	I/O	The Power Management Event signal is an open drain, active low signal. When WOL-bit 18 of CSR 18 be set into "1", means that the AN983B is set into Wake On LAN mode. In this mode, when the AN983B receives a Magic Packet frame from network then the AN983B will active this signal too. In the Wake On LAN mode, when LWS-bit (bit 17) of CSR18 is set into "1" means the LAN-WAKE signal is HP-style signal, otherwise it is IBM-style signal.
33,34 35,36 38,39 40,41 46,47 49,50 51,53 54,56 70,72 73,75 76,78 79,81 84,85 86,88 89,90 93,94	AD-31, 30 AD-29, 28 AD-27, 26 AD-25, 24 AD-23, 22 AD-21, 20 AD-19, 18 AD-17, 16 AD-15, 14 AD-13, 12 AD-11, 10 AD-9, 8 AD-7, 6 AD-5, 4 AD-3, 2 AD-1, 0	I/O	Multiplexed address data pin of PCI Bus

43 57 69 83	C-BEB3 C-BEB2 C-BEB1 C-BEB0	I/O	Bus command and byte enable
44	IDSEL	I	Initialization Device Select. This signal is asserted when host issues the configuration cycles to the AN983B.
59	FRAME#	I/O	Begin and duration of bus access, driven by master device
60	IRDY#	I/O	Master device is ready to data transaction
61	TRDY#	I/O	Slave device is ready to data transaction
63	DEVSEL#	I/O	Device select, target is driving to indicate the address is decoded
64	STOP#	I/O	Target device request the master device to stop the current transaction
65	PERR#	I/O	Data parity error is detected, driven by the agent receiving data
66	SERR#	O/D	Address parity error
68	PAR	I/O	Parity, even parity (AD [31:0] + C/BE [3:0]), master drives par for address and write data phase, target drives par for read data phase
92	Clk-run	I/O O/D	Clock Run for PCI system. In the normal operation situation, Host should assert this signal to indicate AN983B about the normal situation. On the other hand, when Host will deassert this signal when the clock is going down to a non-operating frequency. When AN983B recognizes the deasserted status of clk-run, then it will assert clk-run to request host to maintain the normal clock operation. When clk-run function is disabled then the AN983B will set clk-run in tri-state.
BOOTROM/EEPROM INTERFACE			
98~101, 106,108 ~110, 112, 113, 126, 127, 128, 1~3, 105	BrA0 ~16	I/O	ROM data bus Provides up to 128kB EPROM or Flash-ROM application space.
116~ 120, 121~ 123,	BrD0~4 BrD5/EDO BrD6/EDI BrD7/ECK	IO IO/O IO/I IO/I	BootROM data bus bit (0~7) Inputs/Output data for AN983B; EDO: Data Output of serial EEPROM Inputs/Output data for AN983B; EDI: Data Input of serial EEPROM Inputs/Output data for AN983B; ECK: Clock input of serial EEPROM, the AN983B outputs clock signal to EEPROM
124	EECS	O	Chip Select of serial EEPROM
125	BrCS#	O	BootROM Chip Select
114	BrOE#	O	BootROM Read Enable for flash ROM application

115	BrWE#	O	BootROM Write Enable for flash ROM application.
MII INTERFACE (PROGRAM AN983B AS MAC-ONLY MODE, SET FCH [2:0] = 100B)			
127	Mdc	O	MII Management Data Clock
126	Mtxen	O	MII Transmit Enable
109,110 112,113	MtxD0~3	O	MII Transmit Data
108	Mtxerr	O	MII Transmit Error
101	Mdio	I/O	MII Management Data I/O
120	Mrxdv	I	MII Receive Data Valid
100	Mcrs	I	MII Carrier Sense
116 ~ 119	MrxD0~3	I	MII Receive Data
99	Mcol	I	MII Collision
98	Mrxerr	I	MII Receive Error
115	Rxclk	I	MII Receive Clock
114	Txclk	I	MII Transmit Clock
PHYSICAL INTERFACE			
18, 17	XTLP, XTLN	I	Crystal inputs. To be connected to a 25MHz crystal with 50ppm accuracy
6,7	RXIN, RXIP	I	The differentials receive inputs of 100BASE-TX or 10BASE-T, these pins directly input from Magnetic.
20,21	TXOP, TXON	O	The differential Transmit outputs of 100BASE-TX or 10BASE-T, these pins directly output to Magnetic.
15	RIBB	I	Reference Bias Resistor. To be tied to an external 10.0K (1%) resistor which should be connected to the analog ground at the other end.
9,10,11, 5	TST0, TST1 TST2, TST3	I	Test pin
12,13	NC	O	
LED DISPLAY & MISCELLANEOUS			
102	Led-Act (Led-lnk/act)	O	4Leds mode: LED display for Activity status. This pin will be driven on with 10 Hz blinking frequency when either effective receiving or transmitting is detected. (3Led mode): LED display for link and activity status. This pin will be driven on continually when a good Link test is detected. This pin will be driven on with 10 Hz blinking frequency when either effective receiving or transmitting is detected.
103	Led-10Lnk (Led-fd/col)	O	4Leds mode: LED display for 10M b/s speed. This pin will be driven on continually when the 10M b/s network operating speed is detected. (3Leds mode): LED display for Full Duplex or Collision status. This pin will be driven on continually when a full duplex configuration is detected. This pin

			will be driven on with 20 Hz blinking frequency when a collision status is detected in the half duplex configuration.
104	Led-100Lnk (Led-speed)	O	4Leds mode: LED display for 100Mb/s speed. This pin will be driven on continually when the 100Mb/s network operating speed is detected. (3Leds mode): LED display for 100M b/s or 10M b/s speed. This pin will be driven on continually when the 100M b/s network operating speed is detected.
105	Led-Fd /Col	O	4Leds mode: LED display for Full Duplex or Collision status. This pin will be driven on continually when a full duplex configuration is detected. This pin will be driven on with 20 Hz blinking frequency when a collision status is detected in the half duplex configuration. (3Leds mode): None
95	Vaux	I	When this pin is asserted, it indicates an auxiliary power source is supported ACPI purpose, for detecting the auxiliary power source. This pin should be or-wired connected to 1) 3.3V when 3.3Vaux support, or 2) 5V when 5Vaux support from 3-way switch.
96	Vcc-detect	I	When this pin is asserted, it indicates PCI power source is supported. ACPI purpose, for detecting the main power is remained or not, This pin should be connected to PCI bus power source +5V.
97	PMEP	O	This signal is used as the WOL pin. It provides a programmable positive or negative pulse with approximately 50ms width.

DIGITAL POWER PINS	
26,32,42,45,52,62,71,80,82,91,107,	Vss-pci, Vss-IR, Vss-3
23,28,37,48,55,58,67,74,77,87,111	Vdd-pci Vdd-IR, Vdd-3 Connect to 3.3V
ANALOG POWER PINS	
4,16,22	VAAR, VAAREF, VAAT 3.3V
8,14,19	GNDR, GNDREF, GNDT

7. REGISTERS AND DESCRIPTORS DESCRIPTION

There are three kinds of registers designed for AN983B. They are AN983B configuration registers, PCI control/status registers, and Transceiver control/status registers.

The AN983B configuration registers are used to initialize and configure the AN983B for identifying and querying the AN983B.

The PCI control/status registers are used to communicate between host and AN983B. Host can initialize, control, and read the status of the AN983B through the mapped I/O or memory address space.

Regarding the registers of transceiver portion of AN983B, it includes 7 basic registers which are defined according to the clause 22 “Reconciliation Sub-layer and Media Independent Interface” and clause 28 “Physical Layer link signaling for 10 Mb/s and 100 Mb/s Auto-Negotiation on twisted pair” of IEEE802.3u standard. The AN983B also provides receive and transmit descriptors for packet buffering and management. These descriptors are described in the following section

7.1 AN983B CONFIGURATION REGISTERS

With the configuration registers software driver can initialize and configure AN983B. All of the contents of configuration registers are set to default value when there is any hardware reset occurs. On the other hand, there is no effect to their value when the software reset occurs. To access these configuration registers AN983B provides byte, word, and double word data access length.

7.1.1. AN983B CONFIGURATION REGISTERS LIST

Offset	Index	Name	Descriptions
00h	CR0	LID	Loaded device ID and vendor ID
04h	CR1	CSC	Configuration Status and Command
08h	CR2	CC	Class Code and revision number
0ch	CR3	LT	Latency Timer
10h	CR4	IOBA	IO Base Address
14h	CR5	MBA	Memory Base Address
28h	CR10	CIS	Card Information Structure (for Card bus)
2ch	CR11	SID	Subsystem ID and vendor ID
30h	CR12	BRBA	Boot ROM Base Address (ROM size = 256KB)
34h	CR13	CP	Capability Pointer
3ch	CR15	CINT	Configuration Interrupt
40h	CR16	DS	Driver space for special purpose
80h	CR32	SIG	Signature of AN983B
c0h	CR48	PMR0	Power Management Register 0
c4h	CR49	PMR1	Power Management Register 1

7.1.2. AN983B CONFIGURATION REGISTERS TABLE

Offset	b31 ---------- b16		b15 ---------- b0		
00h	Device ID*		Vendor ID*		
04h	Status		Command		
08h	Base Class Code	Subclass	------	Revision #	Step #
0ch	------	------	Latency timer	Cache line size	
10h	Base I/O address				
14h	Base memory address				
18h~ 24h	Reserved				
28h	ROM-im*	Address space offset*		Add-indi*	
2ch	Subsystem ID*		Subsystem vendor ID*		
30h	Boot ROM base address				
34h	Reserved			Cap_Ptr	
38h	Reserved				
3ch	Max_Lat*	Min_Gnt*	Interrupt pin	Interrupt line	
40h	Reserved		Driver Space	Reserved	
80h	Signature of AN983B				
c0h	PMC		Next_Item_Ptr	Cap_ID	
c4h	Reserved		PMCSR		

Note:
* Automatically recalled from EEPROM when PCI reset is deserted
CIS (28h) is a read-only register
DS (40h), bit15-8, is read/write able register
SIG (80h) is hard wired register, read only.

7.1.3 AN983B CONFIGURATION REGISTERS DESCRIPTIONS

CR0 (offset = 00h), LID - Loaded Identification number of Device and Vendor

Bit #	Name	Descriptions	Default Val	RW Type
31~16	LDID	Loaded Device ID, the device ID number loaded from serial EEPROM.	From EEPROM	R/O
15~0	LVID	Loaded Vendor ID, the vendor ID number loaded from serial EEPROM.	From EEPROM	R/O

From EEPROM: Loaded from EEPROM

CR1 (offset = 04h), CSC - Configuration command and status

Bit #	Name	Descriptions	Default Val	RW Type
31	SPE	Status of Parity Error. 1: means that AN983B detected a parity error. This bit will be set in this condition, even if the parity error response (bit 6 of CR1) is disabled.	0	R/W
30	SES	Status of System Error. 1: means that AN983B asserted the system error pin.	0	R/W
29	SMA	Status of Master Abort. 1: means that AN983B received a master abort and terminated a master transaction.	0	R/W
28	STA	Status of Target Abort. 1: means that AN983B received a target abort and terminated a master transaction.	0	R/W
27	---	Reserved.		
26, 25	SDST	Status of Device Select Timing. The timing of the assertion of device select. 01: means a medium assertion of DEVSEL#	01	R/O
24	SDPR	Status of Data Parity Report. 1: when three conditions are met: AN983B asserted parity error - PERR# or it detected parity error asserted by other device. AN983B is operating as a bus master. AN983B's parity error response bit (bit 6 of CR1) is enabled.	0	R/W
23	SFBB	Status of Fast Back-to-Back Always 1, since AN983B has the ability to accept fast back-to-back transactions.	1	R/O
22~21	---	Reserved.		
20	NC	New Capabilities. This bit indicates that whether the AN983B provides a list of extended capabilities, such as PCI power management.	Same as bit 19 of CSR18	RO

		1: the AN983B provides the PCI management function 0: the AN983B doesn't provide New Capabilities.		
19~ 9	---	Reserved.		
8	CSE	Command of System Error Response 1: enable system error response. AN983B will assert SERR# When it find a parity error on the address phase.	0	R/W
7	---	Reserved.		
6	CPE	Command of Parity Error Response 0: disable parity error response. AN983B will ignore any detected parity error and keep on its operating. Default value is 0. 1: enable parity error response. AN983B will assert system error (bit 13 of CSR5) when a parity error is detected.	0	R/W
5~ 3	---	Reserved.		
2	CMO	Command of Master Operation Ability 0: disable the bus master ability. 1: enable the PCI bus master ability. Default value is 1 for normal operation.	0	R/W
1	CMSA	Command of Memory Space Access 0: disable the memory space access ability. 1: enable the memory space access ability.	0	R/W
0	CIOSA	Command of I/O Space Access 1: enable the I/O space access ability. 0: disable the I/O space access ability.	0	R/W

R/W: Read and Write able. RO: Read able only.

CR2 (offset = 08h), CC - Class Code and Revision Number

Bit #	Name	Descriptions	Default Val	RW Type
31~24	BCC	Base Class Code. It means AN983B is network controller.	02h	RO
23~16	SC	Subclass Code. It means AN983B is a Fast Ethernet Controller.	00h	RO
15~ 8	---	Reserved.		
7 ~ 4	RN	Revision Number identifies the revision number of AN983B.	01h	RO
3 ~ 0	SN	Step Number, identifies the AN983B steps within the current revision.	01h	RO

RO: Read Only.

CR3 (offset = 0ch), LT - Latency Timer

Bit #	Name	Descriptions	Default Val	RW Type
31~16	---	Reserved.		
15~ 8	LT	Latency Timer. This value specifies the latency timer of the AN983B in units of PCI bus clock. Once the AN983B asserts FRAME#, the latency timer starts to count. If the latency	0	R/W

		timer expires and the AN983B still asserted FRAME#, then the AN983B will terminate the data transaction as soon as its GNT# is removed.		
7 ~ 0	CLS	Cache Line Size. This value specifies the system cache line size in units of 32-bit double words (DW). The AN983B supports 8, 16, and 32 DW of cache line size. This value is used by the AN983B driver to program the cache alignment bits (bit 14 and 15 of CSR0). The cache alignment bits are used for cache oriented PCI commands; say memory-read-line, memory-read-multiple, and memory-write-and-invalidate.	0	R/W

CR4 (offset = 10h), IOBA - I/O Base Address

Bit #	Name	Descriptions	Default Val	RW Type
31~ 8	IOBA	I/O Base Address. This value indicate the base address of PCI control and status register (CSR0~28)	0	R/W
7 ~ 1	---	Reserved.		
0	IOSI	I/O Space Indicator. 1: means that the configuration registers map into the I/O space.	1	RO

CR5 (offset = 14h), MBA - Memory Base Address

Bit #	Name	Descriptions	Default Val	RW Type
31~ 10	MBA	Memory Base Address. This value indicate the base address of PCI control and status register (CSR0~28)	0	R/W
9 ~ 1	---	Reserved.		
0	IOSI	Memory Space Indicator. 1: means that the configuration registers map into the I/O space.	0	RO

CR11 (offset = 2ch), SID - Subsystem ID.

Bit #	Name	Descriptions	Default Val	RW Type
31~16	SID	Subsystem ID. This value is loaded from EEPROM after power on or hardware reset.	From EEPROM	RO
15~ 0	SVID	Subsystem Vendor ID. This value is loaded from EEPROM after power on or hardware reset.	From EEPROM	RO

CR12 (offset = 30h), BRBA - Boot ROM Base Address.

Bit #	Name	Descriptions	Default Val	RW Type
31~17	BRBA	Boot ROM Base Address. This value indicates the address mapping of boot ROM field. Besides, it also defines the boot ROM size. The value of bit 17~10 is set to 0 for AN983B supports up to 256KB of boot ROM.	X: b31~18 0: b17~10	R/W RO
16 ~ 1	---	Reserved	0	RO R/W

				R/W
0	BRE	Boot ROM Enable. The AN983B really enables its boot ROM access only if both the memory space access bit (bit 1 of CR1) and this bit are set to 1. 1: enable Boot ROM. (Combines with bit 1 of CR1)	0	R/W

This register should be initialized before accessing the boot ROM space. (Write 32'hffffffff return 32'h fffe0001)

CR13 (offset = 34h), CP - Capabilities Pointer.

Bit #	Name	Descriptions	Default Val	RW Type
31~8	---	Reserved		
7~0	CP	Capabilities Pointer.	C0h	RO

CR15 (offset = 3ch), CI - Configuration Interrupt

Bit #	Name	Descriptions	Default Val	RW Type
31~24	ML	Max_Lat register. This value indicates "how often" the AN983B needs to access to the PCI bus in the units of 250ns. This value is loaded from serial EEPROM after power on or hardware reset.	From EEPROM	RO
23~16	MG	Min_Gnt register. This value indicates how long the AN983B needs to retain the PCI bus ownership whenever it initiates a transaction, in the units of 250ns. This value is loaded from serial EEPROM after power on or hardware reset.	From EEPROM	RO
15~ 8	IP	Interrupt Pin. This value indicates which of the four interrupt request pins that AN983B is connected. Always 01h: means the AN983B connects to INTA#	01h	RO
7 ~ 0	IL	Interrupt Line. This value indicates which of the system interrupt request lines the INTA# of AN983B is routed to. The BIOS will fill this field when it initializes and configures the system. The AN983B driver can use this value to determine priority and vector information.	X	R/W

CR16 (offset = 40h), DS - Driver Space for special purpose.

Bit #	Name	Descriptions	Default Val	RW Type
31~16	---	Reserved		
15~8	DS	Driver Space for special purpose. Since this area won't be cleared in the software reset. The AN983B driver can use this R/W area for special purpose.	X	R/W
7 ~ 0	---	Reserved		

(offset = 80h), SIG - Signature of AN983B

Bit #	Name	Descriptions	Default Val	RW Type
31~16	DID	Device ID, the device ID number of AN983B.	0981h	RO
15~0	VID	Vendor ID, the vendor ID number of ADM Technology Corp.	1317h	RO

CR48 (offset = c0h), PMR0, Power Management Register0.

Bit #	Name	Descriptions	Default Val	RW Type
31~27	PMES	PME_Support. The AN983B will assert PME# signal while in the D0, D1, D2, D3 power state. The AN983B supports Wake-up from the above states.	11111b	RO
26	D2S	D2_Support. The AN983B supports D2 Power Management State.	1	RO
25	D1S	D1_Support. The AN983B supports D1 Power Management State.	1	RO
24~22	AUXC	Aux Current. These three bits report the maximum 3.3 Vaux current requirements for AN983B. If bit 31 of PMR0 is '1', the default value is 0101b, means AN983B need 100 mA to support remote wake-up in D3cold power state.	010b	RO
21	DSI	The Device Specific Initialization bit indicates whether special initialization of this function is required before the generic class device driver is able to use it. 0: indicates that the function does not require a device specific initialization sequence following transition to the D0 un-initialized state.	0	RO
20	---	Reserved.	0	RO
19	PMEC	PME Clock. When "1" indicates that the AN983B relies on the presence of the PCI clock for PME# operation. While "0" indicates the no PCI clock is required for the AN983B to generate PME#.	0	RO
18~16	VER	Version. The value of 010b indicates that the AN983B complies with Revision 1.1 of the PCI Power Management Interface Specification.	010b	RO
15~8	NIP	Next Item Pointer. This value is always 0h, indicates that there is no additional items in the Capabilities List.	00h	RO
7~0	CAPID	Capability Identifier. This value is always 01h, indicates the link list item as being PCI Power Management Registers.	01h	RO

CR49 (offset = c4h), PMR1, Power Management Register 1.

Bit #	Name	Descriptions	Default Val	RW Type
31~16	---	Reserved		
15	PMES	PME_Status, This bit is set when the AN983B would normally assert the PME# signal for wake-up event, this bit is independent of the state of the PME-En bit. Writing a "1" to this bit will clear it and cause the AN983B to stop asserting a PME# (if enabled). Writing a "0" has no effect.	**0**	R/W*
14,13	DSCAL	Data_Scale, indicates the scaling factor to be used when	00b	RO

		interpreting the value of the Data register. This field is required for any function that implements the Data register. Otherwise, it's optional. The AN983B doesn't support Data register and Data_Scale.		
12~9	DSEL	Data_Select, This four-bit field is used to select which data is to be reported through the Data register and Data_Scale field. This field is required for any function that implements the Data register. The AN983B doesn't support Data_select.	0000b	R/W
8	PME_En	PME_En, "1" enables the AN983B to assert PME#. When "0" disables the PME# assertion. Magic packet default enable: When Csr18<18> and csr18<19> are set to 1, than the magic packet wake up event will be default enabled (csr13<9> be set) it doesn't matter the PME_En is set or not.	**0**	R/W
7~2	---	Reserved.	000000b	RO
1,0	PWRS	PowerState, This two-bit field is used both to determine the current power state of the AN983B and to set the AN983B into a new power state. The definition of this field is given below. 00b - D0 01b - D1 10b - D2 11b - D3hot This field is auto cleared to D0 when power resumed.	00b	R/W

R/W*: Read and Write clear

7.2. PCI CONTROL/STATUS REGISTERS

7.2.1. PCI CONTROL/STATUS REGISTERS LIST

Offset from base address of CSR	Index	Name	Descriptions
00h	CSR0	PAR	PCI access register
08h	CSR1	TDR	Transmit demand register
10h	CSR2	RDR	Receive demand register
18h	CSR3	RDB	Receive descriptor base address
20h	CSR4	TDB	Transmit descriptor base address
28h	CSR5	SR	Status register
30h	CSR6	NAR	Network access register
38h	CSR7	IER	Interrupt enable register
40h	CSR8	LPC	Lost packet counter
48h	CSR9	SPR	Serial port register
50h	CSR10	---	Reserved
58h	CSR11	TMR	Timer
60h	CSR12	---	Reserved
68h	CSR13	---	Reserved
70h	CSR14	---	Reserved
78h	CSR15	WTMR	Watchdog timer
80h	CSR16	ACSR5	Status register 2
84h	CSR17	ACSR7	Interrupt enable register 2
88h	CSR18	CR	Command register
8ch	CSR19	PCIC	PCI bus performance counter
90h	CSR20	PMCSR	Power Management Command and Status
94h	CSR21	WTDP	Current transmit descriptor point
98h	CSR22	WRDP	Current receive descriptor point
9ch	CSR23	TXBR	Transmit burst counter/time-out register
a0h	CSR24	FROM	Flash (boot) ROM port
a4h	CSR25	PAR0	Physical address register 0
a8h	CSR26	PAR1	Physical address register 1
ach	CSR27	MAR0	Multicast address hash table register 0
b0h	CSR28	MAR1	Multicast address hash table register 1
fch		OPR	Operation Mode register

7.2.2. CONTROL/STATUS REGISTER DESCRIPTION

CSR0 (offset = 00h), PAR - PCI Access Register

Bit #	Name	Descriptions	Default Val	RW Type
31~25	---	Reserved		
24	MWIE	Memory Write and Invalidate Enable. 1: enable AN983B to generate memory write invalidate command. AN983B will generate this command while writing full cache lines. 0: disable AN983B to generate memory write invalidate command and use memory write commands instead.	0	R/W*
23	MRLE	Memory Read Line Enable. 1: enable AN983B to generate memory read line command, while read access instruction reach the cache line boundary. If the read access instruction doesn't reach the cache line boundary then AN983B uses the memory read command instead.	0	R/W*
22	---	Reserved		
21	MRME	Memory Read Multiple Enable. 1: enable AN983B to generate memory read multiple commands while reading full cache line. If the memory is not cache aligned, the AN983B uses memory read command instead.	0	R/W*
20~19	---	Reserved		
18,17	TAP	Transmit auto-polling in transmit suspended state, 00: disable auto-polling (default) 01: polling own-bit every 200 us 10: polling own-bit every 800 us 11: polling own-bit every 1600 us	00	R/W*
16	---	Reserved		
15, 14	CAL	Cache alignment, address boundary for data burst, set after reset 00: reserved (default) 01: 8 DW boundary alignment 10: 16 DW boundary alignment 11: 32 DW boundary alignment	00	R/W*
13 ~ 8	PBL	Programmable Burst Length. This value defines the maximum number of DW to be transferred in one DMA transaction. Value: 0 (unlimited), 1, 2, 4, 8, 16(default), 32	010000	R/W*
7	BLE	Big or Little Endian selection. 0: little endian (e.g. INTEL) 1: big endian (only for data buffer)	0	R/W*

6 ~ 2	DSL	Descriptor Skip Length. Defines the gap between two descriptions in the units of DW.	0	R/W*
1	BAR	Bus arbitration 0: receive higher priority 1: transmit higher priority	0	R/W*
0	SWR	Software reset 1: reset all internal hardware, except configuration registers. This signal will be cleared by AN983B itself after it completed the reset process.	0	R/W*

R/W* = before writing the transmit and receive operations should be stopped.

CSR1 (offset = 08h), TDR - Transmit demand register

Bit #	Name	Descriptions	Default Val	RW Type
31~ 0	TPDM	Transmit poll demand When written any value in suspended state, trigger read-tx-descriptor process and check the own-bit, if own-bit = 1, then start transmit process	ffffffffh	R/W*

R/W* = before writing the transmit process should be in the suspended state.

CSR2 (offset = 10h), RDR - Receive demand register

Bit #	Name	Descriptions	Default Val	RW Type
31 ~ 0	RPDM	Receive poll demand When written any value in suspended state, trigger the read-rx-descriptor process and check own-bit, if own-bit = 1, then start move data to buffer from FIFO	ffffffffh	R/W*

R/W* = before writing the receive process should be in the suspended state.

CSR3 (offset = 18h), RDB - Receive descriptor base address

Bit #	Name	Descriptions	Default Val	RW Type
31~ 2	SAR	Start address of receive descriptor	xxxxxxx	R/W*
1, 0	RBND	Must be 00, DW boundary	00	RO

R/W* = before writing the receive process should be stopped.

CSR4 (offset = 20h), TDB - Transmit descriptor base address

Bit #	Name	Descriptions	Default Val	RW Type
31~ 2	SAT	Start address of transmit descriptor	xxxxxx	R/W*
1, 0	TBND	Must be 00, DW boundary	00	RO

R/W* = before writing the transmit process should be stopped.

CSR5 (offset = 28h), SR - Status register

Bit #	Name	Descriptions	Default Val	RW Type
31~ 26	----	Reserved		
25~ 23	BET	Bus Error Type. This field is valid only when bit 13 of CSR5 (fatal bus error) is set. There is no interrupt generated by this field.	000	RO

		000: parity error, 001: master abort, 010: target abort 011, 1xx: reserved		
22~ 20	TS	Transmit State. Report the current transmission state only, no interrupt will be generated. 000: stop 001: read descriptor 010: transmitting 011: FIFO fill, read the data from memory and put into FIFO 100: reserved 101: reserved 110: suspended, unavailable transmit descriptor or FIFO overflow 111: write descriptor	000	RO
19~17	RS	Receive State. Report current receive state only, no interrupt will be generated. 000: stop 001: read descriptor 010: check this packet and pre-fetch next descriptor 011: wait for receiving data 100: suspended 101: write descriptor 110: flush the current FIFO 111: FIFO drain, move data from receiving FIFO into memory	000	RO
16	NISS	Normal Interrupt Status Summary. It's set if any of below bits of CSR5 asserted. (Combines with bit 16 of ACSR5) bit0, transmit completed interrupt bit2, transmit descriptor unavailable bit6, receive descriptor interrupt	0	RO/LH*
15	AISS	Abnormal Interrupt Status Summary. It's set if any of below bits of CSR5 asserted. (Combines with bit 15 of ACSR5) bit1, transmit process stopped bit3, transmit jabber timer time-out bit5, transmit under-flow bit7, receive descriptor unavailable bit8, receive processor stopped bit9, receive watchdog time-out bit11, general purpose timer time-out bit13, fatal bus error	0	RO/LH*
14	----	Reserved		
13	FBE	Fatal Bus Error. 1: while any of parity error, master abort, or target abort is occurred (see bits 25~23 of CSR5). AN983B will disable all bus access. The way to recover parity error is by setting software reset.	0	RO/LH*

12	---	Reserved		
11	GPTT	General Purpose Timer Time-out, base on CSR11 timer register	0	RO/LH*
10	---	Reserved		
9	RWT	Receive Watchdog Time-out, based on CSR15 watchdog timer register	0	RO/LH*
8	RPS	Receive Process Stopped, receive state = stop	0	RO/LH*
7	RDU	Receive Descriptor Unavailable 1: while the next receive descriptor can't be applied by AN983B. The receive process is suspended in this situation. To restart the receive process, the ownership bit of next receive descriptor should be set to AN983B and a receive poll demand command should be issued (or a new recognized frame is received, if the receive poll demand is not issued).	0	RO/LH*
6	RCI	Receive Completed Interrupt 1: while a frame reception is completed.	0	RO/LH*
5	TUF	Transmit Under-Flow 1: while the transmit FIFO had an under-flow condition happened during transmitting. The transmit process will enter the suspended state and report the under-flow error on bit1 of TDES0.	0	RO/LH*
4	---	Reserved		
3	TJT	Transmit Jabber Timer Time-out 1: while the transmit jabber timer expired. The transmit processor will enter the stop state and the transmit jabber time-out flag of bit 14 of TDES0 will be asserted.	0	RO/LH*
2	TDU	Transmit Descriptor Unavailable 1: while the next transmit descriptor can't be applied by AN983B. The transmission process is suspended in this situation. To restart the transmission process, the ownership bit of next transmit descriptor should be set to AN983B and if the transmit automatic polling is not enabled then a transmit poll demand command should be issued.	0	RO/LH*
1	TPS	Transmit Process Stopped. 1: while transmit state = stop	0	RO/LH*
0	TCI	Transmit Completed Interrupt. 1: means a frame transmission is completed while bit 31 of TDES1 is asserted in the first transmit descriptor of the frame.	0	RO/LH*

LH = High Latching and cleared by writing 1.

CSR6 (offset = 30h), NAR - Network access register

Bit #	Name	Descriptions	Default Val	RW Type

31~22	---	Reserved		
21	SF	Store and forward for transmit 0: disable 1: enable, ignore the transmit threshold setting	0	R/W*
20	---	Reserved		
19	SQE	SQE Disable 0: enable SQE function for 10BASE-T operation. The AN983B provides SQE test function for 10BASE-T half duplex operation. 1: disable SQE function.	1	R/W*
18~16	-----	Reserved		
15~14	TR	Transmit threshold control 00: 128-byte (100Mbps), 72-byte (10Mbps) 01: 256-byte (100Mbps), 96-byte (10Mbps) 10: 512-byte (100Mbps), 128-byte (10Mbps) 00: 1024-byte (100Mbps), 160-byte (10Mbps)	00	R/W*
13	ST	Stop transmit 0: stop (default) 1: start	0	R/W
12	FC	Force collision mode 0: disable 1: generate collision when transmit (for test in loop-back mode)	0	R/W**
11, 10	OM	Operating Mode 00: normal 01: MAC loop-back 10,11: reserved	00	R/W**
9, 8	---	Reserved		
7	MM	Multicast Mode 1: receive all multicast packets	0	R/W***
6	PR	Promiscuous Mode 1: receive any good packet. 0: receive only the right destination address packets	1	R/W***
5	SBC	Stop Back-off Counter 1: back-off counter stop when carrier is active, and resume when carrier drop. 0: back-off counter is not effected by carrier	0	R/W**
4	---	Reserved		
3	PB	Pass Bad packet 1: receives any packets, if pass address filter, including runt packets, CRC error, truncated packets... For receiving all bad packets, the bit 6 of CSR6 should be set to 1.	0	R/W***

		0: filters all bad packets		
2	---	Reserved		
1	SR	Start/Stop Receive 0: receive processor will enter stop state after the current reception frame completed. This value is effective only when the receive processor is in the running or suspending state. Notice: In "Stop Receive" state, the PAUSE packet and Remote Wake Up packet won't be affected and can be received if the corresponding function is enabled. 1: receive processor will enter running state.	0	R/W
0	---	Reserved		

W* = only write when the transmit processor stopped.
W** = only write when the transmit and receive processor both stopped.
W*** = only write when the receive processor stopped.

CSR7 (offset = 38h), IER - Interrupt Enable Register

Bit #	Name	Descriptions (Refer to CSR5)	Default Val	RW Type
31~17	---	Reserved		
16	NIE	Normal Interrupt Enable 1: enable all the normal interrupt bits (see bit16 of CSR5)	0	R/W
15	AIE	Abnormal Interrupt Enable 1: enable all the abnormal interrupt bits (see bit 15 of CSR5)	0	R/W
14	---	Reserved		
13	FBEIE	Fatal Bus Error Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable fatal bus error interrupt	0	R/W
12				
11	GPTIE	General Purpose Timer Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable general-purpose timer expired interrupt.	0	R/W
10				
9	RWTIE	Receive Watchdog Time-out Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable receive watchdog time-out interrupt.	0	R/W
8	RSIE	Receive Stopped Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable receive stopped interrupt.	0	R/W
7	RUIE	Receive Descriptor Unavailable Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable receive descriptor unavailable interrupt.	0	R/W
6	RCIE	Receive Completed Interrupt Enable	0	R/W

		1: combine this bit and bit 16 of CSR7 to enable receive completed interrupt.		
5	TUIE	Transmit Under-flow Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable transmit under-flow interrupt.	0	R/W
4	---	Reserved		
3	TJTTIE	Transmit Jabber Timer Time-out Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable transmit jabber timer time-out interrupt.	0	R/W
2	TDUIE	Transmit Descriptor Unavailable Interrupt Enable 1: combine this bit and bit 16 of CSR7 to enable transmit descriptor unavailable interrupt.	0	R/W
1	TPSIE	Transmit Processor Stopped Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable transmit processor stopped interrupt.	0	R/W
0	TCIE	Transmit Completed Interrupt Enable 1: combine this bit and bit 16 of CSR7 to enable transmit completed interrupt.	0	R/W

CSR8 (offset = 40h), LPC - Lost packet counter

Bit #	Name	Descriptions	Default Val	RW Type
31~17	---	Reserved		
16	LPCO	Lost Packet Counter Overflow 1: while lost packet counter overflowed. Cleared after read	0	RO/LH
15~0	LPC	Lost Packet Counter Increment the counter while packet discarded since there was no host receives descriptors available. Cleared after read	0	RO/LH

CSR9 (offset = 48h), SPR - Serial port register

Bit #	Name	Descriptions	Default Val	RW Type
31~20	---	Reserved		
19	MDI	MII Management Data Input Specified read data from the external PHY	0	R/W
18	MMC	MII Management Control 0: Write operation to the external PHY 1: Read operation from the external PHY	1	R/W
17	MDO	MII Management Data Output Specified Write Data to the external PHY	0	R/W
16	MDC	MII Management Clock 1: MII Management Clock is a output reference clock to the external PHY	0	R/W

15	---	Reserved		
14	SRC	Serial EEPROM Read Control Set together with CSR9 bit11 to enable read operation from EEPROM	0	R/W
	SWC	Serial EEPROM Write Control Set together with CSR9 bit11 to enable write operation to EEPROM	0	R/W
12	---	Reserved		
11	SRS	Serial EEPROM Select Set together with CSR9 bit14 or 13 to enable EEPROM access	0	R/W
10~4	---	Reserved		
3	SDO	Serial EEPROM data out This bit serially shifts data from the EEPROM to the AN983B.	1	RO
2	SDI	Serial EEPROM data in This bit serially shifts data from the AN983B to the EEPROM.	1	R/W
	SCLK	Serial EEPROM clock High/Low this bit to provide the clock signal for EEPROM.	1	R/W
0	SCS	Serial EEPROM chip select 1: selects the serial EEPROM chip.	0	R/W

CSR11 (offset = 58h), TMR -General-purpose Timer

Bit #	Name	Descriptions	Default Val	RW Type
31~17	---	Reserved		
16	COM	Continuous Operation Mode 1: sets the general-purpose timer in continuous operating mode.	0	R/W
15~0	GTV	General-purpose Timer Value Sets the counter value. This is a countdown counter with the cycle time of 204us.	0	R/W

CSR13 (offset = 68h), WCSR –Wake-up Control/Status Register

Bit #	Name	Descriptions	Default Val	RW Type
31	---	Reserved		
30	CRCT	CRC-16 Type 0: Initial contents = 0000h 1: Initial contents = FFFFh	0	R/W
29	WP1E	Wake-up Pattern One Matched Enable.	0	R/W
28	WP2E	Wake-up Pattern Two Matched Enable.	0	R/W
27	WP3E	Wake-up Pattern Three Matched Enable.	0	R/W

26	WP4E	Wake-up Pattern Four Matched Enable.	0	R/W
25	WP5E	Wake-up Pattern Five Matched Enable.	0	R/W
24-18	---	Reserved		
17	LinkOFF	Link Off Detect Enable. The AN983B will set the LSC bit of CSR13 after it has detected that link status is from ON to OFF.	0	R/W
16	LinkON	Link On Detect Enable. The AN983B will set the LSC bit of CSR13 after it has detected that link status is from OFF to ON.	0	R/W
15-11	---	Reserved	00001	
10	WFRE	Wake-up Frame Received Enable. The AN983B will include the "Wake-up Frame Received" event into wake-up events. If this bit is set, AN983B will assert PMES bit of PMR1 after AN983B has received a matched wake-up frame.	0	R/W
9	MPRE	Magic Packet Received Enable. The AN983B will include the "Magic Packet Received" event into wake-up events. If this bit is set, AN983B will assert PMES bit of PMR1 after AN983B has received a Magic packet.	0	R/W
8	LSCE	Link Status Changed Enable. The AN983B will include the "Link Status Changed" event into wake-up events. If this bit is set, AN983B will assert PMES bit of PMR1 after AN983B has detected a link status changed event.	0	R/W
7-3	---	Reserved		
2	WFR	Wake-up Frame Received, 1: Indicates AN983B has received a wake-up frame. It is cleared by write 1 or upon power-up reset. It is not affected by a hardware or software reset.	X	R/W1C*
1	MPR	Magic Packet Received, 1: Indicates AN983B has received a magic packet. It is cleared by write 1 or upon power-up reset. It is not affected by a hardware or software reset.	X	R/W1C*
0	LSC	Link Status Changed, 1: Indicates AN983B has detected a link status change event. It is cleared by write 1 or upon power-up reset. It is not affected by a hardware or software reset.	X	R/W1C*

R/W1C*, Read only and Write one cleared.

CSR14 (offset = 70h), WPDR –Wake-up Pattern Data Register

All six wake-up patterns filtering information are programmed through WPDR register. The filtering information is as follows,

Offset	**31 16**	**15 8**	**7 0**
0000h	Wake-up pattern 1 mask bits 31:0		
0004h	Wake-up pattern 1 mask bits 63:32		

0008h	Wake-up pattern 1 mask bits 95:64		
000ch	Wake-up pattern 1 mask bits 127:96		
0010h	CRC16 of pattern 1	Reserved	Wake-up pattern 1 offset
0014h	Wake-up pattern 2 mask bits 31:0		
0018h	Wake-up pattern 2 mask bits 63:32		
001ch	Wake-up pattern 2 mask bits 95:64		
0020h	Wake-up pattern 2 mask bits 127:96		
0024h	CRC16 of pattern 2	Reserved	Wake-up pattern 2 offset
0028h	Wake-up pattern 3 mask bits 31:0		
002ch	Wake-up pattern 3 mask bits 63:32		
0030h	Wake-up pattern 3 mask bits 95:64		
0034h	Wake-up pattern 3 mask bits 127:96		
0038h	CRC16 of pattern 3	Reserved	Wake-up pattern 3 offset
003ch	Wake-up pattern 4 mask bits 31:0		
0040h	Wake-up pattern 4 mask bits 63:32		
0044h	Wake-up pattern 4 mask bits 95:64		
0048h	Wake-up pattern 4 mask bits 127:96		
004ch	CRC16 of pattern 4	Reserved	Wake-up pattern 4 offset
0050h	Wake-up pattern 5 mask bits 31:0		
0054h	Wake-up pattern 5 mask bits 63:32		
0058h	Wake-up pattern 5 mask bits 95:64		
005ch	Wake-up pattern 5 mask bits 127:96		
0060h	CRC16 of pattern 5	Reserved	Wake-up pattern 5 offset

1. Offset value is from 0-255 (8-bit width).
2. To load the whole wake-up frame-filtering information, consecutive 25 long words write operation to CSR14 should be done.

CSR15 (offset = 78h), WTMR - Watchdog timer

Bit #	Name	Descriptions	Default Val	RW Type
31~29		Reserved		
28	MRXCK	MII Rx clock reverse 1: reverse (for NS HomePHY 1M only) 0: NOT reverse	0 from EEPROM	R
27~6		Reserved		R
5	RWR	Receive Watchdog Release, the time of release	0	R/W

		watchdog timer from last carrier deserted. 0: 24 bit-time 1: 48 bit-time		
4	RWD	Receive Watchdog Disable 0: If the receiving packet's length is longer than 2560 bytes, the watchdog timer will be expired. 1: disable the receive watchdog.	0	R/W
3	---	Reserved		
2	JCLK	Jabber clock 0: cut off transmission after 2.6 ms (100Mbps) or 26 ms (10Mbps). 1: cut off transmission after 2560 byte-time.	0	R/W
1	NJ	Non-Jabber 0: if jabber expired, re-enable transmit function after 42 ms (100Mbps) or 420ms (10Mbps) 1: immediately re-enable the transmit function after jabber expired	0	R/W
0	JBD	Jabber disable 1: disable transmit jabber function	0	R/W

CSR16 (offset = 80h), ACSR5 - Assistant CSR5 (Status register 2)

Bit #	Name	Descriptions	Default Val	RW Type
31	TEIS	Transmit Early Interrupt status Transmit early interrupt status is set to 1 when Transmit early interrupt function is enabled (set bit 31 of CSR17 = 1) and the transmitted packet is moved completed from descriptors to TX-FIFO buffer. This bit is cleared by written with 1.	0	RO/LH*
30	REIS	Receive Early Interrupt Status. Receive early interrupt status is set to 1 when Receive early interrupt function is enabled (set bit 30 of CSR17 = 1) and the received packet is fill up its first receive descriptor. This bit is cleared by written with 1.	0	RO/LH*
29	LCS	Status of Link status change	0	RO/LH*
28	TDIS	Transmit Deferred Interrupt Status.	0	RO/LH*
27	---	Reserved		
26	PFR	PAUSE Frame Received Interrupt Status 1: indicates a PAUSE frame received when the PAUSE function is enabled.	0	RO/LH*
25~17	---	Reserved		
16	ANISS	Added normal interrupt status summary. 1: any of the added normal interrupts happened.	0	RO/LH*

15	AAISS	Added Abnormal Interrupt Status Summary. 1: any of added abnormal interrupt happened.	0	RO/LH*
14~0		These bits are the same as the status register of CSR5. You can access those status bits through either CSR5 or CSR16.		RO/LH*

LH* = High Latching and cleared by writing 1.

CSR17 (offset = 84h), ACSR7- Assistant CSR7 (Interrupt enable register 2)

Bit #	Name	Descriptions	Default Val	RW Type
31	TEIE	Transmit Early Interrupt Enable	0	R/W
30	REIE	Receive Early Interrupt Enable	0	R/W
29	LCIE	Link Status Change Interrupt Enable	0	R/W
28	TDIE	Transmit Deferred Interrupt Enable	0	R/W
27	---	Reserved		
26	PFRIE	PAUSE Frame Received Interrupt Enable	0	R/W
25~17	---	Reserved		
16	ANISE	Added Normal Interrupt Summary Enable. 1: adds the interrupts of bit 30 and 31 of ACSR7 to the normal interrupt summary (bit 16 of CSR5).	0	R/W
15	AAIE	Added Abnormal Interrupt Summary Enable. 1: adds the interrupt of bit 26, 28 and 29 of ACSR7 to the abnormal interrupt summary.	0	R/W
14~0		These bits are the same as the interrupt enable register of CSR7. You can access those interrupt enable bits through either CSR7 or CSR16.		R/W

CSR18 (offset = 88h), CR - Command Register, bit31 to bit16

Automatically recall from EEPROM

Bit #	Name	Descriptions	Default Val	RW Type
31	D3CS	D3cold support, mapped to CR48<31>	1 From EEPROM	R/W
30-28	AUXCL	Aux Current. These three bits report the maximum 3.3 Vaux current requirements for AN983B. If bit 31 of PMR0 is '1', the default value is 0101b, means AN983B need 100 mA to support remote wake-up in D3cold power state.	010b From EEPROM	RO
27	PMEP	Actively type select 1: create a negative 50ms pulse 0: create a positive 50ms pulse This bit is only active when PMEP enable CSR18 bit 26	0 from EEPROM	R/W
26	PMEPEN	PMEP pin enable 1: enable 0: disable (this pin will be input, to compatible with AN983 circuit)	0 from EEPROM	R/W

25	PWRS_clr	1: PCI_reset rising will automatically reset CR49/ PWRS[1:0] to 00h.	0 from EERROM	R/W
24	Pmes_sticky	1: pmez sticky: While pmez signal is asserted by wake up event, it cannot be auto de-asserted. The software should clear CR49<15> PMES bit to de-assert the pmez signal. 0: pmez auto de-asserted: While pmez signal is asserted by wake up event, it will be de-asserted by power up automatically.	0 From EEPROM	R/W
23	4_3LED	If this bit is reset, 3 LED mode is selected, the LEDs definition is: 100/10 speed Link/Activity Full Duplex/Collision If this bit is set, 4 LED mode is selected, the LEDs definition is: 100 Link 10 Link Activity Full Duplex/Collision	0 From EEPROM	R/W
22, 21	RFS	Receive FIFO size control 11: 1K 10: 2K 01,00: reserved	10 From EEPROM	R/W
20	CRD	Clock Run (clk-run pin) disable 1: disables the function of clock run supports to PCI.	0 From EEPROM	R/W
19	PM	Power Management, enables the AN983B whether to activate the Power Management abilities. When this bit is set into "0" the AN983B will set the Cap_Ptr register to zero, indicating no PCI compliant power management capabilities. The value of this bit will be mapped to NC-bit 20 of CR1. In PCI Power Management mode, the Wake-up events include "Wake-up Frame Received", "Magic Packet Received" and "Link Status Changed" depends on the CSR13 settings	1 From EEPROM	RO
18	APM	APM mode, this bit is effective when PM (csr18 [19]) =1 1: Magic Packet wake-up event default enable 0: Magic Packet wake-up event default disable	1 From EEPROM	R/W
17	LWS	Should be 0	0 From EEPROM	R/W
16~8	----	Reserved		
7	D3_APM	D3_cold APM_mode_en for PC99 certification It doesn't matter the status of PEM_EN, the pmez signal can be asserted by programming this bit 1: Assert pmez signal	0	R/W

		0: de-assert pmez signal		
6	RWP	Reset Wake-up Pattern Data Register Pointer 0: Normal 1: Reset	0	R/W
5	PAUSE	PAUSE function control to disable or enable the PAUSE function for flow control. The default value of PAUSE is decided by the result of Auto-Negotiation. Driver can force to enable or disable it after the Auto-Negotiation completed. 0: PAUSE function is disabled. 1: PAUSE function is enabled	0	R/W
4	RTE	Receive Threshold Enable. 1: the receive FIFO threshold is enabled. 0: disable the receive FIFO threshold selection in bit 3~2 of this register, the receive threshold is set to 64-byte.	0	R/W
3~2	DRT	Drain Receive Threshold 00: 32 bytes (8 DW) 01: 64 bytes (16 DW) 10: store-and -forward 11: reserved	01	R/W
1	SINT	Software interrupt.	0	R/W
0	ATUR	1: enable automatically transmit-underrun recovery.	0	R/W

CSR19 (offset = 8ch) - PCIC, PCI bus performance counter

Bit #	Name	Descriptions	Default Val	RW Type
31~16	CLKCNT	The number of PCI clock from read request asserted to access completed. This PCI clock number is accumulated all the read command cycles from last CSR19 read to current CSR19 read.	0	RO*
15~8	---	Reserved		
7~0	DWCNT	The number of double word accessed by the last bus master. This double word number is accumulated all the bus master data transactions from last CSR19 read to current CSR19 read.	0	RO*

RO* = Read only and cleared by reading.

CSR20 (offset = 90h) - PMCSR, Power Management Command and Status

(The same register value mapping to CR49-PMR1.)

Bit #	Name	Descriptions	Default Val	RW Type
31~16	---	Reserved		
15	PMES	PME_Status, This bit is set when the AN983B would normally assert the PME# signal for wakeup event, this bit is independent of the state of the PME-En bit. Writing a "1" to this bit will clear it and cause the AN983B to stop asserting a PME#(if enabled). Writing a "0" has no	0	RO

		effect. Since the AN983B doesn't supports PME# from D3cold, this bit is defaulted to "0".		
14,13	DSCAL	Data_Scale, indicates the scaling factor to be used when interpreting the value of the Data register. This field is required for any function that implements the Data register. Otherwise, it's optional. The AN983B doesn't support Data register and Data_Scale.	00b	RO
12~9	DSEL	Data_Select, This four bit field is used to select which data is to be reported through the Data register and Data_Scale field. This field is required for any function that implements the Data register. The AN983B doesn't support Data_select.	0000b	RO
8	PME_En	PME_En, "1" enables the AN983B to assert PME#. When "0" disables the PME# assertion. This bit defaults to "0" if the function does not support PME# generation from D3cold.	0	RO
7~2	---	Reserved.	000000b	RO
1,0	PWRS	PowerState, This two bit field is used both to determine the current power state of the AN983B and to set the AN983B into a new power state. The definition of this field is given below. 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus, however the data is discarded a no state change occurs.	00b	RO

CSR21 (offset = 94h) - WTDP, The current working transmit descriptor pointer

Bit #	Name	Descriptions	Default Val	RW Type
31~0	WTDP	The current working transmit descriptor pointer for driver's double-checking or other special purpose.	XXXX	RO

CSR22 (offset = 98h) - WRDP, The current working receive descriptor pointer

Bit #	Name	Descriptions	Default Val	RW Type
31~0	WRDP	The current working receive descriptor pointer for driver's double-checking or other special purpose.	XXXX	RO

CSR23 (offset = 9ch) - TXBR, transmit burst count / time-out

Bit #	Name	Descriptions	Default Val	RW Type
31~21	---	Reserved		

20~16	TBCNT	Transmit Burst Count After this number of consecutive successful transmit, transmit completed interrupt will be generated. Continuously do this function if no reset.	0	R/W
11~0	TTO	Transmit Time-Out = (deferred time + back-off time). When the TDIE (bit28 of ACSR7) is set, the timer is decreased in unit of 2.56us(100M) or 25.6us(10M). If the timer expires before another packet transmit begin, then the TDIE interrupt will be generated.	0	R/W

CSR24 (offset = a0h) - FROM, Flash ROM (also the boot ROM) port

Bit #	Name	Descriptions	Default Val	RW Type
31	Bra16_on	This bit is only effective while 4 LED mode selected (bit 23 of CSR18 is set). When 4 LED mode selected, and this bit is set, then pin 105 is defined as brA16, else it is defined as LED pin – fd/col.	1	R/W
30~28	---	Reserved		
27	REN	Read enable, clear if read data is ready in DATA, bit7-0 of FROM.	0	R/W
26	WEN	Write enable, cleared if write completed	0	R/W
25~8	ADDR	Flash ROM address	0	R/W
7~0	DATA	Read/Write data of flash ROM	0	R/W

CSR25 (offset = a4h) - PAR0, physical address register 0

Automatically recall from EEPROM

Bit #	Name	Descriptions	Default Val	RW Type
31~24	PAB3	Physical address byte 3	From EEPROM	R/W
23~16	PAB2	Physical address byte 2	From EEPROM	R/W
15~8	PAB1	Physical address byte 1	From EEPROM	R/W
7~0	PAB0	Physical address byte 0	From EEPROM	R/W

CSR26 (offset = a8h) - PAR1, physical address register 1

Automatically recall from EEPROM

Bit #	Name	Descriptions	Default Val	RW Type
31~24	---	Reserved		
23~16	---	Reserved		
15~8	PAB5	Physical address byte 5	From EEPROM	R/W
7~0	PAB4	Physical address byte 4	From EEPROM	R/W

For example, physical address = 00-00-e8-11-22-33

PAR0= 11 e8 00 00

PAR1= xx xx 33 22

PAR0 and PAR1 are readable, but can be written only if the receive state is in stopped (CSR5 bit19-17=000).

CSR27 (offset = ach) - MAR0, multicast address register 0

Bit #	Name	Descriptions	Default Val	RW Type
31~24	MAB3	Multicast address byte 3 (hash table 31:24)	0	R/W
23~16	MAB2	Multicast address byte 2 (hash table 23:16)	0	R/W
15~8	MAB1	Multicast address byte 1 (hash table 15:8)	0	R/W
7~0	MAB0	Multicast address byte 0 (hash table 7:0)	0	R/W

CSR28 (offset = b0h) - MAR1, multicast address register 1

Bit #	Name	Descriptions	Default Val	RW Type
31~24	MAB7	Multicast address byte 7 (hash table 63:56)	0	R/W
23~16	MAB6	Multicast address byte 6 (hash table 55:48)	0	R/W
15~8	MAB5	Multicast address byte 5 (hash table 47:40)	0	R/W
7~0	MAB4	Multicast address byte 4 (hash table 39:32)	0	R/W

MAR0 and MAR1 are readable, but can be written only if the receive state is in stopped (CSR5 bit19-17=000).

Multicast 64 Algorithm:

AN983B uses CRC [5:0] to hit one of the 64 entries in UMAR1 [31:0] and MAR0[31:0] by generated CRC32 from Ethernet DA (destination address).

The most significant bit CRC [5] choose the upper or lower double word, (MAR1 or MAR0), the lower 5 bit present for the corresponding bit inside the double word.

Example 1:

If CRC [5] =1'b0 --> hit MAR0

CRC [4:0] = 5'b00010 --> hit MAR0 [2]

Example 2:

CRC [5] = 1'b1 --> hit MAR1

CRC [4:0] = 5'b00100--> hit MAR1 [4]

CSR_29 (offset = b4h) - UAR0, unicast address register 0

Bit #	Name	Descriptions	Default Val	RW Type
31~24	UAB3	Unicast address byte 3 (hash table 31:24)	0	R/W
23~16	UAB2	Unicast address byte 2 (hash table 23:16)	0	R/W
15~8	UAB1	Unicast address byte 1 (hash table 15:8)	0	R/W
7~0	UAB0	Unicast address byte 0 (hash table 7:0)	0	R/W

CSR_30(offset = b8h) - UAR1, unicast address register 1

Bit #	Name	Descriptions	Default Val	RW Type
31~24	UAB7	Unicast address byte 7 (hash table 63:56)	0	R/W
23~16	UAB6	Unicast address byte 6 (hash table 55:48)	0	R/W
15~8	UAB5	Unicast address byte 5 (hash table 47:40)	0	R/W
7~0	UAB4	Unicast address byte 4 (hash table 39:32)	0	R/W

Unicast64 Algorithm:

The algorithm is the with multicast64.

Operation Mode Register (offset 0FCh)

Bit #	Name	Descriptions	Default Val	RW Type
31	SPEED	Network Speed Status 1: 100M 0: 10M	0	RO
30	FD	Full/Half Duplex Status 1: Full duplex 0: Half duplex	0	RO
29	LINK	Network Link Status 1: Link On 2: Link Off	0	RO
28~27	Reserved			
26	EERLOD	Write 1 to this bit will cause AN983B to reload data from EEPROM. After reload completed, this bit will be cleared automatically.	0	R/W
25~3	Reserved			
2~0	OpMode	These three bits are used to configure AN983B's operation mode: 111b: Single Chip mode (Normal operation) At this mode, AN983B is configured as single chip to provide PCI to Ethernet controller. 100b: MAC-only mode The AN983B is configured as a MAC only controller, it provide standard MII interface to link to the external PHY. The MII interface pins are multiplexed with BootROM interface. Others: For diagnostic purpose.	111b	R/W

7.3. PHY REGISTERS (ACCESSED BY CSR9 MDI/MMC/MDO/MDC)

7.3.1. TRANSCEIVER REGISTERS DESCRIPTIONS

Register 0 (MII Control)

BIT	NAME	DESCRIPTION	Read/Write	DEFAULT
15	Reset	1 = PHY Reset 0 = normal operation	R/W, SC	0
14	Loopback	1 = enable loopback 0 = disable loopback	R/W	0
13	Speed selection	1 = 100Mbps/s 0 = 10 Mb/s	R/W	Pin - see note
12	Autonegotiation enable	1 = enable autoneg 0 = disable autoneg	R/W	Pin – see note
11	Power down	1 = Power Down 0 = normal operation	R/W	0
10	Isolate	1 = isolate PHY from MII 0 = normal operation	R/W	0
9	Restart autonegotiation	1 = Restart Autoneg	R/W, SC	0
8	Duplex mode	1 = full, 0 = half	R/W	Pin – see note
7	Collision test	Not implemented	RO	0 - see note
6:0	Reserved		RO	0000000

SC Self Clearing

Reset Reset this port only. This will cause the following:

1. Restart the autonegotiation process.
2. Reset the registers to their default values. Note that this does not affect registers 20, 22, 30 or 31. These registers are not reset by this bit to allow test configurations to be written and then not affected by resetting the port.

Note: No reset is performed to analogue sections of the port. There is also no physical reset to any internal clock synthesisers or the local clock recovery oscillator which will continue to run throughout the reset period. However since the port is restarted and autoneg re-run the process of locking the frequency of the local oscillator (slave) to the reference oscillator (master) will be repeated as it is at the start of any link initialization process.

Loopback Loop back of transmit data to receive via a path as close to the wire as possible.

When set inhibits actual transmission on the wire.

Speed selection Forces speed of Phy only when autonegotiation is disabled. The default state of this bit will be determined by a power-up configuration pin in this case. Otherwise it defaults to 1.

Auto-neg enable Defaults to pin programmed value. When cleared allows forcing of speed and duplex settings. When set (after being cleared) causes re-start of autoneg process. Pin programming at power-up allows it to come up disabled and for software to write the desired capability before allowing the first negotiation to commence.

Restart Negotiation only has effect when autonegotiating. Restarts state machine.

Power down Has no effect in this device. Test mode power down modes may be implemented in other specific modules.

Isolate Puts RMII receive signals into high impedance state and ignores transmit signals.

Duplex mode When bit12 is cleared (i.e. autoneg disabled), this bit forces full duplex (bit = 1) or half duplex (bit = 0).

Collision test Always 0 because collision signal is not implemented.

Register 1 (Status):

BIT	NAME	DESCRIPTION	Read/Write	Default
15	100 BASE T4	Not supported	RO	0
14	100BASE-X Full Duplex	1 = PHY is 100BASE-X full duplex capable 0 = PHY is not 100BASE-X full duplex capable	RO	1
13	100BASE-X Half Duplex	1 = PHY is 100BASE-X half duplex capable 0 = PHY is not 100BASE-X half duplex capable	RO	1
12	10Mbps/s Full Duplex	1 = PHY is 10Mbps/s Full duplex capable 0 = PHY is not 10Mbps/s Full duplex capable	RO	1
11	10 Mb/s Half Duplex	1 = PHY is 10Mbps/s Half duplex capable 0 = PHY is not 10Mbps/s Half duplex capable	RO	1
10	100BASE-T2 full duplex	Not supported	RO	0
9	100BASE-T2 half	Not supported	RO	0

	duplex			
8-7	Reserved		RO	00
6	MF Preamble Suppression	1 = PHY can accept management frames with preamble suppression 0 = PHY cannot accept management frames with preamble suppression	RO	1
5	Autoneg Complete	1 = autoneg completed, 0 = autoneg incomplete	RO	0
4	Remote Fault	1 = remote fault detected, 0 = no remote fault detected	RO, LH	0
3	Autoneg Ability	1 = PHY can auto-negotiate, 0 = PHY cannot auto-negotiate	RO	1
2	Link Status	1 = link is up, 0 = link is down	RO, LL	0
1	Jabber Detect	1 = jabber condition detected	RO, LH	0(see note)
0	Extended Capability	1 = extended register capabilities, 0 = basic register set capabilities only	RO	1

LL Latch Low

LH Latch High

Jabber detect Only used in 10Base-T mode. Reads as 0 in 100Base-TX mode.

Register 2 and 3

Each PHY has an identifier, which is assigned to the device.

The identifier contains a total of 32 bits, which consists of the following: 22 bits of a 24bit organisationally unique identifier (OUI) for the manufacturer; a 6-bit manufacturer's model number; a 4-bit manufacturer's revision number. For an explanation of how the OUI maps to the register, please refer to IEEE 802-1990 clause 5.1

Register 2

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15:0	PHY_ID[31-16]	OUI (bits 3-18)	RO	001D(Hex)

Register 3

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15:10	PHY_ID[15-10]	OUI (bits 19-24)	RO	001001(bin)
9:4	PHY_ID[9-4]	Manufacturer's Model Number	RO	000001(bin)

		(bits 5-0)		
3:0	PHY_ID[3-0]	Revision Number (bits 3-0); Register 3, bit 0 is LS bit of PHY Identifier	RO	0001(bin)

This uses the OUI of ADMtek, device type of 1 and rev 0.

Register 4

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15	Next Page	1 = Device set to use Next Page, 0 = Device not set to use Next Page	R/W	0
14	Reserved		RO	0
13	Remote Fault	1 = Local remote fault sent to link partner 0 = no fault detected	R/W	0
12:11	Not implemented	Technology ability bits A7-A6	RO	00
10	Pause	Technology ability bit A5	R/W	0
9	Not implemented	Technology ability bit A4	RO	0
8	100BASE-TX full duplex	Technology ability bit A3 1 = Unit is capable of Full Duplex 0 = Unit is not capable of Full Duplex	R/W	0
7	100BASE-TX half duplex	Technology ability bit A2 1 = Unit is capable of Half Duplex 0 = Unit is not capable of Half Duplex 100BASE-TX	R/W	0
6	10BASE-T full duplex	Technology ability bit A1 1 = Unit is capable of Full Duplex 10BASE-T 0 = Unit is not capable of Full Duplex 10BASE-T	R/W	0
5	10BASE-T half duplex	Technology ability bit A0 1 = Unit is capable of Half Duplex 10BASE-T 0 = Unit is not capable of Half Duplex 10BASE-T	R/W	0
4:0	Selector Field	Identifies type of message being sent. Currently only one value is defined.	RO	00001

Register 5

The register is used to view the advertised capabilities of the link partner once autonegotiation is complete.

The contents of this register should not be relied upon unless register 1 bit 5 is set (autoneg complete). After negotiation this register should contain a copy of the link partner's register 4. All bits are therefore defined in the same way as for register 4.

All bits are read only.

This register is used for Base Page code word only.

Base Page Register Format

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15	Next Page	1 = Link Partner is requesting Next Page function 0 = Base Page is requested	RO	0
14	Acknowledge	Link Partner acknowledgement bit	RO	0
13	Remote Fault	Link Partner is indicating a fault	RO	0
12:5	Technology Ability	Link Partner technology ability field.	RO	00(hex)
4:0	Selector Field	Link Partner selector field	RO	00000

Register 6

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15:5	Reserved		RO	000(hex)
4	Parallel Detection Fault	1 = Local Device Parallel Detection Fault 0 = No fault detected	RO, LH	0
3	Link Partner Next Page Able	1 = Link Partner is Next Page Able 0 = Link Partner is not Next Page Able	RO	0
2	Next Page Able	1 = Local device is Next Page Able 0 = Local device is not Next Page Able	RO	1
1	Page Received	1 = A New Page has been received 0 = A New Page has not been received	RO, LH	0
0	Link Partner Autonegotiation Able	1 = Link Partner is Autonegotiation able 0 = Link Partner is not Autonegotiation able	RO	0

LH Latch High

7.4. DESCRIPTORS AND BUFFER MANAGEMENT

The AN983B provides receive and transmit descriptors for packet buffering and management.

7.4.1 RECEIVE DESCRIPTOR

7.4.1.1 Receive Descriptor Table

	31				0
RDES0	Own	Status			
RDES1		---	Control	Buffer2 byte-count	Buffer1 byte-count
RDES2	Buffer1 address (DW boundary)				
RDES3	Buffer2 address (DW boundary)				

Descriptors and receive buffers addresses must be longword alignment

7.4.1.2 Receive Descriptor Descriptions

RDES0

Bit #	Name	Descriptions
31	OWN	Own bit 1: indicate the new receiving data can be put into this descriptor 0: Host does not move the receiving data out yet.
30-16	FL	Frame length, including CRC. This field is valid only in last descriptor
15	ES	Error summary, OR of the following bit 0: overflow 1: CRC error 6: late collision 7: frame too long 11: runt packet 14: descriptor error This field is valid only in last descriptor.
14	DE	Descriptor error. This bit is valid only in last descriptor 1: the current receiving packet is not able to put into the current valid descriptor. This packet is truncated.
13-12	DT	Data type. 00: normal 01: MAC loop-back 10: Transceiver loop-back 11: remote loop-back These bits are valid only in last descriptor
11	RF	Runt frame (packet length < 64 bytes). This bit is valid only in last descriptor
10	MF	Multicast frame. This bit is valid only in last descriptor

9	FS	First descriptor.
8	LS	Last descriptor.
7	TL	Too long packet (packet length > 1518 bytes). This bit is valid only in last descriptor
6	CS	Late collision. Set when collision is active after 64 bytes. This bit is valid only in last descriptor
5	FT	Frame type. This bit is valid only in last descriptor. 1: Ethernet type 0: 802.3 type
4	RW	Receive watchdog (refer to CSR15, bit 4). This bit is valid only in last descriptor.
3	Reserved	Default = 0
2	DB	Dribble bit. This bit is valid only in last descriptorEC Packet length is not integer multiple of 8-bit.
1	CE	CRC error. This bit is valid only in last descriptor
0	OF	Overflow. This bit is valid only in last descriptor

RDES1

Bit #	Name	Descriptions
31~26	---	Reserved
25	RER	Receive end of ring Indicates this descriptor is last, return to base address of descriptor
24	RCH	Second address chain Use for chain structure. Indicates the buffer2 address is the next descriptor address. Ring mode takes precedence over chained mode
23~22	---	Reserved
21~11	RBS2	Buffer 2 size (DW boundary)
10~ 0	RBS1	Buffer 1 size (DW boundary)

RDES2

Bit #	Name	Descriptions
31~0	RBA1	Receive Buffer Address 1. This buffer address should be double word aligned.

RDES3

Bit #	Name	Descriptions
31~0	RBA2	Receive Buffer Address 2. This buffer address should be double word aligned.

7.4.2. TRANSMIT DESCRIPTOR

7.4.2.1. Transmit Descriptor Table

	31	**0**

TDES0	Own	Status		
TDES1	Control		Buffer2 byte-count	Buffer1 byte-count
TDES2	Buffer1 address			
TDES3	Buffer2 address			

Descriptor addresses must be longword alignment

7.4.2.2. Transmit Descriptor Descriptions

TDES0

Bit #	Name	Descriptions
31	OWN	Own bit 1: Indicate this descriptor is ready to transmit 0: No transmit data in this descriptor for transmission
30-24	---	Reserved
23-22	UR	Under-run count
21-16	---	Reserved
15	ES	Error summary, OR of the following bit 1: under-run error 8: excessive collision 9: late collision 10: no carrier 11: loss carrier 14: jabber time-out
14	TO	Transmit jabber time-out
13-12	-----	Reserved
11	LO	Loss carrier
10	NC	No carrier
9	LC	Late collision
8	EC	Excessive collision
7	HF	Heartbeat fail
6-3	CC	Collision count
2	-----	Reserved
1	UF	Under-run error
0	DE	Deferred

TDES1

Bit #	Name	Descriptions
31	IC	Interrupt completed
30	LS	Last descriptor
29	FS	First descriptor
28,27	---	Reserved
26	AC	Disable add CRC function

25	TER	End of Ring
24	TCH	2nd address chain Indicate the buffer2 address is the next descriptor address
23	DPD	Disable padding function
22	---	Reserved
21-11	TBS2	Buffer 2 size
10-0	TBS1	Buffer 1 size

TDES2

Bit #	Name	Descriptions
31~0	BA1	Buffer Address 1. Without any limitation on the transmission buffer address.

TDES3

Bit #	Name	Descriptions
31~0	BA2	Buffer Address 2. Without any limitation on the transmission buffer address.

8. FUNCTIONAL DESCRIPTIONS

8.1 INITIALIZATION FLOW

The flow of initialize AN983B is shown as below.

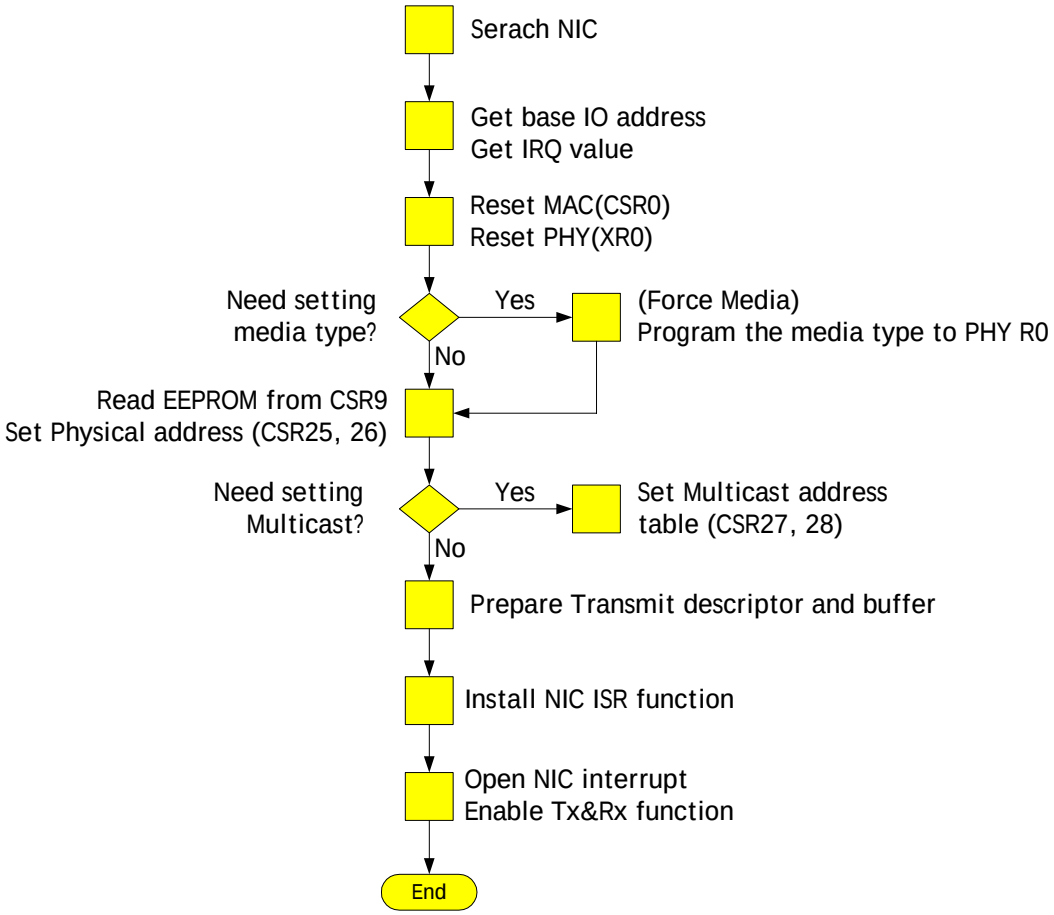


Fig - 4 Initialization flow

8.2 NETWORK PACKET BUFFER MANAGEMENT

8.2.1 DESCRIPTOR STRUCTURE TYPES

For networking operation, the AN983B transmits the data packet from transmit buffers in host memory to AN983B's transmit FIFO and receives the data packet from AN983B's receive FIFO to receive buffers in host memory. The descriptors that the AN983B supports to build in host memory are used as the pointers of these transmit and receive buffers.

There are two structure types for the descriptor, **Ring and Chain**, supported by the AN983B and are shown as below. The type selection is controlled by the bit24 of RDES1 and the bit24 of TDES1.

The transmit and receive buffers are physically built in host memory. Any buffer can contain either a whole packet or just part of a packet. But it can't contain more than one packet.

■ *Ring structure*

There are two buffers per descriptor in the ring structure. Support receives early interrupt.

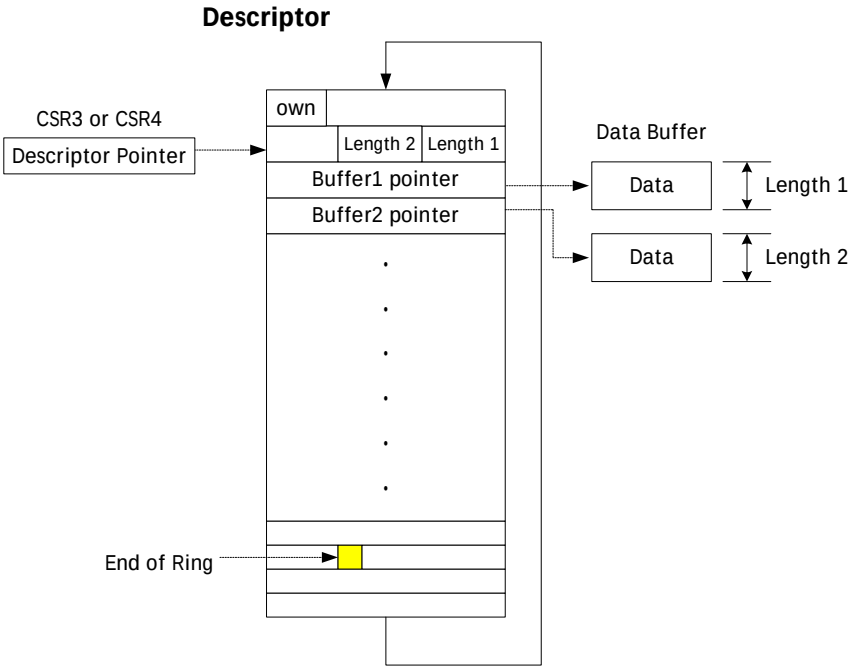


Fig - 5 Ring structure of frame buffer

■ *Chain structure*

There is only one buffer per descriptor in chain structure.

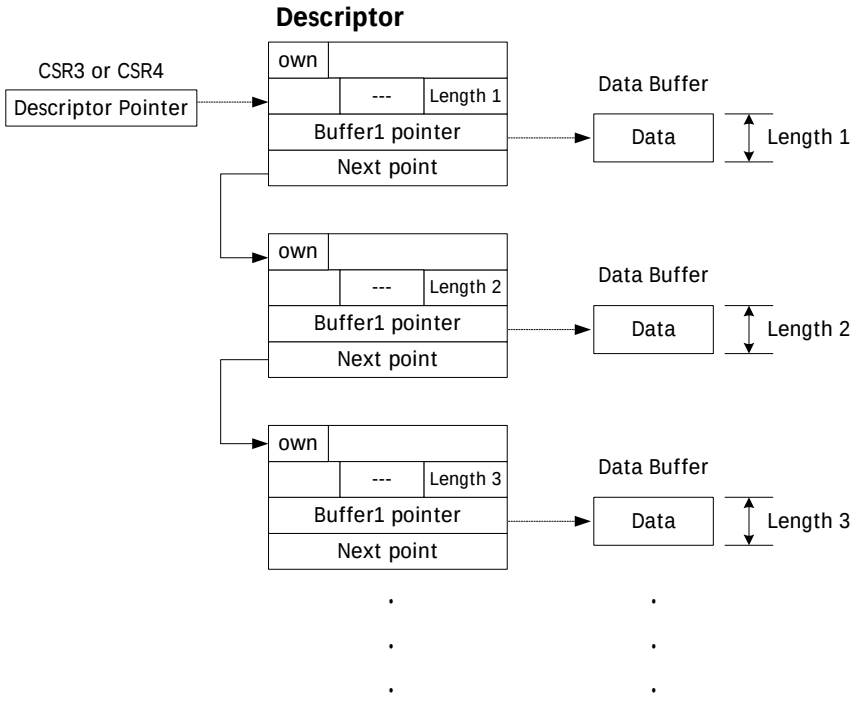


Fig - 6 Chain structure of frame buffer

8.2.2 THE POINT OF DESCRIPTOR MANAGEMENT

OWN bit = 1, ready for network side access

OWN bit = 0, ready for host side access

■ ***Transmit Descriptor Pointers***

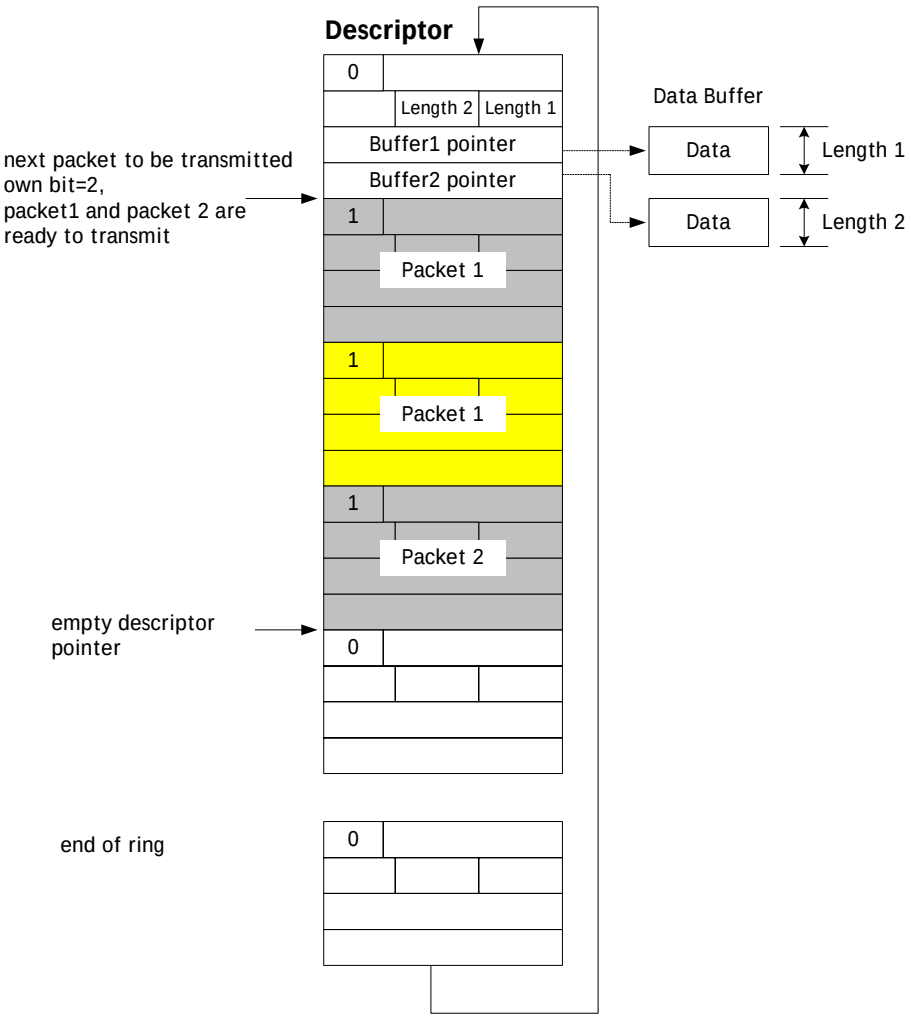


Fig - 7 Transmit pointers for descriptor management

■ *Receive Descriptor Pointers*

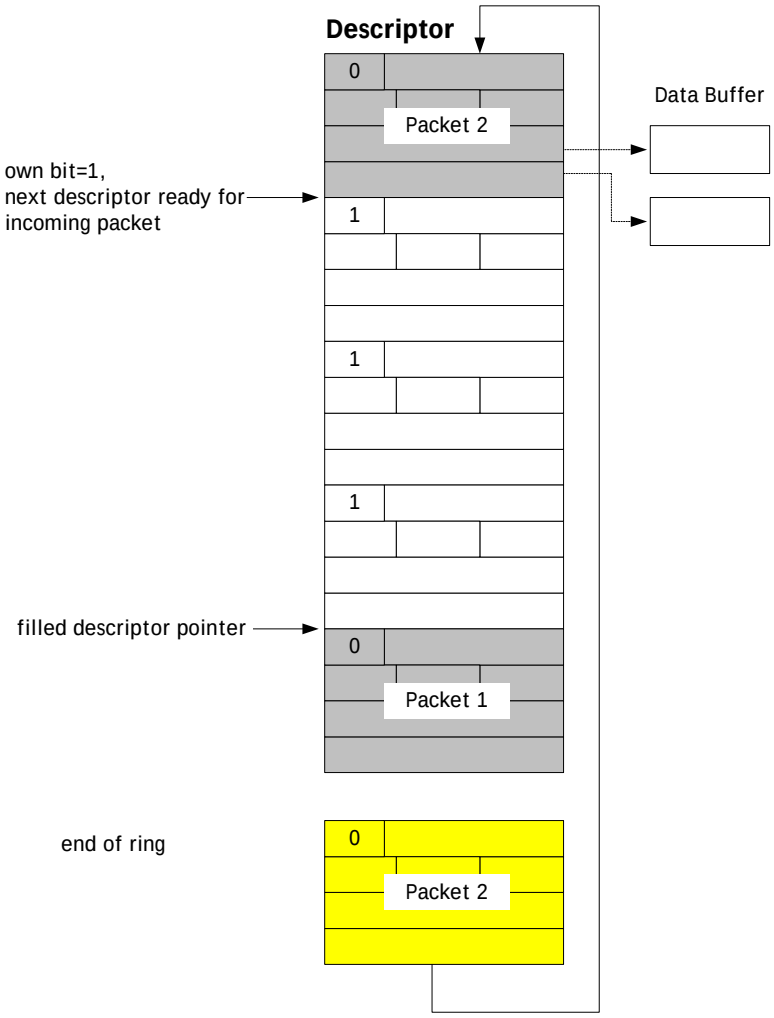


Fig - 8 Receive pointers for descriptor management

8.3 TRANSMIT SCHEME AND TRANSMIT EARLY INTERRUPT

8.3.1 TRANSMIT FLOW

The flow of packet transmit is shown as below.

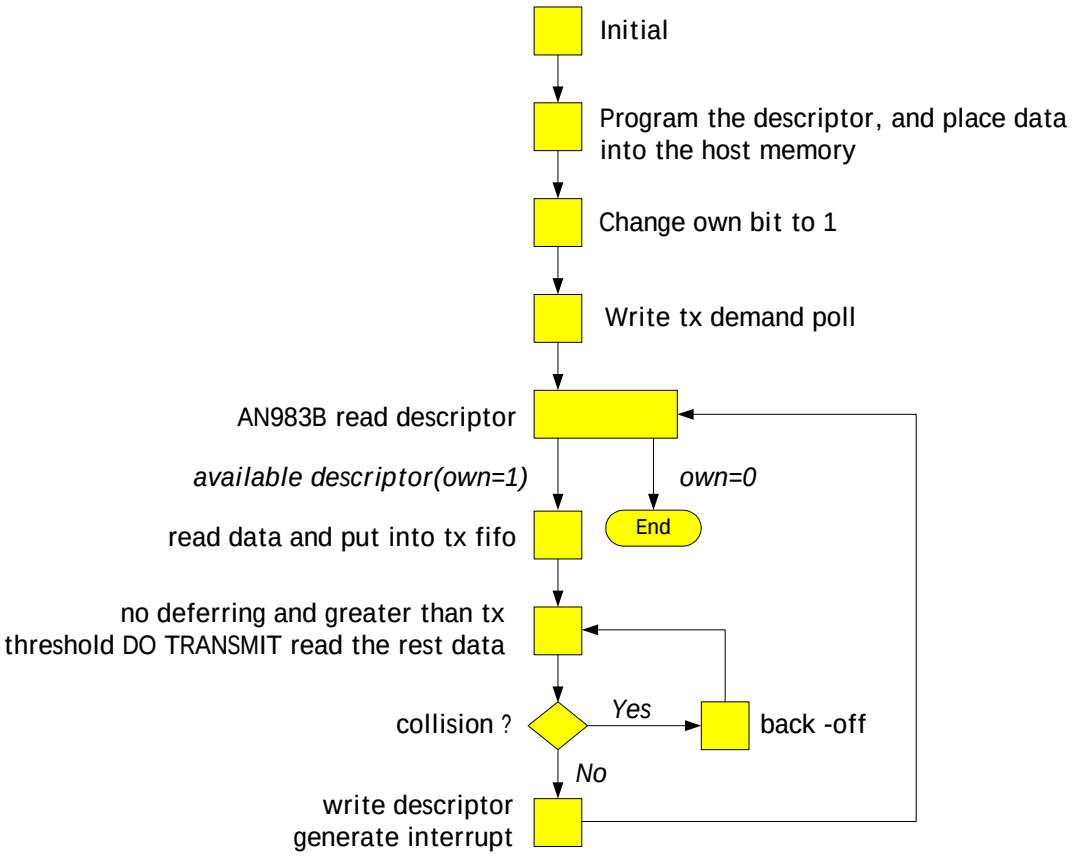


Fig - 9 Transmit flow

8.3.2 TRANSMIT PRE-FETCH DATA FLOW

- ***Transmit FIFO size=2K-byte***
- ***Two packets in the FIFO at the same time***
- ***Meet the transmit min. back-to-back***

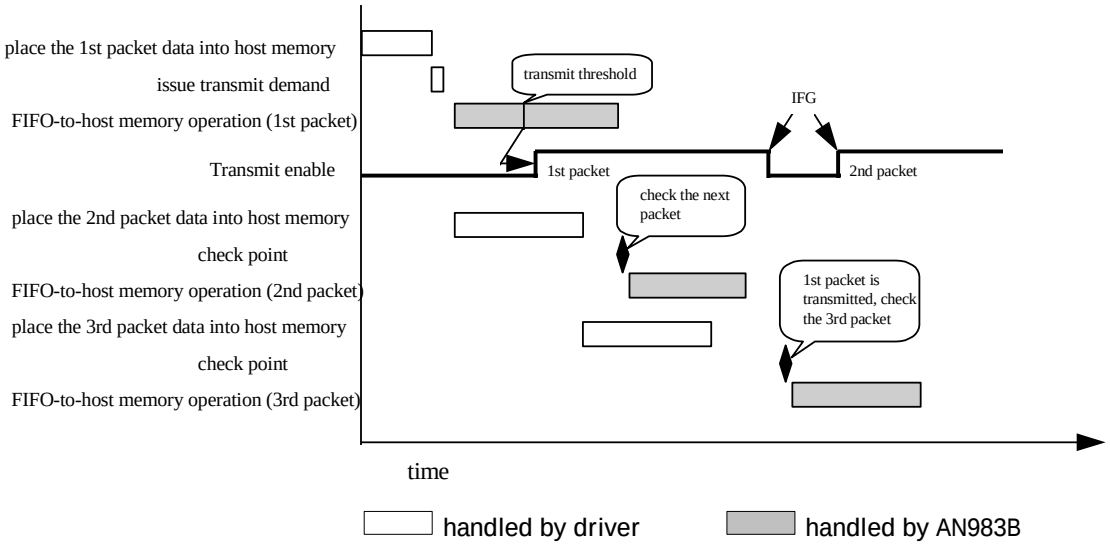


Fig - 10 Transmit data flow of pre-fetch data

8.3.3 TRANSMIT EARLY INTERRUPT SCHEME

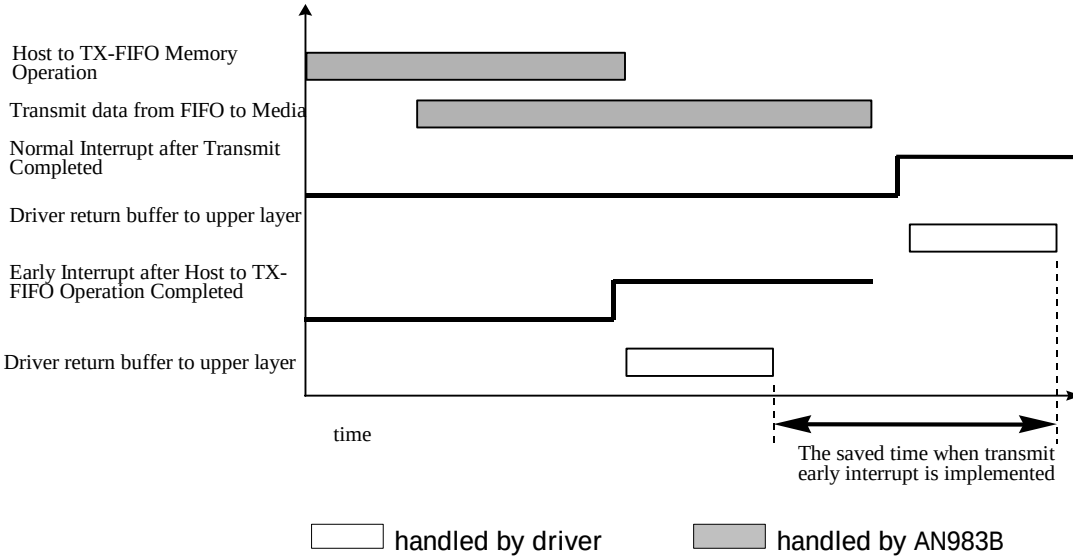


Fig - 11 Transmit normal interrupt and early interrupt comparison

8.4 RECEIVE SCHEME AND RECEIVE EARLY INTERRUPT SCHEME

The following figure shows the difference of timing without early interrupt and with early interrupt.

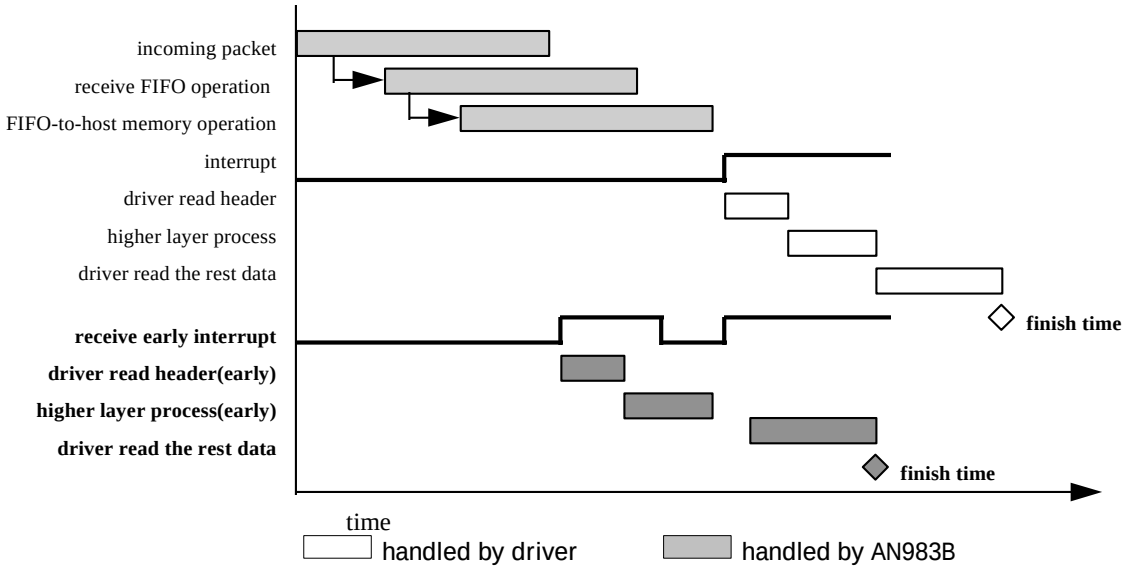


Fig - 12 Receive data flow (without early interrupt and with early interrupt)

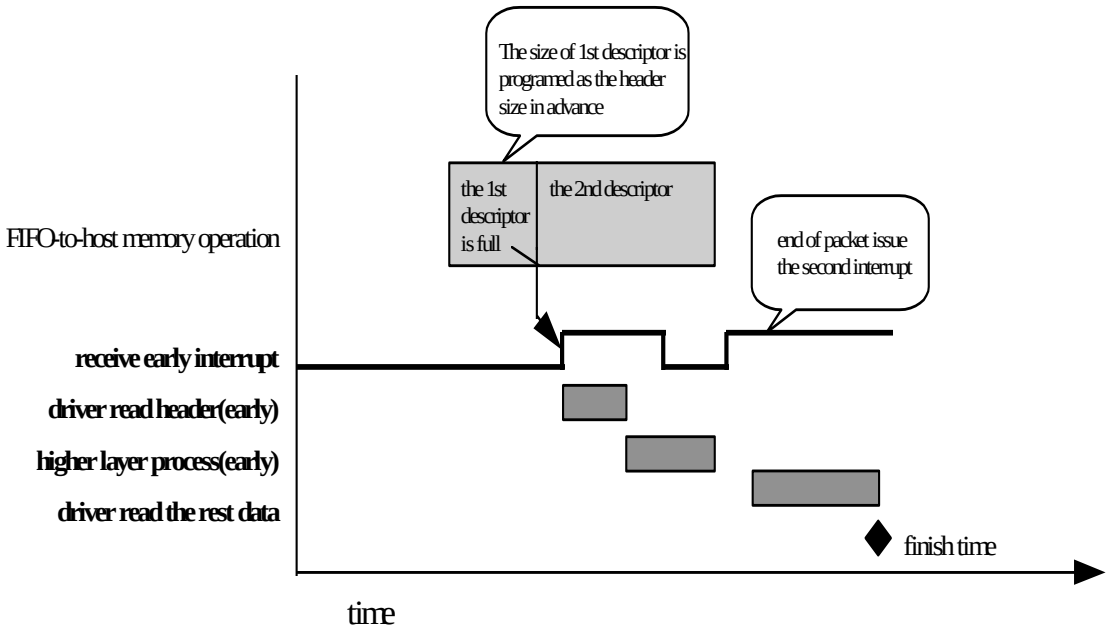


Fig - 13 Detailed receive early interrupt flow

8.5 NETWORK OPERATION

8.5.1 MAC OPERATION

In the MAC (Media Access Control) portion of AN983B, it incorporates the essential protocol requirements for operating as an IEEE802.3 and Ethernet compliant node.

■ Format

Field	Description
Preamble	A 7-byte field of (10101010b)
Start Frame Delimiter	A 1-byte field of (10101011b)
Destination Address	A 6-byte field
Source Address	A 6-byte field
Length/Type	A 2-byte field indicated the frame is in IEEE802.3 format or Ethernet format. IEEE802.3 format: 0000H ~ 05DCH for Length field Ethernet format: 05DD ~ FFFFH for Type field
Data	*46 ~ 1500 bytes of data information
CRC	A 32-bit cyclic redundant code for error detection

*Note: If padding is disabled (TDES1 bit23), the data field may be shorter than 46 bytes.

■ Transmit Data Encapsulation

The differences between the encapsulation and a MAC frame while operating in the 100BASE-TX mode are listed as follow:

1. The first byte of the preamble is replaced by the JK code according to the IEE802.3u, clause 24.

2. After the CRC field of the MAC frame, the AN983B insert the TR code according to the IEE802.3u, clause 24.

■ Receive Data Decapsulation

When operate in 100BASE-TX mode the AN983B detects a JK code for a preamble as well as a TR code for the packet end. If a JK code is not detected, the AN983B will abort this frame receiving and wait for a new JK code detection. If a TR code is not detected, the AN983B will report a CRC error.

■ Deferring

The Inter-Frame Gap (IFG) time is divided into two parts:

1. IFG1 time (64-bit time): If a carrier is detected on the medium during this time, the AN983B will reset the IFG1 time counter and restart to monitor the channel for an idle again.

2. IFG2 time (32-bit time): After counting the IFG2 time the AN983B will access the channel even though a carrier has been sensed on the network.

■ Collision Handling

The scheduling of re-transmissions is determined by a controlled randomization process called "truncated binary exponential back-off". At the end of enforcing a collision (jamming), the AN983B delays before attempting to re-transmit the packet. The delay is an integer multiple of slot time. The number of slot times to delay before the nth re-transmission attempt is chosen as a uniform distributed integer r in the range:

$$0 \leqq r < 2^k \quad \text{where} \quad k = \min(n, 10)$$

8.5.2 TRANSCEIVER OPERATION

In the transceiver portion of the AN983B, it integrates the IEEE802.3u compliant functions of PCS (physical coding sub-layer), PMA (physical medium attachment) sub-layer, and PMD (physical medium dependent) sub-layer for 100BASE-TX, and the IEEE802.3 compliant functions of Manchester encoding/decoding and transceiver for 10BASE-T. All the functions and operation schemes are described in the following sections.

■ 100BASE-TX Transmit Operation

Regarding the 100BASE-TX transmission, the transceiver provides the transmission functions of PCS, PMA, and PMD for encoding of MII data nibbles to five-bit code-groups (4B/5B), scrambling, serialization of scrambled code-groups, converting the serial NRZ code into NRZI code, converting the NRZI code into MLT3 code, and then driving the MLT3 code into the category 5 Unshielded Twisted Pair cable through an isolation transformer with the turns ratio of 1: 1.

- **Data code-groups Encoder:**

  In normal MII mode application, the transceiver receives nibble type 4B data via the TxD0~3 inputs of the MII. These inputs are sampled by the transceiver on the rising edge of Tx-clk and passed to the 4B/5B encoder to generate the 5B code-group used by 100BASE-TX.

- **Idle code-groups**

  In order to establish and maintain the clock synchronization, the transceiver needs to keep transmitting signals to medium. The transceiver will generate Idle code-groups for transmission when there is no real data want to be sent by MAC.

- ***Start-of-Stream Delimiter-SSD (/J/K/)***

  In a transmission stream, the first 16 nibbles are MAC preamble. In order to let partner delineate the boundary of a data transmission sequence and to authenticate carrier events, the transceiver will replace the first 2 nibbles of the MAC preamble with /J/K/ code-groups.

- ***End-of-Stream Delimiter-ESD (/T/R/)***

  In order to indicate the termination of the normal data transmissions, the transceiver will insert 2 nibbles of /T/R/ code-group after the last nibble of FCS.

- ***Scrambling***

  All the encoded data (including the idle, SSD, and ESD code-groups) is passed to data scrambler to reduce the EMI and spread the power spectrum using a 10-bit scrambler seed loaded at the beginning.

- ***Data conversion of Parallel to Serial, NRZ to NRZI, NRZI to MLT3***

  After scrambled, the transmission data with 5B type in 25MHz will be converted to serial bit stream in 125HMz by the parallel to serial function. After serialized, the transmission serial bit stream will be further converted from NRZ to NRZI format. After NRZI converted, the NRZI bit stream is passed through MLT3 encoder to generate the TP-PMD specified MLT3 code. With this MLT3 code, it lowers the frequency and reduces the energy of the transmission signal in the UTP cable and also makes the system easily to meet the FCC specification of EMI.

- ***Wave-Shaper and Media Signal Driver***

  In order to reduce the energy of the harmonic frequency of transmission signals, the transceiver provides the wave-shaper prior the line driver to smooth but keep symmetric the rising/falling edge of transmission signals. The wave-shaped signals include the 100BASE-TX and 10BASE-T both are passed to the same media signal driver. This design can simplify the external magnetic connection with single one.

■ *100BASE-TX Receiving Operation*

Regarding the 100BASE-TX receiving operation, the transceiver provides the receiving functions of PMD, PMA, and PCS for receiving incoming data signals through category 5 UTP cable and an isolation transformer with turn's ratio of 1: 1. It includes the adaptive equalizer and baseline wander, data conversions of MLT3 to NRZI, NRZI to NRZ and serial to parallel, the PLL for clock and data recovery, the de-scrambler, and the decoder of 5B/4B.

- ***Adaptive Equalizer and Baseline Wander***

  Since the high-speed signals over the unshielded (or shielded) twisted Pair cable will induce the amplitude attenuation and phase shifting. Furthermore, these effects are depends on the signal frequency, cable type, cable length and the connectors of the

cabling. So a reliable adaptive equalizer and baseline wander to compensate all the amplitude attenuation and phase shifting are necessary. In the transceiver, it provides the robust circuits to perform these functions.

- ***MLT3 to NRZI Decoder and PLL for Data Recovery***

  After receiving the proper MLT3 signals, the transceiver converts the MLT3 to NRZI code for further processing. After adaptive equalizer, baseline wander, and MLT3 to NRZI decoder, the compensated signals with NRZI type in 125MHz are passed to the Phase Lock Loop circuits to extract out the original data and the synchronous clock.

- ***Data Conversions of NRZI to NRZ and Serial to Parallel***

  After data recovered, the signals will be passed to the NRZI to NRZ converter to generate the 125MHz serial bit stream. This serial bit stream will be packed to parallel 5B type for further processing.

- ***De-scrambling and Decoding of 5B/4B***

  The parallel 5B type data is passed to de-scrambler and 5B/4B decoder to return their original MII nibble type data.

- ***Carrier sensing***

  Carrier Sense (CRS) signal is asserted when the transceiver detects any 2 non-contiguous zeros within any 10bit boundary of the receiving bit stream. CRS is de-asserted when ESD code-group or Idle code-group is detected. In half duplex mode, CRS is asserted during packet transmission or receive. But in full duplex mode, CRS is asserted only during packet reception.

10BASE-T Transmission Operation

It includes the parallel to serial converter, Manchester Encoder, Link test function, Jabber function and the transmit wave-shaper and line driver described in the section of "Wave-Shaper and Media Signal Driver" of "100BASE-T Transmission Operation". It also provides Collision detection and SQE test for half duplex application.

10BASE-T Receive Operation

It includes the carrier sense function, receiving filter, PLL for clock and data recovering, Manchester decoder, and serial to parallel converter.

Loop-back Operation of transceiver

The transceiver provides internal loop-back (also called transceiver loop-back) operation for both the 100BASE-TX and 10BASE-T operations. Setting bit 14 of PHY register 0 to 1 can enable the loop-back operation. In this loop-back operation, PHY will not transmit packets (but PHY will still send MLT3 for Idle).

In the 100BASE-TX internal loop-back operation, the data comes from the transmit output of

NRZ to NRZI converter then loop-back to the receive path into the input of NRZI to NRZ converter.

In the 10BASE-T loop-back operation, the data is through transmitting path and loop-back from the output of the Manchester encoder into the input of Phase Lock Loop circuit of receive path.

■ *Full Duplex and Half Duplex Operation of Transceiver*

The transceiver can operate for either full duplex or half duplex network application. In full duplex, both transmit and receive can be operated simultaneously. Under full duplex mode, collision (COL) signal is ignored and carrier sense (CRS) signal is asserted only when the transceiver is receiving.

In half duplex mode, either transmit or receive can be operated at one time. Under half duplex mode, collision signal is asserted when transmit and receive signals collided and carrier sense asserted during transmission and reception.

■ *Auto-Negotiation Operation*

The Auto-Negotiation function is designed to provide the means to exchange information between the transceiver and the network partner to automatically configure both to take maximum advantage of their abilities, and both are setup accordingly. The Auto-Negotiation function can be controlled through bit 12 of PHY register 0.

The Auto-Negotiation exchanges information with the network partner using the Fast Link Pulses (FLPs) - a burst of link pulses. There are 16 bits of signaling information contained in the burst pulses to advertise all remote partners' capabilities, which are determined by PHY, register 4. According to this information they find out their highest common capability by following the priority sequence as below:

1. 100BASE-TX full duplex

2. 100BASE-TX half duplex

3. 10BASE-T full duplex

4. 10BASE-T half duplex

During power-up or reset, if Auto-Negotiation is found enabled then FLPs will be transmitted and the Auto-Negotiation function will process. Otherwise, the Auto-Negotiation will not occur until the bit 12 of PHY register 0 is set to 1. When the Auto-Negotiation is disabled, then the Network Speed and Duplex Mode are selected by programming PHY register 0.

■ *Power Down Operation*

To reduce the power consumption the transceiver is designed with power down feature, which can save the power consumption significantly. Since the power supply of the 100BASE-TX and 10BASE-T circuits are separated, the transceiver can turn off the circuit of either the 100BASE-TX or 10BASE-T when the other one of them is operating.

8.5.3 FLOW CONTROL IN FULL DUPLEX APPLICATION

The PAUSE function operation is used to inhibit transmission of data frames for a specified period of time. The AN983B supports full duplex protocol of IEEE802.3x. To support PAUSE function, the AN983B implements the MAC Control Sub-layer functions to decode the MAC Control frames received from MAC control clients and execute the relative requests accordingly. When the Full Duplex mode and PAUSE function are selected after Auto-Negotiation completed, then the AN983B enables the PAUSE function for flow control of full duplex application. In this section we will describe how the AN983B implements the PAUSE function.

■ *MAC Control Frame and PAUSE Frame*

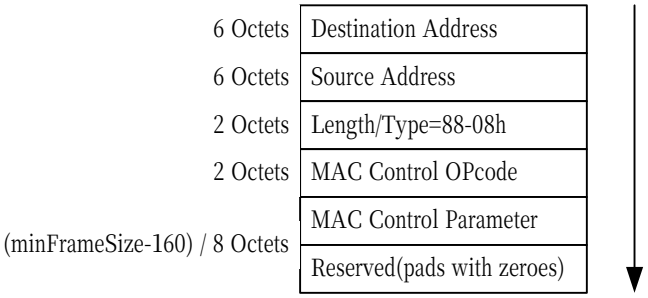


Fig - 14 MAC Control Frame Format

The MAC Control frame is distinguished from other MAC frames only by their Length/Type field identifier. The MAC Control Opcode defined in MAC Control Frame format for PAUSE function is 0001h. Besides, the PAUSE time is specified in the MAC Control Parameters field with 2 Octets, unsigned integer, in the units of Slot-Times. The range of possible PAUSE time is 0 to 65535 Slot-Times.

So, a valid PAUSE frame issued by a MAC control client (could be a switch or a bridge) will contains:

1) The destination address is set equal to the globally assigned 48 bit mulitcast address 01-80-C2-00-00-01, or equal to the unicast address which the MAC control client wishes to inhibit its transmission of data frames.

2) Filled the MAC Control Opcode field with 0001h.

3) 2 Octets of PAUSE time specified in the MAC Control parameter field to indicate the length of time for which the destination is wished to inhibit data frame transmission.

■ *Receive Operation for PAUSE function*

Upon reception of a valid MAC Control frame, the AN983B will start a timer for the length of time specified by the MAC Control Parameters field. When the timer value reaches zero then the AN983B ends PAUSE state. However, a PAUSE frame should not affect the transmission of a frame that has been submitted to the MAC (started Transmit out of the MAC and can't be interrupted). On the other hand, the AN983B shall not begin to transmit a frame more than one Slot-Times after received a valid PAUSE frame with a non-zero PAUSE time. If the AN983B receives a PAUSE frame with a zero PAUSE time value, then

the AN983B ends the PAUSE state immediately.

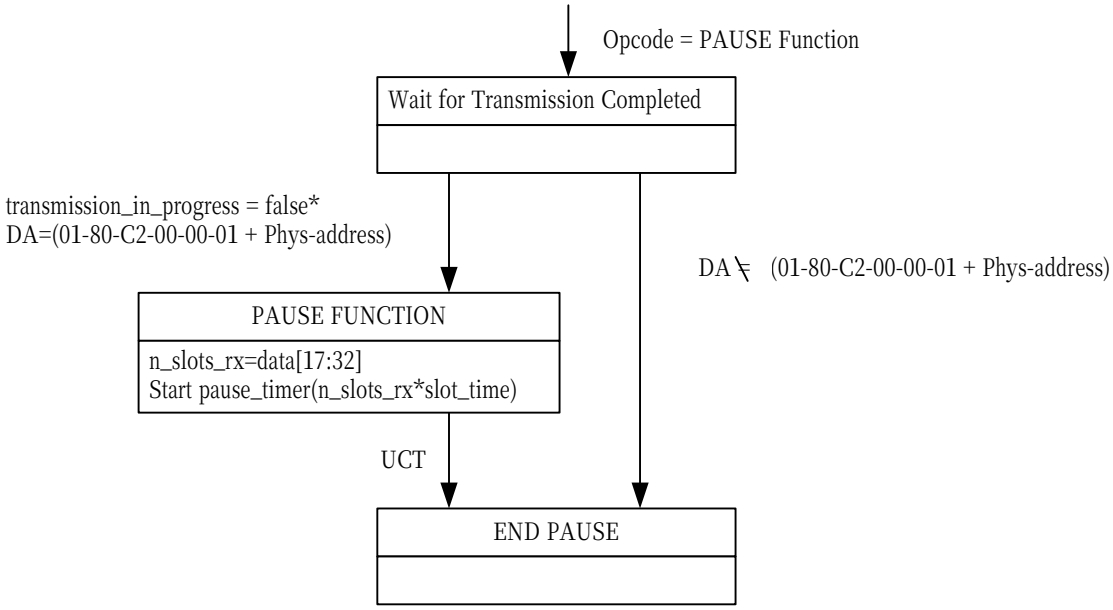


Fig - 15 PAUSE operation receive state diagram

8.6 LED DISPLAY OPERATION

The AN983B provides 2 kinds of LED display mode; the detail descriptions about the operation are described in the PIN Description section.

8.6.1 FIRST MODE - 3 LED DISPLAYS FOR

- *100Mbps(on) or 10Mbps(off)*
- *Link (Keeps on when link ok) or Activity (Blink with 10Hz when receiving or transmitting but not collision)*
- *FD (Keeps on when in Full duplex mode) or Collision (Blink with 20Hz when colliding)*

8.6.2 SECOND MODE – 4 LED DISPLAYS FOR

- *100 Link (On when 100M link ok)*
- *10 Link (On when 10M link ok)*
- *Activity (Blink with 10Hz when receiving or transmitting)*
- *FD (Keeps on when in Full duplex mode) or Collision (Blink with 20Hz when colliding)*

8.7 RESET OPERATION

8.7.1 RESET WHOLE CHIP

There are two ways to reset the AN983B. First, hardware reset, the AN983B can be reset via RST# pin. For ensuring proper reset operation, at least 100μs active Reset input signal is required. Second, software reset, when bit 0 of CSR0 register is set to 1, the AN983B will reset entire circuits and register to default value then clear the bit 0 of CSR0 to 0.

8.7.2 RESET TRANSCEIVER ONLY

When bit 15 of PHY register 0 is set to 1, the transceiver will reset entire circuits and register

contains to default value then clear the bit 15 of PHY register 0 to 0.

8.8 WAKE ON LAN FUNCTION

The AN983B can assert a signal to wake up the system when it received a Magic Packet from the network. The Wake on LAN operation is described as follow.

8.8.1 THE MAGIC PACKET FORMAT

- ***Valid destination address that can pass the address filter of the AN983B***
- ***The payload of frame must include at least 6 contiguous 'FF' followed immediately by 16 repetitions of IEEE address.***
- ***The frame can contain multiple 'six FF + sixteen IEEE address' pattern.***
- ***CRC OK***

8.8.2 THE WAKE ON LAN OPERATION

The Wake on LAN enable function is controlled by bit 18 of CSR18; it is loaded from EEPROM after reset or programmed by driver to enable Wake on LAN function. If the bit 18 of CSR18 is set and the AN983B receive a Magic Packet, it will assert the PME# signal (drive to low) to indicate receiving a wake up frame as well as to set the PME status bit (the bit 15 of CSR20).

8.9 ACPI POWER MANAGEMENT FUNCTION

The AN983B has a built-in capability for Power Management (PM), which controlled by the host system

The AN983B will provide:

- ***Compatibility with Device Class Power Management Reference Specification, Rev1.09***
- ***Compatibility with ACPI specification, Rev 1.0***
- ***Compatibility with PCI Bus Power Management Interface Specification, Rev 1.1***
- ***Compatibility with AMD Magic Packet™ Technology.***

- ***Compatibility with PCI CLKRUN scheme.***

8.9.1 POWER STATES

- ***DO (Fully On)***

In this state the AN983B operates as full functionality and consumes its normal power. While in the D0 state, if the PCI clock is lower than 16MHz, the AN983B may not receive or transmit frames properly.

- ***D1***

In this state the AN983B doesn't response to any accesses, except configuration space and full function context in place. The only network operation the AN983B can initiate is a wake-up event.

- ***D2***

In this state the AN983B only respond to access configuration space and full function context in place. The AN983B can't transmit or receive even the wake-up frame.

- ***$D3_{cold}$ (Power Removed)***

In this state all function context is lost. When power is restored, the function will return to D0.

- ***$D3_{hot}$ (Software Visible D3)***

When the AN983B is brought back to D0 from $D3_{hot}$ the software must perform a full initialization.

The AN983B in the $D3_{hot}$ state respond to configurations cycles as long as power and clock are supplied. This requires the device to perform an internal reset and return to a power-up reset condition without the RST# pin asserted.

Power State

Device State	PCI-Bus State	Function Context	Clock	Power	Supported Actions to Function	Supported Actions from Function
D0	B0	Full function context in place	Full speed	Full power	Any PCI transaction	Any PCI transaction or interrupt
D1	B0, B1	Configuration maintained. No Tx and Rx except wake-up events	Stopped to Full speed		PCI configuration access	Only wake-up events
D2	B0, B1,	Configuration	Stopped to		PCI configuration	

	B2	maintained. No Tx and Rx	Full speed		access (B0, B1)	
D3hot	B0, B1, B2	Configuration lost, full initialization required upon return to D0	Stopped to Full speed		PCI configuration access (B0, B1)	
D3cold	B3	All configurations lost. Power-on defaults in place on return to D0	No clock	No power	Power-on reset	

9. GENERAL EEPROM FORMAT DESCRIPTION

Connection Type Definition

Offset	Length	Description
0	2	AN983B *Signature*: **0x85**, **0x09,** AN985 *Signature*: **0x85**, **0x19**
2	1	Format major version: **0x02**.
3	1	Format minor version: **0x00**
4	4	Reserved
8	6	IEEE network address: **ID1**, **ID2, ID3, ID4, ID5, ID6**
E	1	Reserved, should be **zero.**
F	1	Reserved, should be **zero.**
10	1	Phytype Reserved, should be **zero**.
11	1	Reserved, should be **zero**.
12	2	*Default Connection Type*, See Table 9.1
14	1	BootRom **ENABLE=1**, DISABLE=0
15	1	BootRom Default selection: **0: Using INT 18h** 1: Using INT 19h 2: Using Pnp/BEV (BBS) 0x10: Boot From RPL
16	0xA	Reserved, should be **zero**.
20	2	PCI *Device ID*.:**0X0985 (AN983B), 0x1985(AN985)**
22	2	PCI *Vendor ID*.:**0x1317**
24	2	PCI *Subsystem ID*.
26	2	PCI *Subsystem Vendor ID*.
28	1	**MIN_GNT** value. **0xFF**
29	1	**MAX_LAT** value. **0xFF**
2A	4	CIS Pointer, it will be loaded into CR10. **0x0202**
2E	2	CSR18 (**CR**) bit 31-16 recall data. Please reference AN983B Spec.
30	0x22	Reserved, should be **zero**.
52	2	**Cardbus CIS length.**
54	0x2A	Reserved, should be **zero**.
7E	2	*CheckSum*, the least significant two bytes of **FCS** for data stored in offset 0.7D of EEPROM
140	C0	**Cardbus CIS**

0xFFFF	Software Driver Default
0x0100	Auto-Negotiation
0x0200	Power-on Auto-detection
0x0400	Auto Sense
0x0000	10BaseT
0x0001	BNC
0x0002	AUI
0x0003	100BaseTx
0x0004	100BaseT4
0x0005	100BaseFx
0x0010	10BaseT Full Duplex
0x0013	100BaseTx Full Duplex
0x0015	100BaseFx Full Duplex

10. ELECTRICAL SPECIFICATIONS AND TIMINGS

10.1 ABSOLUTE MAXIMUM RATINGS

- ***Supply Voltage (Vcc)*** ***-0.5V to 3.6V***
- ***Input Voltage*** ***-0.5V to VCC+0.5 V***
- ***Output Voltage*** ***-0.5V to VCC+0.5 V***
- ***Storage Temperature*** ***-65 degree C to 150 degree C***
- ***Ambient Temperature*** ***0° degree C to 70 degree C***
- ***ESD Protection*** ***2000V***

10.2 DC SPECIFICATIONS

General DC Specifications

Parameter	Description	Condition	Min	Typical	Max	Units
Vcc	Supply Voltage		3.0		3.6	V
Icc	Power Supply			150		mA

PCI Interface DC Specifications

Parameter	Description	Condition	Min	Typical	Max	Units
Vilp	Input LOW Voltage		-0.5		0.325vcc	V
Vihp	Input HIGH Voltage		0.475vcc		Vcc+0.5	V
Iilp	Input Leakage Current	0<Vin <Vcc	-10		10	uA
Volp	Output LOW Voltage	Iout=700uA			0.1Vcc	V
Vohp	Output HIGH Voltage	Iout=-150uA	0.9Vcc			V
Cinp	Input Pin Capacitance		5		17	pF
Cclkp	CLK Pin Capacitance		10		22	pF

Flash/EEPROM Interface DC Specifications

Parameter	Description	Condition	Min	Typical	Max	Units
Vilf	Input LOW Voltage		0		0.3Vcc	V
Vihf	Input HIGH Voltage		0.7Vcc		Vcc + 1	V
Iif	Input Leakage Current		-10		10	uA
Volf	Output LOW Voltage				0.2	V
Vohf	Output HIGH Voltage		Vcc – 0.2			V

Cinf	Input Pin Capacitance		5		8	pF

10.3 AC SPECIFICATIONS

PCI Signaling AC Specifications for 3.3V

Parameter	Description	Condition	Min	Typical	Max	Units
Ioh (AC)	Switching Current High			4		mA
Iol (AC)	Switching Current Low			6		mA
	Slew Rate		0.25		1	V/ns
Tr	Unloaded Output Rise Time	0.2vcc~0.6vcc	1		4	V/ns
Tf	Unloaded Output Fall Time	0.6vcc~0.2vcc	1		4	V/ns

10.4 TIMING SPECIFICATIONS

PCI Clock Specifications

Parameter	Description	Condition	Min	Typical	Max	Units
Tcyc	Clock Cycle Time		30			ns
Thigh	Clock High Time		12			ns
Tlow	Clock Low Time		12			ns
	Clock Slew Rate		1		4	V/ns

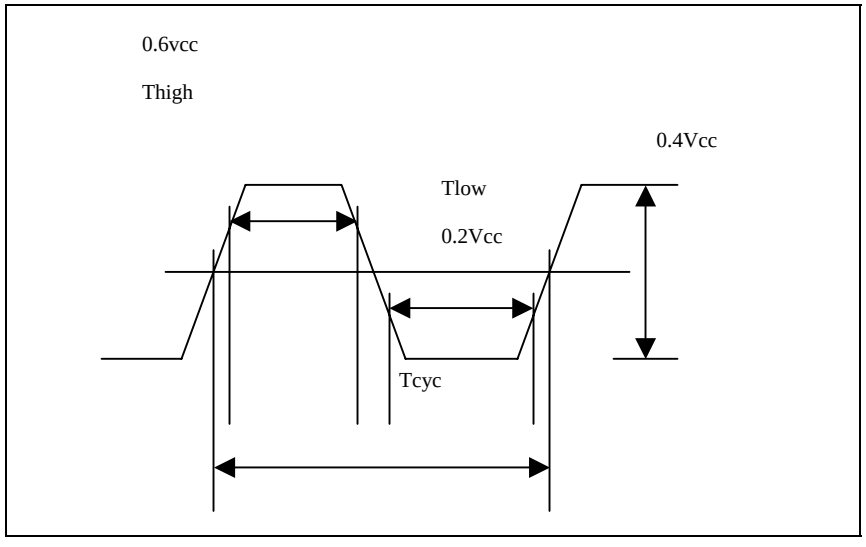


Fig - 16 PCI Clock Waveform

PCI Timings

Parameter	Description	Condition	Min	Typical	Max	Units
Tval	Access time – bused signals		2		11	ns
Tval (ptp)	Access time –point to point		2		12	ns
Ton	Float to Active Delay		2			ns
Toff	Active to Float Delay				28	ns
Tsu	Input Set up Time to Clock – bused signals		7			ns
Tsu (ptp)	Input Set up Time to Clock - point to point		10,12			ns
Th	Input Hold Time from Clock		0			ns
Trst	Reset Active Time after Power Stable		1			ms
Trst-clk	Reset Active Time after CLK Stable		100			us
Trst-off	Reset Active to Output Float delay				40	ns

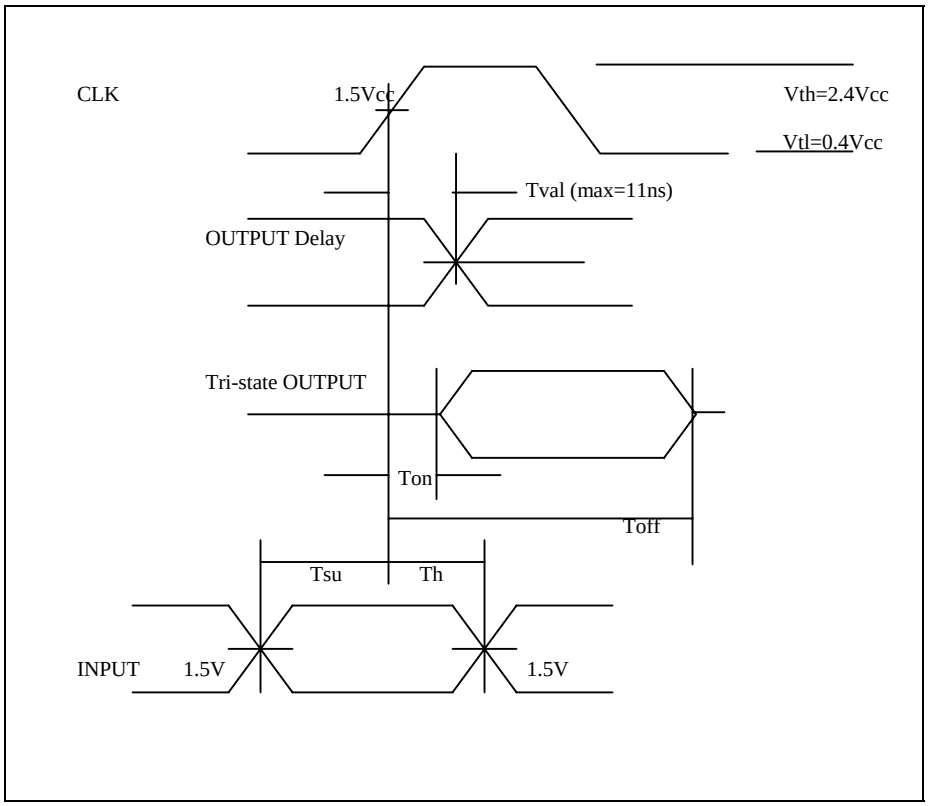


Fig - 17 PCI Timings

Flash Interface Timings

Parameter	Description	Condition	Min	Typical	Max	Units
Trc	Read cycle time		90			ns
Tce	Chip enable access time				90	ns
Taa	Address access time				90	ns
Toe	Output enable access time				45	ns
Tclz	#CE low to active output		0			ns
Tolz	#OE low to active output		0			ns
Tchz	#CE high to active output				45	ns
Tohz	#OE high to active output				45	ns
Toh	Output hold from address change		0			ns
Twc	Write cycle time				10	ms
Tas	Address setup time		0			ns
Tah	Address hold time		50			ns
Tcs	#WE and #CE setup time		0			ns

Tch	#WE and #CE hold time		0			ns
Toes	#OE high setup time		10			ns
Toeh	#OE high hold time		10			ns
Tcp	#CE pulse width		70			ns
Twp	#WE pulse width		70			ns
Twph	#WE high width		150			ns
Tds	Data setup time		50			ns
Tdh	Data hold time		10			ns
Tblc	Byte load cycle time		0.22		200	us
Tblco	Byte laod cycle time out		300			us

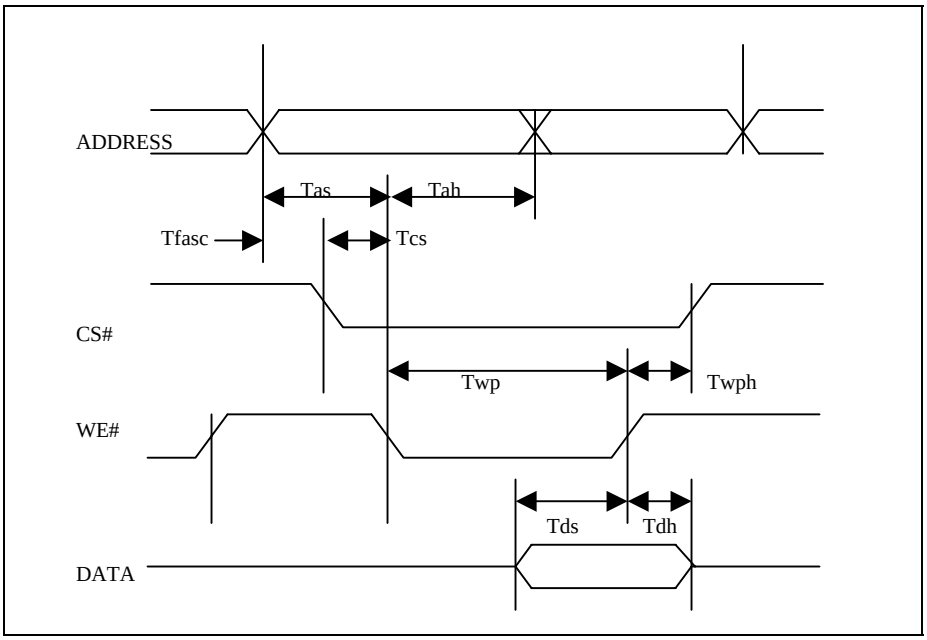


Fig - 18 Flash write timings

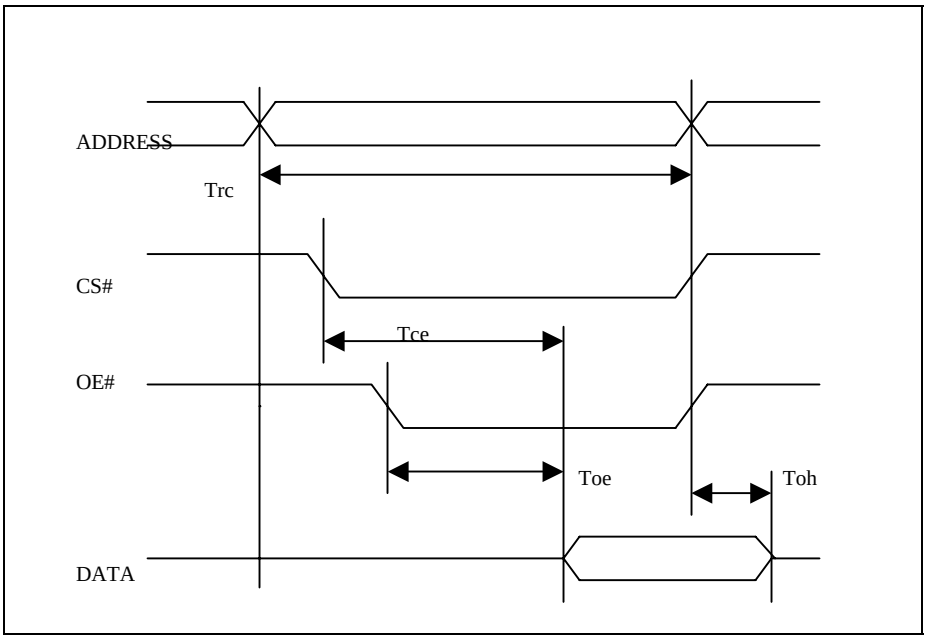


Fig - 19 Flash read timings

EEPROM Interface Timings (AC/AD)

Parameter	Description	Condition	Min	Typical	Max	Units
Tscf	Serial Clock Frequency	2.7V<Vcc<5.5V			0.4M/ 0.1M	Hz
Tecss	Delay from CS High to SK High	2.7V<Vcc<5.5V	160/640			ns
Tecsh	Delay from SK Low to CS Low	2.7V<Vcc<5.5V	1120 /4480			ns
Tedts	Setup Time of DI to SK	2.7V<Vcc<5.5V	160/640			ns
Tedth	Hold Time of DI after SK	2.7V<Vcc<5.5V	2320 /9280			ns
Tecsl	CS Low Time	2.7V<Vcc<5.5V	7400/ 29600			ns

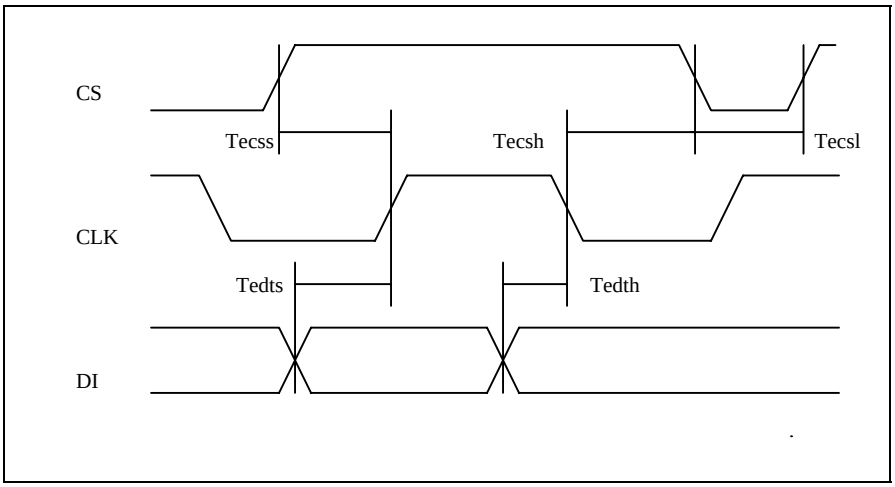


Fig - 20 Serial EEPROM timing

- **MII Interface Timing**

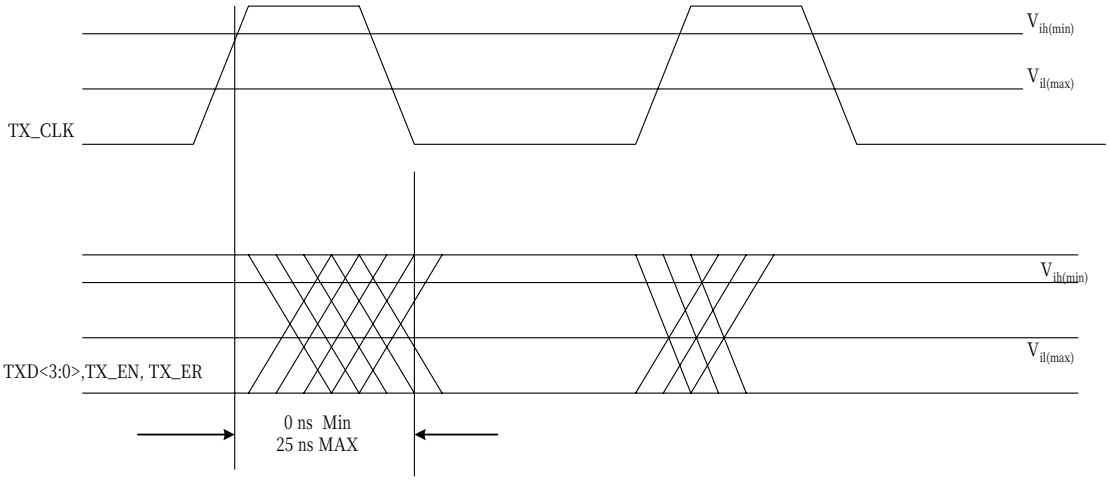


Fig- 21 Transmit signal timing relationships at the MII

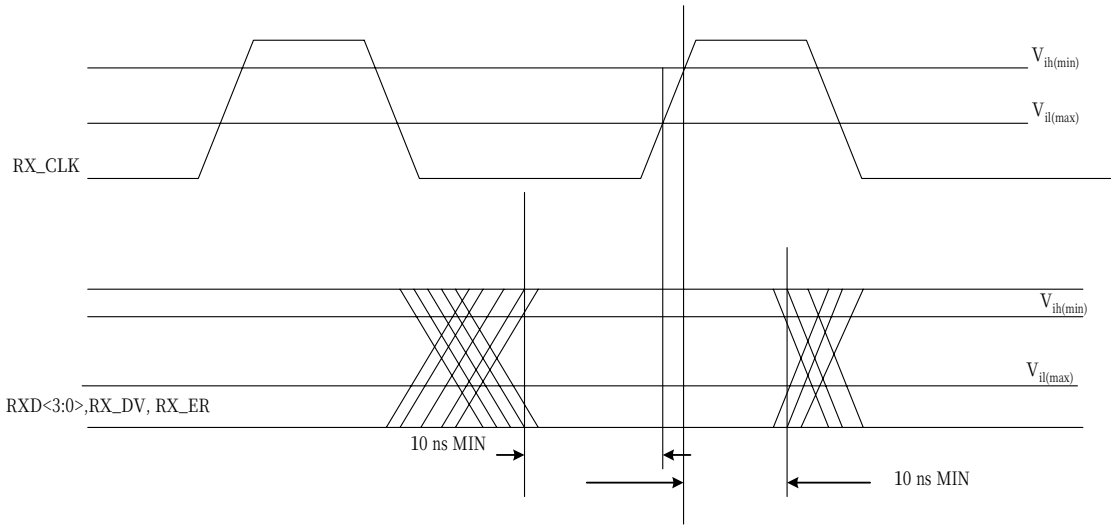


Fig- 22 Receive signal timing relations at the MII

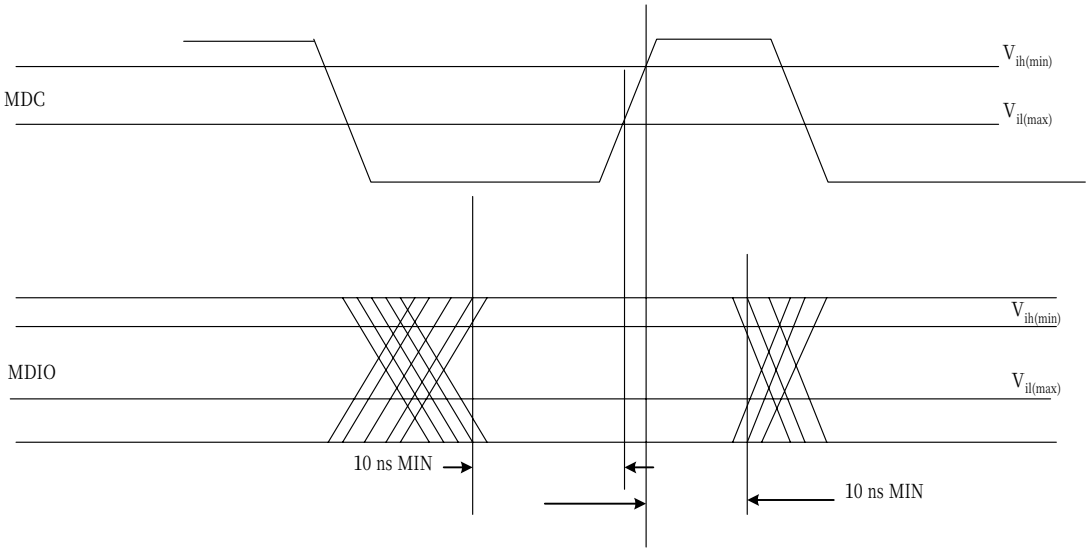


Fig- 23 MDIO sourced by STA

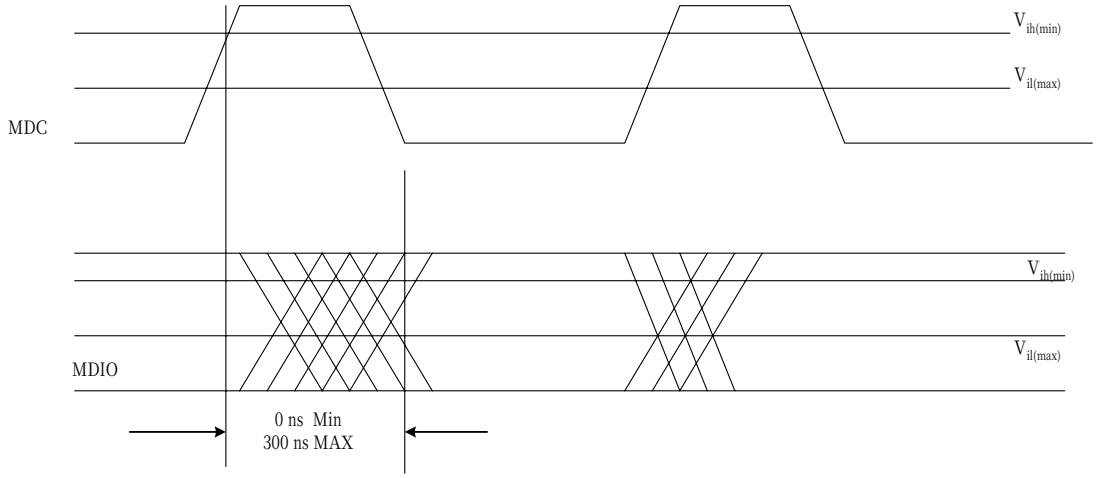


FIG- 24 MDIO SOURCED BY PHY

11. PACKAGE

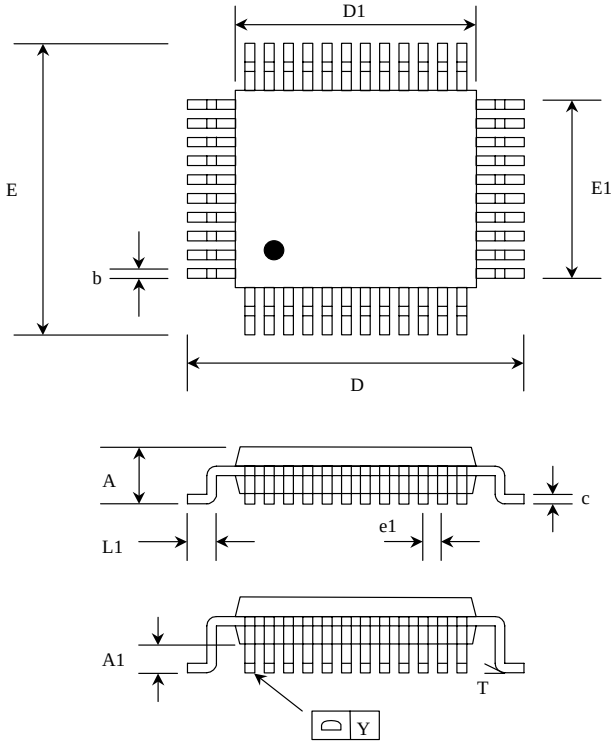


Fig - 25 Package outline for the AN983B / AN983BL

Dimensions for 128 –pin PQFP Package (AN983B)

Symbol	Description	Minimum	Maximum
A	Overall Height	-	3.4mm
A1	Stand Off	0.25mm	-
b	Lead Width	0.17mm	0.27mm
c	Lead Thickness	0.13mm	0.23mm
D	Terminal Dimension 1	23.0mm	23.4mm
D1	Package Body 1	19.9mm	20.1mm
E	Terminal Dimension 2	17.0mm	17.4mm
E1	Package Body 2	13.9mm	14.1mm
e1	Lead Pitch	0.50mm	-
L1	Foot Length	0.65mm	0.95mm
T	Lead Angle	0 °	7 °
Y	Coplanarity		0.076mm

Dimensions for 128 –pin LQFP Package (AN983BL)

Symbol	Description	Minimum	Maximum
A	Overall Height	-	1.6mm
A1	Stand Off	0.05mm	0.15mm
b	Lead Width	0.17mm	0.27mm
c	Lead Thickness	0.13mm	0.23mm
D	Terminal Dimension 1	21.9.0mm	22.1mm
D1	Package Body 1	19.9mm	20.1mm
E	Terminal Dimension 2	15.9.0mm	16.1mm
E1	Package Body 2	13.9mm	14.1mm
e1	Lead Pitch	0.50mm	-
L1	Foot Length	0.45mm	0.75mm
T	Lead Angle	0	7
Y	Coplanarity		0.076mm

12. LAYOUT GUIDE *(REV.1.0B)*

Layout Guide Revision History:

Revision Date	Revision	Description
October, 2000	1.0b	Add Item 2-d to reduce receive CRC error.

12.1 PLACEMENT

- ***Keep the distance as short as possible between Centaur-P and transformer, as well as transformer and RJ45.***
- ***Make crystal device cross to Centaur-P pin x1 x2, and away from the following item:***

  1). Tx+/- Rx+/- differential pairs

  2). PCB edge.

  3). Transformer

  4). Any other high frequency item and associated traces.
- ***Tx pull high resister needs to close to chip and Rx receiving termination resister and cap need to close to transformer.***
- ***De-couple cap should be placed as close to chip as possible. The traces should be short.***
- ***Use ample dc-coupling and bulk capacitors to minimize noise.***
- ***Use X7R ceramic capacitor for better capacitive characteristics over temperature.***

12.2 TRACE ROUTING

- ***Arrangement Tx and Rx trace***

  1). Tx+/- and Rx+/- trace avoid right angle signal trace, suggest round angle >90°

  2). Trace width must be wide that should be 2X layout program minimum request or wide than 8 miles.

  3). Signal trace length between Tx+/- differential pairs should be cross to equal length the total should no long to 2 cm.same require apply to Rx+/-.

  4). Make Tx and Rx trace route at the same signal plane and had better not using bias.

  5). Every differential pairs as cross as possible, but no less then 8 miles and the space should be almost equal.

6). *Keep the distance between the Tx and Rx differential pairs large, even separate ground planes underneath Tx and Rx signal pairs.*

7). *Away from clock and power trace.*

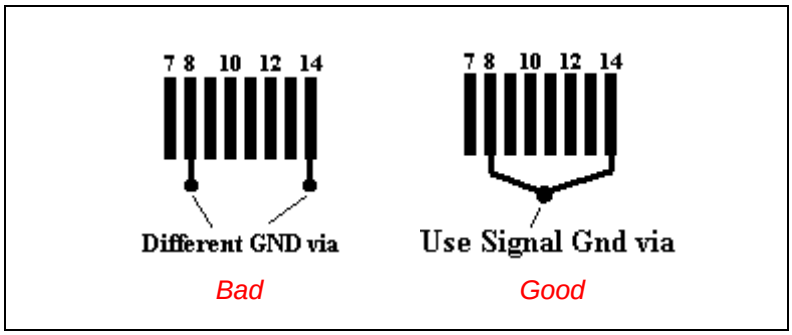
8). *If possible, with GND plane around.*

9). *If Tx rout trace must cross, you can swap the trace between chip and transformer, and transformer to RJ45, too.*

10). *The high frequency signal trace width 10~12mil.*

11). *PCI clk signal trace length must equal 2.5inch and other PCI bus signal trace length should less then 1.5 inch*

- ***Digital signal should away from analog signal and power trace. If can't be avoided, better be cross over by 90 degree with analog/Vcc routing at other plane.***
- ***Vcc trace should short and prefer route in the format of the plane a special for GND.***
- ***Connect Pin 8 and pin 14 together first then use signal via to Gnd.***



12.3 VCC AND GND

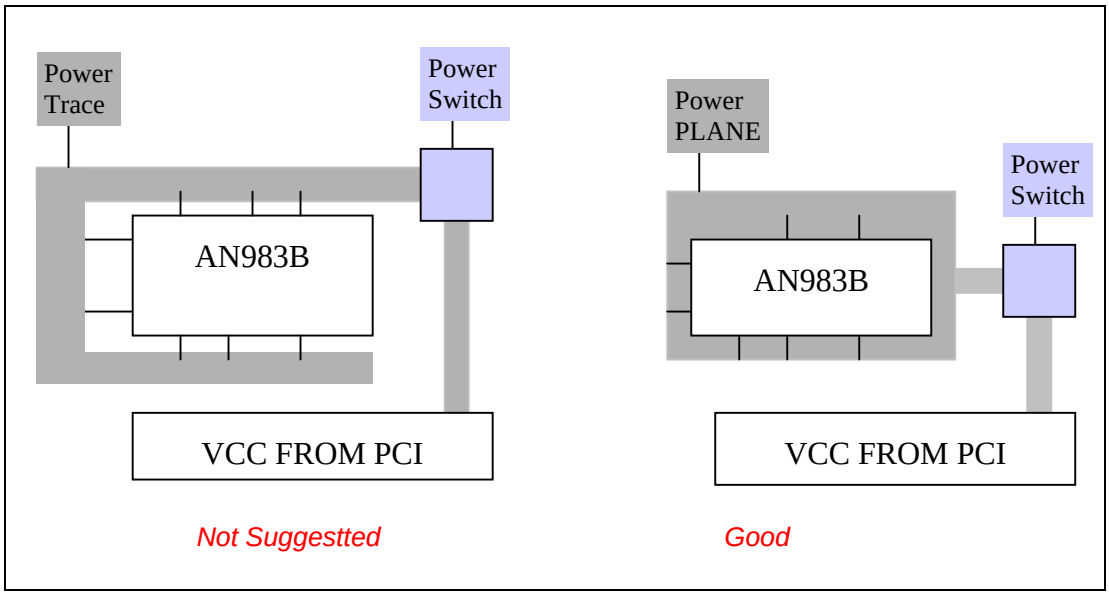
- ***Vcc power:***

1). *Avoid unnecessary Vcc trace to IC's and devices keep these trace as short and wide.*

2). *Power trace width > 40 mils (if power trace route to the other side .It must use several via to connect each other).*

3). *Power source use bulk capacitors (22~47uf) to reduce noise.*

4). Provide sample power and ground planes



■ *GND plane*

1). It is a good idea to fill in unused areas of the signal planes with solid copper

2). The signal ground region should be one continuous, unbroken plane extending from the transformer through the rest of the board.

3). On right angle is recommend when partition the Vcc and GND plane.

4). For EMI consideration, please add 0.1uF caps between system GND and chassis GND.

5). Void the power and ground plane directly under the transformer.

6). The isolation voltage of the transformer should be rated to be greater than 2kv.

7). The sample board Vcc and GND plane at below side.