M66250P/FP

5120×8-BIT LINE MEMORY(FIFO/LIFO)

DESCRIPTION

The M66250P/FP is a high-speed line memory with a FIFO (First In First Out) structure of 5120 -word×8-bit configuration which uses high-performance silicon gate CMOS process technology.

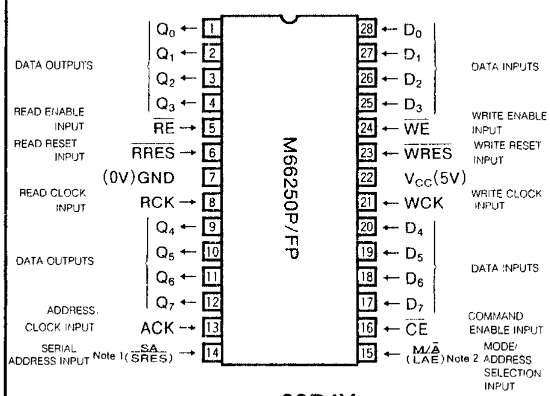
The M66250 can also be used for LIFO (Last In First Out). The start address of reading can be specified.

It has separate clock, enable and reset signals for write and read and is most suitable as a buffer memory between devices with different data processing throughput.

FEATURES

- Memory configuration of 5120 words × 8 bits (dynamic memory)
- High-speed cycle ························ 50ns (Min.)
- High-speed access ························ 40ns(Max.)
- Output hold ························ 5ns (Min.)
- FIFO/LIFO switching function
- Start address specification function (at reading)
- LIFO operation on single chip
- Built in pullup/pulldown resistor for the mode control pin.
- Write and read operations can be performed separately.
- Variable-length delay bit
- Output ························ 3-state

PIN CONFIGURATION (TOP VIEW)



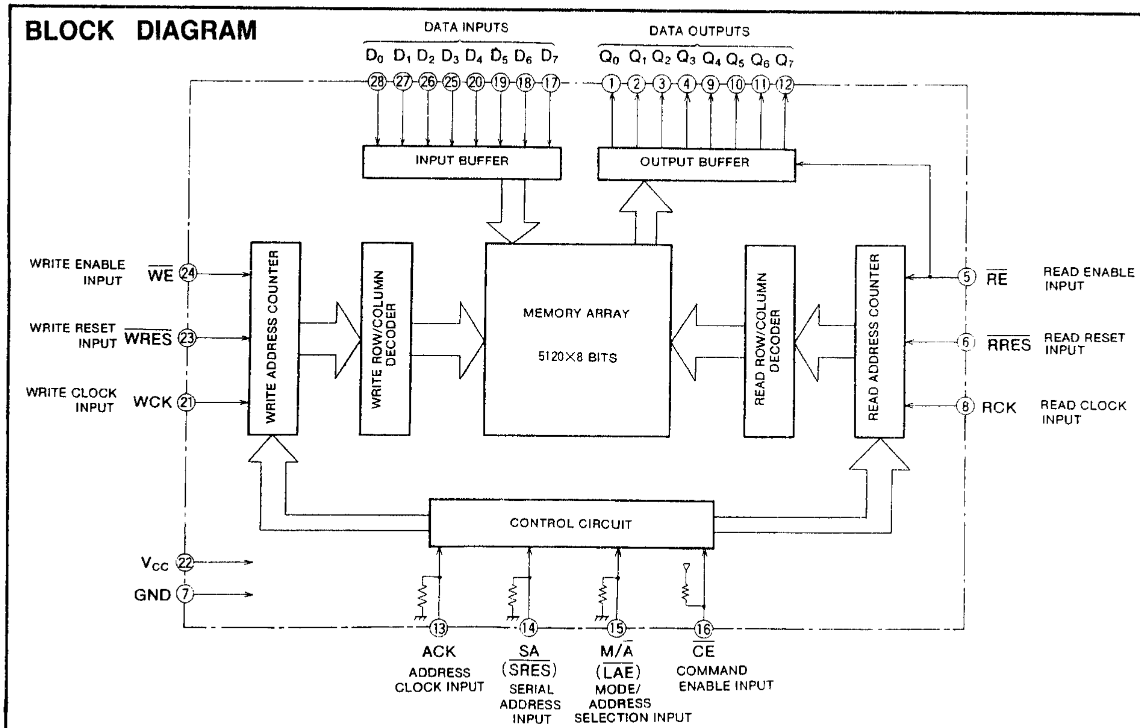
Outline 28P4Y
28P2W-C

Note 1 : $\overline{SRES}$ sets the system reset mode.
Note 2 : $\overline{LAE}$ can switch to a validness or invalidness of start address except during instruction cycles.

APPLICATION

High-speed facsimiles, digital photocopiers, laser beam printers.

BLOCK DIAGRAM



FUNCTION

Write is performed by taking in the content of data inputs $D_0 \sim D_7$, in synchronous with the rise of the write clock input WCK, when write enable input $\overline{\text{WE}}$ is low-level, the write address counter incrementing or decrementing simultaneously. When $\overline{\text{WE}}$ is high-level, write is prohibited and the write address counter stops. When the write reset input $\overline{\text{WRES}}$ is set to low-level, the write address counter is initialized. When the read enable input $\overline{\text{RE}}$ is low-level, read is performed by outputting the memory content to data output $Q_0 \sim Q_7$ in synchronous with the rise of the read clock input RCK, and the read address counter is incremented or decremented at same time.

When $\overline{\text{RE}}$ is high-level, read is prohibited, and the read address counter stops. The output enters the floating state (high-impedance state).

When the read reset input $\overline{\text{RRES}}$ is set to low-level, the read address counter is initialized.

When command enable input $\overline{\text{CE}}$ is low-level, the instruction cycle is enabled. The FIFO/LIFO mode is set by the serial address input SA in synchronous with the rise of the address clock input ACK during the instruction cycle when the mode/address selection input M/$\overline{\text{A}}$ is high-level. The start address is set by the serial address input SA in synchronous with the rise of the address clock input ACK during the instruction cycle when M/$\overline{\text{A}}$ is low-level.

FUNCTIONAL DESCRIPTION

1. Function Setting

(1) Function setting table

① **System reset setting**

$\overline{\text{CE}}$	(SA) $\overline{\text{SRES}}$	$\overline{\text{RRES}}$	RCK	Function
H	L	L	↑	FIFO mode, no start address setting, read counter reset

$\overline{\text{CE}}$	(SA) $\overline{\text{SRES}}$	$\overline{\text{WRES}}$	WCK	Fuction
H	L	L	↑	FIFO mode, no start address setting, write counter reset

② **Mode setting**

$\overline{\text{CE}}$	M/$\overline{\text{A}}$ ($\overline{\text{LAE}}$)	ACK	SA ($\overline{\text{SRES}}$)	Function
L	H	↑	H	FIFO mode setting
L	H	↑	L	LIFO mode setting
L	L	↑	×	Start address setting (13 bits)

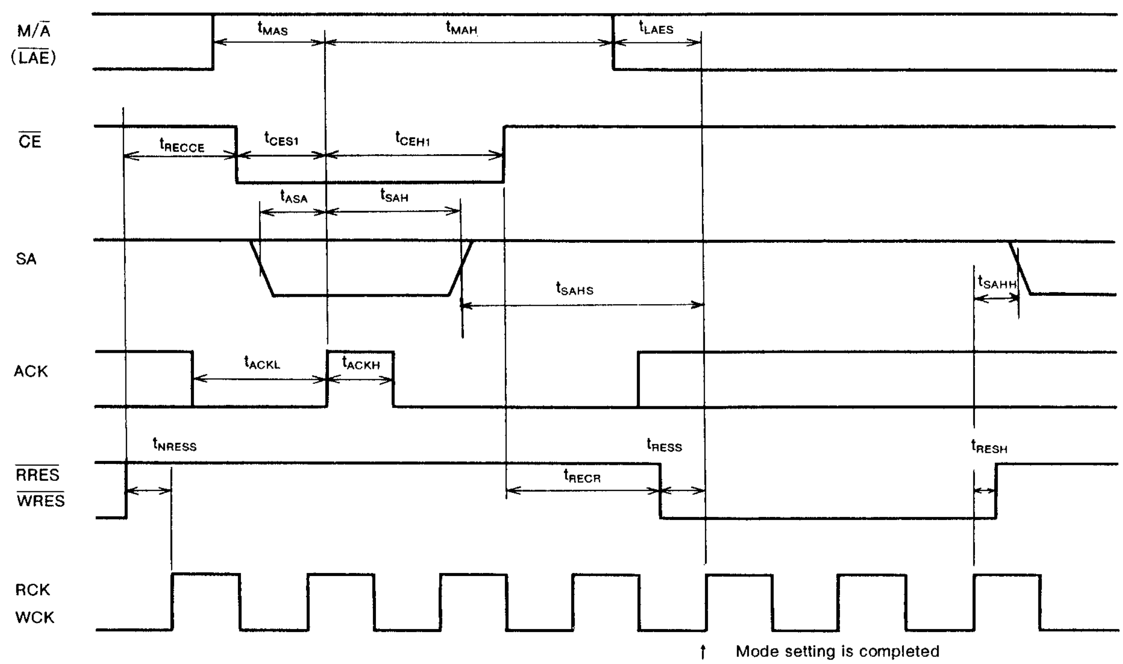
× : L or H

Note : The above mode becomes effective after the first reset.

③ **Effect of start address setting**

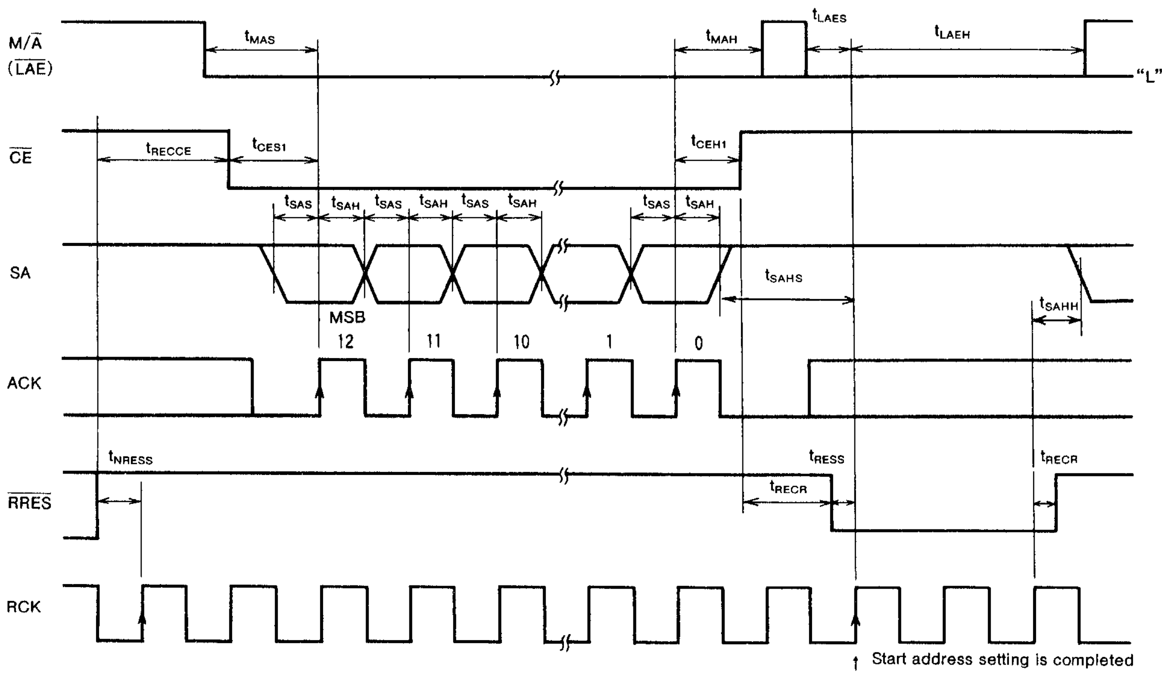
$\overline{\text{CE}}$	SA ($\overline{\text{SRES}}$)	(M/$\overline{\text{A}}$) $\overline{\text{LAE}}$	$\overline{\text{RRES}}$	RCK	Function
H	H	L	L	↑	Start address setting is effective
H	H	H	L	↑	Start address setting is not effective

(2) FIFO/LIFO mode setting
When the mode/address selection input M/$\overline{A}$ is high-level and the command enable input $\overline{CE}$ is low-level, the FIFO/-LIFO mode is selected by the serial address input SA, in synchronous with the address clock input ACK. When the command enable input $\overline{CE}$ is high-level and the write reset input $\overline{WRES}$ is low-level, mode setting is completed in synchronous with the rise of the write clock input WCK, also provided that the write reset input $\overline{WRES}$ is low-level, in synchronous with the rise of the read clock input RCK and the read reset input $\overline{RRES}$ is low-level. The address counter is initialized at the same time.

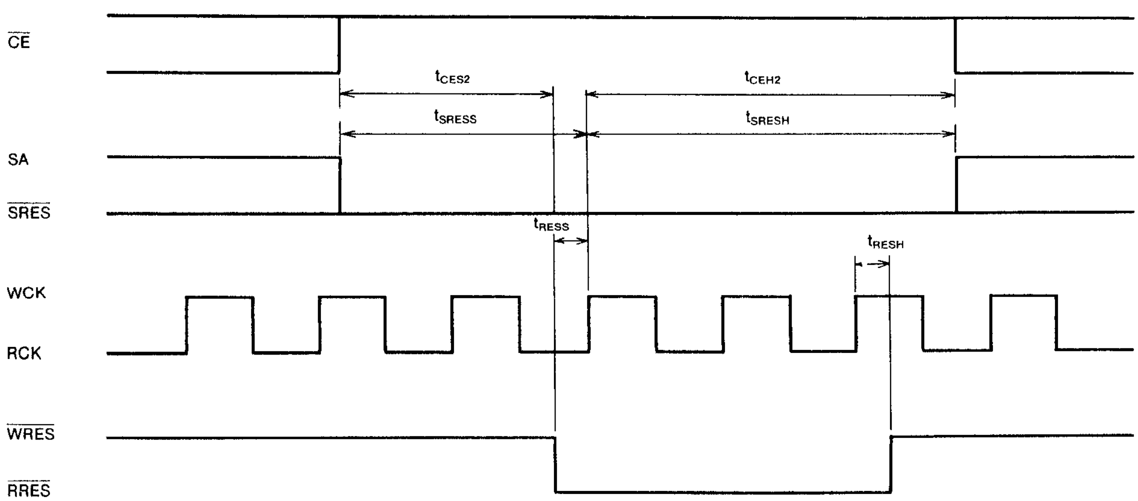


In the FIFO mode, the write address counter moves to address 0 in synchronous with the rise of the write clock input WCK when the write reset input $\overline{WRES}$ is set to low-level. The address of the write address counter increases in synchronous with the rise of the write clock input WCK.
When the read reset input $\overline{RRES}$ is low-level, the read address counter moves to address 0 if the start address is not specified, and moves to the start address if the start address is specified, in synchronous with the rise of the read clock input RCK. The cycles of the read address counter increases in synchronous with the read clock input RCK.
In LIFO mode the write address counter moves to address 0 or 5119 in synchronous with the rise of write clock input WCK, when the write reset input $\overline{WRES}$ is low-level, and, the read address counter moves to address 0 or 5119 if the start address is not specified or to the start address m or 5119-m if the start address is specified, in synchronous with the rise of the read clock input RCK. When the read reset input $\overline{RRES}$ is low-level. The cycle of the write address counter goes up or down in synchronous with the rise of the write clock input WCK.

(3) Start address setting
When the mode/address selection input M/$\overline{A}$ is low-level and the command enable input $\overline{CE}$ is low-level, the address that reading starts from is set by serial address input SA in synchronous with the rise of the address clock input ACK. When the command enable input $\overline{CE}$ is high-level and the read reset input $\overline{RRES}$ is low-level, the read address counter moves to the specified address in synchronous with the rise of the read clock invut RCK.



(4) System reset setting
(FIFO and address counter reset setting)
When the command enable input $\overline{CE}$ is high-level and $\overline{SRES}$ is low-level, and if the write reset input $\overline{WRES}$ and read reset input $\overline{RRES}$ are set to low-level, then the FIFO mode setting and the address counter are reset in synchronous with the rise of WCK and RCK.

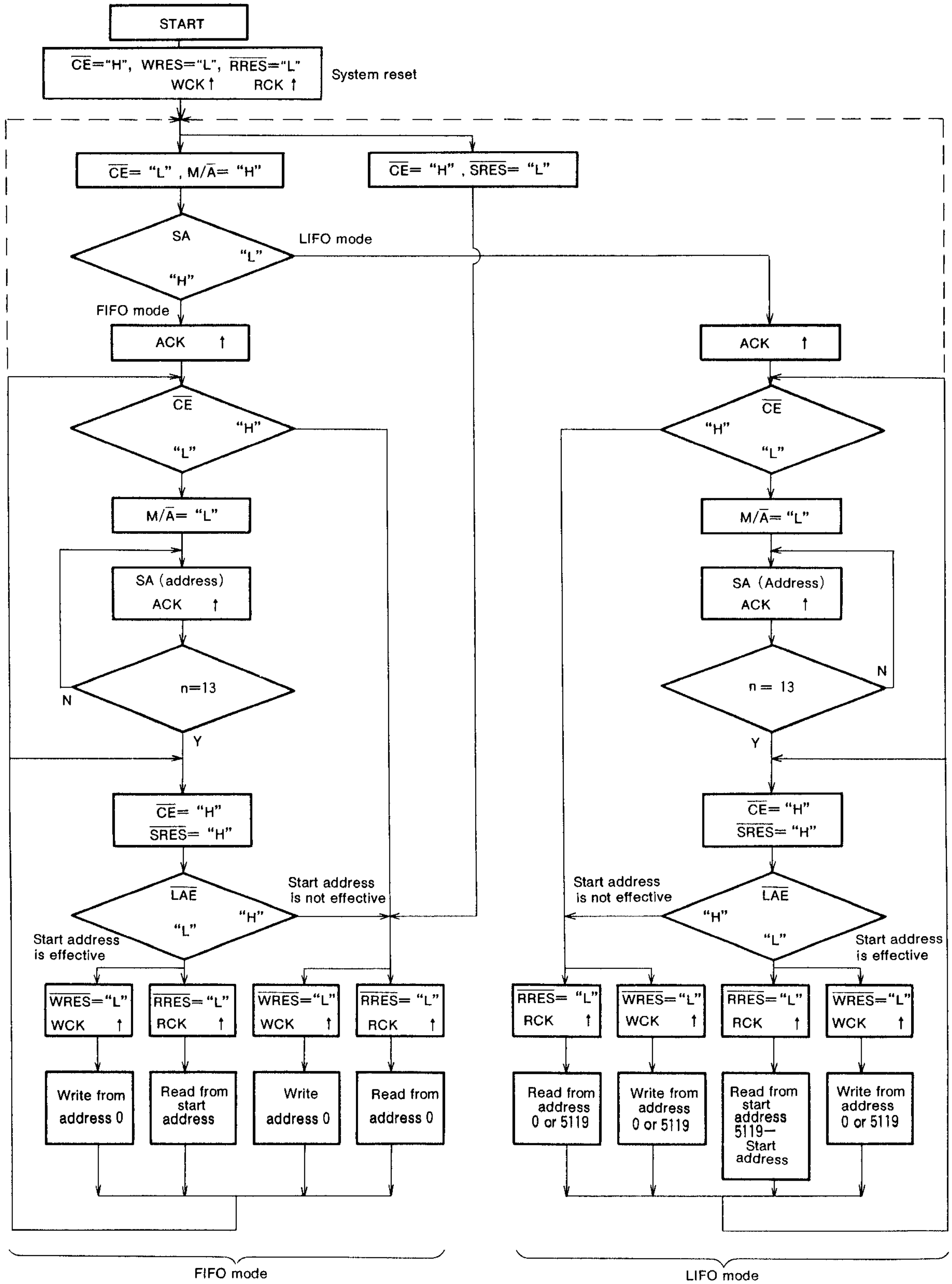


(Note) To uneffect system reset, SA($\overline{SRES}$) should be set to high-level during $\overline{WRES}$ and $\overline{RRES}$ are low-level.

2. Write address and read address operation in FIFO and LIFO mode

FIFO and LIFO mode setting	Start address setting	Write address and read address operation	Write address/read address in read reset/write reset operation
FIFO	No	Write address 0 W A 5119 Read address 0 R A 5119	Write address : address counter is set to 0 Read address : address counter is set to 0
LIFO	No	① Read address 0 R 5119 Write address 0 W 5119 ② Read address R read the write data ① Write address W ③ Read address R read the write data ② Write address W	Write address : the set address of 0 or 5119 is set mutually. Read address : the set address of 0 or 5119 is set mutually.
FIFO	Yes	Write address 0 W A 5119 Read address 0 m R A 5119	Write address : address counter is set to 0 Read address : address counter is set to m which is specified by the start address
LIFO	Yes	① Read address 5119-m R 5119 Write address 0 W m ② Read address R read the write data ① Write address W ③ Read address R read the write data ② Write address W	Write address : the set address of 0 or 5119 is set mutually. Read address : address counter is set to address which is specified as the start address

OPERATION FLOW CHART



Note : Perform write reset and read reset before setting function after power-on.

ABSOLUTE MAXIMUM RATINGS (T_a=−20+70℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+7.0	V
V_I	Input voltage		−0.5～V_{CC}+0.5	V
V_O	Output voltage		−0.5～V_{CC}+0.5	V
P_d	Maximum power dissipation	Ta=25℃	550(Note 1)	mW
Tstg	Storage temperature range		−65 ～+150	℃

Note 1 : Ta≧68℃ are derated at −9.7mw/℃ (28P_2W)

RECOMMENDED OPERATING CONDITIONS (T_a=−20～+70℃)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Ground		0		V
T_{opr}	Operating ambient temperature range	−20		70	℃

ELECTRICAL CHARACTERISTICS (T_a=−20～+70℃, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	I_{OH}=−4mA		V_{CC}−0.8			V
V_{OL}	Low-level output voltage	I_{OL}=4mA				0.55	V
I_{IH}	High-level input current	V_I=V_{CC}	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK, $\overline{CE}$, D0～D7			1.0	μA
		V_I=V_{CC}	ACK, SA($\overline{SRES}$), M/$\overline{A}$($\overline{LAE}$)			0.27	mA
I_{IL}	Low-level input current	V_I=GND	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK, ACK, SA($\overline{SRES}$), M/$\overline{A}$($\overline{LAE}$), D0～D7			−1.0	μA
		V_I=GND	$\overline{CE}$			−0.27	mA
I_{OZH}	Off state high-level output current	V_0=V_{CC}				5.0	μA
I_{OZL}	Off state low-level output current	V_0=GND				−5.0	μA
I_{CC}	Average operating supply current	V_I=V_{IH}, V_{IL} Output open t_{WCK}, t_{RCK}=100ns				100	mA
CI	Input capacitance	f=1MHz				10	pF
CO	Output capacitance when off.	f=1MHz				15	pF

SWITCHING CHARACTERISTICS (T_a=−20～+70℃, V_{CC}= 5 V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AC}	Access time				40	ns
t_{OH}	Output hold time		5			ns
t_{OL}	Output "L" period when reset		5		40	ns
t_{OEN}	Output enable time		5		40	ns
t_{ODIS}	Output disable time		5		40	ns

TIMING REQUIREMENTS (T_a=−20∼+70℃, V_{CC}= 5 V±10%, unless otherwise noted)

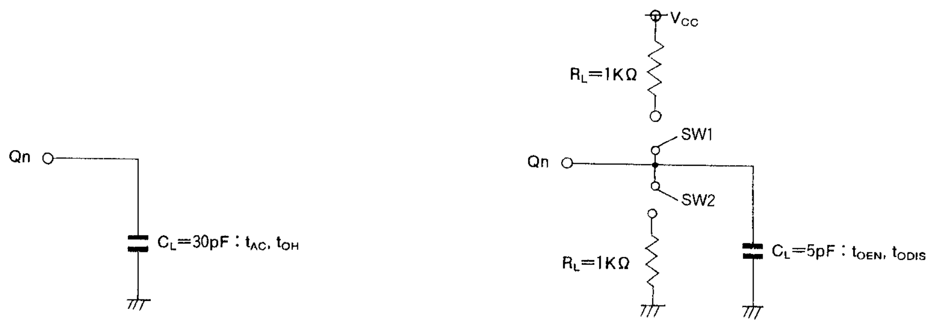
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{WCK}	Write clock (WCK) cycle		50			ns
t_{WCKH}	Write clock (WCK) "H" pulse width		25			ns
t_{WCKL}	Write clock (WCK) "L" pulse width		25			ns
t_{RCK}	Read clock (RCK) cycle		50			ns
t_{RCKH}	Read clock (RCK) "H" pulse width		25			ns
t_{RCKL}	Read clock (RCK) "L" pulse width		25			ns
t_{DS}	Data set up time before WCK		15			ns
t_{DH}	Data hold time after WCK		5			ns
t_{RESS}	Reset set up time before WCK, RCK		15			ns
t_{RESH}	Reset hold time after WCK, RCK		5			ns
t_{NRESS}	Non-reset set up time before WCK, RCK		25			ns
t_{NRESH}	Non-reset hold time after WCK, RCK		5			ns
t_{WES}	$\overline{WE}$ set up time before WCK		15			ns
t_{WEH}	$\overline{WE}$ hold time after WCK		5			ns
t_{NWES}	$\overline{WE}$ non-select set up time before WCK		15			ns
t_{NWEH}	$\overline{WE}$ non-select hold time after WCK		5			ns
t_{RES}	$\overline{RE}$ set up time before RCK		15			ns
t_{REH}	$\overline{RE}$ hold time after RCK		5			ns
t_{NRES}	$\overline{RE}$ non-select set up time before RCK		15			ns
t_{NREH}	$\overline{RE}$ non-select hold time after RCK		5			ns
t_r, t_f	Input pulse rise and fall time				20	ns
t_H	Data hold time				20	ms

Note 1 : For 1 line access, the following should be satis fild:
$\overline{WE}$ "H" level period≦ 20ms−5120·t_{WCK}- $\overline{WRES}$ "L" level period
$\overline{RE}$ "H" level period≦ 20ms−5120·t_{RCK}- $\overline{RRES}$ "L" level period

TIMING REQUIREMENTS (T_a=−20∼+70℃, V_{CC}= 5 V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{MAS}	M/$\overline{A}$ set up time before ACK		25			ns
t_{MAH}	M/$\overline{A}$ hold time after ACK		5			ns
t_{CES1}	$\overline{CE}$ set up time before ACK		25			ns
t_{CEH1}	$\overline{CE}$ hold time after ACK		5			ns
t_{SAS}	SA set up time before ACK		25			ns
t_{SAH}	SA hold time after ACK		5			ns
t_{LAES}	$\overline{LAE}$ set up time before WCK, RCK		25			ns
t_{LAEH}	$\overline{LAE}$ hold time after WCK, RCK		5			ns
t_{SAHS}	SA "H" set up time before WCK, RCK when reset		25			ns
t_{SAHH}	SA "H" hold time after WCK, RCK when reset		5			ns
t_{CES2}	$\overline{CE}$ set up time before WCK, RCK when system reset		25			ns
t_{CEH2}	$\overline{CE}$ hold time after WCK, RCK when system reset		5			ns
t_{SRESS}	$\overline{SRES}$ set up time before WCK, RCK when system reset		25			ns
t_{SRESH}	$\overline{SRES}$ hold time after WCK, RCK when system reset		5			ns
t_{ACKH}	"H" pulse width for ACK		50			ns
t_{ACKL}	"L" pulse width for ACK		50			ns
t_{RECR}	WCK, RCK recovery time after mode set		100			ns
t_{RECCE}	$\overline{CE}$ recovery time after reset		100			ns

TEST CIRCUIT

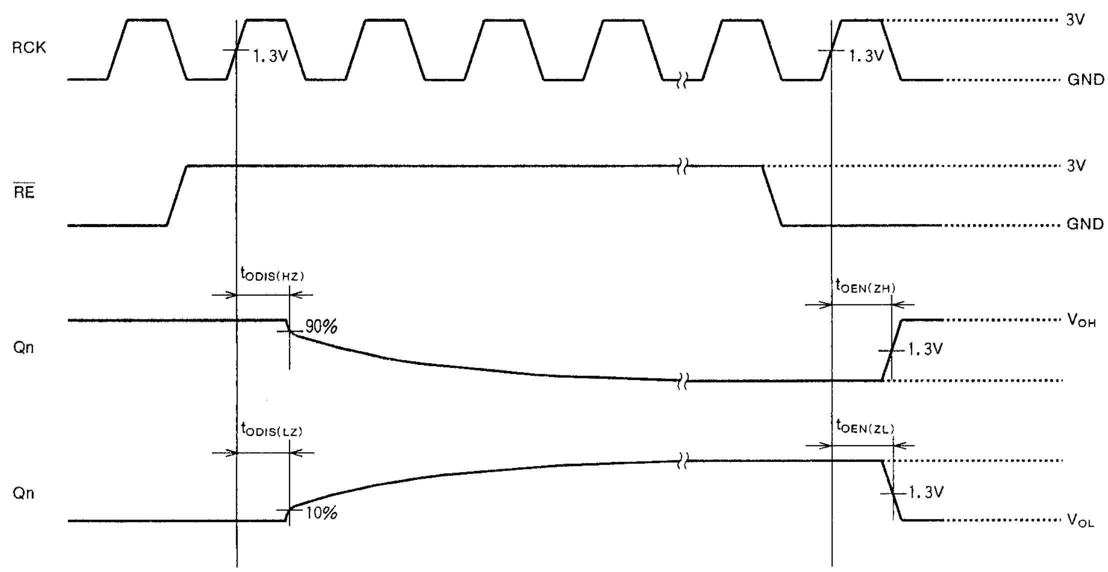


Input pulse amplitude		: 0~3V
Input pulse rise and fall time		: 3ns
Reference voltage	Input	: 1.3V
	Output	: 1.3V (However, $t_{ODIS(LZ)}$ is 10% of output amplitude and $t_{ODIS(HZ)}$ is 90% of that for decision).

Item	SW1	SW2
$t_{ODIS(LZ)}$	Close	Open
$t_{ODIS(HZ)}$	Open	Close
$t_{OEN(ZL)}$	Close	Open
$t_{OEN(ZH)}$	Open	Close

Load capacity C_L includes float capacity of connection and input capacity of probe.

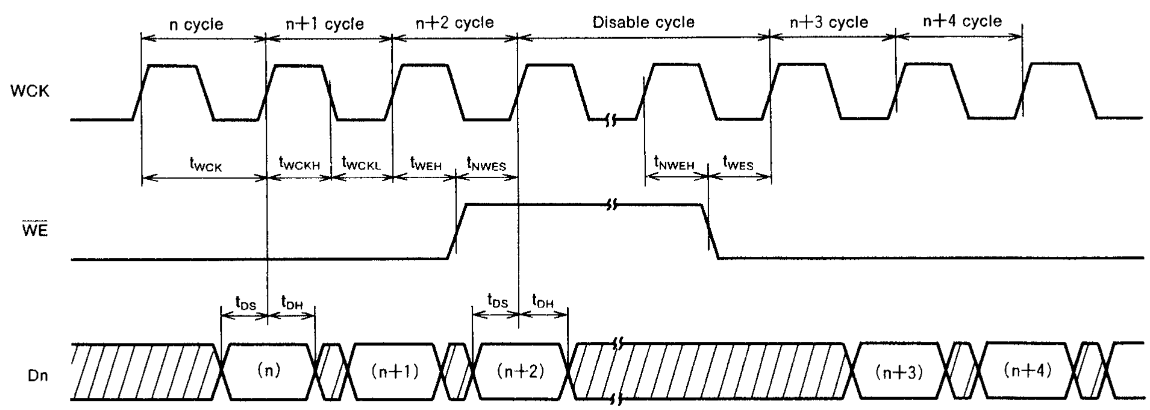
t_{ODIS}, t_{OEN} Test Condition



OPERATION TIMING

1. FIFO mode

- Write cycle (This operation timing is irrelevant to start address setting)

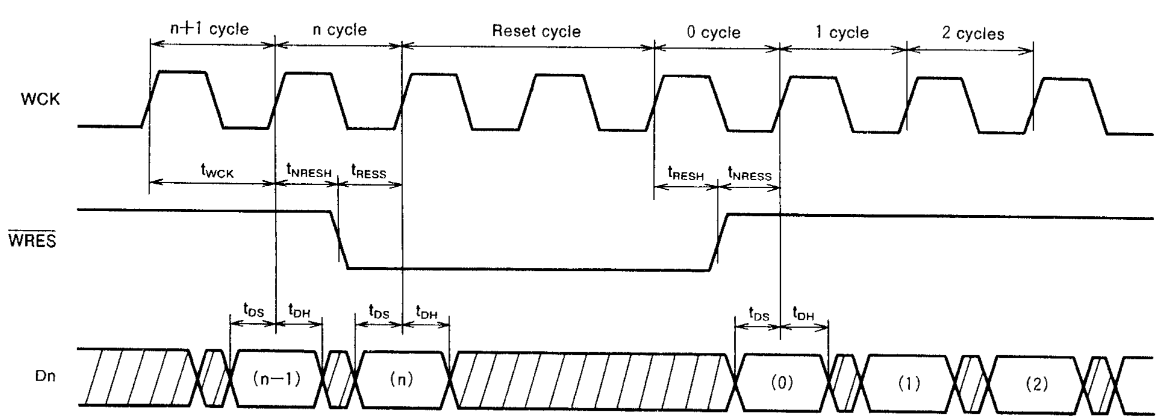


$\overline{WRES}$= "H" , $\overline{LAE}$= "L" or "H"

$\overline{SRES}$= "H"

- Write reset cycle (Irrelevant to start address setting)

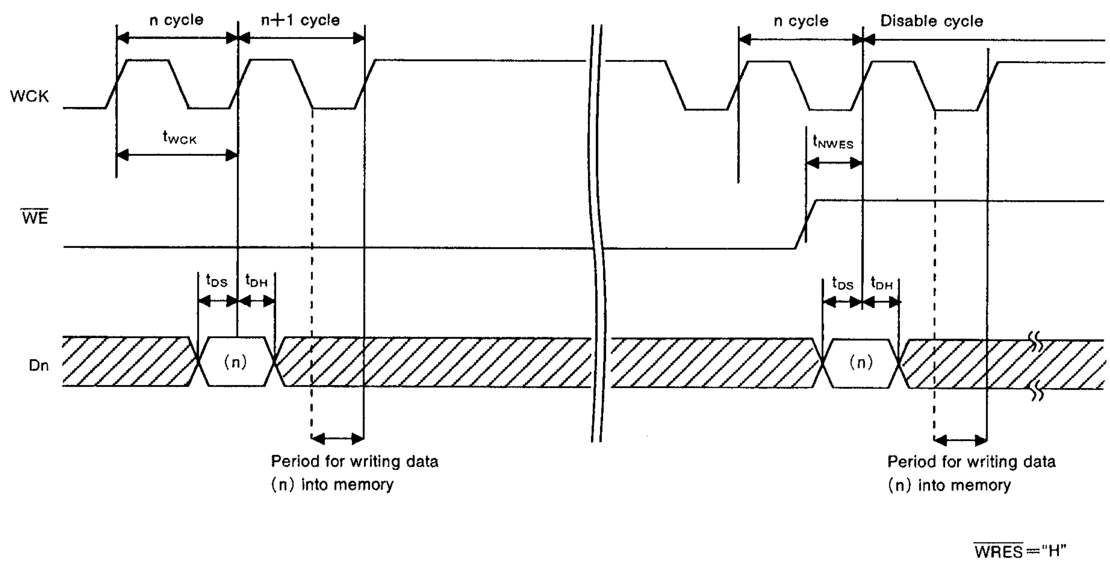
(The reset cycle requires a minimum of two cycles. Before the first reset cycle and after the power is turned on $\overline{WRES}$ should be set to high-level for 1 cycle or more.)



$\overline{WE}$= "L" , $\overline{LAE}$= "L" or "H"

$\overline{SRES}$ "H"

- **Matters that needs attetion when WCK stops**

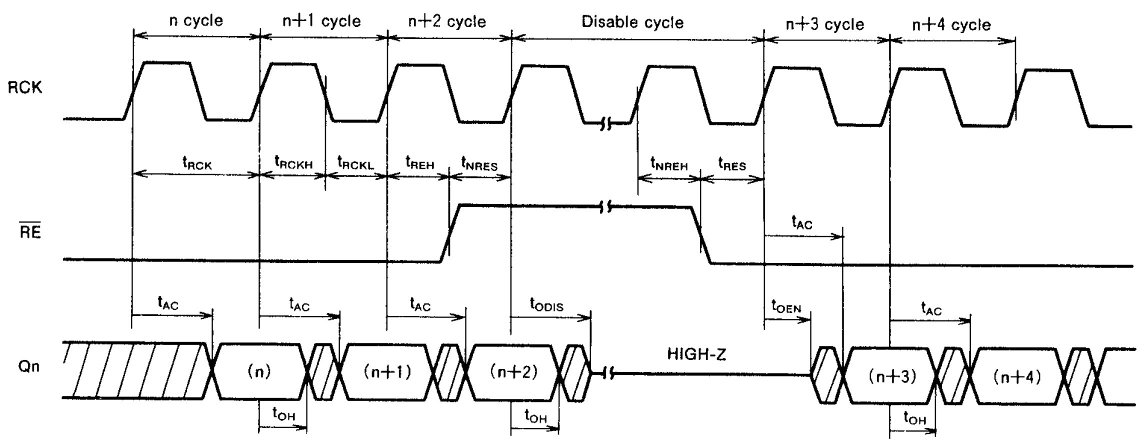


Input data of n cycle is read at the rising edge after WCK of n cycle and writing operation starts in the WCK low-level period of n+1 cycle. The writing operation is complete at the falling edge after n+1 cycle.

To stop reading write data at n cycle, enter WCK before the rising edge after n+1 cycle.

When the cycle next to n cycle is a disable cycle, WCK for a cycle requires to be entered after the disable cycle as well.

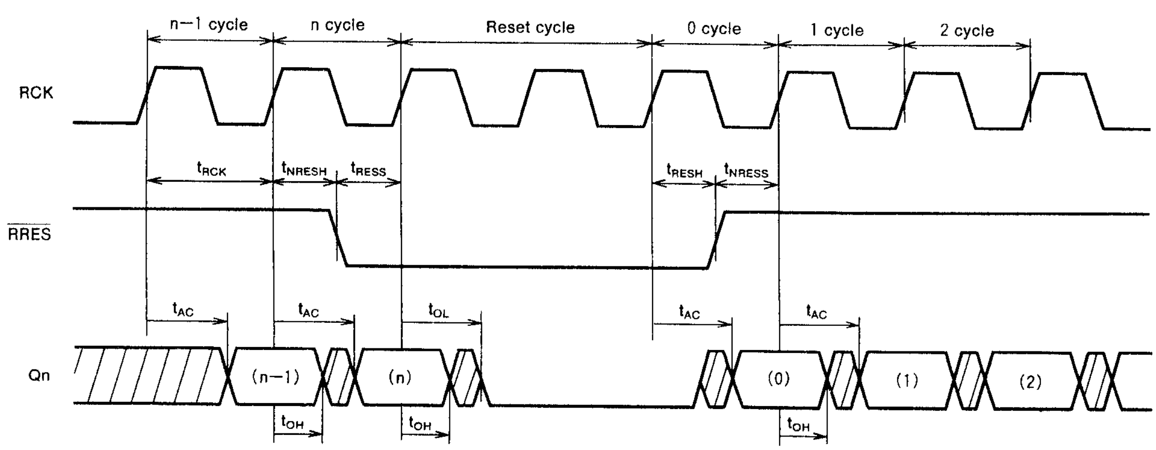
- **Read cycle (This operation timing is irrelevant to start address setting)**



$\overline{RRES}$= "H" , $\overline{LAE}$= "L" or "H"
$\overline{SRES}$= "H"

- **Read reset cycle**

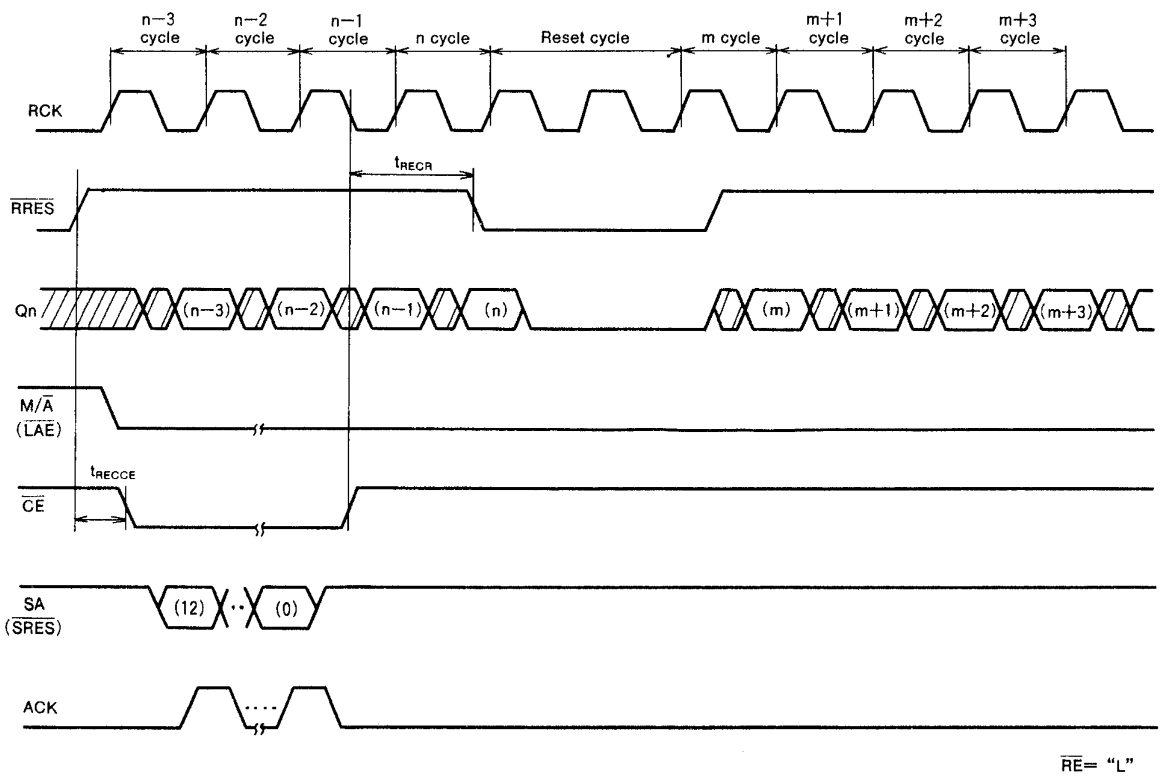
(The reset cycle requires two cycles at minimum. During the first two cycles Qn is low-level. For one cycle or more, $\overline{RRES}$ should be set to high-level befor the first reset cycle, and after power is turned on.)



$\overline{RE}$= "L" , $\overline{LAE}$= "H"
$\overline{SRES}$= "H"

- **Read reset cycle (start address is set)**

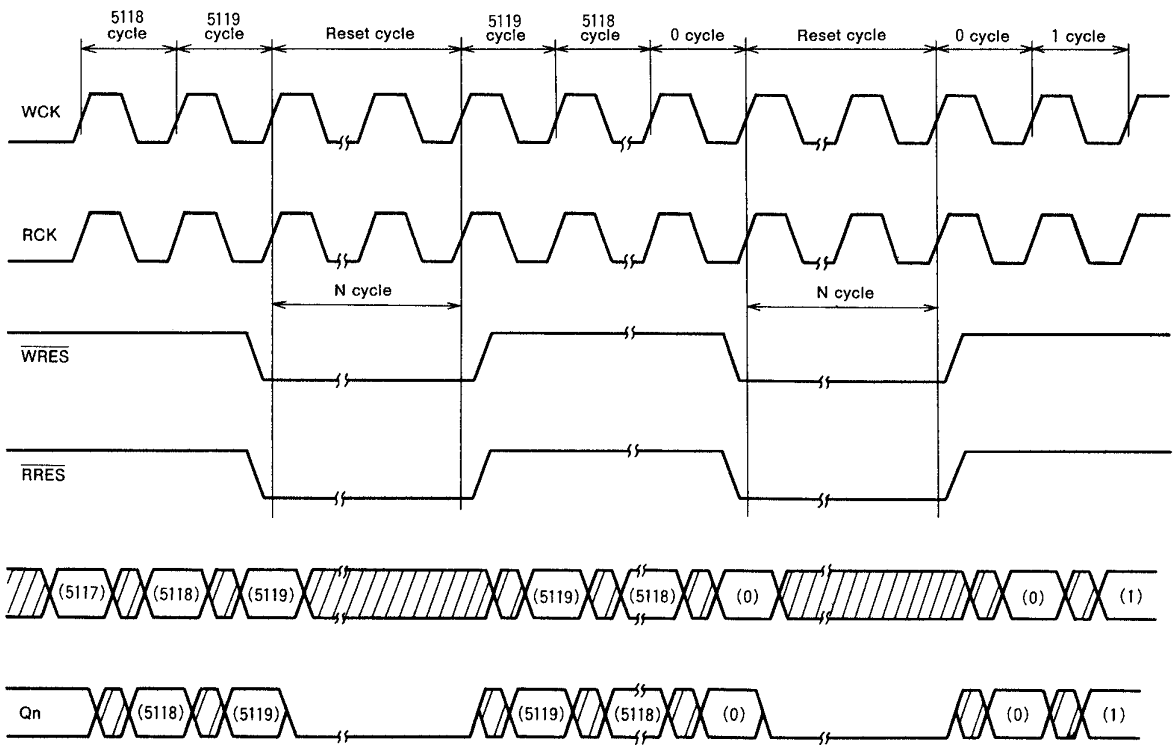
(The reset cycle requires two cycles at minimum. During the first two cycles, Qn is low-level. For at least one cycle $\overline{RRES}$ should be set to high-level before the first reset cycle, and after power is turned on.)



2. LIFO mode

- **Start address is not set**

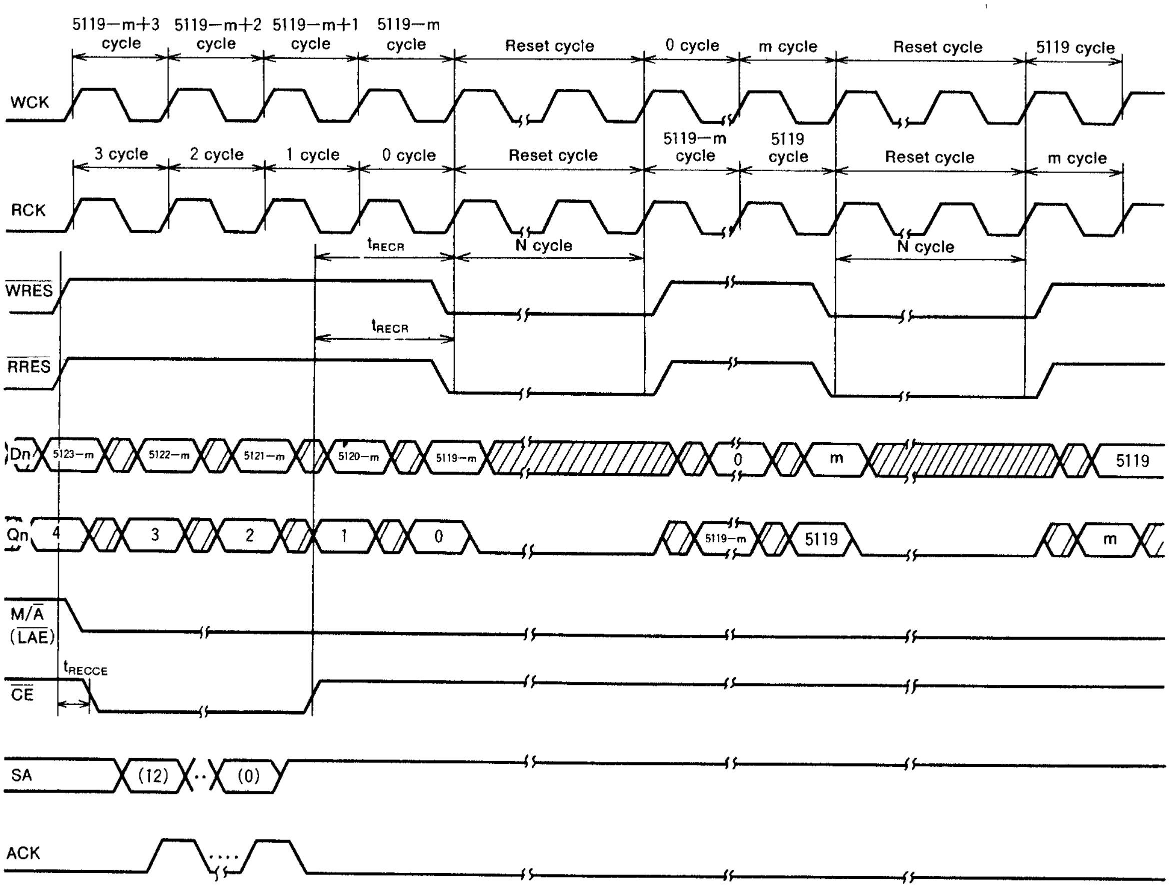
(The reset cycle requires two cycles at minimum. During the first two cycles, Qn is low-level. For at least one cycle, $\overline{\text{RRES}}$ should be set to high-level and $\overline{\text{WRES}}$ should be set to high-level before the first reset cycle and after power is turned on.)



N≧3 $\overline{\text{RE}}$, $\overline{\text{WE}}$ = "L"
$\overline{\text{LAE}}$ = "H"
$\overline{\text{CE}}$ = "H"
$\overline{\text{SRES}}$ = "H"

● **Start address is set**

(The reset cycle requires two cycles at minimum, and the first two cycles Qn is low-level. More than one cycle should be set when $\overline{RRES}$ is high-level before the first reset cycle after power on.)



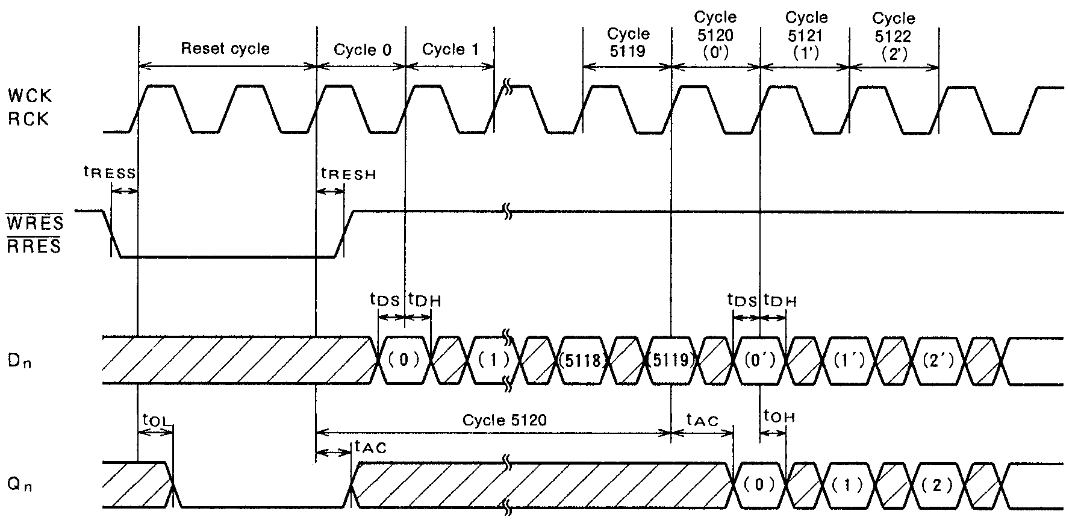
N≧3 $\overline{RE}$, $\overline{WE}$= "L"

3. Variable length delay bits

(1) FIFO mode/without setting of start address

● **1-line (5120 bits) delay**

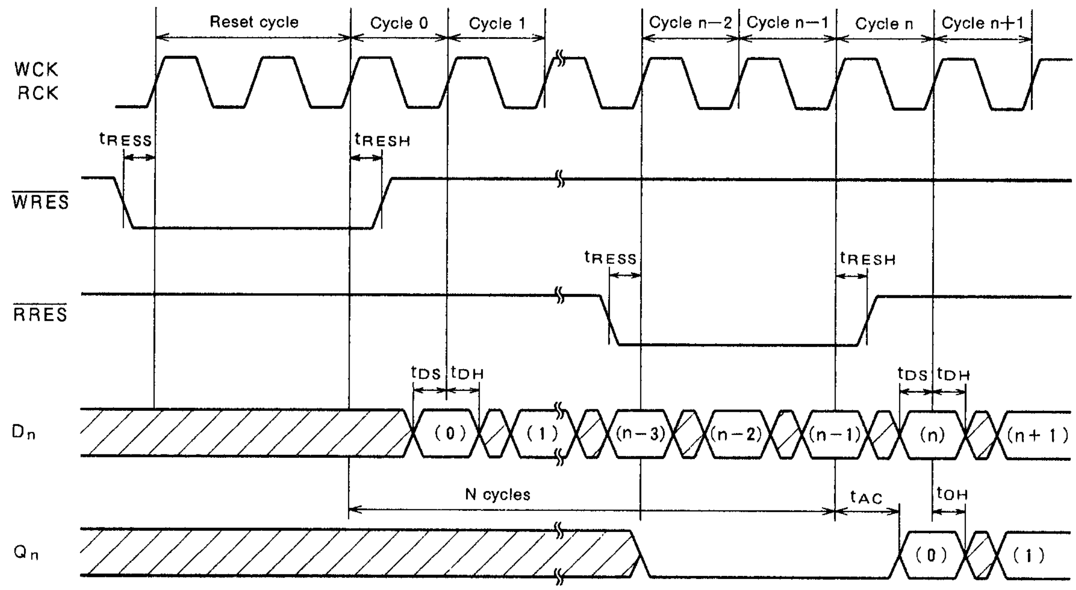
A write input data is written to memory at the second rise edge of WCK in the cycle, and a read output data is output from memory at the first rise edge of RCK in the cycle, so that 1-line delay can be made easily (A reset cycle requires at least 2 cycles. Qn goes to the "L" level during the first 2 cycles. However, it is necessary to set at least one cycle of $\overline{RRES}$="H" and $\overline{WRES}$="H" before the first reset cycle after power is turned on).



$\overline{WE}$, $\overline{RE}$="L", $\overline{LAE}$="H", $\overline{SRES}$="H"

- **N-bit delay 1**

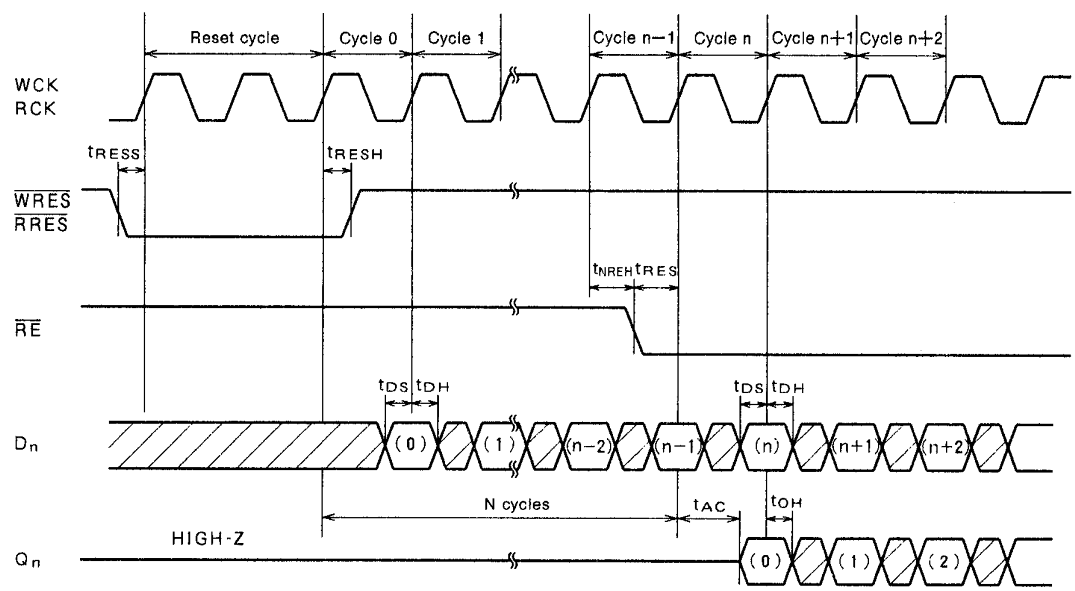
(Sliding input timing of $\overline{WRES}$ and $\overline{RRES}$ at a cycle corresponding to delay length)
(A reset cycle requires at least 2 cycles. Qn goes to the "L" level during the first 2 cycles. However, it is necessary to set at least one cycle of $\overline{RRES}$= "H" and $\overline{WRES}$="H" before the first reset cycle after power is turned on).



$\overline{WE}$, $\overline{RE}$="L", $\overline{LAE}$="H", $\overline{SRES}$="H"
N≧3

- **N-bit delay 2**

(Disabling RE during the period corresponding to delay length to slide an address)
(A reset cycle requires at least 2 cycles. Qn goes to the "L" level during the first 2 cycles. However, it is necessary to set at least one cycle of $\overline{RRES}$= "H" and $\overline{WRES}$="H" before the first reset cycle after power is turned on).

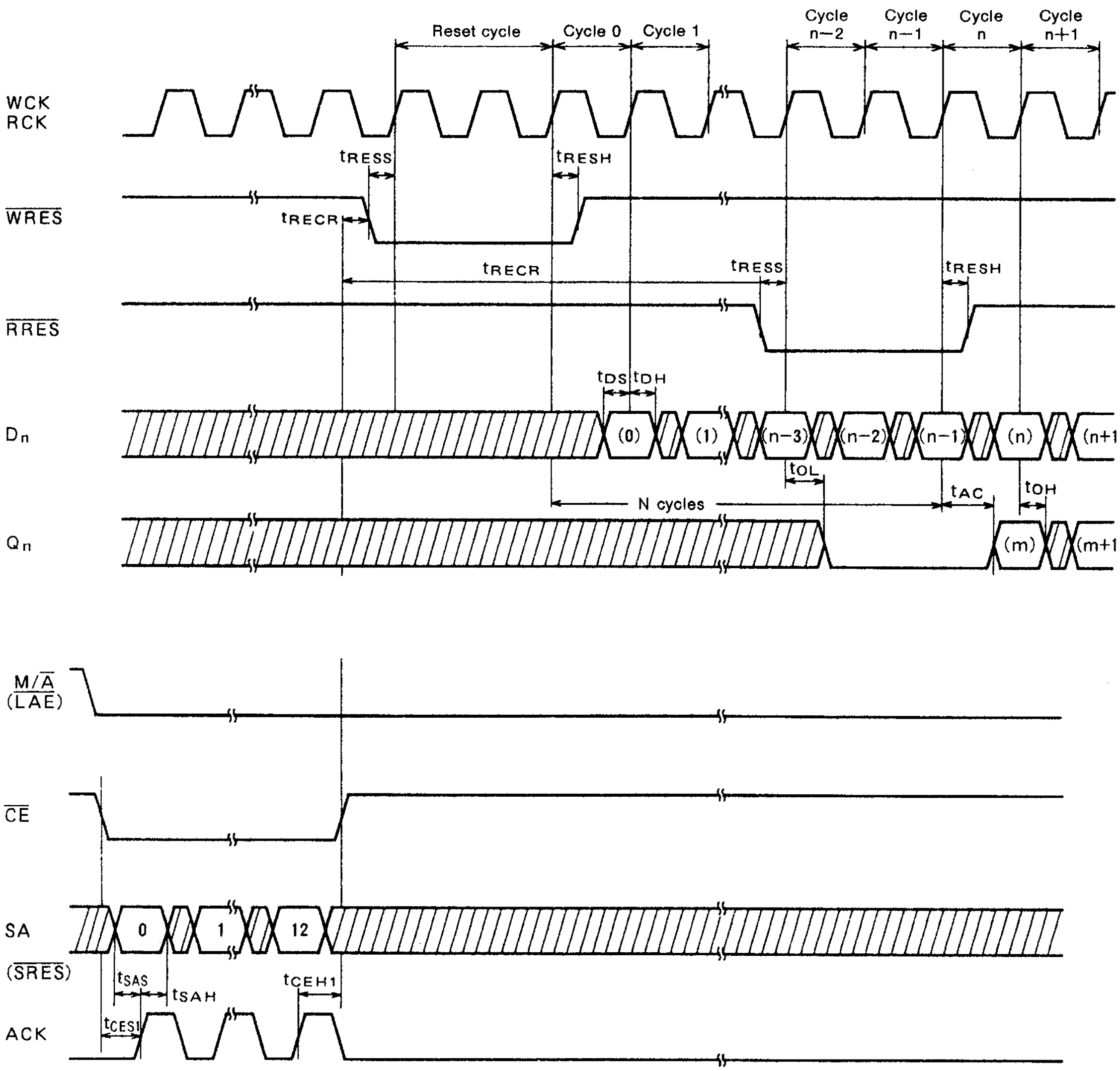


$\overline{WE}$="L", $\overline{LAE}$="H", $\overline{SRES}$="H"
N≧3

(2) FIFO mode/with setting of start address

- **N−m bit delay 1**

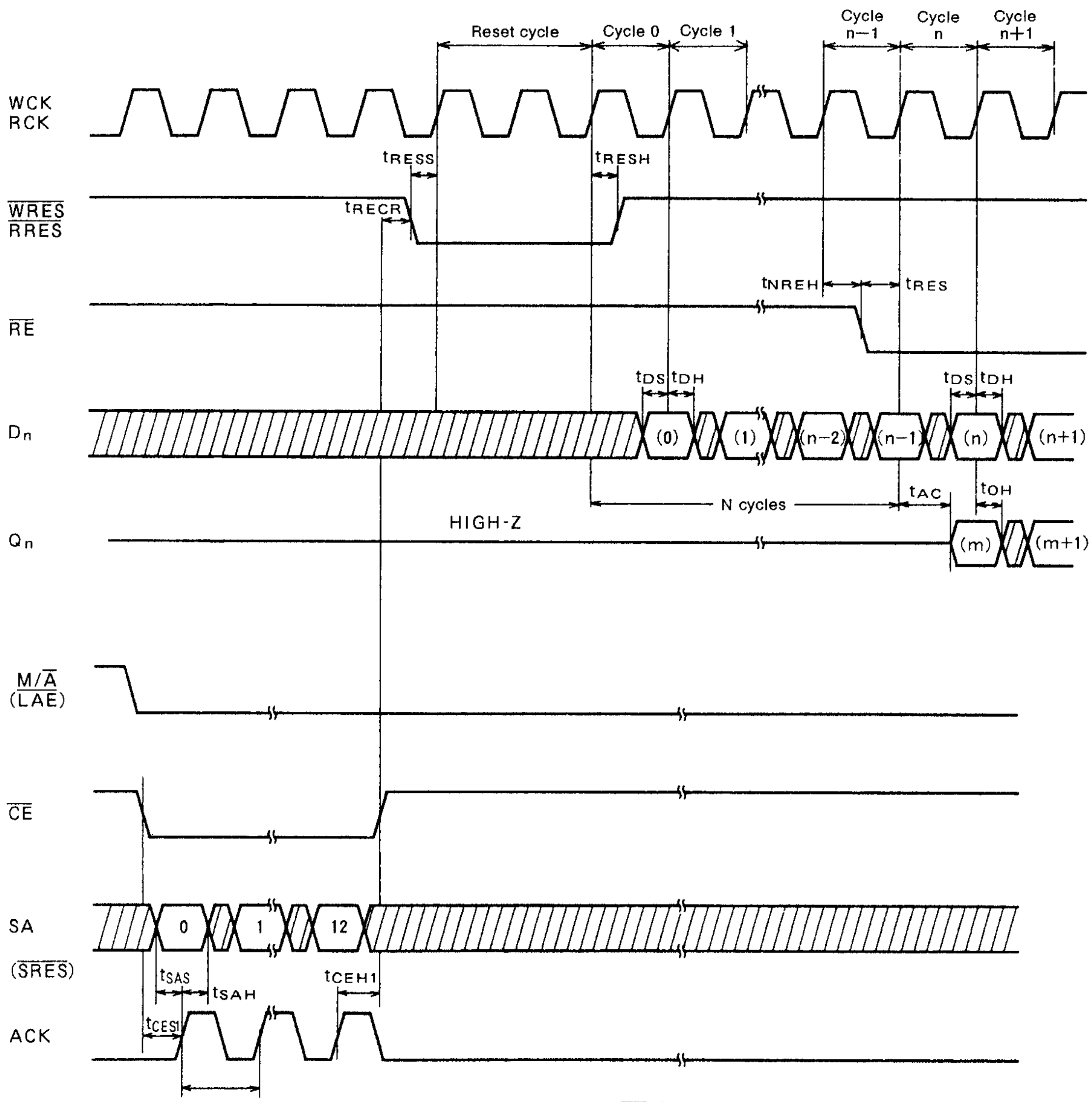
(Sliding input timing of $\overline{WRES}$ and $\overline{RRES}$ at a cycle corresponding to delay length)
(A reset cycle requires at least 2 cycles. Qn goes to the "L" level during the first 2 cycles. However, it is necessary to set at least one cycle of $\overline{RRES}$= "H" and $\overline{WRES}$="H" before the first reset cycle after power is turned on).



$\overline{WE}$, $\overline{RE}$="L"
N≧3
m is an address specified as a start address. m<n

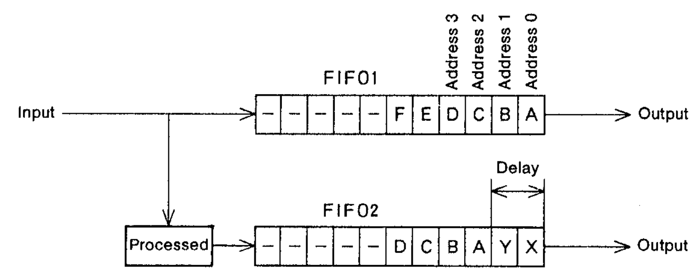
- **N-m bit delay 2**

(Disabling $\overline{RE}$ during the period corresponding to delay length to slide an address)
(A reset cycle requires at least 2 cycles. Qn goes to the L" level during the first 2 cycles. However, it is necessary to set at least one cycle of $\overline{RRES}$= "H" and $\overline{WRES}$="H" before the first reset cycle after power is turned on).



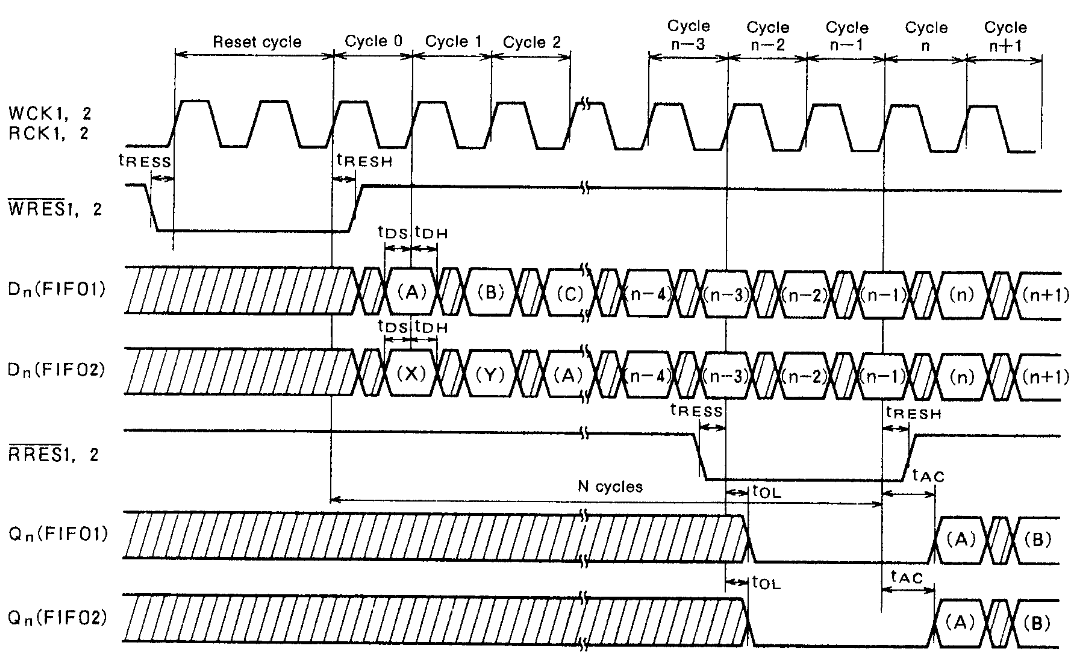
$\overline{WE}$, $\overline{RE}$="L"
N≧3
m is an address specified as a start address. m<n

(3) **Inter-FIFO delay compensation by setting a start address**



FIFO1 Without setting of start address
FIFO2 With setting of start address Address 2

(A reset cycle requires at least 2 cycles. Qn goes to the "L" level during the first 2 cycles. However, it is necessary to set at least one cycle of $\overline{RRES}$="H" and $\overline{WRES}$="H" before the first reset cycle after power is turned on).

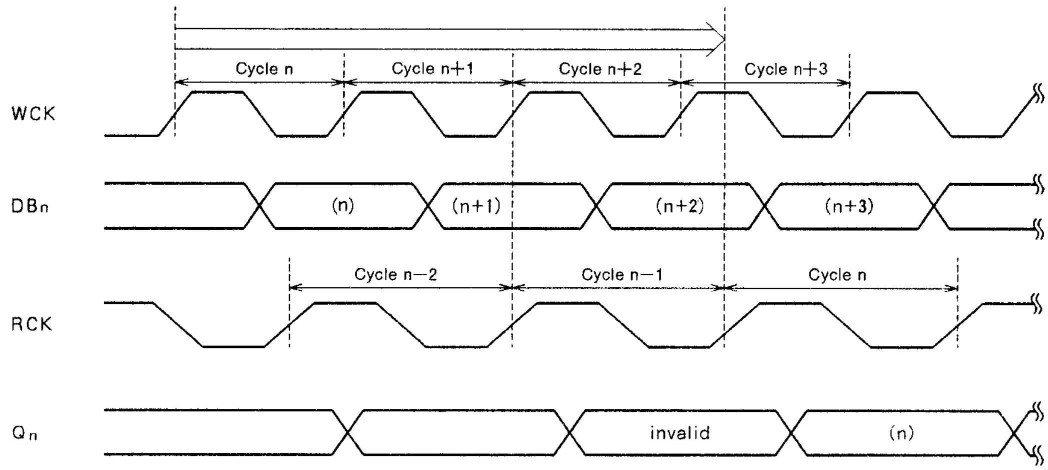


$\overline{WE}$1, 2=$\overline{RE}$1, 2="L"
$\overline{LAE}$1, 2="L"
$\overline{SRES}$1, 2="H"
N≧3

- **Shortest read of data n" written in cycle n**

Cycle n−1 on read side should be started after end of cycle n+1 on write side

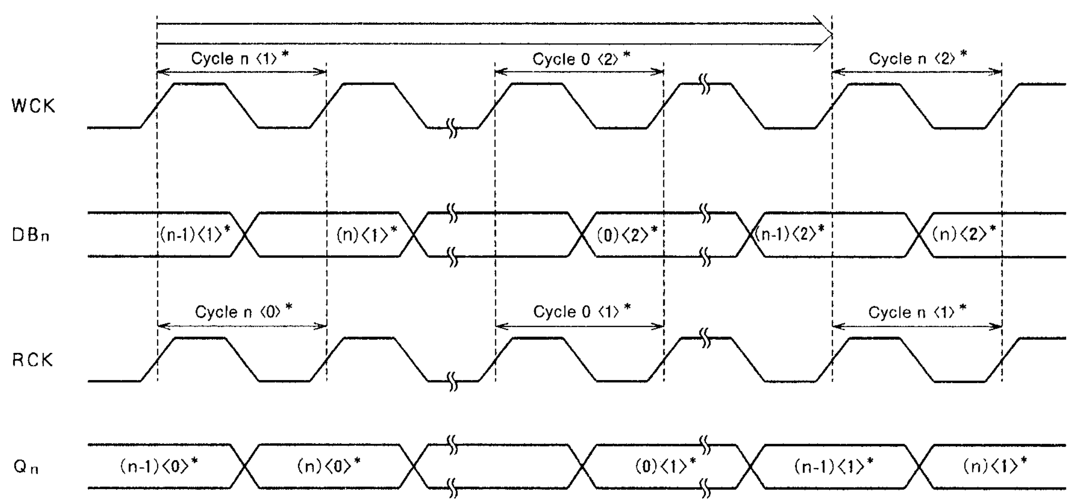
When the start of cycle n−1 on read side is earlier than the end of cycle n+1 on write side, output Qn of cycle n becomes invalid. In the figure shown below, the read of cycle n−1 is invalid.



- **Longest read of data "n" written in cycle n: 1-line delay**

Cycle n 〈1〉* on read side should be started when cycle n 〈2〉* on write is started

Output Qn of n cycle 〈1〉* can be read until the start of reading side n cycle 〈1〉* and the start of writing side n cycle 〈2〉* overlap each other.



〈0〉*, 〈1〉* and 〈2〉*
indicates a line value.