LPC47M182

Advanced I/O Controller with Motherboard GLUE Logic

Datasheet

Product Features

- 3.3V Operation (5V tolerant)
- LPC Interface
  - Multiplexed Command, Address and Data Bus
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
- ACPI 1.0b/2.0 Compliant
- Programmable Wake-up Event Interface
- PC99a/PC2001 Compliant
- General Purpose Input/Output Pins (13)
- Fan Tachometer Inputs (2)
- Green and Yellow Power LEDs
- ISA Plug-and-Play Compatible Register Set
- Motherboard GLUE Logic
  - 5V Reference Generation
  - 5V Standby Reference Generation
  - IDE Reset/Buffered PCI Reset Outputs
  - Power OK Signal Generation
  - Power Sequencing
  - Power Supply Turn On Circuitry
  - Resume Reset Signal Generation
  - Hard Drive Front Panel LED
  - Voltage Translation for DDC to VGA Monitor
  - SMBus Isolation Circuitry
  - CNR Dynamic Down Control
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - Supports One Floppy Drive
  - Configurable Open Drain/Push-Pull Output Drivers
  - Supports Vertical Recording Format
- 16-Byte Data FIFO
  - 100% IBM Compatibility
  - Detects All Overrun and Underrun Conditions
- Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
- 480 Address, Up to Eight IRQ and Three DMA Options
- Enhanced Digital Data Separator
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Keyboard Controller
  - 8042 Software Compatible
  - 8 Bit Microcomputer
  - 2k Bytes of Program ROM
  - 256 Bytes of Data RAM
  - Four Open Drain Outputs Dedicated for Keyboard/Mouse Interface
  - Asynchronous Access to Two Data Registers and One Status Register
  - Supports Interrupt and Polling Access
  - 8 Bit Counter Timer
  - Port 92 Support
  - Fast Gate A20 and KRESET Outputs
- Serial Ports
  - Two Full Function Serial Ports
  - High Speed 16C550A Compatible UART with Send/Receive 16-Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - 480 Address and 15 IRQ Options
- Infrared Port
  - Multiprotocol Infrared Interface
  - 32-Byte Data FIFO
  - IrDA 1.0 Compliant
  - SHARP ASK IR
  - HP-SIR
  - 480 Address, Up to 15 IRQ and Three DMA Options
- Multi-Mode Parallel Port with ChiProtect
  - Standard Mode IBM PC/XT, PC/AT, and PS/2 Compatible Bi-directional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection
  - 960 Address, Up to 15 IRQ and Three DMA Options
- Interrupt Generating Registers
  - Registers Generate IRQ1 – IRQ15 on Serial IRQ Interface.
- XOR-Chain Board Test
- 128 Pin QFP Packages, 3.2 mm Footprint; green, lead-free also available

DATASHEET

ORDERING INFORMATION

Order Number(s):

LPC47M182-NR for 128 pin QFP package

LPC47M182-NW for 128 pin QFP package (green, lead-free)

80 Arkay Drive
Hauppauge, NY 11788
(631) 435-6000
FAX (631) 273-3123

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Chapter 1 General Description

The LPC47M182* is a 3.3V (5V tolerant) PC99a/PC2001 compliant Advanced I/O controller for Desktop PCs. The device, which implements the Low Pin Count (LPC) interface, includes I/O functionality as well as Motherboard GLUE logic into a 128-pin package. This is space saving solution on the motherboard resulting in lower cost. The LPC47M182 also provides 13 general purpose pins, which offer flexibility to the system designer, and two Fan Tachometer Inputs. The LPC47M182's LPC interface supports LPC I/O and DMA cycles.

The LPC47M182 includes complete legacy I/O: a keyboard interface; SMSC's true CMOS 765B floppy disk controller with advanced digital data separator; two 16C550A compatible UARTs; one Multi-Mode parallel port including ChiProtect circuitry plus EPP and ECP. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures, in addition, it provides data overflow and underflow protection. The SMSC's patented advanced digital data separator allows for ease of testing and use. The parallel port is compatible with IBM PC/AT architecture, as well as IEEE 1284 EPP and ECP. The LPC47M182 incorporates sophisticated power control circuitry (PCC) which includes support for keyboard and mouse wake up events as well as PME support. The PCC supports multiple low power-down modes. The LPC47M182 is ACPI 1.0b/2.0 compatible.

The Motherboard GLUE logic includes various power management logic; including generation of nRSMRST, Power OK signal generation, 5V main and standby reference generation. There are also three LEDs to indicate power status and hard drive activity. The translation circuit converts 3.3V signals to 5V signals. Also included is SMBus main power well to resume power well isolation circuitry.

The LPC47M182 supports the ISA Plug-and-Play Standard register set (Version 1.0a). The I/O Address, DMA Channel and hardware IRQ of each logical device in the LPC47M182 may be reprogrammed through the internal configuration registers. There are up to 480 (960 for Parallel Port) I/O address location options, a Serialized IRQ interface, and three DMA channels. On chip, Interrupt Generating Registers enable external software to generate IRQ1 through IRQ15 on the Serial IRQ Interface.

The LPC47M182's Enhanced Digital Data Separator does not require any external filter components and is therefore easy to use and offers lower system costs and reduced board area. The LPC47M182 is register compatible with SMSC's proprietary 82077AA core.

*The "2" at the end of the part number is a designator for particular BIOS used inside the specific chip.

Chapter 2 Pin Layout

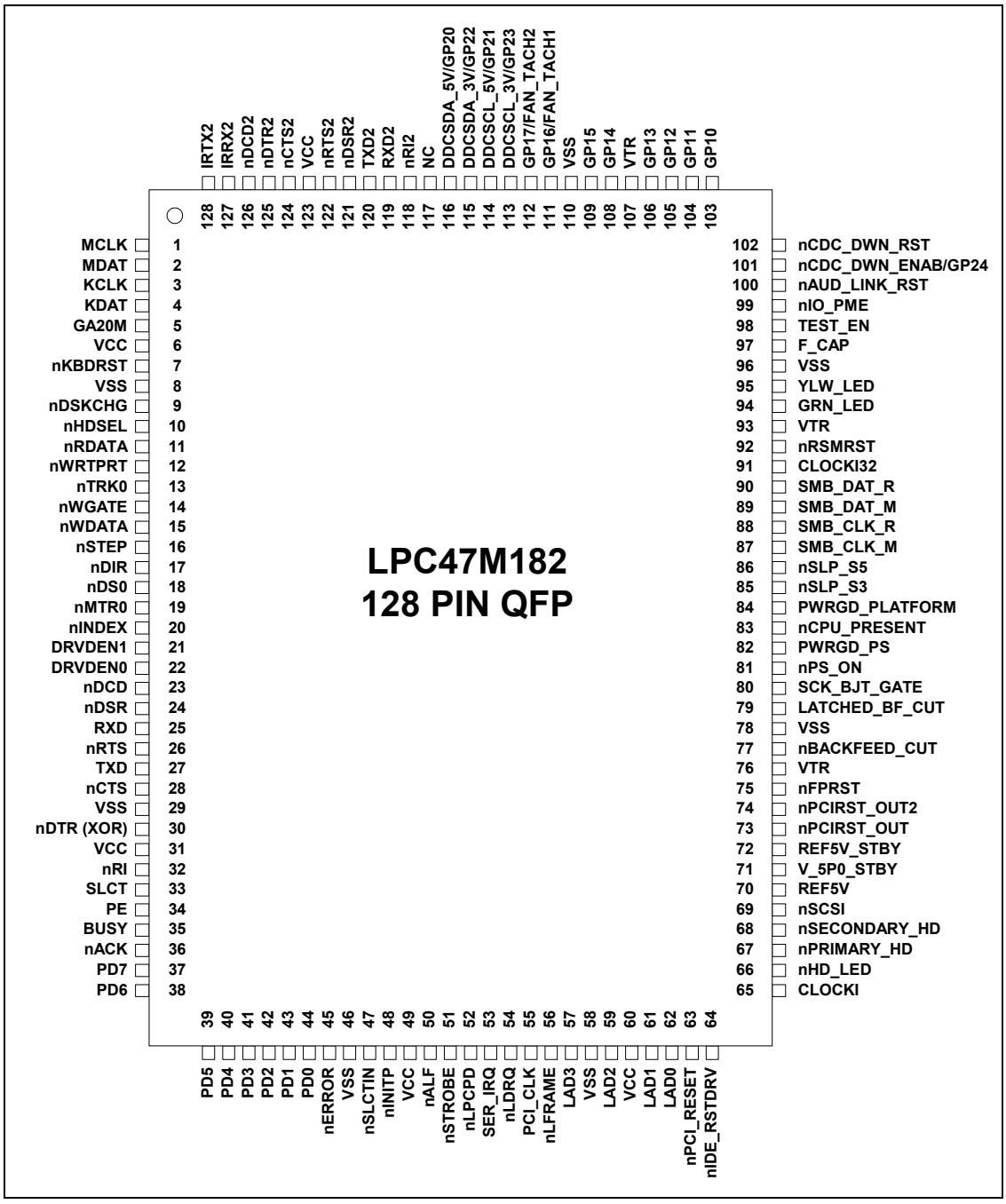


Figure 2.1 - LPC47M182 Pin Layout

Note: Pin 117 is used to select the mode of the logical device numbering. This pin affects the LD_NUM bit in the TEST 7 register (configuration register 0x29), which is used to select logical device numbering in the LPC47M182. The pin functions as follows:

- The pin has an internal pull-down resistor that selects the non-SMSC mode. To select this mode, the pin should be left unconnected. This configuration clears the LD_NUM bit to '0' and the associated functionality corresponds to the existing functionality in the part when the LD_NUM bit=0.
- Connecting this pin to VTR will select the SMSC mode of the logical device numbering. This configuration sets the LD_NUM bit to '1' and the associated functionality corresponds to the existing functionality in the part when the LD_NUM bit=1.

Chapter 3 Description of Pin Functions

Table 3.1 - LPC47M182 Pin Description

PIN#	NAME (NOTE 1)	DESCRIPTION	BUFFER NAME (NOTE 2)	PWR WELL (NOTE 3)	NOTES
POWER AND GROUND PINS (20)					
6,31, 49,60, 123	VCC	+3.3 Volt Main Supply Voltage (5)	PWR		
76,93, 107	VTR	+3.3 Volt Standby Supply Voltage (4)	PWR		
71	V_5P0_STBY	+5 Volt Standby Supply Voltage.	PWR		
8,29, 46,58, 78,96, 110	VSS	Ground (7)	PWR		
70	REF5V	5V Reference Output. Requires external pull-up to VCC5V.	AO	VCC	
72	REF5V_STBY	Highest System Standby Voltage. Requires external pull-up to V_5P0_STBY.	AO	VTR	
97	F_CAP	Internal Regulator Filter Capacitor. This pin is a no connect. A filter capacitor can be placed on this pin if it is required by system board layout.			
CLOCKS (2)					
65	CLOCKI	14.318Mhz Clock Input	IS	VCC	
91	CLOCKI32	32.768kHz Clock Input	IS	VTR	4
PROCESSOR/HOST LPC INTERFACE (11)					
52	nLPCPD	Active low input Power Down signal indicates that the LPC47M182 should prepare for power to be shut-off on the LPC interface.	PCI_I	VCC	5
53	SER_IRQ	Serial IRQ pin used with the PCI_CLK pin to transfer LPC47M182 interrupts to the host.	PCI_IO	VCC	
54	nLDRQ	Active low output used for encoded DMA/Bus Master request for the LPC interface.	PCI_O	VCC	
55	PCI_CLK	33.33 MHz PCI Clock input.	PCI_ICLK	VCC	
56	nLFRAME	Active low input indicates start of new cycle and termination of broken cycle.	PCI_I	VCC	
57,59, 61,62	LAD[3:0]	Active high LPC I/O used for multiplexed command, address and data bus.	PCI_IO	VCC	
63	nPCI_RESET	Active low input used as LPC Interface Reset. 3.3V and 5V buffered copy of PCI Reset signal is available on nPCIRST_OUT and nIDE_RSTDRV. These pins are listed under GLUE PINS.	PCI_I	VCC	

PIN#	NAME (NOTE 1)	DESCRIPTION	BUFFER NAME (NOTE 2)	PWR WELL (NOTE 3)	NOTES
99	nIO_PME	Power Management Event Output. This active low Power Management Event signal allows to request wakeup. This pin can be configured as Push-Pull Output.	OD8	VTR	
FDD INTERFACE (14)					
9	nDSKCHG	This input senses that the drive door is open or that the diskette has possibly been changed since the last drive selection. This input is inverted and read via bit 7 of I/O address 3F7H. The nDSKCHG bit also depends upon the state of the Force Disk Change bits in the Force Disk Change register (see section Chapter 11 Configuration).	IS	VCC	
10	nHDSEL	Head Select Output. This high current output selects the floppy disk side for reading or writing. A logic “1” on this pin means side 0 will be accessed, while a logic “0” means side 1 will be accessed. Can be configured as an Open-Drain Output.	O12	VCC	
11	nRDATA	Raw serial bit stream from the disk drive, low active. Each falling edge represents a flux transition of the encoded data.	IS	VCC	
12	nWRTPRT	This active low Schmitt Trigger input senses from the disk drive that a disk is write protected. Any write command is ignored. The nWRPRT bit also depends upon the state of the Force Write Protect bit in the FDD Option register (see the Configuration Registers section).	IS	VCC	
13	nTRK0	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.	IS	VCC	
14	nWGATE	Write Gate Output. This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette. Can be configured as an Open-Drain Output.	O12	VCC	
15	nWDATA	Write Disk Data Output. This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media. Can be configured as an Open-Drain Output.	O12	VCC	
16	nSTEP	Step Pulse Output. This active low high current driver issues a low pulse for each track-to-track movement of the head. Can be configured as an Open-Drain Output.	O12	VCC	

PIN#	NAME (NOTE 1)	DESCRIPTION	BUFFER NAME (NOTE 2)	PWR WELL (NOTE 3)	NOTES
17	nDIR	Step Direction Output. This high current low active output determines the direction of the head movement. A logic “1” on this pin means outward motion, while a logic “0” means inward motion. Can be configured as an Open-Drain Output.	O12	VCC	
18	nDS0	Drive Select 0 Output. Can be configured as an Open-Drain Output.	O12	VCC	
19	nMTR0	Motor On 0 Output. Can be configured as an Open-Drain Output.	O12	VCC	
20	nINDEX	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.	IS	VCC	
21	DRVDEN1	Drive Density Select 1 Output. Indicates the drive and media selected. Can be configured as Open-Drain Output.	O12	VCC	
22	DRVDEN0	Drive Density Select 0 Output. Indicates the drive and media selected. Can be configured as Open-Drain Output.	O12	VCC	
SERIAL PORT 1 INTERFACE (8)					
23	nDCD1	Active low Data Carrier Detect input for the serial port. Handshake signal that notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of nDCD signal by reading bit 7 of Modem Status Register (MSR). A nDCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDCD changes state. Note: Bit 7 of MSR is the complement of nDCD.	I	VCC	
24	nDSR1	Active low Data Set Ready input for the serial port. Handshake signal that notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of nDSR signal by reading bit 5 of Modem Status Register (MSR). A nDSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDSR changes state. Note: Bit 5 of MSR is the complement of nDSR.	I	VCC	
25	RXD1	Receiver serial data input.	IS	VCC	

PIN#	NAME (NOTE 1)	DESCRIPTION	BUFFER NAME (NOTE 2)	PWR WELL (NOTE 3)	NOTES
26	nRTS1	Active low Request to Send output for the Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of the Modem Control Register (MCR). The hardware reset will reset the nRTS signal to inactive mode (high). nRTS is forced inactive during loop mode operation.	O8	VCC	
27	TXD1	Transmit serial data output.	O12	VCC	
28	nCTS1	Active low Clear to Send input for the serial port. Handshake signal that notifies the UART that the modem is ready to receive data. The CPU can monitor the status of nCTS signal by reading bit 4 of Modem Status Register (MSR). A nCTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when nCTS changes state. The nCTS signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of nCTS.	I	VCC	
30	nDTR1 (XOR)	Active low Data Terminal Ready output for the serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the nDTR signal to inactive mode (high). nDTR is forced inactive during loop mode operation. XOR Chain Output.	O8	VCC	
32	nRI1	Active low Ring Indicator input for the serial port. Handshake signal that notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of nRI signal by reading bit 6 of Modem Status Register (MSR). A nRI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nRI changes state. Note: Bit 6 of MSR is the complement of nRI.	I	VTR	6
SERIAL PORT 2 INTERFACE (8)					
118	nRI2	Active low Ring Indicator input for serial port 2. See description for nRI1.	IPD	VTR	6, 10
119	RXD2	Receiver serial data input.	ISPD_400	VCC	
120	TXD2	Transmit serial data output.	O12	VCC	

PIN#	NAME (NOTE 1)	DESCRIPTION	BUFFER NAME (NOTE 2)	PWR WELL (NOTE 3)	NOTES
121	nDSR2	Active low Data Set Ready input for serial port 2. See description for nDSR1.	IPD	VCC	10
122	nRTS2	Active low Request to Send output for Serial Port 2. See description for nRTS1.	O8	VCC	
124	nCTS2	Active low Clear to Send input for serial port 2. See description for nCTS1.	IPD	VCC	10
125	nDTR2	Active low Data Terminal Ready output for serial port 2. See description for nDTR1.	O8	VCC	
126	nDCD2	Active low Data Carrier Detect input for serial port 2. See description for nDCD1.	IPD	VCC	10
INFRARED INTERFACE (2)					
127	IRRX2	Infrared receive input.	ISPD_400	VCC	10
128	IRTX2	Infrared transmit output.	O12	VCC	9
PARALLEL PORT INTERFACE (17)					
33	SLCT	This high active input from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.	I	VCC	
34	PE	Another status input from the printer, a high indicating that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.	I	VCC	
35	BUSY	This is a status input from the printer, a high indicating that the printer is not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.	I	VCC	
36	nACK	A low active input from the printer indicating that it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the nACK input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.	I	VCC	
37	PD7	Port Data 7 I/O	IOP14	VCC	
38	PD6	Port Data 6 I/O	IOP14	VCC	
39	PD5	Port Data 5 I/O	IOP14	VCC	
40	PD4	Port Data 4 I/O	IOP14	VCC	
41	PD3	Port Data 3 I/O	IOP14	VCC	
42	PD2	Port Data 2 I/O	IOP14	VCC	
43	PD1	Port Data 1 I/O	IOP14	VCC	
44	PD0	Port Data 0 I/O	IOP14	VCC	

PIN#	NAME (NOTE 1)	DESCRIPTION	BUFFER NAME (NOTE 2)	PWR WELL (NOTE 3)	NOTES
45	nERROR	A low on this input from the printer indicates that there is an error condition at the printer. Bit 3 of the Printer Status register reads the nERR input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.	I	VCC	
47	nSLCTIN	This active low output selects the printer. This is the complement of bit 3 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode. Can be Configured as an Open-Drain Output.	OP14	VCC	
48	nINITP	This output is bit 2 of the printer control register. This is used to initiate the printer when low. Refer to Parallel Port description for use of this pin in ECP and EPP mode. Can be configured as an Open-Drain Output.	OP14	VCC	
50	nALF	This output goes low to cause the printer to automatically feed one line after each line is printed. The nALF output is the complement of bit 1 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode. Can be configured as an Open-Drain Output.	OP14	VCC	
51	nSTROBE	An active low pulse on this output is used to strobe the printer data into the printer. The nSTROBE output is the complement of bit 0 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode. Can be configured as an Open-Drain Output.	OP14	VCC	
KEYBOARD/MOUSE INTERFACE (6)					
1	MCLK	Mouse Clock I/O	IOD24	VCC	
2	MDAT	Mouse Data I/O	IOD24	VCC	6
3	KCLK	Keyboard Clock I/O	IOD24	VCC	
4	KDAT	Keyboard Data I/O	IOD24	VCC	6
5	GA20M	Gate A20 Open-Drain Output	OD8	VCC	7
7	nKBDRST	Keyboard Reset Open-Drain Output	OD8	VCC	7
GLUE PINS (29)					
64	nIDE_RSTDRV	IDE Reset Output	OD8	VCC	3
66	nHD_LED	Hard Drive Front Panel LED Open-Drain Output	OD12	VCC	3
67	nPRIMARY_ HD	IDE Primary Drive Active Input	ISPU_400	VCC	
68	nSECONDARY _HD	IDE Secondary Drive Active Input	ISPU_400	VCC	
69	nSCSI	SCSI Drive Active Input	ISPU_400	VCC	

PIN#	NAME (NOTE 1)	DESCRIPTION	BUFFER NAME (NOTE 2)	PWR WELL (NOTE 3)	NOTES
73	nPCIRST_OUT	Buffered PCI Reset Output	OP14	VTR	
74	nPCIRST_OUT 2	Second Buffered PCI Reset Output	OP14	VTR	
75	nFPRST	Reset Input from Front Panel	ISPU_400	VTR	
77	nBACKFEED_ CUT	Open-Drain Output used for STR Circuitry	OD8	VTR	3
79	LATCHED_BF_ CUT	Latched Backfeed Cut Output for STR Circuitry	OP14	VTR	
80	SCK_BJT_ GATE	Open-Drain Gate Output for the SCK_BJT in Suspend-to-RAM	OD8	VTR	3
81	nPS_ON	Power Supply Turn-ON Open Drain Output	OD8	VTR	3
82	PWRGD_PS	Power Good Input from Power Supply	ISPU_400	VTR	
83	nCPU_PRESENT	CPU Present Input from Processor	ISPU_400	VTR	
84	PWRGD_PLAT FORM	Power Good Output	O8	VTR	
85	nSLP_S3	S3 Power State Input from South Bridge	IS_400	VTR	
86	nSLP_S5	Input from South Bridge for Transitioning to the S5 Power State	IS_400	VTR	
87	SMB_CLK_M	SMBus Clock Main	IO_SW	VTR	
88	SMB_CLK_R	SMBus Clock Resume	IO_SW	VTR	
89	SMB_DAT_M	SMBus Data Main	IO_SW	VTR	
90	SMB_DAT_R	SMBus Data Resume	IO_SW	VTR	
92	nRSMRST	Resume Reset Output	O8	VTR	
100	nAUD_LINK_ RST	AC97 Link Reset Input	I	VTR	
101	nCDC_DWN_ ENAB/GP24	AC97 Codec Down Enable Input. General Purpose I/O. GPIO can be configured as an open-drain output.	IO12	VTR	6
102	nCDC_DWN_ RST	AC97 Codec Down Reset Output.	O12	VTR	
113	DDCSCL_3V/ GP23	3.3V DDC Clock General Purpose I/O. GPIO can be configured as an open-drain output.	IO_SW/ISOD8	VTR	3, 6, 8
114	DDCSCL_5V/ GP21	5V DDC Clock General Purpose I/O. GPIO can be configured as an open-drain output.	IO_SW/ISOD8	VTR	3, 6, 8
115	DDCSDA_3V/ GP22	3.3V DDC Data General Purpose I/O. GPIO can be configured as an open-drain output.	IO_SW/ISOD8	VTR	3, 6, 8
116	DDCSDA_5V/ GP20	5V DDC Data General Purpose I/O. GPIO can be configured as an open-drain output.	IO_SW/ISOD8	VTR	3, 6, 8
POWER LEDS (2)					
94	GRN_LED	Green Power LED Open-Drain Output	OD24	VTR	
95	YLW_LED	Yellow Power LED Open-Drain Output	OD24	VTR	
GENERAL PURPOSE I/O (8)					
103-105	GP10-GP12	General Purpose I/O. GPIO can be configured as an open-drain output.	ISO8	VTR	6

PIN#	NAME (NOTE 1)	DESCRIPTION	BUFFER NAME (NOTE 2)	PWR WELL (NOTE 3)	NOTES
106, 108, 109	GP13-GP15	General Purpose I/O. GPIO can be configured as an open-drain output.	IO8	VTR	6
111	GP16/ FAN_TACH1	General Purpose I/O. GPIO can be configured as an open-drain output. Fan Tachometer 1 Input	IO8	VTR	6
112	GP17/ FAN_TACH2	General Purpose I/O. GPIO can be configured as an open-drain output. Fan Tachometer 2 Input	IO8	VTR	6
TEST (1)					
98	TEST_EN	Test Enable Input for XOR-Chain test – the external pull-up or internal pull-down sets the strap value. The XOR output is the nDTR1 pin.	IPD	VTR	
		NO CONNECT (1)			
117	NC	No Connect	IPD	-	11

Note 1: The “n” as the first letter of a signal name or the “#” as the suffix of a signal name indicates an “Active Low” signal. The primary and secondary functions on the pins are separated by “/”.

Note 2: The buffer names are described in the “Buffer Name Descriptions” section.

Note 3: Open-drain pins should be pulled-up externally to supply shown in the power well column. The nIDE_RSTDRV, nHD_LED, DDCSDA_5V and DDCSCL_5V open-drain pins require external pull-ups to VCC5V. The nBACKFEED_CUT, SCK_BJT_GATE and nPS_ON open-drain pins require external pull-ups to V_5P0_STBY. Inputs with internal pull-ups are pulled internally to the supply shown in the power well column. All other pins are driven under the power well shown. See the “Pins With Internal Resistors”, “Pins That Require External Resistors” and “Default State of Pins” sections.

Note 4: The 32.768 kHz input clock must not be driven high when VTR = 0V. CLOCKI32 is clock source to various logic in the part, including LED, “wake on specific key” and nFPRST debounce circuitry. The 32 KHz input clock must always be connected. There is a bit in the configuration register at 0xF0 in Logical Device A that indicates whether or not the 32KHz clock is connected. This bit determines the clock source for the logic. This bit must always be set to ‘0’ (‘0’=32 KHz clock connected; reset default=‘0’).

Note 5: The nLPCPD pin may be tied high. The LPC interface will function properly if the nPCI_RESET signal follows the protocol defined for the nLRESET signal in the “Low Pin Count Interface Specification”. However, if nLPCPD is tied high, the keyboard wakeup isolation logic will be affected.

Note 6: These pins (except DDC and FAN_TACH functions) are also inputs to VTR powered logic internal to the part. If DDC and FAN_TACH functions are selected on GPIOs, the pins will tri-state when VCC power is removed.

Note 7: External pullups must be placed on the nKBDRST and GA20M pins. If the nKBDRST and GA20M functions are to be used, the system must ensure that these pins are high. See the “That Require External Resistors” section.

Note 8: When DDC functions are selected on GP20-GP23, the pins become IO_SW type and require external pull-ups to the appropriate voltages. See the “That Require External Resistors” section. When the GPIO functions are selected, the pins are IS0D8.

Note 9: The IRTX2 pin is driven low upon power-up of VCC. This pin will remain low following a power-up (VCC POR) until it is selected via the IR MUX bits and serial port 2 is enabled by setting the activate bit, at which

time the pin will reflect the state of the transmit output of the Serial Port 2 block. This is a VCC powered pin.

Note 10: These pins are internally pulled down to VSS only until Serial Port 2 is enabled. Once Serial Port 2 is enabled, the pull-downs are removed until VTR POR.

Note 11: Pin 117 is used to select the mode of the logical device numbering. This pin affects the LD_NUM bit in the TEST 7 register (configuration register 0x29), which is used to select logical device numbering in the LPC47M182. The pin has an internal pull-down resistor that selects the non-SMSC mode. To select this mode, the pin should be left unconnected. Connecting this pin to VTR will select the SMSC mode of the logical device numbering.

3.1 Buffer Name Descriptions

Note: Refer to the “Electrical Characteristics” section.

PWR	Power and Ground
I	Input TTL Compatible.
IPU	Input with 30uA Integrated Pull-Up
IPD	Input with 30uA Integrated Pull-Down
IS	Input with 250mV Schmitt Trigger.
IS_400	Input with 400mV Schmitt Trigger.
ISPU_400	Input with 400mV Schmitt Trigger and 30uA Integrated Pull-Up.
ISPD_400	Input with 400mV Schmitt Trigger and 30uA Integrated Pull-Down.
O8	Output, 8mA sink, 4mA source.
OD8	Output (Open Drain), 8mA sink.
O12	Output, 12mA sink, 6mA source.
OD12	Output (Open Drain), 12mA sink.
OP14	Output, 14mA sink, 14mA source.
OD24	Output (Open Drain), 24mA sink.
AO	Output – Analog with 5V Level
IO8	Input/Output, 8mA sink, 4mA source.
ISO8	Input with 250mV Schmitt Trigger /Output, 8mA sink, 4mA source.
ISOD8	Input with 250mV Schmitt Trigger, Low Leakage/Output (Open-Drain), 8mA sink.
IO12	Input with Schmitt Trigger/Output, 12mA sink, 6mA source.
IOP14	Input/Output, 14mA sink, 14mA source.
IOD24	Input/Output (Open Drain), 24mA sink.
IO_SW	Input/Output, special type. Pins of this type are connected in pairs through a switch. The switch provides a 25 ohm (max) resistance to ground when closed.
PCI_IO	Input/Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_O	Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_I	Input. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_ICLK	Clock Input. These pins meet the PCI 3.3V AC and DC Characteristics and timing. (Note 2)

Note 1: See the “PCI Local Bus Specification,” Revision 2.1, Section 4.2.2.
Note 2: See the “PCI Local Bus Specification,” Revision 2.1, Section 4.2.2 and 4.2.3.

3.2 Pins With Internal Resistors

The following pins have internal resistors:

Table 3.2 – Pins with Internal Resistors

SIGNAL NAME	RESISTOR VALUE	NOTES
nCPU_PRESENT	30uA	Pull-up to VTR
nFPRST	30uA	Pull-up to VTR
nPRIMARY_HD	30uA	Pull-up to VCC
PWRGD_PS	30uA	Pull-up to VTR
nSCSI	30uA	Pull-up to VCC
nSECONDARY_HD	30uA	Pull-up to VCC
TEST_EN	30uA	Pull-down to VSS

3.3 Pins That Require External Resistors

The following pins require external resistors:

Table 3.3 – Pins that Require External Resistors

SIGNAL NAME	RESISTOR VALUE	NOTES
SER_IRQ	10 kohm	Pull-up to VCC
nLDRQ	100 kohm	Pull-up to VCC
LAD[3:0]	100 kohm	Pull-up to VCC
MCLK	2.7 kohm	Pull-up to VREG_PS2. The VREG_PS2 is the voltage regulator for the PS/2 ports.
MDAT		
KCLK		
KDAT		
GA20M	10 kohm	Pull-up to VCC
KBDRST	10 kohm	Pull-up to VCC
nIO_PME	10 kohm	Pull-up to VTR
nHDSEL	10 kohm	Pull-up required if used as Open-Drain Output. Pull-up to VCC.
nWGATE	10 kohm	
nWDATA	10 kohm	
nSTEP	10 kohm	
nDIR	10 kohm	
nDS0	10 kohm	
nMTR0	10 kohm	
DRVDEN1	10 kohm	
DRVDEN0	10 kohm	
nDSKCHG	1 kohm	Pull-up to VCC
nRDATA	1 kohm	Pull-up to VCC
nWRTPRT	1 kohm	Pull-up to VCC
nTRK0	1 kohm	Pull-up to VCC
nINDEX	10 kohm	Pull-up to VCC
REF5V	1 kohm	Pull-up to VCC5V
REF5V_STBY	1 kohm	Pull-up to V_5P0_STBY
nIDE_RSTDRV	1 kohm	Pull-up to VCC5V
nPS_ON	1 kohm	Pull-up to V_5P0_STBY
nBACKFEED_CUT	1 kohm	Pull-up to V_5P0_STBY
SCK_BJT_GATE	1 kohm	Pull-up to V_5P0_STBY
nCDC_DWN_ENAB	10 kohm	Pull-down to VSS
YLW_LED	220 ohm	Pull-up to VTR
nHD_LED	330 ohm	Pull-up to VCC
DDCSDA_3V	4.7 kohm	Pull-up to VCC
DDCSCL_3V	4.7 kohm	Pull-up to VCC
DDCSDA_5V	2.2 kohm	Pull-up to VCC5V
DDCSCL_5V	2.2 kohm	Pull-up to VCC5V
SMB_CLK_M	2.7 kohm	Pull-up to VCC
SMB_CLK_R	2.7 kohm	Pull-up to VTR

SIGNAL NAME	RESISTOR VALUE	NOTES
SMB_DAT_M	2.7 kohm	Pull-up to VCC
SMB_DAT_R	2.7 kohm	Pull-up to VTR
GRN_LED	220 ohm	Pull-up to VTR
GPIOs	design-dependant	Pull-up to appropriate voltage (not to exceed 5V)

3.4 Default State of Pins

The following table shows the default state of pins.

Notes:

Off
The pin is not powered by suspend supply and is valid under main power only.

Hi-Z
The pin is powered, but tri-stated either because the pin is open-drain or VCC function is selected on VTR powered pin. The pin requires external pull-up when tri-stated.

Active
The pin is powered and active high.

Running
The input clock is powered and running.

Input
The pin is powered and driven by external circuitry to high or low level.

Out
The pin is powered and driven to high or low level by the part.

The input or output configuration state of the pin is retained and is not affected by PCI Reset or VCC POR.

Table 3.4 – Default State of Pins

SIGNAL NAME	PWR WELL	PCI RESET	VCC POR	VTR POR	NOTES
REF5V_STBY	VTR	-	-	Active	This pin requires external pull-up to V_5P0_STBY
REF5V	VCC	Active	Active	Off	This pin requires external pull-up to VCC5V
CLOCKI	VCC	Running	Running	Off	
CLOCKI32	VTR	Running	Running	Running	
nIO_PME	VTR	-	-	Hi-Z	
PCI_CLK	VCC	Input	Input	Off	
nLPCPD	VCC	Input	Input	Off	
nPCI_RESET	VCC	Input	Input	Off	
SER_IRQ	VCC	Input	Input	Off	
nLDRQ	VCC	Input	Input	Off	
nLFRAME	VCC	Input	Input	Off	
LAD[0:3]	VCC	Input	Input	Off	
nDSKCHG	VCC	Input	Input	Off	
nHDSEL	VCC	Out – low	Out – low	Off	

SIGNAL NAME	PWR WELL	PCI RESET	VCC POR	VTR POR	NOTES
nRDATA	VCC	Input	Input	Off	
nWRTPRT	VCC	Input	Input	Off	
nTRK0	VCC	Input	Input	Off	
nWGATE	VCC	Hi-Z	Hi-Z	Off	
nWDATA	VCC	Hi-Z	Hi-Z	Off	
nSTEP	VCC	Out – low	Out – low	Off	
nDIR	VCC	Out – low	Out – low	Off	
nDS0	VCC	Hi-Z	Hi-Z	Off	
nMTR0	VCC	Hi-Z	Hi-Z	Off	
nINDEX	VCC	Input	Input	Off	
DRVDEN0	VCC	Out – high	Out – high	Off	
DRVDEN1	VCC	Out – high	Out – high	Off	
nDCD1	VCC	Input	Input	Off	
nDSR1	VCC	Input	Input	Off	
RXD1	VCC	Input	Input	Off	
nRTS1	VCC	Out – high	Out – high	Off	
TXD1	VCC	Out – low	Out – low	Off	
nCTS1	VCC	Input	Input	Off	
nDTR1 (XOR)	VCC	Out – high	Out – high	Off	
nRI1	VTR	-	-	Input	
nDCD2	VCC	Input	Input	Off	This pin is internally pulled down to VSS until Serial Port 2 is enabled.
nDSR2	VCC	Input	Input	Off	This pin is internally pulled down to VSS until Serial Port 2 is enabled.
RXD2	VCC	Input	Input	Off	This pin is internally pulled down to VSS until Serial Port 2 is enabled.
nRTS2	VCC	Out – high	Out – high	Off	
TXD2	VCC	Out – low	Out – low	Off	
nCTS2	VCC	Input	Input	Off	This pin is internally pulled down to VSS until Serial Port 2 is enabled.
nDTR2	VCC	Out – high	Out – high	Off	
nRI2	VTR	-	-	Input	This pin is internally pulled down to VSS until Serial Port 2 is enabled.
IRRX2	VCC	Input	Input	Off	This pin is internally pulled down to VSS until Serial Port 2 is enabled.
IRTX2	VCC	Out – low	Out – low	Off	
SLCT	VCC	Input	Input	Off	
PE	VCC	Input	Input	Off	
BUSY	VCC	Input	Input	Off	
nACK	VCC	Input	Input	Off	
PD[7:0]	VCC	Input	Input	Off	
ERROR	VCC	Input	Input	Off	
nSLCTIN	VCC	Out – High	Out – High	Off	

SIGNAL NAME	PWR WELL	PCI RESET	VCC POR	VTR POR	NOTES
nINITP	VCC	Out – High	Out – High	Off	
nALF	VCC	Out – High	Out – High	Off	
nSTROBE	VCC	Out – High	Out – High	Off	
MCLK	VCC	Hi-Z	Hi-Z	Off	
MDAT	VCC	-	-	Input	
KCLK	VCC	Hi-Z	Hi-Z	Off	
KDAT	VCC	-	-	Input	
GA20M	VCC	Hi-Z	Hi-Z	Off	
nKBDRST	VCC	Hi-Z	Hi-Z	Off	
nAUD_LINK_RST	VTR	-	-	Input	
nCDC_DWN_ENAB/ GP24	VTR	-	-	Input	
nCDC_DWN_RST	VTR	-	-	Out – low	
nFPRST	VTR	-	-	Input	This pin is pulled up internally
nBACKFEED_CUT	VTR	-	-	Hi-Z	This pin requires external pull-up to V_5P0_STBY.
LATCHED_BF_CUT	VTR	-	-	Out – low	
SCK_BJT_GATE	VTR	-	-	Hi-Z	This pin requires external pull-up to V_5P0_STBY.
nSCSI	VCC	Input	Input	Off	This pin is pulled up internally
GRN_LED	VTR	-	-	Out – low	
YLW_LED	VTR	-	-	Out – low	
nHD_LED	VCC	Hi-Z	Hi-Z	Off	
nSECONDARY_HD	VCC	Input	Input	Off	This pin is pulled up internally
nPRIMARY_HD	VCC	Input	Input	Off	This pin is pulled up internally
nIDE_RSTDRV	VCC	Out – low	Out – low	Off	Requires external pull-up to VCC5V
PWRGD_PS	VTR	-	-	Input	
nPS_ON	VTR	-	-	Hi-Z	Requires external pull-up to V_5P0_STBY
nCPU_PRESENT	VTR	-	-	Input	This pin is pulled up internally
nSLP_S3	VTR	-	-	Input	
nSLP_S5	VTR	-	-	Input	
nRSMRST	VTR	-	-	Out – low	
PWRGD_PLATFORM	VTR	-	-	Out – low	
nPCIRST_OUT	VTR	Out – low	Out – low	Out – low	
nPCIRST_OUT2	VTR	Out – low	Out – low	Out – low	
GP10-GP15	VTR	-	-	Input	
GP16	VTR	-	-	Input	The GPIO and FAN_TACH functions are multiplexed on the same pin with GPIO as the default function.
FAN_TACH1		Hi-Z	Hi-Z	Hi-Z	
GP17	VTR	-	-	Input	
FAN_TACH2		Hi-Z	Hi-Z	Hi-Z	
SMB_CLK_M	VTR	Hi-Z	Hi-Z	Hi-Z	
SMB_CLK_R	VTR	-	-	Hi-Z	
SMB_DAT_M	VTR	Hi-Z	Hi-Z	Hi-Z	
SMB_DAT_R	VTR	-	-	Hi-Z	
DDCSDA_5V	VTR	Hi-Z	Hi-Z	Hi-Z	The DDC and GPIO functions

SIGNAL NAME	PWR WELL	PCI RESET	VCC POR	VTR POR	NOTES
GP20		-	-	Hi-Z	are multiplexed on the same pin with DDC as the default function. DDC function requires external pull-up to VCC5V.
DDCSCL_5V	VTR	Hi-Z	Hi-Z	Hi-Z	
GP21		-	-	Hi-Z	
DDCSDA_3V	VTR	Hi-Z	Hi-Z	Hi-Z	The DDC and GPIO functions are multiplexed on the same pin with DDC as the default function. DDC function requires external pull-up to VCC.
GP22		-	-	Hi-Z	
DDCSCL_3V	VTR	Hi-Z	Hi-Z	Hi-Z	
GP23		-	-	Hi-Z	
TEST_EN	VTR	-	-	Input	Test Mode pin. This pin has internally pull-down to VSS. External pull-up required to enable the test mode.

Chapter 4 Block Diagram

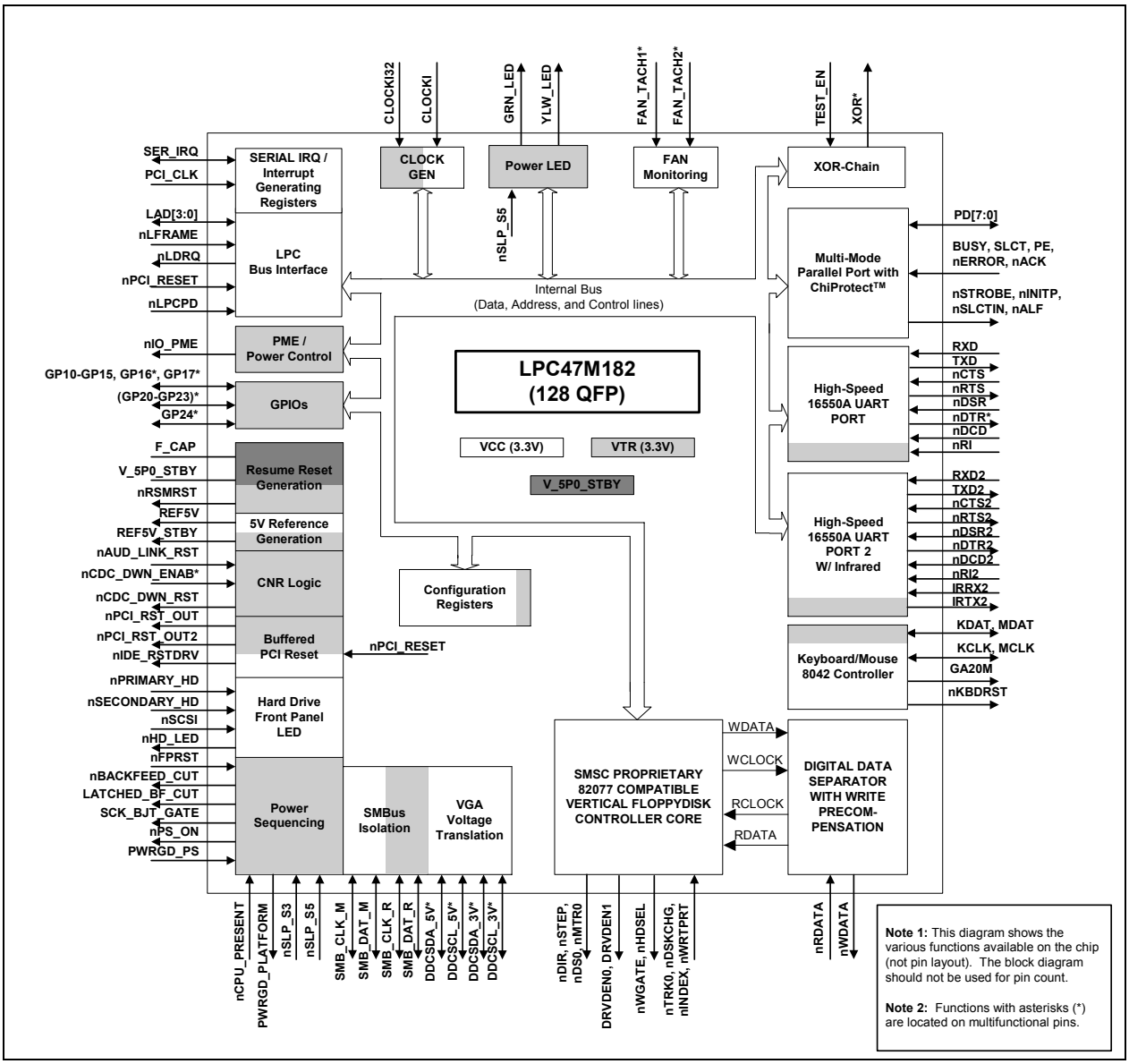


Figure 4.1 – LPC47M182 Block Diagram

Chapter 5 Power and Clock Functionality

The LPC47M182 has three power planes: VCC, VTR and V5P0_STBY.

5.1 3 Volt Operation / 5 Volt Tolerance

The LPC47M182 is a 3.3 Volt part. It is intended solely for 3.3V applications. Non-LPC bus pins are 5V tolerant; that is, the operating input voltage is 5.5V max, and the I/O buffer output pads are backdrive protected (they do not impose a load on any external VCC powered circuitry).

The LPC interface pins are 3.3 V only. These signals meet PCI DC specifications for 3.3V signaling. The nRSMRST pin is also 3.3V only.

The following lists the pins that are 3.3V only (not 5V tolerant):

- LAD[3:0]
- nLFRAME
- nLDRQ
- nLPCPD
- nRSMRST

The input voltage for all other pins is 5.5V max. These pins include all non-LPC Bus pins and the following pins:

- nPCI_RESET
- PCI_CLK
- SER_IRQ
- nIO_PME

5.2 VCC Power

The LPC47M182 is a 3.3 Volt part. The VCC supply is 3.3 Volts (nominal). See section 12.2 Operational DC Characteristics and section 12.1 Maximum Guaranteed Ratings.

5.3 VTR Power

The LPC47M182 requires a trickle supply (VTR) to provide sleep current for the programmable wake-up events in the PME interface and other suspend state logic when VCC is removed. The VTR supply is 3.3 Volts (nominal). See the Operational Description Section. The maximum VTR current that is required depends on the functions that are used in the part. See Trickle Power Functionality subsection and Maximum Current Values subsection. If the LPC47M182 is not intended to provide wake-up and/or suspend power capabilities on standby current, VTR can be connected to VCC. The VTR pin generates a VTR Power-on-Reset signal to initialize these components.

Note: If VTR is to be used for programmable wake-up events when VCC is removed, VTR must be at its full minimum potential at least 10 μs before VCC begins a power-on cycle. When VTR and VCC are fully powered, the potential difference between the two supplies must not exceed 500mV.

5.3.1 Trickle Power Functionality

When the LPC47M182 is running under VTR only (VCC removed), PME wakeup events are active and (if enabled) able to assert the nIO_PME pin active low. The following lists the wakeup events:

- UART1 and UART 2 Ring Indicator
- Keyboard data
- Mouse data
- "Wake on Specific Key" Logic
- GPIOs for wakeup. See below.

The following requirements apply to all I/O pins that are specified to be 5 volt tolerant.

I/O buffers that are wake-up event compatible are powered by VCC. Under VTR power (VCC=0), these pins may only be configured as inputs. These pins have input buffers into the wakeup logic that are powered by VTR.

I/O buffers that may be configured as either push-pull or open drain under VTR power (VCC=0), are powered by VTR. This means, at a minimum, they will source their specified current from VTR even when VCC is present.

The GPIOs that are used for PME wakeup as input are GP10-GP17 and GP20-GP23

Buffers are powered by VTR. These pins have input buffers into the wakeup logic that are powered by VTR. GP24 does not have input buffer into the wakeup logic.

The output buffer of GP24 is by VTR but does this pin does not have an input buffer into wakeup logic powered by VTR.

For blocks, registers and pins that are powered by VTR see Table 3.1 and Figure 4.1.

5.4 V5P0_STBY Power

The V5P0_STBY pin is used in nRSMRST generation circuit. The V5P0_STBY, however, does not power the nRSMRST pad.

5.5 32.768 kHz Trickle Clock Input

The LPC47M182 utilizes a 32.768 kHz trickle input to supply a clock signal for the nFPRST debounce circuitry, LED blink and wake on specific key function.

5.5.1 Indication of 32KHZ Clock

There is a bit to indicate whether or not the 32kHz clock input is connected to the LPC47M182. This bit is located at bit 0 of the CLOCKI32 configuration register at 0xF0 in the Power Control Logical Device (when LD_NUM=0) or Runtime Register Block Logical Device (when LD_NUM=1). This register is powered by VTR and reset on a VTR POR.

Bit[0] (CLK32_PRSN) is defined as follows:

0=32kHz clock is connected to the CLKI32 pin (default)

1=32kHz clock is not connected to the CLKI32 pin (pin is grounded).

Bit 0 controls the source of the 32kHz (nominal) clock for the nFPRST debounce circuitry, the LED blink logic and the “wake on specific key” logic. When the external 32kHz clock is connected, that will be the source for the nFPRST debounce circuitry, LED and “wake on specific key” logic. When the external 32kHz clock is not connected, an internal 32kHz clock source will be derived from the 14MHz clock for the “wake on specific key” logic. The nFPRST debounce cirucitry and LED require the 32kHz clock be always connected.

The “wake on specific key” function will not work under VTR power (VCC removed) if the external 32kHz clock is not connected. It will work under VCC power even if the external 32 kHz clock is not connected.

5.6 14.318 MHz Clock Input

The LPC47M182 utilizes a 14.318 MHz clock input (CLOCKI). This clock is used to generate specific clocks needed for various logic (including SIO functions, Fan Tachometer, etc.) in the LPC47M182. The CLOCKI is powered by VCC and is not available in VTR power only (VCC=0).

5.7 Internal PWRGOOD

An internal PWRGOOD logical control is included to minimize the effects of pin-state uncertainty in the host interface as VCC cycles on and off. When the internal PWRGOOD signal is “1” (active), VCC > 2.3V (nominal), and the LPC47M182 host interface is active. When the internal PWRGOOD signal is “0” (inactive), VCC <= 2.3V (nominal), and the LPC47M182 host interface is inactive; that is, LPC bus reads and writes will not be decoded.

The LPC47M182 device pins nIO_PME, CLOCKI32, KDAT, MDAT, nRI1, nRI2, and most GPIOs (as input) are part of the PME interface and remain active when the internal PWRGOOD signal has gone inactive, provided VTR is powered. Other VTR powered pins listed in Table 3.1 also remain active when the internal PWRGOOD signal has gone inactive, provided VTR is powered. See Trickle Power Functionality section.

5.8 Maximum Current Values

See the “Operational Description” section for the maximum current values.

The maximum VTR current, I_{TR}, is given with all outputs open (not loaded), and all inputs transitioning from/to 0V to/from 3.3V. The total maximum current for the part is the unloaded value PLUS the maximum current sourced by the pin that is driven by VTR. The pins that are powered by VTR are listed in the Table 3.1. The push-pull capable outputs will source minimum current specified in Table 12.2 at 2.4V when driving.

The maximum VCC current, I_{CC}, is given with all outputs open (not loaded) and all inputs transitioning from/to 0V to/from 3.3V.

5.9 Power Management Events (PME/SCI)

The LPC47M182 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events. The terms PME and SCI are used synonymously throughout this document to refer to the indication of an event to the chipset via the assertion of the nIO_PME output signal. See the “PME Support” section.

Chapter 6 Functional Description

The following sections describe the functional blocks located in the LPC47M182 (see Figure 4.1). The various Super I/O components are described in the following sections and their registers are implemented as typical Plug-and-Play components (see section Chapter 11 – Configuration on page 167).

6.1 Super I/O Registers

Table 6.1 shows the logical device number and addresses of FDC, Serial and Parallel ports, Keyboard/Mouse, Power Control and GPIO Block, and configuration register block of the Super I/O immediately after power up. The logical device numbering is controlled by the LD_NUM bit in the TEST 7 configuration register (0x29. The base addresses of the blocks can be programmed via the configuration registers. Refer to the "Configuration" section for configuration register description.

Table 6.1 – Super I/O Block Logical Device Number and Addresses

LD_NUM bit = 0 (default)			LD_NUM bit = 1		
LD NUMBER	**DEVICE NAME**	**BLOCK ADDRESS**	**LD NUMBER**	**DEVICE NAME**	**BLOCK ADDRESS**
00h	Floppy Disk Controller	Base+(0-5) and +(7)	00h	Floppy Disk Controller	Base+(0-5) and +(7)
01h	Parallel Port	Base+(0-3) Base+(0-7) Base+(0-3), +(400-402) Base+(0-7), +(400-402)	01h	-	-
02h	Serial Port 2	Base+(0-7)	02h	Serial Port 2	Base+(0-7)
03h	Serial Port 1	Base+(0-7)	03h	Parallel Port	Base+(0-3) Base+(0-7) Base+(0-3), +(400-402) Base+(0-7), +(400-402)
04h	Power Control	Base+(0-31)	04h	Serial Port 1	Base+(0-7)
05h	Mouse		05h	-	-
06h	Keyboard	60, 64	06h	-	-
07h	GPIO	Base+(0-31)	07h	Keyboard/Mouse	60, 64
08h	-	-	08h	-	-
09h	-	-	09h	-	-
0Ah	-	-	0Ah	Runtime Register Block – contains Power Control and GPIO Block registers in this mode.	Base+(0-63)
-	Configuration	Base + (0-1)	-	Configuration	Base + (0-1)

6.2 Host Processor Interface (LPC)

The host processor communicates with the LPC47M182 through a series of read/write registers via the LPC interface. The port addresses for these registers are shown in Table 6.1. Register access is accomplished through I/O cycles or DMA transfers. All registers are 8 bits wide.

6.3 LPC Interface

The following sub-sections specify the implementation of the LPC bus.

6.3.1 LPC Interface Signal Definition

The signals required for the LPC bus interface are described in the table below. LPC bus signals use PCI 33MHz electrical signal characteristics.

SIGNAL NAME	TYPE	DESCRIPTION
LAD[3:0]	I/O	LPC address/data bus. Multiplexed command, address and data bus.
nLFRAME	Input	Frame signal. Indicates start of new cycle and termination of broken cycle
nPCI_RESET	Input	PCI Reset. Used as LPC Interface Reset.
nLDRQ	Output	Encoded DMA/Bus Master request for the LPC interface.
nIO_PME	OD	Power Mgt Event signal. Allows the LPC47M182 to request wakeup.
nLPCPD	Input	Powerdown Signal. Indicates that the LPC47M182 should prepare for power to be shut on the LPC interface.
SER_IRQ	I/O	Serial IRQ.
PCI_CLK	Input	PCI Clock.

Note: The CLKRUN# signal is not implemented in this part.

6.3.2 LPC Cycles

The following cycle types are supported by the LPC protocol.

CYCLE TYPE	TRANSFER SIZE
I/O Write	1 Byte
I/O Read	1 Byte
DMA Write	1 Byte
DMA Read	1 Byte

LPC47M182 ignores cycles that it does not support.

6.3.3 Field Definitions

The data transfers are based on specific fields that are used in various combinations, depending on the cycle type. These fields are driven onto the LAD[3:0] signal lines to communicate address, control and data information over the LPC bus between the host and the LPC47M182. See the *Low Pin Count (LPC) Interface Specification* Revision 1.0 from Intel, Section 4.2 for definition of these fields.

6.3.4 NLFRAME Usage

nLFRAME is used by the host to indicate the start of cycles and the termination of cycles due to an abort or time-out condition. This signal is to be used by the LPC47M182 to know when to monitor the bus for a cycle.

This signal is used as a general notification that the LAD[3:0] lines contain information relative to the start or stop of a cycle, and that the LPC47M182 monitors the bus to determine whether the cycle is intended for it. The use of nLFRAME allows the LPC47M182 to enter a lower power state internally. There is no need for the LPC47M182 to monitor the bus when it is inactive, so it can decouple its state machines from the bus, and internally gate its clocks.

When the LPC47M182 samples nLFRAME active, it immediately stops driving the LAD[3:0] signal lines on the next clock and monitor the bus for new cycle information.

The nLFRAME signal functions as described in the Low Pin Count (LPC) Interface Specification, Revision 1.0.

6.3.5 I/O Read and Write Cycles

The LPC47M182 is the target for I/O cycles. I/O cycles are initiated by the host for register or FIFO accesses, and will generally have minimal Sync times. The minimum number of wait-states between bytes is 1. EPP cycles will depend on the speed of the external device, and may have much longer Sync times.

Data transfers are assumed to be exactly 1-byte. If the CPU requested a 16 or 32-bit transfer, the host will break it up into 8-bit transfers.

See the “Low Pin Count (LPC) Interface Specification” Reference, Section 5.2, for the sequence of cycles for the I/O Read and Write cycles.

6.3.6 DMA Read and Write Cycles

DMA read cycles involve the transfer of data from the host (main memory) to the LPC47M182. DMA write cycles involve the transfer of data from the LPC47M182 to the host (main memory). Data will be coming from or going to a FIFO and will have minimal Sync times. Data transfers to/from the LPC47M182 are 1, 2 or 4 bytes.

See the “Low Pin Count (LPC) Interface Specification” Reference, Section 6.4, for the field definitions and the sequence of the DMA Read and Write cycles.

6.3.7 DMA Protocol

DMA on the LPC bus is handled through the use of the nLDRQ lines from the LPC47M182 and special encodings on LAD[3:0] from the host.

The DMA mechanism for the LPC bus is described in the “Low Pin Count (LPC) Interface Specification,” Revision 1.0.

6.3.8 POWER MANAGEMENT

CLOCKRUN Protocol

The CLKRUN# pin is not implemented in the LPC47M182.

See the “Low Pin Count (LPC) Interface Specification” Revision 1.0, Section 8.1.

LPCPD Protocol

See the “Low Pin Count (LPC) Interface Specification” Revision 1.0, Section 8.2.

6.3.9 SYNC Protocol

See the “Low Pin Count (LPC) Interface Specification” Revision 1.0, Section 4.2.1.8 for a table of valid SYNC values.

Typical Usage

The SYNC pattern is used to add wait states. For read cycles, the LPC47M182 immediately drives the SYNC pattern upon recognizing the cycle. The host immediately drives the sync pattern for write cycles. If the LPC47M182 needs to assert wait states, it does so by driving 0101 or 0110 on LAD[3:0] until it is ready, at which point it will drive 0000 or 1001. The LPC47M182 will choose to assert 0101 or 0110, but not switch between the two patterns.

The data (or wait state SYNC) will immediately follow the 0000 or 1001 value. The SYNC value of 0101 is intended to be used for normal wait states, wherein the cycle will complete within a few clocks. The LPC47M182 uses a SYNC of 0101 for all wait states in a DMA transfer.

The SYNC value of 0110 is intended to be used where the number of wait states is large. This is provided for EPP cycles, where the number of wait states could be quite large (>1 microsecond). However, the LPC47M182 uses a SYNC of 0110 for all wait states in an I/O transfer.

The SYNC value is driven within 3 clocks.

SYNC Timeout

The SYNC value is driven within 3 clocks. If the host observes 3 consecutive clocks without a valid SYNC pattern, it will abort the cycle.

The LPC47M182 does not assume any particular timeout. When the host is driving SYNC, it may have to insert a very large number of wait states, depending on PCI latencies and retries.

SYNC Patterns and Maximum Number of SYNCS

If the SYNC pattern is 0101, then the host assumes that the maximum number of SYNCs is 8.

If the SYNC pattern is 0110, then no maximum number of SYNCs is assumed. The LPC47M182 has protection mechanisms to complete the cycle. This is used for EPP data transfers and should utilize the same timeout protection that is in EPP.

SYNC Error Indication

The LPC47M182 reports errors via the LAD[3:0] = 1010 SYNC encoding.

If the host was reading data from the LPC47M182, data will still be transferred in the next two nibbles. This data may be invalid, but it will be transferred by the LPC47M182. If the host was writing data to the LPC47M182, the data had already been transferred.

In the case of multiple byte cycles, such as memory and DMA cycles, an error SYNC terminates the cycle. Therefore, if the host is transferring 4 bytes from a device, if the device returns the error SYNC in the first byte, the other three bytes will not be transferred.

6.3.10 I/O and DMA START Fields

I/O and DMA cycles use a START field of 0000.

Reset Policy

The following rules govern the reset policy:

When nPCI_RESET goes inactive (high), the clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.

When nPCI_RESET goes active (low):

- the host drives the nLFRAME signal high, tristates the LAD[3:0] signals, and ignores the nLDRQ signal.
- the LPC47M182 must ignore nLFRAME, tristate the LAD[3:0] pins and drive the nLDRQ signal inactive (high).

6.3.11 LPC TRANSFERS

Wait State Requirements

I/O Transfers

The LPC47M182 inserts three wait states for an I/O read and two wait states for an I/O write cycle. A SYNC of 0110 is used for all I/O transfers. The exception to this is for transfers where IOCHRDY would normally be deasserted in an ISA transfer (i.e., EPP or IrCC transfers) in which case the sync pattern of 0110 is used and a large number of syncs may be inserted (up to 330 which corresponds to a timeout of 10us).

DMA Transfers

The LPC47M182 inserts three wait states for a DMA read and four wait states for a DMA write cycle. A SYNC of 0101 is used for all DMA transfers.

See the example timing for the LPC cycles in the “Timing Diagrams” section.

6.4 Floppy Disk Controller

The Floppy Disk controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC is compatible to the 82077AA using SMSC's proprietary floppy disk controller core.

6.4.1 FDC Configuration Registers

The FDC configuration registers are summarized in Table 11.1 in Chapter 11 Configuration. The FDC logical device configuration registers (0xF0, 0xF1, 0xF2 and 0xF4) are defined in Table 11.9.

6.4.2 FDC Internal Registers

The Floppy Disk Controller contains eight internal registers which facilitate the interfacing between the host microprocessor and the disk drive. Table 6.2 shows the addresses required to access these registers. Registers other than the ones shown are not supported. The rest of the description assumes that the primary addresses have been selected.

Table 6.2 - Status, Data and Control Registers

(Shown with base addresses of 3F0 and 370)

PRIMARY ADDRESS	SECONDARY ADDRESS	R/W	REGISTER
3F0	370	R	Status Register A (SRA)
3F1	371	R	Status Register B (SRB)
3F2	372	R/W	Digital Output Register (DOR)
3F3	373	R/W	Tape Drive Register (TDR)
3F4	374	R	Main Status Register (MSR)
3F4	374	W	Data Rate Select Register (DSR)
3F5	375	R/W	Data (FIFO)
3F6	376		Reserved
3F7	377	R	Digital Input Register (DIR)
3F7	377	W	Configuration Control Register (CCR)

6.4.3 STATUS REGISTER A (SRA)

Address 3F0 READ ONLY

This register is read-only and monitors the state of the internal interrupt signal and several disk interface pins in PS/2 and Model 30 modes. The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 – D7 are held in a high impedance state for a read of address 3F0.

PS/2 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	nDRV2	STEP	nTRK0	HDSEL	nINDX	nWP	DIR
RESET COND.	0	1	0	N/A	0	N/A	N/A	0

BIT 0 DIRECTION

Active high status indicating the direction of head movement. A logic “1” indicates inward direction; a logic “0” indicates outward direction.

BIT 1 nWRITE PROTECT

Active low status of the WRITE PROTECT disk interface input. A logic “0” indicates that the disk is write protected.

BIT 2 nINDEX

Active low status of the INDEX disk interface input.

BIT 3 HEAD SELECT

Active high status of the HDSEL disk interface input. A logic “1” selects side 1 and a logic “0” selects side 0.

BIT 4 nTRACK 0

Active low status of the TRK0 disk interface input.

BIT 5 STEP

Active high status of the STEP output disk interface output pin.

BIT 6 nDRV2

This function is not supported. This bit is always read as “1”.

BIT 7 INTERRUPT PENDING

Active high bit indicating the state of the Floppy Disk Interrupt output.

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	DRQ	STEP F/F	TRK0	nHDSEL	INDEX	WP	nDIR
RESET COND.	0	0	0	N/A	1	N/A	N/A	1

BIT 0 DIRECTION

Active low status indicating the direction of head movement. A logic “0” indicates inward direction; a logic “1” indicates outward direction.

BIT 1 WRITE PROTECT

Active high status of the WRITE PROTECT disk interface input. A logic “1” indicates that the disk is write protected.

BIT 2 INDEX

Active high status of the INDEX disk interface input.

BIT 3 HEAD SELECT

Active low status of the HDSEL disk interface input. A logic “0” selects side 1 and a logic “1” selects side 0.

BIT 4 TRACK 0

Active high status of the TRK0 disk interface input.

BIT 5 STEP

Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

BIT 6 DMA REQUEST

Active high status of the DMA request pending.

BIT 7 INTERRUPT PENDING

Active high bit indicating the state of the Floppy Disk Interrupt.

6.4.4 STATUS REGISTER B (SRB)

Address 3F1 READ ONLY

This register is read-only and monitors the state of several disk interface pins in PS/2 and Model 30 modes. The SRB can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 – D7 are held in a high impedance state for a read of address 3F1.

PS/2 Mode

	7	6	5	4	3	2	1	0
	1	1	DRIVE SEL0	WDATA TOGGLE	RDATA TOGGLE	WGATE	MOT EN1	MOT EN0
RESET COND.	1	1	0	0	0	0	0	0

BIT 0 MOTOR ENABLE 0

Active high status of the MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 1 MOTOR ENABLE 1

Active high status of the MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 2 WRITE GATE

Active high status of the WGATE disk interface output.

BIT 3 READ DATA TOGGLE

Every inactive edge of the RDATA input causes this bit to change state.

BIT 4 WRITE DATA TOGGLE

Every inactive edge of the WDATA input causes this bit to change state.

BIT 5 DRIVE SELECT 0

Reflects the status of the Drive Select 0 bit of the DOR (address 3F2 bit 0). This bit is cleared after a hardware reset and it is unaffected by a software reset.

BIT 6 RESERVED

Always read as a logic “1”.

BIT 7 RESERVED

Always read as a logic “1”

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	nDRV2	nDS1	nDS0	WDATA F/F	RDATA F/F	WGATE F/F	nDS3	nDS2
RESET COND.	N/A	1	1	0	0	0	1	1

BIT 0 nDRIVE SELECT 2

The DS2 disk interface is not supported.

BIT 1 nDRIVE SELECT 3

The DS3 disk interface is not supported.

BIT 2 WRITE GATE

Active high status of the latched WGATE output signal. This bit is latched by the active going edge of WGATE and is cleared by the read of the DIR register.

BIT 3 READ DATA

Active high status of the latched RDATA output signal. This bit is latched by the inactive going edge of RDATA and is cleared by the read of the DIR register.

BIT 4 WRITE DATA

Active high status of the latched WDATA output signal. This bit is latched by the inactive going edge of WDATA and is cleared by the read of the DIR register. This bit is not gated with WGATE.

BIT 5 nDRIVE SELECT 0

Active low status of the DS0 disk interface output.

BIT 6 nDRIVE SELECT 1

Active low status of the DS1 disk interface output.

BIT 7 nDRV2

Active low status of the DRV2 disk interface input. Note: This function is not supported.

6.4.5 DIGITAL OUTPUT REGISTER (DOR)

Address 3F2 READ/WRITE

The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT

These two bits are binary encoded for the drive selects, thereby allowing only one drive to be selected at one time.

BIT 2 nRESET

A logic “0” written to this bit resets the Floppy disk controller. This reset will remain active until a logic “1” is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN

PC/AT and Model 30 Mode:

Writing this bit to logic “1” will enable the DMA and interrupt functions. This bit being a logic “0” will disable the DMA and interrupt functions. This bit is a logic “0” after a reset and in these modes.

PS/2 Mode: In this mode the DMA and interrupt functions are always enabled. During a reset, this bit will be cleared to a logic “0”.

BIT 4 MOTOR ENABLE 0

This bit controls the MTR0 disk interface output. A logic “1” in this bit will cause the output pin to go active.

BIT 5 MOTOR ENABLE 1

This bit controls the MTR1 disk interface output. A logic “1” in this bit will cause the output pin to go active.

DRIVE	DOR VALUE
0	1CH
1	2DH

Table 6.3 - Internal 2 Drive Decode – Normal

DIGITAL OUTPUT REGISTER				DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	1	0	0	1	0	nBIT 5	nBIT 4
1	X	0	1	0	1	nBIT 5	nBIT 4
0	0	X	X	1	1	nBIT 5	nBIT 4

Table 6.4 - Internal 2 Drive Decode – Drives 0 and 1 Swapped

DIGITAL OUTPUT REGISTER				DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	1	0	0	0	1	nBIT 4	nBIT 5
1	X	0	1	1	0	nBIT 4	nBIT 5
0	0	X	X	1	1	nBIT 4	nBIT 5

BIT 6 MOTOR ENABLE 2

The MTR2 disk interface output is not supported in the LPC47M182.

BIT 7 MOTOR ENABLE 3

The MTR3 disk interface output is not supported in the LPC47M182.

6.4.6 TAPE DRIVE REGISTER (TDR)

Address 3F3 READ/WRITE

The Tape Drive Register (TDR) is included for 82077 software compatibility and allows the user to assign tape support to a particular drive during initialization. Any future references to that drive automatically invokes tape support. The TDR Tape Select bits TDR.[1:0] determine the tape drive number. Table 6.5 illustrates the Tape Select Bit encoding. Note that drive 0 is the boot device and cannot be assigned tape support. The remaining Tape Drive Register bits TDR.[7:2] are tristated when read. The TDR is unaffected by a software reset.

Table 6.5 - Tape Select Bits

TAPE SEL1 (TDR.1)	TAPE SEL0 (TDR.0)	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

Normal Floppy Mode

Normal mode.Register 3F3 contains only bits 0 and 1. When this register is read, bits 2 – 7 are '0'.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	0	0	0	0	0	0	tape sel1	tape sel0

Enhanced Floppy Mode 2 (OS2)

Register 3F3 for Enhanced Floppy Mode 2 operation.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Reserved	Reserved	Drive Type ID		Floppy Boot Drive		tape sel1	tape sel0

Table 6.6 - Drive Type ID

DIGITAL OUTPUT REGISTER		REGISTER 3F3 – DRIVE TYPE ID	
Bit 1	Bit 0	Bit 5	Bit 4
0	0	L0-CRF2 – B1	L0-CRF2 – B0
0	1	L0-CRF2 – B3	L0-CRF2 – B2
1	0	L0-CRF2 – B5	L0-CRF2 – B4
1	1	L0-CRF2 – B7	L0-CRF2 – B6

Note: L0-CRF2-Bx = FDC Logical Device, Configuration Register F2, Bit x.

6.4.7 DATA RATE SELECT REGISTER (DSR)

Address 3F4 WRITE ONLY

This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30.

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
RESET COND.	0	0	0	0	0	0	1	0

This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30.

Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250 Kbps.

BIT 0 and 1 DATA RATE SELECT

These bits control the data rate of the floppy controller. See Table 6.8 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 through 4 PRECOMPENSATION SELECT

These three bits select the value of write precompensation that will be applied to the WDATA output signal. Table 6.7 shows the precompensation values for the combination of these bits settings. Track 0 is the default starting track number to start precompensation. This starting track number can be changed by the configure command.

Table 6.7 - Precompensation Delays

PRECOMP 432	PRECOMPENSATION DELAY (nsec)	
	<2Mbps	2Mbps
111	0.00	0
001	41.67	20.8
010	83.34	41.7
011	125.00	62.5
100	166.67	83.3
101	208.33	104.2
110	250.00	125
000	Default	Default

Default: See Table 6.10

BIT 5 UNDEFINED

Should be written as a logic “0”.

BIT 6 LOW POWER

A logic "1" written to this bit will put the floppy controller into manual low power mode. The floppy controller clock and data separator circuits will be turned off. The controller will come out of manual low power mode after a software reset or access to the Data Register or Main Status Register.

BIT 7 SOFTWARE RESET

This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.

Separator circuits will be turned off. The controller will come out of manual low power.

Note: The DSR is Shadowed in the Floppy Data Rate Select Shadow Register, located at the offset 0x19 in the Power Control Logical Device (when LD_NUM=0) or Runtime Register Block Logical Device (when LD_NUM=1).

Table 6.8 - Data Rates

DRIVE RATE		DATA RATE		DATA RATE		DENSEL	DRATE(1)	
DRT1	DRT0	SEL1	SEL0	MFM	FM		1	0
0	0	1	1	1Meg	---	1	1	1
0	0	0	0	500	250	1	0	0
0	0	0	1	300	150	0	0	1
0	0	1	0	250	125	0	1	0
0	1	1	1	1Meg	---	1	1	1
0	1	0	0	500	250	1	0	0
0	1	0	1	500	250	0	0	1
0	1	1	0	250	125	0	1	0
1	0	1	1	1Meg	---	1	1	1
1	0	0	0	500	250	1	0	0
1	0	0	1	2Meg	---	0	0	1
1	0	1	0	250	125	0	1	0

Drive Rate Table (Recommended) 00 = 360K, 1.2M, 720K, 1.44M and 2.88M Vertical Format
01 = 3-Mode Drive
10 = 2 Meg Tape

Note 1: The DRATE and DENSEL values are mapped onto the DRVDEN pins.

Table 6.9 - DRVDEN Mapping

DT1	DT0	DRVDEN1 (1)	DRVDEN0 (1)	DRIVE TYPE
0	0	DRATE0	DENSEL	4/2/1 MB 3.5" 2/1 MB 5.25" FDDS 2/1.6/1 MB 3.5" (3-MODE)
1	0	DRATE0	DRATE1	
0	1	DRATE0	nDENSEL	PS/2
1	1	DRATE1	DRATE0	

Table 6.10 - Default Precompensation Delays

DATA RATE	PRECOMPENSATION DELAYS
2 Mbps	20.8 ns
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

6.4.8 MAIN STATUS REGISTER

Address 3F4 READ ONLY

The Main Status Register is a read-only register and indicates the status of the disk controller. The Main Status Register can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before each byte transferring to or from the data register except in DMA mode. No delay is required when reading the MSR after a data transfer.

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	Reserved	Reserved	DRV1 BUSY	DRV0 BUSY

BIT 0 – 1 DRV x BUSY

These bits are set to 1s when a drive is in the seek portion of a command, including implied and overlapped seeks and recalibrates.

BIT 4 COMMAND BUSY

This bit is set to a 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (Seek, Recalibrate commands), this bit is returned to a 0 after the last command byte.

BIT 5 NON-DMA

Reserved, read '0'. This part does not support non-DMA mode.

BIT 6 DIO

Indicates the direction of a data transfer once a RQM is set. A 1 indicates a read and a 0 indicates a write is required.

BIT 7 RQM

Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

6.4.9 DATA REGISTER (FIFO)

Address 3F5 READ/WRITE

All command parameter information, disk data and result status are transferred between the host processor and the floppy disk controller through the Data Register.

Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 6.11 gives several examples of the delays with a FIFO.

The data is based upon the following formula:

$$\text{Threshold \#} \times \frac{1}{\text{DATA RATE}} \times 8 - 1.5\ \text{us} = \text{DELAY}$$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

Table 6.11 - FIFO Service Delay

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 2 Mbps DATA RATE
1 byte	1 x 4 us - 1.5 us = 2.5 us
2 bytes	2 x 4 us - 1.5 us = 6.5 us
8 bytes	8 x 4 us - 1.5 us = 30.5 us
15 bytes	15 x 4 us - 1.5 us = 58.5 us

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 1 Mbps DATA RATE
1 byte	1 x 8 us - 1.5 us = 6.5 us
2 bytes	2 x 8 us - 1.5 us = 14.5 us
8 bytes	8 x 8 us - 1.5 us = 62.5 us
15 bytes	15 x 8 us - 1.5 us = 118.5 us

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 500 Kbps DATA RATE
1 byte	1 x 16 us - 1.5 us = 14.5 us
2 bytes	2 x 16 us - 1.5 us = 30.5 us
8 bytes	8 x 16 us - 1.5 us = 126.5 us
15 bytes	15 x 16 us - 1.5 us = 238.5 us

6.4.10 DIGITAL INPUT REGISTER (DIR)

Address 3F7 READ ONLY

This register is read-only in all modes.

PC-AT Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	0	0	0	0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

BIT 0 – 6 UNDEFINED

The data bus outputs D0 – 6 are read as '0'.

BIT 7 DSKCHG

This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register. The register is located in the Power Control Logical Device (when LD_NUM=0) or Runtime Register Block Logical Device (when LD_NUM=1)at offset 0x18.

PS/2 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	1	1	1	1	DRATE SEL1	DRATE SEL0	nHIGH DENS
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

BIT 0 nHIGH DENS

This bit is low whenever the 500 Kbps or 1 Mbps data rates are selected, and high when 250 Kbps and 300 Kbps are selected.

BITS 1 – 2 DATA RATE SELECT

These bits control the data rate of the floppy controller. See Table 6.8 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BITS 3 – 6 UNDEFINED

Always read as a logic "1"

BIT 7 DSKCHG

This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register. This register is located in the Power Control Logical Device (when LD_NUM=0) or Runtime Register Block Logical Device (when LD_NUM=1)at offset 0x18.

Model 30 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	DMAEN	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	0	0	0	0	0	1	0

BITS 0 – 1 DATA RATE SELECT

These bits control the data rate of the floppy controller. See Table 6.8 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 NOPREC

This bit reflects the value of NOPREC bit set in the CCR register.

BIT 3 DMAEN

This bit reflects the value of DMAEN bit set in the DOR register bit 3.

BITS 4 – 6 UNDEFINED

Always read as a logic “0”

BIT 7 DSKCHG

This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register. This register is located in the Power Control Logical Device (when LD_NUM=0) or Runtime Register Block Logical Device (when LD_NUM=1)at offset 0x18.

6.4.11 CONFIGURATION CONTROL REGISTER (CCR)

Address 3F7 WRITE ONLY

PC/AT and PS/2 Modes

	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1

These bits determine the data rate of the floppy controller. See Table 6.8 for the appropriate values.

BIT 2 – 7 RESERVED

Should be set to a logical “0”

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	0	0	0	0	0	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1

These bits determine the data rate of the floppy controller. See Table 6.8 for the appropriate values.

BIT 2 NO PRECOMPENSATION

This bit can be set by software, but it has no functionality. It can be read by bit 2 of the DSR when in Model 30 register mode. Unaffected by software reset.

BIT 3 – 7 RESERVED

Should be set to a logical “0”

Table 6.9 shows the state of the DENSEL pin. The DENSEL pin is set high after a hardware reset and is unaffected by the DOR and the DSR resets.

6.4.12 STATUS REGISTER ENCODING

During the Result Phase of certain commands, the Data Register contains data bytes that give the status of the command just executed.

Table 6.12 - Status Register 0

BIT NO.	SYMBOL	NAME	DESCRIPTION
7,6	IC	Interrupt Code	00 - Normal termination of command. The specified command was properly executed and completed without error. 01 - Abnormal termination of command. Command execution was started, but was not successfully completed. 10 - Invalid command. The requested command could not be executed. 11 - Abnormal termination caused by Polling.
5	SE	Seek End	The FDC completed a Seek, Relative Seek or Recalibrate command (used during a Sense Interrupt Command).
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. Step pulses in the Recalibrate command. 2. The Relative Seek command caused the FDC to step outward beyond Track 0.
3			Unused. This bit is always "0".
2	H	Head Address	The current head address.
1,0	DS1,0	Drive Select	The current selected drive.

Table 6.13 - Status Register 1

BIT NO.	SYMBOL	NAME	DESCRIPTION
7	EN	End of Cylinder	The FDC tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data command.
6			Unused. This bit is always "0".
5	DE	Data Error	The FDC detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the FDC does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3			Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. Read Data, Read Deleted Data command - the FDC did not find the specified sector. 2. Read ID command - the FDC cannot read the ID field without an error. 3. Read A Track command - the FDC cannot find the proper sector sequence.
1	NW	Not Writeable	WP pin became a "1" while the FDC is executing a Write Data, Write Deleted Data, or Format A Track command.
0	MA	Missing Address Mark	Any one of the following: 1. The FDC did not detect an ID address mark at the specified track after encountering the index pulse from the nINDEX pin twice. 2. The FDC cannot detect a data address mark or a deleted data address mark on the specified track.

Table 6.14 - Status Register 2

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: Read Data command - the FDC encountered a deleted data address mark. Read Deleted Data command - the FDC encountered a data address mark.
5	DD	Data Error in Data Field	The FDC detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3			Unused. This bit is always "0".
2			Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 6.15 - Status Register 3

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WRTPRT pin.
5			Unused. This bit is always "1".
4	T0	Track 0	Indicates the status of the TRK0 pin.
3			Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the DS1, DS0 pins.

RESET

There are three sources of system reset on the FDC: the nPCI_RESET pin, a reset generated via a bit in the DOR, and a reset generated via a bit in the DSR. At power on, a Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upon a nPCI_RESET, and the FDC enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the Configure command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new Configure command.

nPCI_RESET Pin (Hardware Reset)

The nPCI_RESET pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset vs. DSR Reset (Software Reset)

These two resets are functionally the same. Both will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR reset clears itself automatically while the DOR reset requires the host to manually clear it. DOR reset has precedence over the DSR reset. The DOR reset is set automatically upon a pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

6.5 MODES OF OPERATION

The FDC has three modes of operation, PC/AT mode, PS/2 mode and Model 30 mode. These are determined by the state of the Interface Mode bits in FDC logical device -CRF0[3,2].

6.5.1 PC/AT mode

The PC/AT register set is enabled, the DMA enable bit of the DOR becomes valid (controls the interrupt and DMA functions), and DENSEL is an active high signal.

6.5.2 PS/2 mode

This mode supports the PS/2 models 50/60/80 configuration and register set. The DMA bit of the DOR becomes a “don’t care”. The DMA and interrupt functions are always enabled, and DENSEL is active low.

6.5.3 Model 30 mode

This mode supports PS/2 Model 30 configuration and register set. The DMA enable bit of the DOR becomes valid (controls the interrupt and DMA functions), and DENSEL is active low.

6.6 DMA TRANSFERS

DMA transfers are enabled with the Specify command and are initiated by the FDC by activating a DMA request cycle. DMA read, write and verify cycles are supported. The FDC supports two DMA transfer modes: Single Transfer and Burst Transfer. Burst mode is enabled via FDC Logical Device -CRF0-Bit[1].

6.7 CONTROLLER PHASES

For simplicity, command handling in the FDC can be divided into three phases: Command, Execution, and Result. Each phase is described in the following sections.

6.7.1 Command Phase

After a reset, the FDC enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the FDC before the command phase is complete. (Please refer to section 6.10 Command Set/Descriptions). These bytes of data must be transferred in the order prescribed.

Before writing to the FDC, the host must examine the RQM and DIO bits of the Main Status Register. RQM and DIO must be equal to “1” and “0” respectively before command bytes may be written. RQM is set false by the FDC after each write cycle until the received byte is processed. The FDC asserts RQM again to request each parameter byte of the command unless an illegal command condition is detected. After the last parameter byte is received, RQM remains “0” and the FDC automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to provide for the proper handling of the “Invalid Command” condition.

6.7.2 Execution Phase

All data transfers to or from the FDC occur during the execution phase, which can proceed in DMA mode as indicated in the Specify command.

After a reset, the FIFO is disabled. Each data byte is transferred by a read/write or DMA cycle depending on the DMA mode. The Configure command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the FDC when service is requested from the host and ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

Non-DMA Mode – Transfers from the FIFO to the Host

This part does not support non-DMA mode.

Non-DMA Mode – Transfers from the Host to the FIFO

This part does not support non-DMA mode.

DMA Mode – Transfers from the FIFO to the Host

The FDC generates a DMA request cycle when the FIFO contains (16 - <threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The FDC will deactivate the DMA request when the FIFO becomes empty by generating the proper sync for the data transfer.

DMA Mode – Transfers from the Host to the FIFO.

The FDC generates a DMA request cycle when entering the execution phase of the data transfer commands. The DMA controller must respond by placing data in the FIFO. The DMA request remains active until the FIFO becomes full. The DMA request cycle is reasserted when the FIFO has <threshold> bytes remaining in the FIFO. The FDC will terminate the DMA cycle after a TC, indicating that no more data is required.

6.8 Data Transfer Termination

The FDC supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer.

If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the FDC will continue to complete the sector as if a TC cycle was received. The only difference between these implicit functions and TC cycle is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the FDC, the internal sector count will be complete when the FDC reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the FDC to read the last 16 bytes from the FIFO. The host must tolerate this delay.

6.9 Result Phase

The generation of the interrupt determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the FDC before the result phase is complete. These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared, indicating that the FDC is ready to accept the next command.

6.10 Command Set/Descriptions

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it is invalid, an interrupt is issued. The user sends a Sense Interrupt Status command which returns an invalid command error. Refer to Table 6.16 for explanations of the various symbols used. Table 6.17 lists the required parameters and the results associated with each command that the FDC is capable of performing.

Table 6.16 – Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
C	Cylinder Address	The currently selected address; 0 to 255.
D	Data Pattern	The pattern to be written in each sector data field during formatting.
D0, D1	Drive Select 0-1	Designates which drives are perpendicular drives on the Perpendicular Mode Command. A "1" indicates a perpendicular drive.
DIR	Direction Control	If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.
DS0, DS1	Disk Drive Select	DS1 DS0 DRIVE 0 0 Drive 0 0 1 Drive 1
DTL	Special Sector Size	By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.
EC	Enable Count	When this bit is "1" the "DTL" parameter of the Verify command becomes SC (number of sectors per track).
EFIFO	Enable FIFO	This active low bit when a 0, enables the FIFO. A "1" disables the FIFO (default).
EIS	Enable Implied Seek	When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.
EOT	End of Track	The final sector number of the current track.
GAP		Alters Gap 2 length when using Perpendicular Mode.
GPL	Gap Length	The Gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).
H/HDS	Head Address	Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	Head Load Time	The time interval that FDC waits after loading the head and before initializing a read or write operation. Refer to the Specify command for actual delays.
HUT	Head Unload Time	The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the Specify command for actual delays.

SYMBOL	NAME	DESCRIPTION
LOCK		Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE COMMAND can be reset to their default values by a “software Reset”. (A reset caused by writing to the appropriate bits of either the DSR or DOR)
MFM	MFM/FM Mode Selector	A one selects the double density (MFM) mode. A zero selects single density (FM) mode.
MT	Multi-Track Selector	When set, this flag selects the multi-track operating mode. In this mode, the FDC treats a complete cylinder under head 0 and 1 as a single track. The FDC operates as this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0.
N	Sector Size Code	This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the user's responsibility to not select combinations that are not possible with the drive. N SECTOR SIZE 00 128 Bytes 01 256 Bytes 02 512 Bytes 03 1024 Bytes … … 07 16K Bytes
NCN	New Cylinder Number	The desired cylinder number.
ND	Non-DMA Mode Flag	Write ‘0’. This part does not support non-DMA mode.
OW	Overwrite	The bits D0-D3 of the Perpendicular Mode Command can only be modified if OW is set to 1. OW id defined in the Lock command.
PCN	Present Cylinder Number	The current position of the head at the completion of Sense Interrupt Status command.
POLL	Polling Disable	When set, the internal polling routine is disabled. When clear, polling is enabled.
PRETRK	Precompensation Start Track Number	Programmable from track 00 to FFH.
R	Sector Address	The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	Relative Cylinder Number	Relative cylinder offset from present cylinder as used by the Relative Seek command.
SC	Number of Sectors Per Track	The number of sectors per track to be initialized by the Format command. The number of sectors per track to be verified during a Verify command when EC is set.
SK	Skip Flag	When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to “0”, the sector is read or written the same as the read and write commands.

SYMBOL	NAME	DESCRIPTION
SRT	Step Rate Interval	The time interval between step pulses issued by the FDC. Programmable from 0.5 to 8 milliseconds in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Registers within the FDC which store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	Write Gate	Alters timing of WE to allow for pre-erase loads in perpendicular drives.

6.10.1 Instruction Set

Table 6.17 - Instruction Set

READ DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ DELETED DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DATA										
		DATA BUS								
PHASE	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**REMARKS**
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA										
		DATA BUS								
PHASE	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**REMARKS**
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution.
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and system. FDC reads all of cylinders' contents from index hole to EOT.
Result	R					ST0				Status information after Command execution.
	R					ST1				
	R					ST2				
	R					C				Sector ID information after Command execution.
	R					H				
	R					R				
	R					N				

VERIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution.
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL/SC				
Execution										No data transfer takes place.
Result	R					ST0				Status information after Command execution.
	R					ST1				
	R					ST2				
	R					C				Sector ID information after Command execution.
	R					H				
	R					R				
	R					N				

VERSION										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

FORMAT A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					N				Bytes/Sector
	W					SC				Sectors/Cylinder
	W					GPL				Gap 3
	W					D				Filler Byte
Execution for Each Sector Repeat:	W					C				Input Sector Parameters
	W					H				
	W					R				
	W					N				
										FDC formats an entire cylinder
Result	R					ST0				Status information after Command execution
	R					ST1				
	R					ST2				
	R					Undefined				
	R					Undefined				
	R					Undefined				
	R					Undefined				

RECALIBRATE									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt.

SENSE INTERRUPT STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R					ST0				Status information at the end of each seek operation.
	R					PCN				

SPECIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W			SRT				HUT		
	W					HLT			ND	

SENSE DRIVE STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	ST3								Status information about FDD

SEEK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	NCN								
Execution										Head positioned over proper cylinder on diskette.

CONFIGURE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	FIFOTHR				
Execution	W	PRETRK								

RELATIVE SEEK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	RCN								

DUMPREG										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	*Note: Registers placed in FIFO
Execution										
Result	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	SRT				HUT				
	R	HLT							ND	
	R	SC/EOT								
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL	FIFOTHR				
	R	PRETRK								

READ ID										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R					ST0				Status information after Command execution.
										Disk status after the Command has completed
	R					ST1				
	R					ST2				
	R					C				
	R					H				
	R					R				
	R					N				

PERPENDICULAR MODE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Codes
		OW	0	D3	D2	D1	D0	GAP	WGATE	

INVALID CODES										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	Invalid Codes								Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	ST0								ST0 = 80H

LOCK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

SC is returned if the last command that was issued was the Format command. EOT is returned if the last command was a Read or Write.

Note: These bits are used internally only. They are not reflected in the Drive Select pins. It is the user's responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

6.11 Data Transfer Commands

All of the Read Data, Write Data and Verify type commands use the same parameter bytes and return the same results information, the only difference being the coding of bits 0-4 in the first byte.

An implied seek will be executed if the feature was enabled by the Configure command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it is reflected in the results status normally returned for a Read/Write Data command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

6.11.1 Read Data

A set of nine (9) bytes is required to place the FDC in the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of the TC cycle, or an implied TC (FIFO overrun/underrun), the FDC stops sending data but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector, terminate the Read Data Command.

N determines the number of bytes per sector (see Table 6.18 below). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for CRC errors. For writes, it completes the 128-byte sector by filling in zeros. If N is not set to 00 Hex, DTL should be set to FF Hex and has no impact on the number of bytes transferred.

Table 6.18 - Sector Sizes

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	…
07	16 Kbytes

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track) and N (number of bytes/sector).

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing the last sector of the same track at Side 1.

If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 6.19.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify command) has elapsed. If the host issues another command before the head unloads, then the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the nINDEX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the Read Data Command.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the Read Data Command. Table 6.20 describes the effect of the SK bit on the Read Data command execution and results. Except where noted in Table 6.20, the C or R value of the sector address is automatically incremented (see Table 6.22).

Table 6.19 - Effects of MT and N Bits

MT	N	MAXIMUM TRANSFER CAPACITY	FINAL SECTOR READ FROM DISK
0	1	256 x 26 = 6,656	26 at side 0 or 1
1	1	256 x 52 = 13,312	26 at side 1
0	2	512 x 15 = 7,680	15 at side 0 or 1
1	2	512 x 30 = 15,360	15 at side 1
0	3	1024 x 8 = 8,192	8 at side 0 or 1
1	3	1024 x 16 = 16,384	16 at side 1

Table 6.20 - Skip Bit vs Read Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	No	Normal termination.
0	Deleted Data	Yes	Yes	Address not incremented. Next sector not searched for.
1	Normal Data	Yes	No	Normal termination.
1	Deleted Data	No	Yes	Normal termination. Sector not read ("skipped").

6.12 Read Deleted Data

This command is the same as the Read Data command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 6.21 describes the effect of the SK bit on the Read Deleted Data command execution and results. Except where noted in Table 6.21, the C or R value of the sector address is automatically incremented (see Table 6.22).

Table 6.21 - Skip Bit vs. Read Deleted Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	Yes	Address not incremented. Next sector not searched for.
0	Deleted Data	Yes	No	Normal termination.
1	Normal Data	No	Yes	Normal termination. Sector not read ("skipped").
1	Deleted Data	Yes	No	Normal termination.

6.13 Read A Track

This command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the nINDEX pin, the FDC starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The FDC compares the ID information read from each sector with the specified value in the command and sets the ND flag of Status Register 1 to a "1" if there no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors has not been read. If the FDC does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the nINDEX pin, then it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

Table 6.22 - Result Phase Table

MT	HEAD	FINAL SECTOR TRANSFERRED TO HOST	ID INFORMATION AT RESULT PHASE			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	LSB	01	NC

NC: No Change, the same value as the one at the beginning of command execution.
LSB: Least Significant Bit, the LSB of H is complemented.

6.14 Write Data

After the Write Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the Specify command), and begins reading ID fields. When the sector address read from the diskette matches the sector address specified in the command, the FDC reads the data from the host via the FIFO and writes it to the sector's data field.

After writing data into the current sector, the FDC computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the FDC continues writing to the next data field. The FDC continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros. The FDC reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the Write Data command.

The Write Data command operates in much the same manner as the Read Data command. The following items are the same. Please refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command

Definition of DTL when N = 0 and when N does not = 0

6.15 Write Deleted Data

This command is almost the same as the Write Data command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

6.16 Verify

The Verify command is used to verify the data stored on a disk. This command acts exactly like a Read Data command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously-stored value.

Because data is not transferred to the host, the TC cycle cannot be used to terminate this command. By setting the EC bit to "1", an implicit TC will be issued to the FDC. This implicit TC will occur when the SC value has decremented to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0", DTL/SC should be programmed to 0FFH. Refer to Table 6.22 and Table 6.23 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:
Sectors Per Side = Number of formatted sectors per each side of the disk.
Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 6.23 - Verify Command Result Phase Table

MT	EC	SC/EOT VALUE	TERMINATION RESULT
0	0	SC = DTL EOT <= # Sectors Per Side	Success Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC <= # Sectors Remaining AND EOT <= # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT <= # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC <= # Sectors Remaining AND EOT <= # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

Note: If MT is set to “1” and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

6.17 Format A Track

The Format command allows an entire track to be formatted. After a pulse from the nINDEX pin is detected, the FDC starts writing data on the disk including gaps, address marks, ID fields, and data fields per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID field for each sector is supplied by the host; that is, four data bytes per sector are needed by the FDC for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the FDC for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the FDC encounters a pulse on the nINDEX pin again and it terminates the command.

Table 6.24 contains typical values for gap fields that are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

FORMAT FIELDS

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP4a 80x 4E	SYNC 12x 00	IAM		GAP1 50x 4E	SYNC 12x 00	IDAM		CYL	HD	SEC	NO	CRC	GAP2 22x 4E	SYNC 12x 00	DATA AM		DATA	CRC	GAP3	GAP 4b
		3x C2	FC			3x A1	FE								3x A1	FB F8				

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a 40x FF	SYNC 6x 00	IAM	GAP1 26x FF	SYNC 6x 00	IDAM	CYL	HD	SEC	NO	CRC	GAP2 11x FF	SYNC 6x 00	DATA AM	DATA	CRC	GAP3	GAP 4b
		FC			FE								FB or F8				

PERPENDICULAR FORMAT

GAP4a 80x 4E	SYNC 12x 00	IAM		GAP1 50x 4E	SYNC 12x 00	IDAM		CYL	HD	SEC	NO	CRC	GAP2 41x 4E	SYNC 12x 00	DATA AM		DATA	CRC	GAP3	GAP 4b
		3x C2	FC			3x A1	FE								3x A1	FB F8				

Table 6.24 - Typical Values for Formatting

	FORMAT	SECTOR SIZE	N	SC	GPL1	GPL2
5.25" Drives	FM	128	00	12	07	09
		128	00	10	10	19
		512	02	08	18	30
		1024	03	04	46	87
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512*	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
3.5" Drives	FM	128	0	0F	07	1B
		256	1	09	0F	2A
		512	2	05	1B	3A
	MFM	256	1	0F	0E	36
		512**	2	09	1B	54
		1024	3	05	35	74

GPL1 = suggested GPL values in Read and Write commands to avoid splice point between data field and ID field of contiguous sections.

GPL2 = suggested GPL value in Format A Track command.

*PC/AT values (typical)

**PS/2 values (typical). Applies with 1.0 MB and 2.0 MB drives.

Note: All values except sector size are in hex.

6.18 Control Commands

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete: Read ID, Recalibrate, and Seek. The other control commands do not generate an interrupt.

6.18.1 Read ID

The Read ID command is used to find the present position of the recording heads. The FDC stores the values from the first ID field it is able to read into its registers. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the nINDEX pin, it then sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the Sense Interrupt Status command. Otherwise, valuable interrupt status information will be lost.

6.18.2 Recalibrate

This command causes the read/write head within the FDC to retract to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the nTRK0 pin from the FDD. As long as the nTRK0 pin is low, the DIR signal remains 0 and step pulses are issued. When the nTRK0 pin goes high, the SE bit in Status Register 0 is set to "1" and the command is terminated. If the nTRK0 pin is still low after 255 step pulses have been issued, the FDC sets the SE and the EC bits of Status Register 0 to "1" and terminates the command. Disks capable of handling more than 256 tracks per side may require more than one Recalibrate command to return the head back to physical Track 0.

The Recalibrate command does not have a result phase. The Sense Interrupt Status command must be issued after the Recalibrate command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in a NON-BUSY state. At this time, another Recalibrate command may be issued, and in this manner parallel Recalibrate operations may be done on up to four drives at once. Upon power up, the software must issue a Recalibrate command to properly initialize all drives and the controller.

6.18.3 Seek

The read/write head within the drive is moved from track to track under the control of the Seek command. The FDC compares the PCN, which is the current head position, with the NCN and performs the following operation if there is a difference:

PCN < NCN: Direction signal to drive set to "1" (step in) and issues step pulses.

PCN > NCN: Direction signal to drive set to "0" (step out) and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN the SE bit in Status Register 0 is set to "1" and the command is terminated. During the command phase of the seek or recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in the

NON-BUSY state. At this time, another Seek or Recalibrate command may be issued, and in this manner, parallel seek operations may be done on up to four drives at once.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1) Seek command - Step to the proper track
2) Sense Interrupt Status command - Terminate the Seek command
3) Read ID - Verify head is on proper track
4) Issue Read/Write command.

The Seek command does not have a result phase. Therefore, it is highly recommended that the Sense Interrupt Status command is issued after the Seek command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return to a "0". When exiting POWERDOWN mode, the FDC clears the PCN value and the status information to zero. Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the Sense Interrupt Status command.

6.19 Sense Interrupt Status

An interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Track command
   g. Write Deleted Data command
   h. Verify command
2. End of Seek, Relative Seek, or Recalibrate command

The Sense Interrupt Status command resets the interrupt signal and, via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt.

Table 6.25 - Interrupt Identification

SE	IC	INTERRUPT DUE TO
0	11	Polling
1	00	Normal termination of Seek or Recalibrate command
1	01	Abnormal termination of Seek or Recalibrate command

The Seek, Relative Seek, and Recalibrate commands have no result phase. The Sense Interrupt Status command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a Sense Interrupt Status is not issued, the drive will continue to be BUSY and may affect the operation of the next command.

6.20 Sense Drive Status

Sense Drive Status obtains drive status information. It has not execution phase and goes directly to the result phase from the command phase. Status Register 3 contains the drive status information.

6.21 Specify

The Specify command sets the initial values for each of the three internal times. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the read/write operation starts. The values change with the data rate speed selection and are documented in Table 6.26. The values are the same for MFM and FM.

DMA operation is selected by the ND bit. When ND is “0”, the DMA mode is selected. This part does not support non-DMA mode. In DMA mode, data transfers are signaled by the DMA request cycles.

6.22 Configure

The Configure command is issued to select the special features of the FDC. A Configure command need not be issued if the default values of the FDC meet the system requirements.

Table 6.26 - Drive Control Delays (ms)

	HUT					SRT				
	2M	**1M**	**500K**	**300K**	**250K**	**2M**	**1M**	**500K**	**300K**	**250K**
0	64	128	256	426	512	4	8	16	26.7	32
1	4	8	16	26.7	32	3.75	7.5	15	25	30
..	..	..	..	..	..	..	..	..	..	..
E	56	112	224	373	448	0.5	1	2	3.33	4
F	60	120	240	400	480	0.25	0.5	1	1.67	2

	HLT				
	2M	**1M**	**500K**	**300K**	**250K**
00	64	128	256	426	512
01	0.5	1	2	3.3	4
02	1	2	4	6.7	8
..	..	..	..	..	.
7F	63	126	252	420	504
7F	63.5	127	254	423	508

6.22.1 Configure Default Values:

EIS - No Implied Seeks
EFIFO - FIFO Disabled
POLL - Polling Enabled
FIFOTHR - FIFO Threshold Set to 1 Byte
PRETRK - Pre-Compensation Set to Track 0

EIS - Enable Implied Seek. When set to "1", the FDC will perform a Seek operation before executing a read or write command. Defaults to no implied seek.

EFIFO - A "1" disables the FIFO (default). This means data transfers are asked for on a byte-by-byte basis. Defaults to "1", FIFO disabled. The threshold defaults to "1".

POLL - Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR - The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A "00" selects one byte; "0F" selects 16 bytes.

PRETRK - Pre-Compensation Start Track Number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0; "FF" selects track 255.

6.23 Version

The Version command checks to see if the controller is an enhanced type or the older type (765A). A value of 90 H is returned as the result byte.

6.24 Relative Seek

The command is coded the same as for Seek, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

DIR	ACTION
0	Step Head Out
1	Step Head In

The Relative Seek command differs from the Seek command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The Seek command is good for drives that support a maximum of 256 tracks. Relative Seeks cannot be overlapped with other Relative Seeks. Only one Relative Seek can be active at a time. Relative Seeks may be overlapped with Seeks and Recalibrates. Bit 4 of Status Register 0 (EC) will be set if Relative Seek attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks. The host needs to read track 300 and the head is on any track (0-255). If a Seek command is issued, the head will stop at track 255. If a Relative Seek command is issued, the FDC will move the head the specified number of tracks, regardless of the internal cylinder position register (but will increment the register). If the head was on track 40 (d), the maximum track that the FDC could position the head on using Relative Seek will be 295 (D), the initial track + 255 (D). The maximum count that the head can be moved with a single Relative Seek command is 255 (D).

The internal register, PCN, will overflow as the cylinder number crosses track 255 and will contain 39 (D). The resulting PCN value is thus (RCN + PCN) mod 256. Functionally, the FDC starts counting from 0 again as the track number goes above 255 (D). It is the user's responsibility to compensate FDC functions (precompensation track number) when accessing tracks greater than 255. The FDC does not keep track that it is working in an "extended track area" (greater than 255). Any command issued will use the current PCN value except for the Recalibrate command, which only looks for the TRACK0 signal. Recalibrate will return an error if the head is farther than 255 due to its limitation of issuing a maximum of 256 step pulses. The user simply needs to issue a second Recalibrate command. The Seek command and implied seeks will function correctly within the 44 (D) track (299-255) area of the "extended track area". It is the user's

responsibility not to issue a new track position that will exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0-255) of tracks, a Relative Seek should be issued to cross the track 255 boundary.

A Relative Seek can be used instead of the normal Seek, but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a Read ID command to ensure that the head is physically on the track that software assumes it to be. Different FDC commands will return different cylinder results which may be difficult to keep track of with software without the Read ID command.

6.25 Perpendicular Mode

The Perpendicular Mode command should be issued prior to executing Read/Write/Format commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 6.27 describes the effects of the WGATE and GAP bits for the Perpendicular Mode command. Upon a reset, the FDC will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate Select Register. The user must ensure that these two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal, the pre-erase head is also activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes. The Format Fields table illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the FDC, the controller must begin synchronization at the beginning of the sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But, when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, and approximate two-byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the Write Data case, the FDC activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP =0).

It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the Perpendicular Mode command is invoked, FDC software behavior from the user standpoint is unchanged.

The perpendicular mode command is enhanced to allow specific drives to be designated Perpendicular recording drives. This enhancement allows data transfers between Conventional and Perpendicular drives without having to issue Perpendicular mode commands between the accesses of the different drive types, nor having to change write pre-compensation values.

When both GAP and WGATE bits of the PERPENDICULAR MODE COMMAND are both programmed to "0" (Conventional mode), then D0, D1, D2, D3, and D4 can be programmed independently to "1" for that drive to be set automatically to Perpendicular mode. In this mode the following set of conditions also apply:

1. The GAP2 written to a perpendicular drive during a write operation will depend upon the programmed data rate.
2. The write pre-compensation given to a perpendicular mode drive will be 0ns.
3. For D0-D3 programmed to "0" for conventional mode drives any data written will be at the currently programmed write pre-compensation.

Note: Bits D0-D3 can only be overwritten when OW is programmed as a "1".If either GAP or WGATE is a "1" then D0-D3 are ignored.

Software and hardware resets have the following effect on the PERPENDICULAR MODE COMMAND:

- "Software" resets (via the DOR or DSR registers) will only clear GAP and WGATE bits to "0". D0-D3 are unaffected and retain their previous value.
- "Hardware" resets will clear all bits (GAP, WGATE and D0-D3) to "0", i.e all conventional mode.

Table 6.27 - Effects of WGATE and GAP Bits

WGATE	GAP	MODE	LENGTH OF GAP2 FORMAT FIELD	PORTION OF GAP 2 WRITTEN BY WRITE DATA OPERATION
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500 Kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1 Mbps)	41 Bytes	38 Bytes

6.26 Lock

In order to protect systems with long DMA latencies against older application software that can disable the FIFO the LOCK Command has been added. This command should only be used by the FDC routines, and application software should refrain from using it. If an application calls for the FIFO to be disabled then the CONFIGURE command should be used.

The LOCK command defines whether the EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to logic "1" all subsequent "software RESETS by the DOR and DSR registers will not change the previously set parameters to their default values. All "hardware" RESET from the nPCI_RESET pin will set the LOCK bit to logic "0" and return the EFIFO, FIFOTHR, and PRETRK to their default values. A status byte is returned immediately after issuing a LOCK command. This byte reflects the value of the LOCK bit set by the command byte.

6.27 Enhanced DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. To accommodate the LOCK command and the enhanced PERPENDICULAR MODE command the eighth byte of the DUMPREG command has been modified to contain the additional data from these two commands.

6.27.1 COMPATIBILITY

The LPC47M182 was designed with software compatibility in mind. It is a fully backwards- compatible solution with the older generation 765A/B disk controllers. The FDC also implements on-board registers for compatibility with the PS/2, as well as PC/AT and PC/XT, floppy disk controller subsystems. After a hardware reset of the FDC, all registers, functions and enhancements default to a PC/AT, PS/2 or PS/2 Model 30 compatible operating mode, depending on how the IDENT and MFM bits are configured by the system BIOS.

6.28 Serial Port (UART)

The LPC47M182 incorporates two full function UARTs. They are compatible with the 16450, the 16450 ACE registers and the 16C550A. The UARTs perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable

from 460.8K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UARTs are also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt. The second UART also supports IrDA, HP-SIR, and ASK-IR infrared modes of operation.

Note: Input pins of Serial Port 2 are internally pulled down to VSS only until Serial Port 2 is enabled. Once Serial Port 2 is enabled, the pull-downs are removed until VTR POR.

6.28.1 REGISTER DESCRIPTION

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial port is defined by the configuration registers (see "Configuration" section). The Serial Port registers are located at sequentially increasing addresses above these base addresses (see Table 6.28).

Table 6.28 – Addressing the Serial Port

DLAB*	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write

***Note**: DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

6.28.2 RECEIVE BUFFER REGISTER (RB)

Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

6.28.3 TRANSMIT BUFFER REGISTER (TB)

Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

6.28.4 INTERRUPT ENABLE REGISTER (IER)

Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the LPC47M182. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0

This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic “1”.

Bit 1

This bit enables the Transmitter Holding Register Empty Interrupt when set to logic “1”.

Bit 2

This bit enables the Received Line Status Interrupt when set to logic “1”. The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3

This bit enables the MODEM Status Interrupt when set to logic “1”. This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7

These bits are always logic “0”.

6.28.5 FIFO CONTROL REGISTER (FCR)

Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. Note: DMA is not supported. The UART is shadowed in the UART1 FIFO Control Shadow Register (Located at offset 0x1A in the Power Control Logical Device, when LD_NUM=0, or Runtime Register Block Logical Device, when LD_NUM=1).

Bit 0

Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1

Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2

Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3

Writing to this bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

Bit 4,5

Reserved

Bit 6,7

These bits are used to set the trigger level for the RCVR FIFO interrupt.

6.28.6 INTERRUPT IDENTIFICATION REGISTER (IIR)

Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

Receiver Line Status (highest priority)

Received Data Ready

Transmitter Holding Register Empty

MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0

This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic “0”, an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic “1”, no interrupt is pending.

Bits 1 and 2

These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table.

Bit 3

In non-FIFO mode, this bit is a logic “0”. In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5

These bits of the IIR are always logic “0”.

Bits 6 and 7

These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

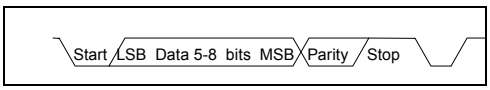
Bit 7	Bit 6	RCVR FIFO Trigger Level (BYTES)
0	0	1
0	1	4
1	0	8
1	1	14

Table 6.29 - Interrupt Control Table

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

6.28.7 LINE CONTROL REGISTER (LCR)

Address Offset = 3H, DLAB = 0, READ/WRITE



Serial Data

This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1

These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

The Start, Stop and Parity bits are not included in the word length.

BIT 1	BIT 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2

This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

BIT 2	WORD LENGTH	NUMBER OF STOP BITS
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3

Parity Enable bit. When bit 3 is a logic “1”, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4

Even Parity Select bit. When bit 3 is a logic “1” and bit 4 is a logic “0”, an odd number of logic “1”’s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic “1” and bit 4 is a logic “1” an even number of bits is transmitted and checked.

Bit 5

This bit is the Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as a 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0 Stick Parity is disabled.

Bit 6

Set Break Control bit. When bit 6 is a logic “1”, the transmit data output (TXD) is forced to the Spacing or logic “0” state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7

Divisor Latch Access bit (DLAB). It must be set high (logic “1”) to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic “0”) to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

6.28.8 MODEM CONTROL REGISTER (MCR)

Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

Bit 0

This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic “1”, the nDTR output is forced to a logic “0”. When bit 0 is a logic “0”, the nDTR output is forced to a logic “1”.

Bit 1

This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

Bit 2

This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3

Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4

This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic “1”, the following occur:

1. The TXD is set to the Marking State(logic “1”).
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is “looped back” into the Receiver Shift Register input.
4. All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5. The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI, DCD).
6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts’ sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7

These bits are permanently set to logic zero.

6.28.9 LINE STATUS REGISTER (LSR)

Address Offset = 5H, DLAB = X, READ/WRITE

Bit 0

Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

Bit 1

Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

Bit 2

Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

Bit 3

Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Bit 4

Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least ½ bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5

Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

Bit 6

Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty,

Bit 7

This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

6.28.10 MODEM STATUS REGISTER (MSR)

Address Offset = 6H, DLAB = X, READ/WRITE

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

Bit 0

Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

Bit 1

Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

Bit 2

Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic "0" to logic "1".

Bit 3

Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

Bit 4

This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic “1”, this bit is equivalent to nRTS in the MCR.

Bit 5

This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic “1”, this bit is equivalent to DTR in the MCR.

Bit 6

This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic “1”, this bit is equivalent to OUT1 in the MCR.

Bit 7

This bit is the complement of the Data Carrier Detect (nDCD) input. If bit 4 of the MCR is set to logic “1”, this bit is equivalent to OUT2 in the MCR.

6.28.11 SCRATCHPAD REGISTER (SCR)

Address Offset =7H, DLAB =X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

6.29 Programmable Baud Rate Generator (And Divisor Latches DLH, DLL)

The Serial Port contains a programmable Baud Rate Generator that is capable of dividing the internal PLL clock by any divisor from 1 to 65535. The internal PLL clock is divided down to generate a 1.8462MHz frequency for Baud Rates less than 38.4k, a 1.8432MHz frequency for 115.2k, a 3.6864MHz frequency for 230.4k and a 7.3728MHz frequency for 460.8k. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is a 1.8462 MHz clock. Table 6.30 shows the baud rates possible.

6.29.1 Effect Of The Reset on Register File

The Reset Function (details the effect of the Reset input on each of the registers of the Serial Port.

6.29.2 FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = "1", IER bit 0 = "1"), RCVR interrupts occur as follows:

A. The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.
B. The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.
C. The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.
D. The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

A. A FIFO timeout interrupt occurs if all the following conditions exist:
   At least one character is in the FIFO.
   The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay).
   The most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12 bit character.

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).
C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"), XMIT interrupts occur as follows:

A. The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

6.29.3 FIFO POLLED MODE OPERATION

With FCR bit 0 = "1" resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

Bit 0=1 as long as there is one byte in the RCVR FIFO.

Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.

Bit 5 indicates when the XMIT FIFO is empty.

Bit 6 indicates that both the XMIT FIFO and shift register are empty.

Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Table 6.30 - Baud Rates

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL[1]	HIGH SPEED BIT[2]
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

Note[1]: The percentage error for all baud rates, except where indicated otherwise, is 0.2%.
Note [2]: The High Speed bit is located in the Device Configuration Space.

Table 6.31 - Reset Function Table

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1 - 7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5, 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
TXD1, TXD2	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low
OUT2B	RESET	High
RTSB	RESET	High
DTRB	RESET	High
OUT1B	RESET	High
RCVR FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low
XMIT FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low

Table 6.32 - Register Summary for an Individual UART Channel

REGISTER ADDRESS*	REGISTER NAME	REGISTER SYMBOL	BIT 0	BIT 1
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 1)	Data Bit 1
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	“0” if Interrupt Pending	Interrupt ID Bit
ADDR = 2	FIFO Control Register (Write Only)	FCR (Note 7)	FIFO Enable	RCVR FIFO Reset
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)
ADDR = 7	Scratch Register (Note 4)	SCR	Bit 0	Bit 1
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9

*DLAB is Bit 7 of the Line Control Register (ADDR = 3).
Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Table 37 - Register Summary for an Individual UART Channel (continued)

BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Enable Receiver Line Status Interrupt (ELSI)	Enable MODEM Status Interrupt (EMSI)	0	0	0	0
Interrupt ID Bit	Interrupt ID Bit (Note 5)	0	0	FIFOs Enabled (Note 5)	FIFOs Enabled (Note 5)
XMIT FIFO Reset	DMA Mode Select (Note 6)	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
OUT1 (Note 3)	OUT2 (Note 3)	Loop	0	0	0
Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 2)	Error in RCVR FIFO (Note 5)
Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 3: This bit no longer has a pin associated with it.
Note 4: When operating in the XT mode, this register is not available.
Note 5: These bits are always zero in the non-FIFO mode.
Note 6: Writing a one to this bit has no effect. DMA modes are not supported in this chip.
Note 7: The UART FCR's is shadowed in the UART1 FIFO Control Shadow Register (Located at offset 0x1A in the in the Power Control Logical Device, when LD_NUM=0, or Runtime Register Block Logical Device, when LD_NUM=1).

Chapter 7 Notes On Serial Port Operation

7.1 FIFO Mode Operation:

7.1.1 GENERAL

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

7.1.2 TX AND RX FIFO OPERATION

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. **The UART will prevent loads to the Tx FIFO if it currently holds 16 characters**. Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. **Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay**.

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. **To prevent the software from having to check for this situation the chip incorporates a timeout interrupt**.

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256 kbaud).

7.2 Infrared Interface

The infrared interface provides a two-way wireless communications port using infrared as a transmission medium. Several IR implementations have been provided for the second UART in this chip, IrDA, HP-SIR and Amplitude Shift Keyed IR. The IR transmission can use the standard UART2 TXD2 and RXD2 pins or optional IRTX2 and IRRX2 pins. These can be selected through the configuration registers.

IrDA 1.0 allows serial communication at baud rates up to 115.2 kbps. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a single IR pulse at the beginning of the serial bit time. A one is signaled by sending no IR pulse during the bit time. Please refer to the AC timing for the parameters of these pulses and the IrDA waveform.

The Amplitude Shift Keyed IR allows asynchronous serial communication at baud rates up to 19.2K Baud. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a 500KHz waveform for the duration of the serial bit time. A one is signaled by sending no transmission during the bit time. Please refer to the AC timing for the parameters of the ASK-IR waveform.

If the Half Duplex option is chosen, there is a time-out when the direction of the transmission is changed. This time-out starts at the last bit transferred during a transmission and blocks the receiver input until the timeout expires. If the transmit buffer is loaded with more data before the time-out expires, the timer is restarted after the new byte is transmitted. If data is loaded into the transmit buffer while a character is being received, the transmission will not start until the time-out expires after the last receive bit has been received. If the start bit of another character is received during this time-out, the timer is restarted after the new character is received. The IR half duplex time-out is programmable via CRF2 in Logical Device 5. This register allows the time-out to be programmed to any value between 0 and 10msec in 100usec increments.

IR Transmit Pins

The following description pertains to the TXD2 and IRTX2 pins of the LPC47M182.

Following a VCC POR, the TXD2 and IRTX2 pins will be output and low. They will remain low until one of the following conditions are met:

IRTX2 Pin:

This pin will remain low following a VCC POR until serial port 2 is enabled by setting the activate bit, at which time the pin will reflect the state of the IR transmit output of the IRCC block.

TXD2 Pin:

This pin will remain low following a VCC POR until serial port 2 is enabled by setting the activate bit, at which time the pin will reflect the state of the IR transmit output of the IRCC block (if IR is enabled through the IR Option Register for Serial Port 2).

This pin will remain low following a VCC POR until serial port 2 is enabled by setting the activate bit, at which time the pin will reflect the state of the transmit output of serial port 2.

7.3 Parallel Port

The LPC47M182 incorporates an IBM XT/AT compatible parallel port. This supports the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port modes. Refer to the Configuration Registers for information on disabling, power down, changing the base address of the parallel port, and selecting the mode of operation.

The Parallel Port configuration registers are summarized in Table 11.1 in Chapter 11 Configuration. The Parallel Port logical device configuration registers (0xF0 and 0xF1) are defined in Table 11.11.

The parallel port also incorporates SMSC's ChiProtect circuitry, which prevents possible damage to the parallel port due to printer power-up.

The functionality of the Parallel Port is achieved through the use of eight addressable ports, with their associated registers and control gating. The control and data port are read/write by the CPU, the status port is read/write in the EPP mode. The address map of the Parallel Port is shown below:

DATA PORT	BASE ADDRESS + 00H	EPP DATA PORT 0	BASE ADDRESS + 04H
STATUS PORT	BASE ADDRESS + 01H	EPP DATA PORT 1	BASE ADDRESS + 05H
CONTROL PORT	BASE ADDRESS + 02H	EPP DATA PORT 2	BASE ADDRESS + 06H
EPP ADDR PORT	BASE ADDRESS + 03H	EPP DATA PORT 3	BASE ADDRESS + 07H

The bit map of these registers is:

	D0	D1	D2	D3	D4	D5	D6	D7	NOTE
DATA PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	1
STATUS PORT	TMOUT	0	0	nERR	SLCT	PE	nACK	nBUSY	1
CONTROL PORT	STROBE	AUTOFD	nINIT	SLC	IRQE	PCD	0	0	1
EPP ADDR PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 0	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 1	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 2	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 3	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2

Note 1: These registers are available in all modes.
Note 2: These registers are only available in EPP mode.

Table 7.1 - Parallel Port Connector

HOST CONNECTOR	SMSC PIN NUMBER	STANDARD	EPP	ECP
1	See section Chapter 3 Description of Pin Functions.	nSTROBE	nWrite	nStrobe
2-9		PD<0:7>	PData<0:7>	PData<0:7>
10		nACK	Intr	nAck
11		BUSY	nWait	Busy, PeriphAck(3)
12		PE	(User Defined)	PError, nAckReverse (3)
13		SLCT	(User Defined)	Select
14		nALF	nDatastb	nAutoFd, HostAck(3)
15		nERROR	(User Defined)	nFault (1) nPeriphRequest (3)
16		nINITP	nRESET	nInit(1) nReverseRqst(3)
17		nSLCTIN	nAddrstrb	nSelectIn(1,3)

(1) = Compatible Mode
(3) = High Speed Mode

Note: For the cable interconnection required for ECP support and the Slave Connector pin numbers, refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14, July 14, 1993. This document is available from Microsoft.

7.4 IBM XT/AT Compatible, Bi-Directional and EPP Modes

7.4.1 DATA PORT

ADDRESS OFFSET = 00H

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the internal data bus. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation in SPP mode, PD0 - PD7 ports are buffered (not latched) and output to the host CPU.

7.4.2 Status Port

ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of a read cycle. The bits of the Status Port are defined as follows:

BIT 0 TMOUT - TIME OUT

This bit is valid in EPP mode only and indicates that a 10 usec time out has occurred on the EPP bus. A logic O means that no time out error has occurred; a logic 1 means that a time out error has been detected. This bit is cleared by a RESET. If the TIMEOUT_SELECT bit (bit 4 of the Parallel Port Mode Register 2, 0xF1 in Serial Port Logical Device Configuration Registers) is '0', writing a one to this bit clears the TMOUT status bit. Writing a zero to this bit has no effect. If the TIMEOUT_SELECT bit (bit 4 of the Parallel Port Mode Register 2, 0xF1 in Serial Port Logical Device Configuration Registers) is '1', the TMOUT bit is cleared on the trailing edge of a read of the EPP Status Register.

BITS 1, 2 - are not implemented as register bits, during a read of the Printer Status Register these bits are a low level.

BIT 3 nERR – nERROR

The level on the nERROR input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic 1 means no error has been detected.

BIT 4 SLT - PRINTER SELECTED STATUS

The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic 1 means the printer is on line; a logic 0 means it is not selected.

BIT 5 PE - PAPER END

The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic 1 indicates a paper end; a logic 0 indicates the presence of paper.

BIT 6 nACK - ACKNOWLEDGE

The level on the nACK input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the printer has received a character and can now accept another. A logic 1 means that it is still processing the last character or has not received the data.

BIT 7 nBUSY - nBUSY

The complement of the level on the BUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic 1 means that it is ready to accept the next character.

7.4.3 CONTROL PORT

ADDRESS OFFSET = 02H

The Control Port is located at an offset of '02H' from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE

This bit is inverted and output onto the nSTROBE output.

BIT 1 AUTOFD - AUTOFEED

This bit is inverted and output onto the nAutoFd output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 nINIT - INITIATE OUTPUT

This bit is output onto the nINITP output without inversion.

BIT 3 SLCTIN - PRINTER SELECT INPUT

This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 IRQE - INTERRUPT REQUEST ENABLE

The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going nACK input. When the IRQE bit is programmed low the IRQ is disabled.

BIT 5 PCD - PARALLEL CONTROL DIRECTION

Parallel Control Direction is not valid in printer mode. In printer mode, the direction is always out regardless of the state of this bit. In bi-directional, EPP or ECP mode, a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

7.4.4 EPP ADDRESS PORT

ADDRESS OFFSET = 03H

The EPP Address Port is located at an offset of '03H' from the base address. The address register is cleared at initialization by RESET. During a WRITE operation, the contents of the internal data bus DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports. An LPC I/O write cycle causes an EPP ADDRESS WRITE cycle to be performed, during which the data is latched for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read. An LPC I/O read cycle causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the deassertion of ADDRSTB latches the PData for the duration of the read cycle. This register is only available in EPP mode.

7.4.5 EPP DATA PORT 0

ADDRESS OFFSET = 04H

The EPP Data Port 0 is located at an offset of '04H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the contents of the internal data bus DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports. An LPC I/O write cycle causes an EPP DATA WRITE cycle to be performed, during which the data is latched for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read. An LPC I/O read cycle causes an EPP READ

cycle to be performed and the data output to the host CPU, the deassertion of DATASTB latches the PData for the duration of the read cycle. This register is only available in EPP mode.

7.4.6 EPP DATA PORT 1

ADDRESS OFFSET = 05H

The EPP Data Port 1 is located at an offset of '05H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

7.4.7 EPP DATA PORT 2

ADDRESS OFFSET = 06H

The EPP Data Port 2 is located at an offset of '06H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

7.4.8 EPP DATA PORT 3

ADDRESS OFFSET = 07H

The EPP Data Port 3 is located at an offset of '07H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

7.5 EPP 1.9 Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle to nWAIT being deasserted (after command). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

During an EPP cycle, if STROBE is active, it overrides the EPP write signal forcing the PDx bus to always be in a write mode and the nWRITE signal to always be asserted.

7.5.1 Software Constraints

Before an EPP cycle is executed, the software must ensure that the control register bit PCD is a logic "0" (i.e., a 04H or 05H should be written to the Control port). If the user leaves PCD as a logic "1", and attempts to perform an EPP write, the chip is unable to perform the write (because PCD is a logic "1") and will appear to perform an EPP read on the parallel bus, no error is indicated.

7.6 EPP 1.9 Write

The timing for a write operation (address or data) is shown in timing diagram EPP Write Data or Address cycle. The chip inserts wait states into the LPC I/O write cycle until it has been determined that the write cycle can complete. The write cycle can complete under the following circumstances:

1. If the EPP bus is not ready (nWAIT is active low) when nDATASTB or nADDRSTB goes active then the write can complete when nWAIT goes inactive high.
2. If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of nDATASTB, nWRITE or nADDRSTB. The write can complete once nWAIT is determined inactive.

Write Sequence of operation

1. The host initiates an I/O write cycle to the selected EPP register.
2. If WAIT is not asserted, the chip must wait until WAIT is asserted.
3. The chip places address or data on PData bus, clears PDIR, and asserts nWRITE.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
5. Peripheral deasserts nWAIT, indicating that any setup requirements have been satisfied and the chip may begin the termination phase of the cycle.
6. a) The chip deasserts nDATASTB or nADDRSTRB, this marks the beginning of the termination phase. If it has not already done so, the peripheral should latch the information byte now.
   b) The chip latches the data from the internal data bus for the PData bus and drives the sync that indicates that no more wait states are required followed by the TAR to complete the write cycle.
7. Peripheral asserts nWAIT, indicating to the host that any hold time requirements have been satisfied and acknowledging the termination of the cycle.
8. Chip may modify nWRITE and nPDATA in preparation for the next cycle.

7.7 EPP 1.9 Read

The timing for a read operation (data) is shown in timing diagram EPP Read Data cycle. The chip inserts wait states into the LPC I/O read cycle until it has been determined that the read cycle can complete. The read cycle can complete under the following circumstances:

1. If the EPP bus is not ready (nWAIT is active low) when nDATASTB goes active then the read can complete when nWAIT goes inactive high.
2. If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of nWRITE or before nDATASTB goes active. The read can complete once nWAIT is determined inactive.

Read Sequence of Operation

1. The host initiates an I/O read cycle to the selected EPP register.
2. If WAIT is not asserted, the chip must wait until WAIT is asserted.
3. The chip tri-states the PData bus and deasserts nWRITE.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
5. Peripheral drives PData bus valid.
6. Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
7. a) The chip latches the data from the PData bus for the internal data bus and deasserts nDATASTB or nADDRSTRB. This marks the beginning of the termination phase.
   b) The chip drives the sync that indicates that no more wait states are required and drives valid data onto the LAD[3:0] signals, followed by the TAR to complete the read cycle.
8. Peripheral tri-states the PData bus and asserts nWAIT, indicating to the host that the PData bus is tri-stated.
9. Chip may modify nWRITE, PDIR and nPDATA in preparation for the next cycle.

7.8 EPP 1.7 Operation

When the EPP 1.7 mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle to the end of the cycle. If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

7.8.1 Software Constraints

Before an EPP cycle is executed, the software must ensure that the control register bits D0, D1 and D3 are set to zero. Also, bit D5 (PCD) is a logic “0” for an EPP write or a logic “1” for and EPP read.

7.9 EPP 1.7 Write

The timing for a write operation (address or data) is shown in timing diagram EPP 1.7 Write Data or Address cycle. The chip inserts wait states into the I/O write cycle when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The write cycle can complete when nWAIT is inactive high.

Write Sequence of Operation

1. The host sets PDIR bit in the control register to a logic “0”. This asserts nWRITE.
2. The host initiates an I/O write cycle to the selected EPP register.
3. The chip places address or data on PData bus.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
5. If nWAIT is asserted, the chip inserts wait states into I/O write cycle until the peripheral deasserts nWAIT or a time-out occurs.
6. The chip drives the final sync, deasserts nDATASTB or nADDRSTRB and latches the data from the internal data bus for the PData bus.
7. Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

7.10 EPP 1.7 Read

The timing for a read operation (data) is shown in timing diagram EPP 1.7 Read Data cycle. The chip inserts wait states into the I/O read cycle when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The read cycle can complete when nWAIT is inactive high.

Read Sequence of Operation

1. The host sets PDIR bit in the control register to a logic “1”. This deasserts nWRITE and tri-states the PData bus.
2. The host initiates an I/O read cycle to the selected EPP register.
3. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
4. If nWAIT is asserted, the chip inserts wait states into the I/O read cycle until the peripheral deasserts nWAIT or a time-out occurs.
5. The Peripheral drives PData bus valid.
6. The Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
7. The chip drives the final sync and deasserts nDATASTB or nADDRSTRB.
8. Peripheral tri-states the PData bus.

9. Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

Table 7.2 - EPP Pin Descriptions

EPP SIGNAL	EPP NAME	TYPE	EPP DESCRIPTION
nWRITE	nWrite	O	This signal is active low. It denotes a write operation.
PD<0:7>	Address/Data	I/O	Bi-directional EPP byte wide address and data bus.
INTR	Interrupt	I	This signal is active high and positive edge triggered. (Pass through with no inversion, Same as SPP).
nWAIT	nWait	I	This signal is active low. It is driven inactive as a positive acknowledgement from the device that the transfer of data is completed. It is driven active as an indication that the device is ready for the next transfer.
nDATASTB	nData Strobe	O	This signal is active low. It is used to denote data read or write operation.
nRESET	nReset	O	This signal is active low. When driven active, the EPP device is reset to its initial operational mode.
nADDRSTB	Address Strobe	O	This signal is active low. It is used to denote address read or write operation.
PE	Paper End	I	Same as SPP mode.
SLCT	Printer Selected Status	I	Same as SPP mode.
nERR	Error	I	Same as SPP mode.

Note 1: SPP and EPP can use 1 common register.
Note 2: nWrite is the only EPP output that can be over-ridden by SPP control port during an EPP cycle. For correct EPP read cycles, PCD is required to be a low.

7.10.1 Extended Capabilities Parallel Port

ECP provides a number of advantages, some of which are listed below. The individual features are explained in greater detail in the remainder of this section.

High performance half-duplex forward and reverse channel Interlocked handshake, for fast reliable transfer Optional single byte RLE compression for improved throughput (64:1) Channel addressing for low-cost peripherals Maintains link and data layer separation Permits the use of active output drivers permits the use of adaptive signal timing Peer-to-peer capability.

7.10.2 Vocabulary

The following terms are used in this document:

assert: When a signal asserts it transitions to a "true" state, when a signal deasserts it transitions to a "false" state.
forward: Host to Peripheral communication.
reverse: Peripheral to Host communication
Pword: A port word; equal in size to the width of the LPC interface. For this implementation, PWord is always 8 bits.
1 A high level.
0 A low level.

These terms may be considered synonymous:

PeriphClk, nAck
HostAck, nAutoFd
PeriphAck, Busy
nPeriphRequest, nFault
nReverseRequest, nInit
nAckReverse, PError
Xflag, Select
ECPMode, nSelectIn
HostClk, nStrobe

Reference Document: IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev 1.14, July 14, 1993. This document is available from Microsoft.

The bit map of the Extended Parallel Port registers is:

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
dsr	nBusy	nAck	PError	Select	nFault	0	0	0	1
dcr	0	0	Direction	ackIntEn	SelectIn	nInit	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	Parallel Port IRQ			Parallel Port DMA			
ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Note 1: These registers are available in all modes.
Note 2: All FIFOs use one common 16 byte FIFO.
Note 3: The ECP Parallel Port Config Reg B reflects the IRQ and DMA channel selected by the Configuration Registers.

7.11 ECP Implementation Standard

This specification describes the standard interface to the Extended Capabilities Port (ECP). All LPC devices supporting ECP must meet the requirements contained in this section or the port will not be supported by Microsoft. For a description of the ECP Protocol, please refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14, July 14, 1993. This document is available from Microsoft.

7.11.1 Description

The port is software and hardware compatible with existing parallel ports so that it may be used as a standard LPT port if ECP is not required. The port is designed to be simple and requires a small number of gates to implement. It does not do any “protocol” negotiation, rather it provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward and reverse directions.

Small FIFOs are employed in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes deep. The port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The port also supports run length encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. Hardware support for compression is optional.

Table 7.3 - ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
nStrobe	O	During write operations nStrobe registers data or address into the slave on the asserting edge (handshakes with Busy).
PData 7:0	I/O	Contains address or data or RLE data.
nAck	I	Indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
PeriphAck (Busy)	I	This signal deasserts to indicate that the peripheral can accept data. This signal handshakes with nStrobe in the forward direction. In the reverse direction this signal indicates whether the data lines contain ECP command information or data. The peripheral uses this signal to flow control in the forward direction. It is an “interlocked” handshake with nStrobe. PeriphAck also provides command information in the reverse direction.
PError (nAckReverse)	I	Used to acknowledge a change in the direction the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. It is an “interlocked” handshake with nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select	I	Indicates printer on line.
nAutoFd (HostAck)	O	Requests a byte of data from the peripheral when asserted, handshaking with nAck in the reverse direction. In the forward direction this signal indicates whether the data lines contain ECP address or data. The host drives this signal to flow control in the reverse direction. It is an “interlocked” handshake with nAck. HostAck also provides command information in the forward phase.
nFault (nPeriphRequest)	I	Generates an error interrupt when asserted. This signal provides a mechanism for peer-to-peer communication. This signal is valid only in the forward direction. During ECP Mode the peripheral is permitted (but not required) to drive this pin low to request a reverse transfer. The request is merely a “hint” to the host; the host has ultimate control over the transfer direction. This signal would be typically used to generate an interrupt to the host CPU.
nInit	O	Sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. The peripheral is only allowed to drive the bi-directional data bus while in ECP Mode and HostAck is low and nSelectIn is high.
nSelectIn	O	Always deasserted in ECP mode.

7.12 Register Definitions

The register definitions are based on the standard IBM addresses for LPT. All of the standard printer ports are supported. The additional registers attach to an upper bit decode of the standard LPT port definition to avoid conflict with standard ISA devices. The port is equivalent to a generic parallel port interface and may be operated in that mode. The port registers vary depending on the mode field in the ecr. The table below lists these dependencies. Operation of the devices in modes other than those specified is undefined.

Table 7.4 - ECP Register Definitions

NAME	ADDRESS (Note 1)	ECP MODES	FUNCTION
data	+000h R/W	000-001	Data Register
ecpAFifo	+000h R/W	011	ECP FIFO (Address)
dsr	+001h R/W	All	Status Register
dcr	+002h R/W	All	Control Register
cFifo	+400h R/W	010	Parallel Port Data FIFO
ecpDFifo	+400h R/W	011	ECP FIFO (DATA)
tFifo	+400h R/W	110	Test FIFO
cnfgA	+400h R	111	Configuration Register A
cnfgB	+401h R/W	111	Configuration Register B
ecr	+402h R/W	All	Extended Control Register

Note 1: These addresses are added to the parallel port base address as selected by configuration register or jumpers.
Note 2: All addresses are qualified with AEN. Refer to the AEN pin definition.

Table 7.5 - Mode Descriptions

MODE	DESCRIPTION*
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the configuration registers)
101	Reserved
110	Test mode
111	Configuration mode

*Refer to ECR Register Description

7.12.1 DATA and ecpAFifo PORT

ADDRESS OFFSET = 00H

Modes 000 and 001 (Data Port)

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.

Mode 011 (ECP FIFO - Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is only defined for the forward direction (direction is 0). Refer to the ECP Parallel Port Forward Timing Diagram, located in the Timing Diagrams section of this datasheet .

7.12.2 DEVICE STATUS REGISTER (dsr)

ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. Bits0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

BIT 3 nFault

The level on the nFault input is read by the CPU as bit 3 of the Device Status Register.

BIT 4 Select

The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

BIT 5 PError

The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

BIT 6 nAck

The level on the nAck input is read by the CPU as bit 6 of the Device Status Register.

BIT 7 nBusy

The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

7.12.3 DEVICE CONTROL REGISTER (dcr)

ADDRESS OFFSET = 02H

The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE

This bit is inverted and output onto the nSTROBE output.

BIT 1 AUTOFD - AUTOFEED

This bit is inverted and output onto the nAutoFd output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 nINIT - INITIATE OUTPUT

This bit is output onto the nINITP output without inversion.

BIT 3 SELECTIN

This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 ackIntEn - INTERRUPT REQUEST ENABLE

The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due to a low to high transition on the nACK input. Refer to the description of the interrupt under Operation, Interrupts.

BIT 5 DIRECTION

If mode=000 or mode=010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, Direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

BITS 6 and 7 during a read are a low level, and cannot be written.

7.12.4 CFIFO (Parallel Port Data FIFO)

ADDRESS OFFSET = 400h

Mode = 010

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

7.12.5 ECPDFIFO (ECP Data FIFO)

ADDRESS OFFSET = 400H

Mode = 011

Bytes written or DMAed from the system to this FIFO, when the direction bit is 0, are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

Data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO when the direction bit is 1. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

7.12.6 tFifo (Test FIFO Mode)

ADDRESS OFFSET = 400H

Mode = 110

Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO will not be transmitted to the to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port data lines.

The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full tFIFO, the new data is not accepted into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance metrics.

The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and serviceIntr bits.

The writeIntrThreshold can be determined by starting with a full tFIFO, setting the direction bit to 0 and emptying it a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntrThreshold can be determined by setting the direction bit to 1 and filling the empty tFIFO a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of tFIFO regardless of the value of the direction bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as was written.

7.12.7 cnfgA (Configuration Register A)

ADDRESS OFFSET = 400H

Mode = 111
This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation. (PWord = 1 byte)

7.12.8 cnfgB (Configuration Register B)

ADDRESS OFFSET = 401H
Mode = 111

BIT 7 compress

This bit is read only. During a read it is a low level. This means that this chip does not support hardware RLE compression. It does support hardware de-compression.

BIT 6 intrValue

Returns the value of the interrupt to determine possible conflicts.

BIT [5:3] Parallel Port IRQ (read-only)

to Table 7.7

BITS [2:0] Parallel Port DMA (read-only)

to Table 7.8

7.12.9 ecr (Extended Control Register)

ADDRESS OFFSET = 402H
Mode = all
This register controls the extended ECP parallel port functions.

BITS 7,6,5

These bits are Read/Write and select the Mode.

BIT 4 nErrIntrEn

Read/Write (Valid only in ECP Mode)
1: Disables the interrupt generated on the asserting edge of nFault.
0: Enables an interrupt pulse on the high to low edge of nFault. Note that an interrupt will be generated if nFault is asserted (interrupting) and this bit is written from a 1 to a 0. This prevents interrupts from being lost in the time between the read of the ecr and the write of the ecr.

BIT 3 dmaEn

Read/Write
1: Enables DMA (DMA starts when serviceIntr is 0).
0: Disables DMA unconditionally.

BIT 2 serviceIntr

Read/Write
1: Disables DMA and all of the service interrupts.
0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred serviceIntr bit shall be set to a 1 by hardware. It must be reset to 0 to re-enable the interrupts. Writing this bit to a 1 will not cause an interrupt.

case dmaEn=1:
During DMA (this bit is set to a 1 when terminal count is reached).
case dmaEn=0 direction=0:
This bit shall be set to 1 whenever there are writeIntrThreshold or more bytes free in the FIFO.
case dmaEn=0 direction=1:
This bit shall be set to 1 whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

BIT 1 full

Read only
1: The FIFO cannot accept another byte or the FIFO is completely full.
0: The FIFO has at least 1 free byte.

BIT 0 empty

Read only
1: The FIFO is completely empty.
0: The FIFO contains at least 1 byte of data.

Table 7.6 - Extended Control Register

R/W	MODE
000:	Standard Parallel Port Mode . In this mode the FIFO is reset and common drain drivers are used on the control lines (nStrobe, nAutoFd, nInit and nSelectIn). Setting the direction bit will not tri-state the output drivers in this mode.
001:	PS/2 Parallel Port Mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull).
010:	Parallel Port FIFO Mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).
011:	ECP Parallel Port Mode. In the forward direction (direction is 0) bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (direction is 1) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. All drivers have active pull-ups (push-pull).
100:	Selects EPP Mode: In this mode, EPP is selected if the EPP supported option is selected in Parallel Port configuration register CRF0. All drivers have active pull-ups (push-pull).
101:	Reserved
110:	Test Mode. In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull).
111:	Configuration Mode. In this mode the confgA, confgB registers are accessible at 0x400 and 0x401. All drivers have active pull-ups (push-pull).

Table 7.7 – Programming for Configuration Register B (Bits 5:3)

IRQ SELECTED	CONFIG REG B BITS 5:3
15	110
14	101
11	100
10	011
9	010
7	001
5	111
All Others	000

Table 7.8 – Programming for Configuration Register B (Bits 2:0)

DMA SELECTED	CONFIG REG B BITS 2:0
3	011
2	010
1	001
All Others	000

7.13 Operation

7.13.1 Mode Switching/Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

Once in an extended forward mode the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case all control signals will be deasserted before the mode switch. In an ecp reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001. Since the automatic hardware ecp reverse handshake only cares about the state of the FIFO it may have acquired extra data which will be discarded. It may in fact be in the middle of a transfer when the mode is changed back to 000 or 001. In this case the port will deassert nAutoFd independent of the state of the transfer. The design shall not cause glitches on the handshake signals if the software meets the constraints above.

7.14 ECP Operation

Prior to ECP operation the Host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol. This is a somewhat complex negotiation carried out under program control in mode 000.

After negotiation, it is necessary to initialize some of the port bits. The following are required:

Set Direction = 0, enabling the drivers.

Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo respectively.

Note that all FIFO data transfers are byte wide and byte aligned. Address/RLE transfers are byte-wide and only allowed in the forward direction.

The host may switch directions by first switching to mode = 001, negotiating for the forward or reverse channel, setting direction to 1 or 0, then setting mode = 011. When direction is 1 the hardware shall handshake for each ECP read data byte and attempt to fill the FIFO. Bytes may then be read from the ecpDFifo as long as it is not empty.

ECP transfers may also be accomplished (albeit slowly) by handshaking individual bytes under program control in mode = 001, or 000.

7.15 Termination from ECP Mode

Termination from ECP Mode is similar to the termination from Nibble/Byte Modes. The host is permitted to terminate from ECP Mode only in specific well-defined states. The termination can only be executed while the bus is in the forward direction. To terminate while the channel is in the reverse direction, it must first be transitioned into the forward direction.

7.16 Command/Data

ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8 bit data or 8 bit commands.

When in the forward direction, normal data is transferred when HostAck is high and an 8 bit command is transferred when HostAck is low.

The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.

When in the reverse direction, normal data is transferred when PeriphAck is high and an 8 bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero. Reverse channel addresses are seldom used and may not be supported in hardware.

Table 7.9 - Channel/Data Commands supported in ECP mode

Forward Channel Commands (HostAck Low)
Reverse Channel Commands (PeripAck Low)

D7	D[6:0]
0	Run-Length Count (0-127) (mode 0011 0X00 only)
1	Channel Address (0-127)

7.17 Data Compression

The ECP port supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

7.18 Pin Definition

The drivers for nStrobe, nAutoFd, nInit and nSelectIn are open-drain in mode 000 and are push-pull in all other modes.

7.19 LPC Connections

The interface can never stall causing the host to hang. The width of data transfers is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the next section). Single byte wide transfers are always possible with standard or PS/2 mode using program control of the control signals.

7.20 Interrupts

The interrupts are enabled by serviceIntr in the ecr register.
serviceIntr = 1 Disables the DMA and all of the service interrupts.

serviceIntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupts generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

An interrupt is generated when:

1) For DMA transfers: When serviceIntr is 0, dmaEn is 1 and the DMA TC cycle is received.
2) For Programmed I/O:
   a) When serviceIntr is 0, dmaEn is 0, direction is 0 and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are writeIntrThreshold or more free bytes in the FIFO.
   b) When serviceIntr is 0, dmaEn is 0, direction is 1 and there are readIntrThreshold or more bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are readIntrThreshold or more bytes in the FIFO.

3) When nErrIntrEn is 0 and nFault transitions from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.
4) When ackIntEn is 1 and the nAck signal transitions from a low to a high.

7.21 FIFO Operation

The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or DMA cycle depending on the selection of DMA or Programmed I/O mode.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a "fast" system. A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

7.21.1 DMA TRANSFERS

DMA transfers are always to or from the ecpDFifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to 1 and serviceIntr to 0. The ECP requests DMA transfers from the host by encoding the nLDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests a DMA cycle shall not be requested for more than 32 DMA cycles in a row. The FIFO is enabled directly by the host initiating a DMA cycle for the requested channel, and addresses need not be valid. An interrupt is generated when a TC cycle is received. (Note: The only way to properly terminate DMA transfers is with a TC cycle.)

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting serviceIntr to 1, followed by setting dmaEn to 0, and waiting for the FIFO to become empty or full. Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to 1, followed by setting serviceIntr to 0.

7.21.2 DMA Mode - Transfers from the FIFO to the Host

(**Note**: In the reverse mode, the peripheral may not continue to fill the FIFO if it runs out of data to transfer, even if the chip continues to request more data from the peripheral.)

The ECP requests a DMA cycle whenever there is data in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The ECP stops requesting DMA cycles when the FIFO becomes empty or when a TC cycle is received, indicating that no more data is required. If the ECP stops requesting DMA cycles due to the FIFO going empty, then a DMA cycle is requested again as soon as there is one byte in the FIFO. If the ECP stops requesting DMA cycles due to the TC cycle, then a DMA cycle is requested again when there is one byte in the FIFO, and serviceIntr has been re-enabled.

7.21.3 Programmed I/O Mode or Non-DMA Mode

The ECP or parallel port FIFOs may also be operated using interrupt driven programmed I/O. Software can determine the writeIntrThreshold, readIntrThreshold, and FIFO depth by accessing the FIFO in Test Mode.

Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. To use the programmed I/O transfers, the host first sets up the direction and state, sets dmaEn to 0 and serviceIntr to 0.

The ECP requests programmed I/O transfers from the host by activating the interrupt. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

Note: A threshold of 16 is equivalent to a threshold of 15. These two cases are treated the same.

7.21.4 Programmed I/O - Transfers from the FIFO to the Host

In the reverse direction an interrupt occurs when serviceIntr is 0 and readIntrThreshold bytes are available in the FIFO. If at this time the FIFO is full it can be emptied completely in a single burst, otherwise readIntrThreshold bytes may be read from the FIFO in a single burst.

readIntrThreshold =(16-<threshold>) data bytes in FIFO

An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is greater than or equal to (16-<threshold>). (If the threshold = 12, then the interrupt is set whenever there are 4-16 bytes in the FIFO). The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. If at this time the FIFO is full, it can be completely emptied in a single burst, otherwise a minimum of (16-<threshold>) bytes may be read from the FIFO in a single burst.

7.21.5 Programmed I/O - Transfers from the Host to the FIFO

In the forward direction an interrupt occurs when serviceIntr is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with writeIntrThreshold bytes.

writeIntrThreshold = (16-<threshold>) free bytes in FIFO

An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is less than or equal to <threshold>. (If the threshold = 12, then the interrupt is set whenever there are 12 or less bytes of data in the FIFO.) The host must respond to the request by writing data to the FIFO. If at this time the FIFO is empty, it can be completely filled in a single burst, otherwise a minimum of (16-<threshold>) bytes may be written to the FIFO in a single burst. This process is repeated until the last byte is transferred into the FIFO.

7.22 Power Management

Direct power management capability is provided for the following logical devices: floppy disk, UART, and the parallel port. Direct power management is controlled by CR22. Refer to CR22 in Table 11.3 for more information.

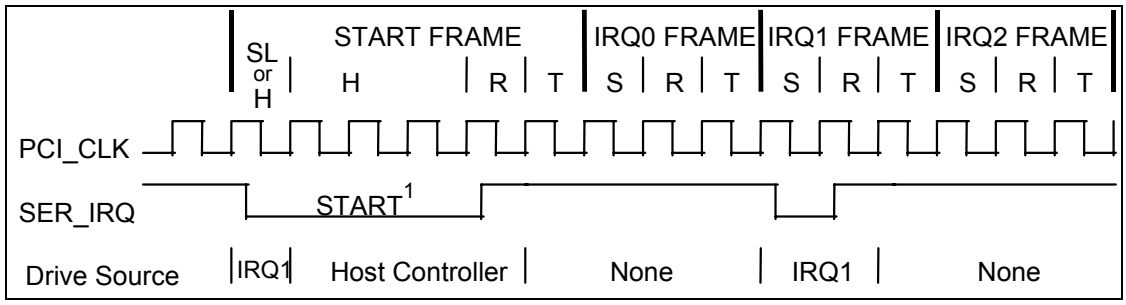
Note on FDC Direct Powerdown: The Direct powerdown mode requires at least 8us delay at 250K bits/sec configuration and 4us delay at 500K bits/sec. The delay should be added so that the internal microcontroller can prepare itself to accept commands.

7.23 Serial IRQ

The LPC47M182 supports the serial interrupt to transmit interrupt information to the host system. The serial interrupt scheme adheres to the Serial IRQ Specification for PCI Systems, Version 6.0.

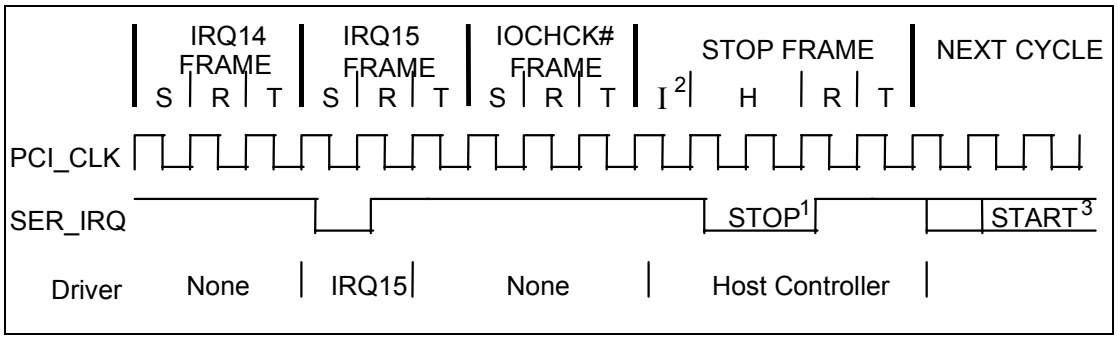
7.23.1 Timing Diagrams For SER_IRQ Cycle

A) Start Frame timing with source sampled a low pulse on IRQ1



Note: H=Host Control; R=Recovery; T=Turn-Around; SL=Slave Control; S=Sample
Note 1: Start Frame pulse can be 4-8 clocks wide depending on the location of the device in the PCI bridge hierarchy in a synchronous bridge design.

B) Stop Frame Timing with Host using 17 SER_IRQ sampling period



Note: H=Host Control; R=Recovery; T=Turn-Around; S=Sample; I=Idle
Note 1: The next SER_IRQ cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.
Note 2: There may be none, one or more Idle states during the Stop Frame.
Note 3: Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.

7.23.2 SER_IRQ Cycle Control

There are two modes of operation for the SER_IRQ Start Frame:

1) Quiet (Active) Mode: Any device may initiate a Start Frame by driving the SER_IRQ low for one clock, while the SER_IRQ is Idle. After driving low for one clock the SER_IRQ must immediately be tri-stated without at any time driving high. A Start Frame may not be initiated while the SER_IRQ is Active. The SER_IRQ is Idle between Stop and Start Frames. The SER_IRQ is Active between Start and Stop Frames. This mode of operation allows the SER_IRQ to be Idle when there are no IRQ/Data transitions which should be most of the time.

Once a Start Frame has been initiated the Host Controller will take over driving the SER_IRQ low in the next clock and will continue driving the SER_IRQ low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the Host Controller will drive the SER_IRQ back high for one clock, then tri-state.

If LPC47M182 detects any transition on an IRQ/Data line for which it is responsible, it initiates a Start Frame in order to update the Host Controller unless the SER_IRQ is already in an SER_IRQ Cycle and the IRQ/Data transition can be delivered in that SER_IRQ Cycle

2) Continuous (Idle) Mode: Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other SER_IRQ agents become passive and may not initiate a Start Frame. SER_IRQ will be driven low for four to eight clocks by Host Controller. This mode has two functions. It can be used to stop or idle the SER_IRQ or the Host Controller can operate SER_IRQ in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An SER_IRQ mode transition can only occur during the Stop Frame. Upon reset, SER_IRQ bus is defaulted to Continuous mode, therefore only the Host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next SER_IRQ Cycle's mode.

7.23.3 SER_IRQ Data Frame

Once a Start Frame has been initiated, the LPC47M182 will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the Sample phase the LPC47M182 drives the SER_IRQ low, if and only if, its last detected IRQ/Data value was low. If its detected IRQ/Data value is high, SER_IRQ is left tri-stated. During the Recovery phase the LPC47M182 drives the SER_IRQ high, if and only if, it had driven the SER_IRQ low during the previous Sample Phase. During the Turn-around Phase the LPC47M182 tri-states the SER_IRQ. The LPC47M182 drives the SER_IRQ line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the Start Frame.

The Sample Phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one. (e.g. The IRQ5 Sample clock is the sixth IRQ/Data Frame, (6 x 3) - 1 = 17th clock after the rising edge of the Start Pulse).

SER_IRQ Sampling Periods

SER_IRQ PERIOD	SIGNAL SAMPLED	# OF CLOCKS PAST START
1	Not Used	2
2	IRQ1	5
3	IRQ2	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47

SER_IRQ Period 14 is used to transfer IRQ13. Logical devices FDC, Parallel Port, Serial Port, and Keyboard have IRQ13 as a choice for their primary interrupt.

7.23.4 Stop Cycle Control

Once all IRQ/Data Frames have completed the Host Controller will terminate SER_IRQ activity by initiating a Stop Frame. Only the Host Controller can initiate the Stop Frame. A Stop Frame is indicated when the SER_IRQ is low for two or three clocks. If the Stop Frame's low time is two clocks then the next SER_IRQ Cycle's sampled mode is the Quiet mode; and any SER_IRQ device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks then the next SER_IRQ Cycle's sampled mode is the Continuos mode; and only the Host Controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

7.23.5 Latency

Latency for IRQ/Data updates over the SER_IRQ bus in bridge-less systems with the minimum Host supported IRQ/Data Frames of seventeen, will range up to 96 clocks (3.84μS with a 25MHz PCI Bus or 2.88uS with a 33MHz PCI Bus). If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

7.23.6 EOI/ISR Read Latency

Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the SER_IRQ Cycle latency in order to ensure that these events do not occur out of order.

7.23.7 AC/DC Specification Issue

All SER_IRQ agents must drive / sample SER_IRQ synchronously related to the rising edge of PCI bus clock. The SER_IRQ pin uses the electrical specification of PCI bus. Electrical parameters will follow PCI spec. section 4, sustained tri-state.

7.23.8 Reset and Initialization

The SER_IRQ bus uses nPCI_RESET as its reset signal. The SER_IRQ pin is tri-stated by all agents while nPCI_RESET is active. With reset, SER_IRQ Slaves are put into the (continuous) IDLE mode. The Host Controller is responsible for starting the initial SER_IRQ Cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent SER_IRQ Cycles. It is Host Controller's responsibility to provide the default values to 8259's and other system logic before the first SER_IRQ Cycle is performed. For SER_IRQ system suspend, insertion, or removal application, the Host controller should be programmed into Continuous (IDLE) mode first. This is to guarantee SER_IRQ bus is in IDLE state before the system configuration changes.

7.24 Interrupt Generating Registers

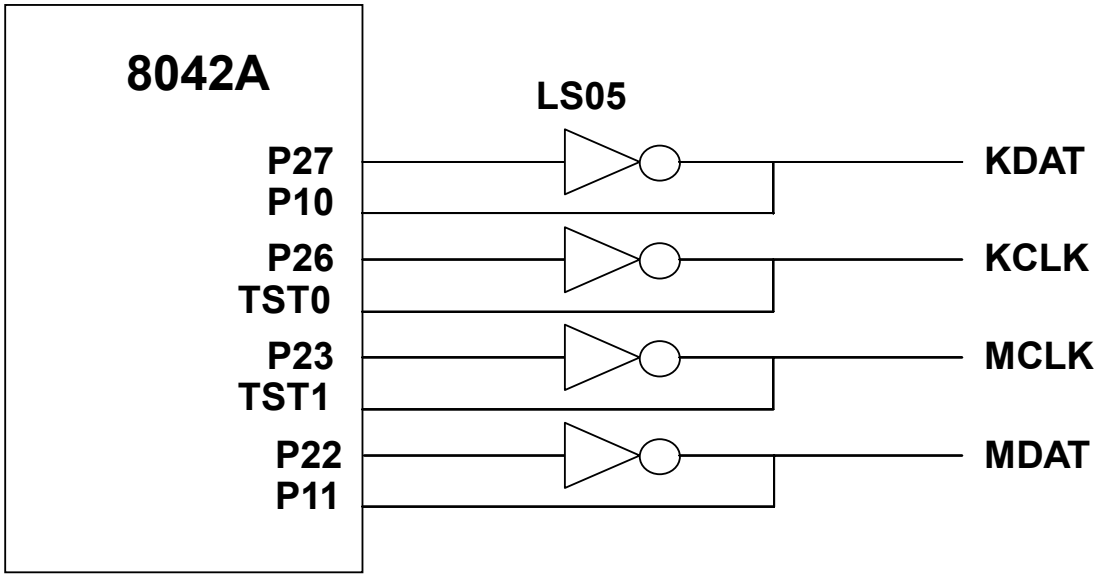
The LPC47M182 contains on-chip Interrupt Generating Registers to enable external software to generate IRQ1 through IRQ15 on the Serial IRQ Interface. These registers, INT_GEN1 and INT_GEN2, are located at offsets 0x1B and 0x1C, respectively, in the in the Power Control Logical Device, when LD_NUM=0, or Runtime Register Block Logical Device, when LD_NUM=1, from the base address setting (set at Index 0x60 and 0x61 Configuration Registers). See "Power Control Runtime Registers" and "Runtime Register Block Runtime Registers" sections.

Registers INT_GEN1 and INT_GEN2 are enabled to output to the Serial IRQ stream by setting Power Control Block Configuration Register, at Index 0xF1, Bit [0] to '1'. When Bit [0] is set to '0', INT_GEN1 and INT_GEN2 are prevented from outputting to the Serial IRQ stream.

Writing Bits 0 through 7 to '0' in registers INT_GEN1 and INT_GEN2 enable the corresponding interrupt (INT1 through INT15) to be asserted (made active) in the Serial IRQ stream. Producing an interrupt in the Serial IRQ stream by writing these bits to '0' overrides other interrupt sources for the Serial IRQ stream. No other functional logic in the LPC47M182 sets bits in these registers. The asserted interrupt in the Serial IRQ stream from registers INT_GEN1 and INT_GEN2 is removed by writing the corresponding bit to '1'.

7.25 8042 Keyboard Controller Description

The LPC47M182 is a Super I/O and Universal Keyboard Controller that is designed for intelligent keyboard management in desktop computer applications. The Universal Keyboard Controller uses an 8042 microcontroller CPU core. This section concentrates on the LPC47M182 enhancements to the 8042. For general information about the 8042, refer to the "Hardware Description of the 8042" in the 8-Bit Embedded Controller Handbook.



Keyboard and Mouse Interface

KIRQ is the Keyboard IRQ
MIRQ is the Mouse IRQ
Port 21 is used to create a GATEA20 signal from the LPC47M182.

7.25.1 Keyboard Interface

The LPC47M182 LPC interface is functionally compatible with the 8042 style host interface. It consists of the D0-7 data signals; the read and write signals and the Status register, Input Data register, and Output Data register. Table 7.10 shows how the interface decodes the control signals. In addition to the above signals, the host interface includes keyboard and mouse IRQs.

Table 7.10 - I/O Address Map

ADDRESS	COMMAND	BLOCK	FUNCTION (NOTE 1)
0x60	Write	KDATA	Keyboard Data Write (C/D=0)
	Read	KDATA	Keyboard Data Read
0x64	Write	KDCTL	Keyboard Command Write (C/D=1)
	Read	KDCTL	Keyboard Status Read

Note 1: These registers consist of three separate 8 bit registers. Status, Data/Command Write and Data Read.

7.25.2 Keyboard Data Write

This is an 8 bit write only register. When written, the C/D status bit of the status register is cleared to zero and the IBF bit is set.

7.25.3 Keyboard Data Read

This is an 8 bit read only register. If enabled by “ENABLE FLAGS”, when read, the KIRQ output is cleared and the OBF flag in the status register is cleared. If not enabled, the KIRQ and/or AUXOBF1 must be cleared in software.

7.25.4 Keyboard Command Write

This is an 8 bit write only register. When written, the C/D status bit of the status register is set to one and the IBF bit is set.

7.25.5 Keyboard Status Read

This is an 8 bit read only register. Refer to the description of the Status Register for more information.

7.25.6 CPU-to-Host Communication

The LPC47M182 CPU can write to the Output Data register via register DBB. A write to this register automatically sets Bit 0 (OBF) in the Status register. See Table 7.11.

Table 7.11 - Host Interface Flags

8042 INSTRUCTION	FLAG
OUT DBB	Set OBF, and, if enabled, the KIRQ output signal goes high

7.25.7 Host-to-CPU Communication

The host system can send both commands and data to the Input Data register. The CPU differentiates between commands and data by reading the value of Bit 3 of the Status register. When bit 3 is “1”, the CPU interprets the register contents as a command. When bit 3 is “0”, the CPU interprets the register contents as data. During a host write operation, bit 3 is set to “1” if SA2 = 1 or reset to “0” if SA2 = 0.

7.25.8 KIRQ

If “EN FLAGS” has been executed and P24 is set to a one: the OBF flag is gated onto KIRQ. The KIRQ signal can be connected to system interrupt to signify that the LPC47M182 CPU has written to the output data register via “OUT DBB,A”. If P24 is set to a zero, KIRQ is forced low. On power-up, after a valid RST pulse has been delivered to the device, KIRQ is reset to 0. KIRQ will normally reflects the status of writes “DBB”. (KIRQ is normally selected as IRQ1 for keyboard support.)

If “EN FLAGS” has not been executed: KIRQ can be controlled by writing to P24. Writing a zero to P24 forces KIRQ low; a high forces KIRQ high.

7.25.9 MIRQ

If “EN FLAGS” has been executed and P25 is set to a one:; IBF is inverted and gated onto MIRQ. The MIRQ signal can be connected to system interrupt to signify that the LPC47M182 CPU has read the DBB register. If “EN FLAGS” has not been executed, MIRQ is controlled by P25, Writing a zero to P25 forces MIRQ low, a high forces MIRQ high. (MIRQ is normally selected as IRQ12 for mouse support).

Gate A20

A general purpose P21 is used as a software controlled Gate A20 or user defined output.

8042 PINS

The 8042 functions P17, P16 and P12 are not supported in LPC47M182.

7.25.10 External Keyboard and Mouse Interface

Industry-standard PC-AT-compatible keyboards employ a two-wire, bidirectional TTL interface for data transmission. Several sources also supply PS/2 mouse products that employ the same type of interface. To facilitate system expansion, the LPC47M182 provides four signal pins that may be used to implement this interface directly for an external keyboard and mouse.

The LPC47M182 has four high-drive, open-drain output, bidirectional port pins that can be used for external serial interfaces, such as external keyboard and PS/2-type mouse interfaces. They are KCLK, KDAT, MCLK, and MDAT. P26 is inverted and output as KCLK. The KCLK pin is connected to TEST0. P27 is inverted and output as KDAT. The KDAT pin is connected to P10. P23 is inverted and output as MCLK. The MCLK pin is connected to TEST1. P22 is inverted and output as MDAT. The MDAT pin is connected to P11.

Note: External pull-ups may be required.

7.25.11 Keyboard Power Management

The keyboard provides support for two power-saving modes: soft powerdown mode and hard powerdown mode. In soft powerdown mode, the clock to the ALU is stopped but the timer/counter and interrupts are still active. In hard power down mode the clock to the 8042 is stopped.

7.25.12 Soft Power Down Mode

This mode is entered by executing a HALT instruction. The execution of program code is halted until either RESET is driven active or a data byte is written to the DBBIN register by a master CPU. If this mode is exited using the interrupt, and the IBF interrupt is enabled, then program execution resumes with a CALL to the interrupt routine, otherwise the next instruction is executed. If it is exited using RESET then a normal reset sequence is initiated and program execution starts from program memory location 0.

7.25.13 Hard Power Down Mode

This mode is entered by executing a STOP instruction. The oscillator is stopped by disabling the oscillator driver cell. When either RESET is driven active or a data byte is written to the DBBIN register by a master CPU, this mode will be exited (as above). However, as the oscillator cell will require an initialization time, either RESET must be held active for sufficient time to allow the oscillator to stabilize. Program execution will resume as above.

7.25.14 Interrupts

The LPC47M182 provides the two 8042 interrupts: IBF and the Timer/Counter Overflow.

7.25.15 Memory Configurations

The LPC47M182 provides 2K of on-chip ROM and 256 bytes of on-chip RAM.

7.25.16 Register Definitions

Host I/F Data Register

The Input Data register and Output Data register are each 8 bits wide. A write to this 8 bit register will load the Keyboard Data Read Buffer, set the OBF flag and set the KIRQ output if enabled. A read of this register will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag. Refer to the KIRQ and Status register descriptions for more information.

Host I/F Status Register

The Status register is 8 bits wide.

Table 7.12 shows the contents of the Status register.

Table 7.12 - Status Register

D7	D6	D5	D4	D3	D2	D1	D0
UD	UD	UD	UD	C/D	UD	IBF	OBF

Status Register

This register is cleared on a reset. This register is read-only for the Host and read/write by the LPC47M182 CPU.

UD Writable by LPC47M182 CPU. These bits are user-definable.

C/D (Command Data)-This bit specifies whether the input data register contains data or a command (0 = data, 1 = command). During a host data/command write operation, this bit is set to "1" if SA2 = 1 or reset to "0" if SA2 = 0.

IBF (Input Buffer Full)- This flag is set to 1 whenever the host system writes data into the input data register. Setting this flag activates the LPC47M182 CPU's nIBF (MIRQ) interrupt if enabled. When the LPC47M182 CPU reads the input data register (DBB), this bit is automatically reset and the interrupt is cleared. There is no output pin associated with this internal signal.

OBF (Output Buffer Full) - This flag is set to whenever the LPC47M182 CPU write to the output data register (DBB). When the host system reads the output data register, this bit is automatically reset.

7.25.17 External Clock Signal

The LPC47M182 Keyboard Controller clock source is a 12 MHz clock generated from a 14.318 MHz clock. The reset pulse must last for at least 24 16 MHz clock periods. The pulse-width requirement applies to both internally (Vcc POR) and externally generated reset signals. In powerdown mode, the external clock signal is not loaded by the chip.

7.25.18 Default Reset Conditions

The LPC47M182 has one source of hardware reset: an external reset via the nPCI_RESET pin. Refer to Table 7.13 for the effect of each type of reset on the internal registers.

Table 7.13 - Keyboard and Mouse Pin/Register Reset Values

DESCRIPTION	HARDWARE RESET (nPCI_RESET)
KCLK	Low
KDAT	Low
MCLK	Low
MDAT	Low
Host I/F Data Reg	N/A
Host I/F Status Reg	00H

N/A: Not Applicable

7.25.19 GATEA20 AND KEYBOARD RESET

The LPC47M182 provides two options for GateA20 and Keyboard Reset: 8042 Software Generated GateA20 and KRESET and Port 92 Fast GateA20 and KRESET.

7.26 Port 92 Fast Gatea20 and Keyboard Reset

7.26.1 Port 92 Register

This port can only be read or written if Port 92 has been enabled via bit 2 of the KRST_GA20 Register (Keyboard Logical Device, 0xF0) set to 1.

This register is used to support the alternate reset (nALT_RST) and alternate A20 (ALT_A20) functions.

Table 7.14 – Keyboard Port 92 Register

NAME	PORT 92
Location	92h
Default Value	24h
Attribute	Read/Write
Size	8 bits

PORT 92 REGISTER	
BIT	**FUNCTION**
7:6	Reserved. Returns 00 when read
5	Reserved. Returns a 1 when read
4	Reserved. Returns a 0 when read
3	Reserved. Returns a 0 when read
2	Reserved. Returns a 1 when read
1	ALT_A20 Signal control. Writing a 0 to this bit causes the ALT_A20 signal to be driven low. Writing a 1 to this bit causes the ALT_A20 signal to be driven high.
0	Alternate System Reset. This read/write bit provides an alternate system reset function. This function provides an alternate means to reset the system CPU to effect a mode switch from Protected Virtual Address Mode to the Real Address Mode. This provides a faster means of reset than is provided by the Keyboard controller. This bit is set to a 0 by a system reset. Writing a 1 to this bit will cause the nALT_RST signal to pulse active (low) for a minimum of 1 µs after a delay of 500 ns. Before another nALT_RST pulse can be generated, this bit must be written back to a 0.

Bit 0 of Port 92, which generates the nALT_RST signal, is used to reset the CPU under program control. This signal is AND'ed together with the reset signal (KRST) from the keyboard controller to provide a software means of resetting the CPU. This provides a faster means of reset than is provided by the keyboard controller. Writing a 1 to bit 0 in the Port 92 Register causes this signal to pulse low for a minimum of 6µs, after a delay of a minimum of 14µs. Before another nALT_RST pulse can be generated, bit 0 must be set to 0 either by a system reset of a write to Port 92. Upon reset, this signal is driven inactive high (bit 0 in the Port 92 Register is set to 0).

If Port 92 is enabled, i.e., bit 2 of KRST_GA20 is set to 1, then a pulse is generated by writing a 1 to bit 0 of the Port 92 Register and this pulse is AND'ed with the pulse generated from the 8042. This pulse is output on pin nKBDRST and its polarity is controlled by the GPI/O polarity configuration.

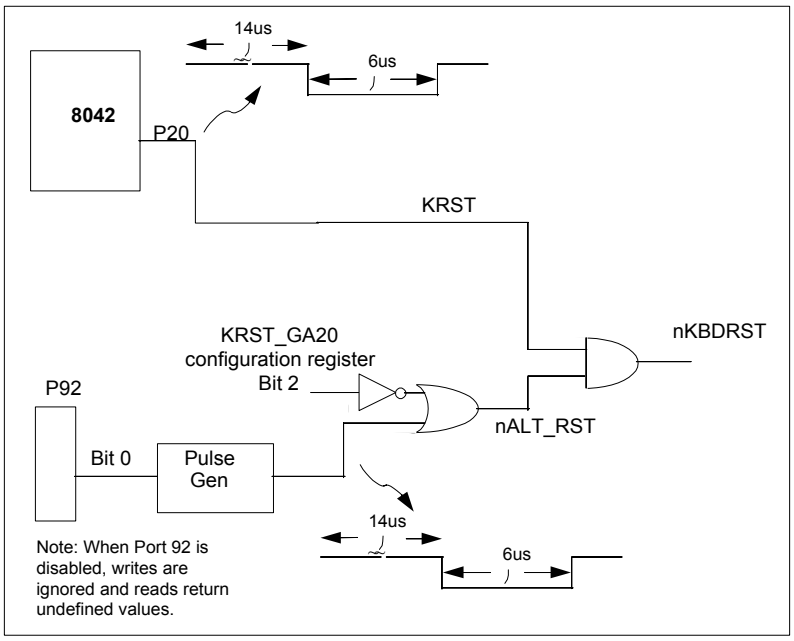


Figure 7.1 – NKBDRST Circuit

Bit 1 of Port 92, the ALT_A20 signal, is used to force nA20M to the CPU low for support of real mode compatible software. This signal is OR'ed with the A20GATE signal from the keyboard controller and nKBDRST to control the nA20M input of the CPU. Writing a 0 to bit 1 of the Port 92 Register forces ALT_A20 low. ALT_A20 low drives nA20M to the CPU low, if A20GATE from the keyboard controller is also low. Writing a 1 to bit 1 of the Port 92 Register forces ALT_A20 high. ALT_A20 high drives nA20M to the CPU high, regardless of the state of A20GATE from the keyboard controller. Upon reset, this signal is driven low.

Table 7.15 – nA20M Truth Table

8042 P21	ALT_A20	SYSTEM nA20M
0	0	0
0	1	1
1	0	1
1	1	1

Latches On Keyboard and Mouse IRQs

The implementation of the latches on the keyboard and mouse interrupts is shown below.

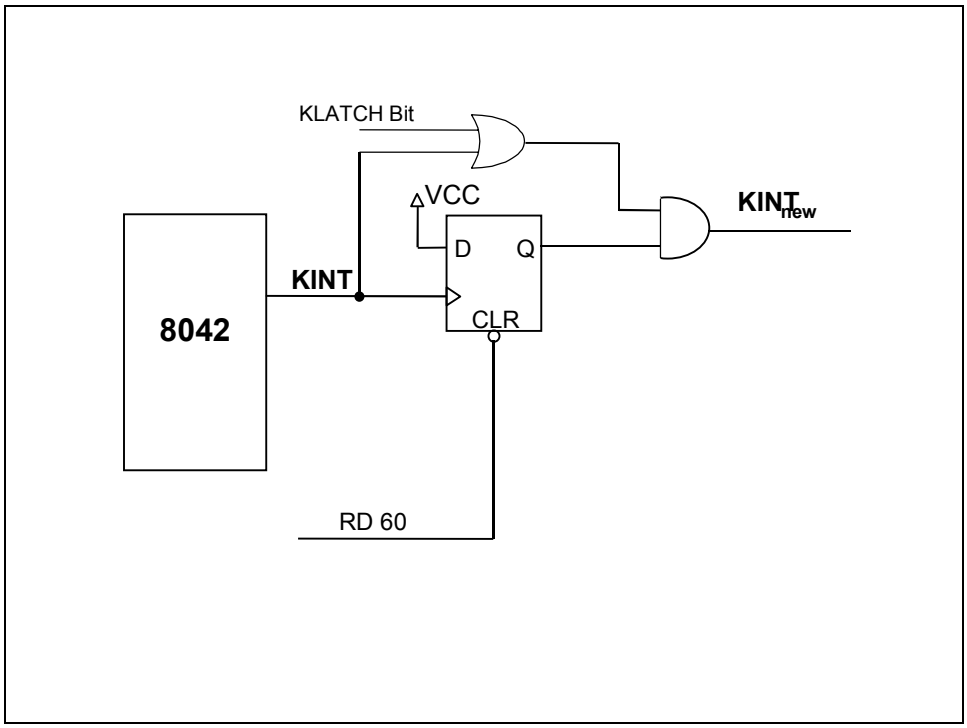


Figure 7.2 – Keyboard Latch

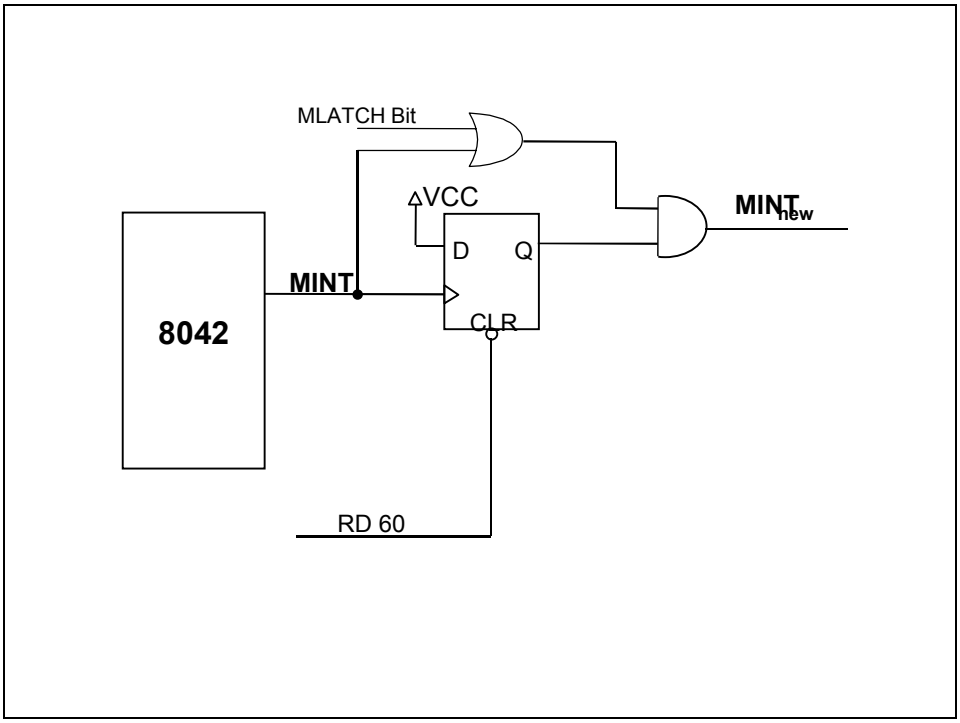


Figure 7.3 – Mouse Latch

The KLATCH and MLATCH bits are located in the KRST_GA20 register, in Keyboard Logical Device at 0xF0.

These bits are defined as follows:

Bit[4]: MLATCH – Mouse Interrupt latch control bit. 0=MINT is the 8042 MINT ANDed with Latched MINT (default), 1=MINT is the latched 8042 MINT.

Bit[3]: KLATCH – Keyboard Interrupt latch control bit. 0=KINT is the 8042 KINT ANDed with Latched KINT (default), 1=KINT is the latched 8042 KINT.

See the "Configuration" section for a description of this register.

7.26.2 Keyboard and Mouse PME Generation

The LPC47M182 sets the associated PME Status bits when the following conditions occur:

- Keyboard Interrupt
- Mouse Interrupt
- Active Edge on Keyboard Data Signal (KDAT)
- Active Edge on Mouse Data Signal (MDAT)

These events can cause a PME to be generated if the associated PME Wake Enable register bit and the global PME_EN bit are set. Refer to the PME Support section for more details on the PME interface logic and refer to the "Power Control Runtime Registers" and "Runtime Register Block Runtime Registers" sections for details on the PME Status and Enable registers.

The keyboard interrupt and mouse interrupt PMEs can be generated when the part is powered by VCC. The keyboard data and mouse data PMEs can be generated both when the part is powered by VCC, and when the part is powered by VTR (VCC=0).

When using the keyboard and mouse data signals for wakeup, it may be necessary to isolate the keyboard signals (KCLK, KDAT, MCLK, MDAT) from the 8042 prior to entering certain system sleep states. This is due to the fact that the normal operation of the 8042 can prevent the system from entering a sleep state or trigger false PME events. The LPC47M182 has a mode to select the isolation of keyboard and mouse clock and data signals by hardware when the nLPCPD signal is active and/or when the isolation bits are set by software. The mode allows the keyboard and mouse data signals to go into the wakeup logic but block the clock and data signals from the 8042. The mode may be used anytime it is necessary to isolate the 8042 keyboard and mouse signals from the 8042 before entering a system sleep state. This mode applies to ANYKEY wakeup from S3, but it does not affect wake from S1. The mode is selected by ISO_MODE bit in the Keyboard logical device configuration register 0xF0. The ISO_MODE bit is defined as follows:

Bit[7] ISO_MODE in KRST_GA20 register (0xF0)
0: Mode 1 (default) – Isolate the 8042 in hardware while the nLPCPD signal is active OR when the Keyboard and Mouse isolation bits are set by software.
1: Mode 2 – Keyboard and mouse isolation bits set by software only. (Note: the input path to the 8042 is also isolated while the nLPCPD signal is active.)

The bits used to isolate the keyboard and mouse signals from the 8042 are located in Keyboard Logical Device, Register 0xF0 (KRST_GA20) and are defined below. These bits reset on VTR POR only.

Bit[6] M_ISO. Enables/disables isolation of mouse signals into 8042. Does not affect the MDAT signal to the mouse wakeup (PME) logic.
1=block mouse clock and data signals into 8042
0= do not block mouse clock and data signals into 8042

Bit[5] K_ISO. Enables/disables isolation of keyboard signals into 8042. Does not affect the KDAT signal to the keyboard wakeup (PME) logic.
1=block keyboard clock and data signals into 8042
0= do not block keyboard clock and data signals into 8042

See the SMSC Application Note titled "Using the Enhanced Keyboard and Mouse Wakeup Feature in SMSC Super I/O Parts" for more information on isolation bits.

If either of the isolation bits (M_ISO, K_SIO) is set prior to entering a sleep state where VCC goes inactive (S3-S5), then the 8042 must be reset upon exiting the sleep mode. Write 0x40 to global configuration register 0x2C to reset the 8042. The 8042 must then be taken out of reset by writing 0x00 to register 0x2C since the bit that resets the 8042 is not self-clearing. Caution: Bit 6 of configuration register 0x2C is used to put the 8042 into reset - do not set any of the other bits in register 0x2C, as this may produce undesired results.

It is not necessary to reset the 8042 if the isolation bits are used for a sleep state where VCC does not go inactive (S1, S2).

Note: It not necessary to reset the 8042 when ISO_MODE bit is set to '0', and M_ISO and K_ISO isolation bit are not set. This is because nLPCPD goes inactive high (it will remove isolation of the signals when system sleep state is exited) prior to nPCI_RESET going inactive high. The nPCI_RESET going inactive high resets the 8042.

User Note Regarding External Keyboard and Mouse:

This is an application matter resulting from the behavior of the external 8042 in the keyboard.

When the external keyboard and external mouse are powered up, the KDAT and MDAT lines are driven low. This sets the KBD bit (D3) and the MOUSE bit (D4) of the PME Wake Status Register since the KDAT and MDAT signals cannot be isolated internal to the part. This causes an nIO_PME to be generated if the keyboard and/or mouse PME events are enabled. Note that the keyboard and mouse isolation modes only prevent the internal 8042 in the part from setting these status bits.

Case 1: Keyboard and/or Mouse Powered by VTR

The KBD and/or MOUSE status bits will be set upon a VTR POR if the keyboard and/or mouse are powered by VTR. In this case, an nIO_PME will not be generated, since the keyboard and mouse PME enable bits are reset to zero on a VTR POR. The BIOS software needs to clear these PME status bits after power-up.

Case 2: Keyboard and/or Mouse Powered by VCC

The KBD and/or MOUSE status bits will be set upon a VCC POR if the keyboard and/or mouse are powered by VCC. In this case, an nIO_PME will be generated if the enable bits were set for wakeup, since the keyboard and mouse PME enable bits are VTR powered. Therefore, if the keyboard and mouse are powered by VCC, the enable bits for keyboard and mouse events should be cleared prior to entering a sleep state where VCC is removed (i.e., S3) to prevent a false PME from being generated. In this case, the keyboard and mouse should only be used as PME and/or wake events from the S0 and/or S1 states. The BIOS software needs to clear these PME status bits after power-up.

7.27 General Purpose I/O

The LPC47M182 provides a set of flexible Input/Output control functions to the system designer through the 13 independently programmable General Purpose I/O pins (GPIO). The GPIO pins can perform basic I/O and can be individually enabled to generate a PME (except GP24). GPIOs must be programmed as inputs to generate a PME.

7.27.1 GPIO Pins

The Table 7.16 summarizes the GPIO functionality, including PME, Either Edge Triggered Interrupt (EETI) input capability and the power source for the buffer on the I/O pads.

Table 7.16 – GPIO Summary

DEFAULT FUNCTION	ALT FUNC 1	ALT FUNC 2	PWR WELL	PCI RESET	VCC POR	VTR POR	PME/EETI
nCDC_DWN_ENAB	GP24	-	VTR	-	-	Input	-
GP10	-	-	VTR	-	-	Input	PME
GP11	-	-	VTR	-	-	Input	PME
GP12	-	-	VTR	-	-	Input	PME
GP13	-	-	VTR	-	-	Input	PME
GP14	-	-	VTR	-	-	Input	PME
GP15	-	-	VTR	-	-	Input	PME
GP16	FAN_TACH1 (Note 1)	-	VTR	-	-	Input	PME
GP17	FAN_TACH2 (Note 1)	-	VTR	-	-	Input	PME
DDCSDA_5V	GP20	EETI0	VTR[Note 1]	-	-	Hi-Z	PME/EETI
DDCSCL_5V	GP21	EETI1	VTR[Note 1]	-	-	Hi-Z	PME/EETI
DDCSDA_3V	GP22	-	VTR[Note 1]	-	-	Hi-Z	PME
DDCSCL_3V	GP23	-	VTR[Note 1]	-	-	Hi-Z	PME

Note 1: When DDC functions are selected, these pins require external pull-ups to appropriate voltages.

7.27.2 Description

Each GPIO port has a 1-bit data register and an 8-bit configuration control register. The data register for each GPIO port is represented as a bit in one of the 8-bit GPIO DATA Registers, GP1 to GP2. The bits in these registers reflect the value of the associated GPIO pin as follows. Pin is an input: The bit is the value of the GPIO pin. Pin is an output: The value written to the bit goes to the GPIO pin. Latched on read and write. All of the GPIO registers are located in the GPIO/Runtime Register logical device (see "GPIO Runtime Registers" section when LD_NUM=0 and "Runtime Register Block Runtime Registers" section when LD_NUM=1). The GPIO ports with their alternate functions and configuration state register addresses are listed in Table 7.17.

Table 7.17 – General Purpose I/O Port Assignments

DEFAULT FUNCTION	ALT. FUNC. 1	ALT. FUNC. 2	DATA REGISTER[1]	DATA REGISTER BIT NO.	GPIO RUNTIME REGISTER OFFSET (HEX)
nCDC_DWN_ENAB	GP24	-	GP1	0	15
GP10	-	-		1	
GP11	-	-		2	
GP12	-	-		3	
GP13	-	-		4	
GP14	-	-		5	
GP15	-	-		6	
GP16	FAN_TACH1	-		7	
GP17	FAN_TACH2	-	GP2	0	16

DEFAULT FUNCTION	ALT. FUNC. 1	ALT. FUNC. 2	DATA REGISTER[1]	DATA REGISTER BIT NO.	GPIO RUNTIME REGISTER OFFSET (HEX)
DDCSDA_5V	GP20	EETI0		1	
DDCSCL_5V	GP21	EETI1		2	
DDCSDA_3V	GP22	-		3	
DDCSCL_3V	GP23	-		4	
Reserved	-	-		7:5	

Note 1: The GPIO Data and Configuration Registers are located in GPIO/Runtime Register block at the offset shown from the GPIO/Runtime Register Block logical device base address.

7.27.3 GPIO Control

Each GPIO port has an 8-bit control register that controls the behavior of the pin. (See "GPIO Runtime Registers" section when LD_NUM=0 and "Runtime Register Block Runtime Registers" section when LD_NUM=1).

Each GPIO port may be configured as either an input or an output. If the pin is configured as an output, it can be programmed as open-drain or push-pull. Inputs and outputs can be configured as non-inverting or inverting. Bit[0] of each GPIO Configuration Register determines the port direction, bit[1] determines the signal polarity, and bit[7] detemines the output driver type select.

The Polarity Bit (bit 1) of the GPIO control registers control the GPIO pin when the pin is configured for the GPIO function and when the pin is configured for the alternate function for all pins, with the exception of the either edge triggered interrupts and DDC functions.

The basic GPIO configuration options are summarized in Table 7.18.

Table 7.18 – GPIO Configuration Summary

SELECTED FUNCTION	DIRECTION BIT	POLARITY BIT	DESCRIPTION
	B0	B1	
GPIO	0	0	Pin is a non-inverted output.
	0	1	Pin is an inverted output.
	1	0	Pin is a non-inverted input.
	1	1	Pin is an inverted input.

7.27.4 GPIO Operation

The operation of the GPIO ports is illustrated in Figure 7.4.

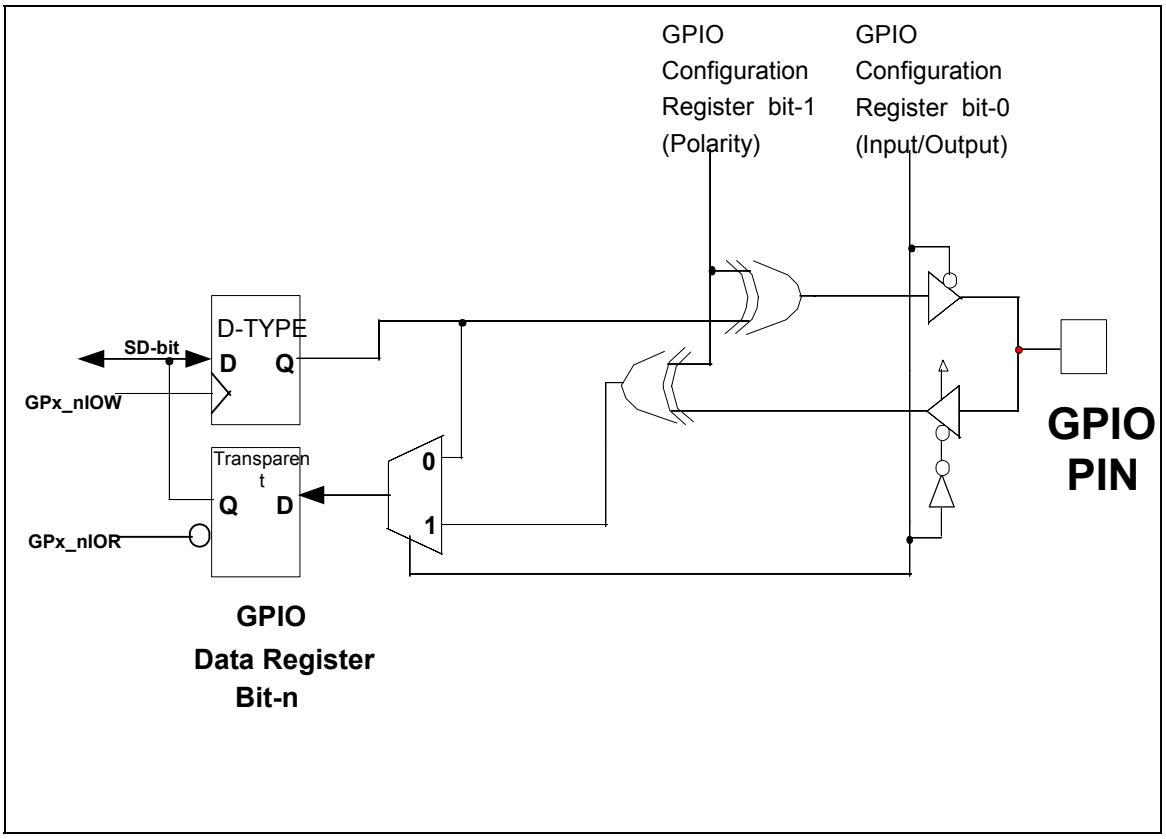


Figure 7.4 – GPIO Function Illustration

Note: Figure 7.4 is for illustration purposes only and is not intended to suggest specific implementation details.

When a GPIO port is programmed as an input, reading it through the GPIO data register latches either the inverted or non-inverted logic value present at the GPIO pin. Writing to a GPIO port that is programmed as an input has no effect (Table 7.19)

When a GPIO port is programmed as an output, the logic value or the inverted logic value that has been written into the GPIO data register is output to the GPIO pin. Reading from a GPIO port that is programmed as an output returns the last value written to the data register (Table 7.19). When the GPIO is programmed as an output, the pin is excluded from the PME logic.

Table 7.19 – GPIO Read/Write Behavior

HOST OPERATION	GPIO INPUT PORT	GPIO OUTPUT PORT
READ	LATCHED VALUE OF GPIO PIN	LAST WRITE TO GPIO DATA REGISTER
WRITE	NO EFFECT	BIT PLACED IN GPIO DATA REGISTER

7.27.5 GPIO PME Functionality

The LPC47M182 provides 12 GPIOs that can directly generate a PME. See the Table 7.16. The polarity bit in the GPIO control registers select the edge on these GPIO pins that will set the associated status bit in the PME_STS2 and PME_STS3 registers. The default is the low-to-high edge. If the corresponding enable bit in the PME_EN2 and PME_EN3 registers and the PME_EN bit in the PME_EN register is set, a PME will be generated. The PME registers are runtime registers which are located at the address contained in the configuration registers 0x60 and 0x61 in Power Control Logical Device when LD_NUM=0 or the Runtime Register Block Logical Device when LD_NUM=1. See the "Power Control Runtime Registers" and "Runtime Register Block Runtime Registers" sections. The PME status bits for the GPIOs are cleared on a write of '1'.

The following GPIOs are dedicated wakeup GPIOs with a status and enable bit in the PME status and enable registers:

GP10-GP17

GP20-GP23

The following PME status and enable registers for these GPIOs:

PME_STS2 and PME_EN2 for GP10-GP17

PME_STS3 and PME_EN3 for GP20-GP23

7.27.6 Either Edge Triggered Interrupts

GP21 and GP22 are implemented such that they allow an PME interrupt to be generated on both a high-to-low and a low-to-high edge transition, instead of one or the other as selected by the polarity bit.

The either edge triggered interrupts (EETI) function as follows: If the EETI function is selected for the GPIO pin, then the bits that control input/output, polarity and open drain/push-pull have no effect on the function of the pin. However, the polarity bit does affect the value of the GP bit (i.e., register GP2, bit 2 for GP22).

A PME interrupt occurs if the PME enable bit is set for the corresponding GPIO and the EETI function is selected on the GPIO. The PME status bit is set when the EETI pin transitions (on either edge) and are cleared on a write of '1'. There are also status bits for the EETIs located in the MSC_STS register, which are also cleared on a write of '1'. The MSC_STS register provides the status of all of the EETI interrupts within one register. The PME or MSC status is valid whether or not the interrupt is enabled and whether or not the EETI function is selected for the pin.

The MSC_STS register is defined in the "Power Control Runtime Registers" section when LD_NUM=0 or the "Runtime Register Block Runtime Registers" section when LD_NUM=1.

7.28 PME Support

The LPC47M182 offers support for power management events (PMEs), also referred to as a System Control Interrupt (SCI) events in an ACPI system. A power management event is indicated to the chipset via the assertion of the nIO_PME signal. In the LPC47M182, the nIO_PME is asserted by active transitions on the ring indicator inputs nRI1 and nRI2, active keyboard-data edges, active mouse-data edges, programmable edges on GPIO pins and fan tachometer event. The nIO_PME pin, can be programmed to be active high or active low via the polarity bit in the nIO_PME Register. The output buffer type of the pin can be programmed to be open-drain or push-pull via bit 7 of the nIO_PME Register. The nIO_PME pin function defaults to active low, open-drain output. The nIO_PME Register is located at offset

0x16in the Power Control Logical Device, when LD_NUM=0, or Runtime Register Block Logical Device, when LD_NUM=1. See the “Power Control Runtime Registers” and “Runtime Register Block Runtime Registers” sections.

The PME functionality is controlled by the PME status and enable registers defined in the “Power Control Runtime Registers” and “Runtime Register Block Runtime Registers” section, is located at the address programmed in configuration registers 0x60 and 0x61 in Power Control/Runtime Register Logical Device. The Power Control Logical Device is selected when LD_NUM=0, and the runtime Registers Locial Device is selected when LD_NUM=1. The PME Enable bit, PME_EN, globally controls PME Wake-up events. When PME_EN is inactive, the nIO_PME signal can not be asserted. When PME_EN is asserted, any wake source whose individual PME Wake Enable register bit is asserted can cause nIO_PME to become asserted.

The PME Status register indicates that an enabled wake source has occurred, and if the PME_EN bit is set, asserted the nIO_PME signal. The PME Status bit is asserted by active transitions of PME wake sources. PME_Status will become asserted independent of the state of the global PME enable bit, PME_EN.

The following pertains to the PME status bits for each event:

- The output of the status bit for each event is combined with the corresponding enable bit to set the PME status bit.
- The status bit for any pending events must be cleared in order to clear the PME_STS bit. Status bits are cleared on a write of ‘1’.

For the GPIO events, the polarity of the edge used to set the status bit and generate a PME is controlled by the polarity bit of the GPIO control register. For non-inverted polarity (default) the status bit is set on the low-to-high edge. If the EETI function is selected for a GPIO then both a high-to-low and a low-to-high edge will set the corresponding PME status bits. Status bits are cleared on a write of ‘1’.

The PME Wake registers also include status and enable bits for the fan tachometer input. The fan tachometers are not intended to be wakeup events and are only valid when VCC power is active. User Note: Clear the PME enable bits for the fan tachometers before removing VCC.

See the “Keyboard and Mouse PME Generation” section for information about using the keyboard and mouse signals to generate a PME.

In the LPC47M182 the nIO_PME pin can be programmed to be an open drain, active low, driver. The LPC47M182 nIO_PME pin is fully isolated from other external devices that might pull the nIO_PME signal low; i.e., the nIO_PME signal is capable of being driven high externally by another active device or pullup even when the LPC47M182 VCC is grounded, providing VTR power is active. The LPC47M182 nIO_PME driver sinks 6mA at .55V max (see section 4.2.1.1 DC Specifications, page 122, in the “PCI Local Bus Specification,” revision 2.1).

7.28.1 ‘Wake on Specific Key’ Option

The LPC47M182 has logic to detect a single keyboard scan code for wakeup (PME generation). The scan code is programmed onto the Keyboard Scan Code Register, a runtime register at offset 0x11 from the base address located in the primary base I/O address in Power Control Block Logical Device when LD_NUM =0, or the Runtime Register Block Logical Device when LD_NUM =1. This register is powered by VTR and reset on VTR POR.

The PME status bit for this event is located in the PME_STS1 register at bit 5 and the PME enable bit for this event is located in the PME_EN1 register at bit 5. See the “Power Control Runtime Registers” sections for a definition of these registers.

Data transmissions from the keyboard consist of an 11-bit serial data stream. A logic 1 is sent at an active high level. The following table shows the functions of the bits.

BIT	FUNCTION
1	Start bit (always 0)
2	Data bit 0 (least significant bit)
3	Data bit 1
4	Data bit 2
5	Data bit 3
6	Data bit 4
7	Data bit 5
8	Data bit 6
9	Data bit 7 (most significant bit)
10	Parity bit (odd parity)
11	Stop Bit (always 1)

The timing for the keyboard clock and data signals are shown in the “Timing Diagrams” section.

The process to find a match for the scan code stored in the Keyboard Scan Code register is as follows:

Begin sampling the data at the first falling edge of the keyboard clock following a period where the clock line has been high for 115-145usec. The data at this first clock edge is the start bit. The first data bit follows the start bit (clock 2). Sample the data on each falling edge of the clock. Store the eight bits following the stop bit to compare with the scan code stored in the Keyboard Scan Code register. Sample the comparator within 100usec of the falling edge of clock 9 (for example, at clock 10).

Sample the parity bit and check that the 8 data bits plus the parity bit always have an odd number of 1’s (odd parity).

Repeat until a match is found. If the 8 data bits match the scan code stored in the Keyboard Scan Code register and the parity is correct, then it is considered a match. When a match is found and if the stop bit is 1, set the event status bit (bit 5 of the PME_STS1 register) to ‘1’ within 100usec of the falling edge of clock 10.

The state machine will reset after 11 clocks and the process will restart. The process will continue until it is shut off by setting the SPEKEY_EN bit (see following sub-section).

The state machine will reset if there is a period where the clock remains high for more than one keyboard clock period (115-145usec) in the middle of the transmission (i.e., before clock 11). This is to prevent the generation of a false PME.

The SPEKEY_EN bit at bit 1 of the CLOCKI32 register at 0xF0 in Power Control Block Logical Device when LD_NUM=0 and the Runtime Register Block Logical Device when LD_NUM=1. This register is used to control the “wake-on-specific feature. This bit is used to turn the logic for this feature on and off. It will disable the 32kHz clock input to the logic. The logic will draw no power when disabled. The bit is defined as follows:

0= “Wake on specific key” logic is on (default)

1= “Wake on specific key” logic is off

Note: The generation of a PME for this event is controlled by the PME enable bit (located in the PME_EN1 register at bit 5) when the logic for feature is turned on.

7.29 Fan Monitoring

The chip monitors the speed of the fans by utilizing fan tachometer input signals from fans equipped with tachometer outputs. The fan tachometer inputs are monitored by using the Fan Tachometer registers. These signals, as well as the Fan Tachometer registers, are described below.

7.29.1 Fan Tachometer Inputs

A fan tachometer input is used to measure the speed at which a fan is rotating. The fan tachometer input is a train of square pulses with a 50% duty cycle (see Figure 7.5) that are derived from the magnetic fields generated by the rotating rotor of the fan. The speed of the fan can be determined by calculating the period of the Fan Tachometer input pulse.

Note: All calculations are based on fans that emit 2 square pulses per revolution. Reading registers reflect a count value for one complete revolution (2 pulses).

The clock source to the Fan Tachometer logic is 90kHz (nominal) derived from 14.318 MHz clock and is active when VCC power is active.

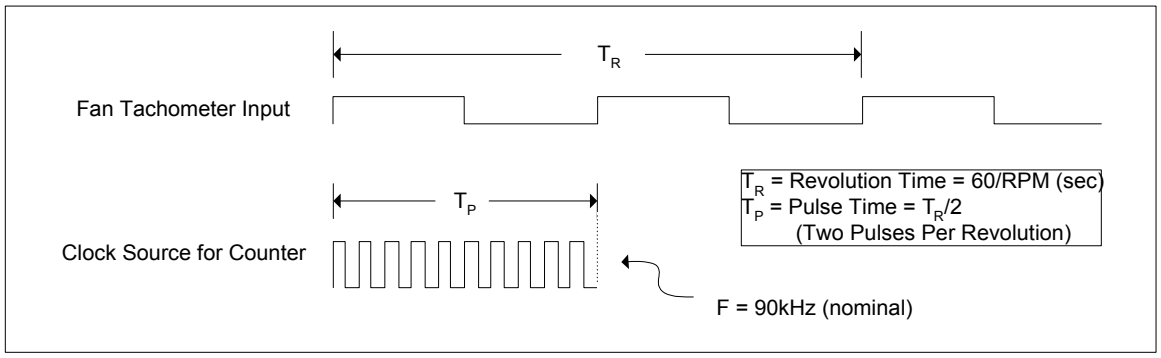


Figure 7.5 – Fan Tachometer Input and Clock Source

The counter is used to determine the period of the Fan Tachometer input pulse. This counter is reset on the rising edge of every other fan tachometer input pulse, and thus measures the number of clock pulses generated by the clock source for the duration of one fan tachometer revolution. Since two fan tachometer input pulses are generated per revolution of the fan rotor, the speed of the fan is easily calculated. The fan tachometer input resets the counter on every other pulse and simultaneously loads the count into its respective reading register. This value is used by the operating system to monitor the speed of the fan.

The Fan Tachometer Reading registers contain the number of 11.11us periods (90kHz nominal) between full fan revolutions. Fans produce 2 pulses per revolution. These registers are updated at least once every second. This register is latched on the rising edge of every other fan tachometer pulse and when the fan count reaches FFFFh. The value FFFFh indicates that the fan is not spinning (stalled fan event), or the tachometer input is not connected to a valid signal (this could be triggered by a counter overflow)

The Fan Tachometer Reading registers always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional.

The Tachometer Reading registers are 16 bits, unsigned. When one byte of a 16-bit register is read, the other byte latches the current value until it is read, in order to ensure a valid reading. The order is LSB first, MSB second. These registers are read only – a write to these registers has no effect.

The fan tachometer reading registers are Tach1 LSB, Tach1_MSB, Tach2 LSB and Tach2 MSB. See "Power Control Runtime Registers" section when LD_NUM=0 and "Runtime Register Block Runtime Registers" section when LD_NUM=1.

7.29.2 Detection of a Stalled Fan

The fan failure bit in the interrupt status register is set in the event of a stalled fan. Note: the fan tachometer reading register, which holds the count value, does not roll over – it stays at FFFFh in the event of a stalled fan. The internal count register does rollover, however, and continuously counts to FFFFh as long as the fan is stalled.

In the event the counter reaches FFFFh, the PME status bit is set and the count value is latched into the register. The second subsequent fan tach pulse resets the counter but does not latch the count value. Every second fan tach pulse latches the fan count value into the fan tachometer register except for this special case.

The fan stalled event can generate a PME if properly enabled. Note the fan stalled PME is not a wakeup event, and it can indicate a fan stalled event if VCC is active.

7.30 Hard Drive and Power LED Logic

7.30.1 Hard Drive Front Panel LED (Red)

Table 7.20 – Hard Drive Front Panel Pins

NAME	BUFFER	POWER WELL	DESCRIPTION
nSCSI	ISPU_400	VCC	SCSI Drive Active Input
nHD_LED	OD12	VCC	Hard Drive Front Panel LED Open-Drain Output
nSECONDARY_HD	ISPU_400	VCC	IDE Secondary Drive Active Input
nPRIMARY_HD	ISPU_400	VCC	IDE Primary Drive Active Input

Notes:

- The nHD_LED requires external pull-up to VCC.
- ISPU_400 is defined as: Input with Schmitt Trigger, 400 mV hysteresis, with 30uA internal pull-up.
- The nHD_LED pin is a logical AND of the inputs nPRIMARY_HD, nSECONDARY_HD and nSCSI used to drive a single color LED. The inputs are internally pulled to VCC. See table below for state definitions.

The nHD_LED pin is used at the system's front panel header to drive the hard drive activity LED. Note that external LEDs should be driven such that the voltage at the nHD_LED pin does not exceed 5V. The output is open-drain and should be externally pulled to VCC through a resistor.

Table 7.21 – nHD_LED Truth Table

INPUTS			OUTPUT	
NPRIMARY_HD	**NSECONDARY_HD**	**NSCSI**	**nHD_LED**	**NOTES**
0	X	X	0	LED On
X	0	X	0	LED On
X	X	0	0	LED On
1	1	1	Hi-Z	LED Off

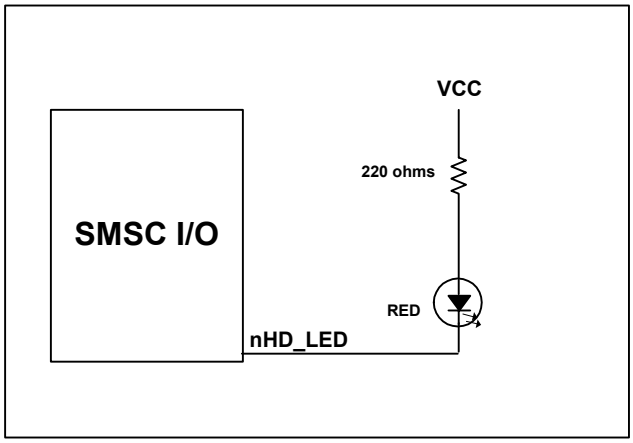


Figure 7.6 – NHD_LED Circuit

7.30.2 Yellow and Green Power LED Pins

Table 7.22-- LED Pins

NAME	BUFFER	POWER WELL	DESCRIPTION
GRN_LED	OD24	VTR	Green Power LED Open-Drain Output
YLW_LED	OD24	VTR	Yellow Power LED Open-Drain Output
nSLP_S5	I	VTR	Input from South Bridge for Transitioning to the S5 Power State

Note: The LEDs require external pull-up to VTR.

The green and yellow LED outputs are controlled by the LED register accessible via the LPC bus. The GRN_YLW bit controls which output is asserted. In addition, the SDY_BLK bit indicates whether the selected LED is steady or blinking. The LED register is located at offset 10h in the Power Control Logical Device (LD_NUM=O) or the Runtime Register Block Logical Device (LD_NUM=1).

These LED outputs are also controlled by the nSLP_S5 sleep input pin. The functionality is shown in the table below.

The green and yellow LED outputs are powered by VTR.

Table 7.23 - LED Truth Table

INPUTS			OUTPUTS	
NSLP_S5	**GRN_YLW BIT**	**SDY_BLK BIT**	**GRN_LED**	**YLW_LED**
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0.67 Hz
1	0	1	0	Hi-Z
1	1	0	0.67 Hz	0
1	1	1	Hi-Z	0

Note: The LED is ON in the **Hi-Z** state. The LED is blinking at 0.67 Hz in the **0.67 Hz** state.

The 32.768 kHz clock input is used to control the blink rate and duty cycle of the LEDs. The blink rate is 0.67Hz, and the duty cycle is 39.6%. This corresponds to a LED low output of exactly 0.90625 seconds (depending on the accuracy of the 32.768 kHz clock).

YLW_LED and GRN_LED require external pull-ups to power the LEDs. A resistor value of 220 ohms to VTR is recommended. These are open drain active high outputs. When the LEDs are off, the open drain output is sinking the current from VTR through the 220 ohm resistor to ground. When the LEDs are on, they are powered through the 220 ohm resistor.

The following figure shows the recommended external LED circuit.

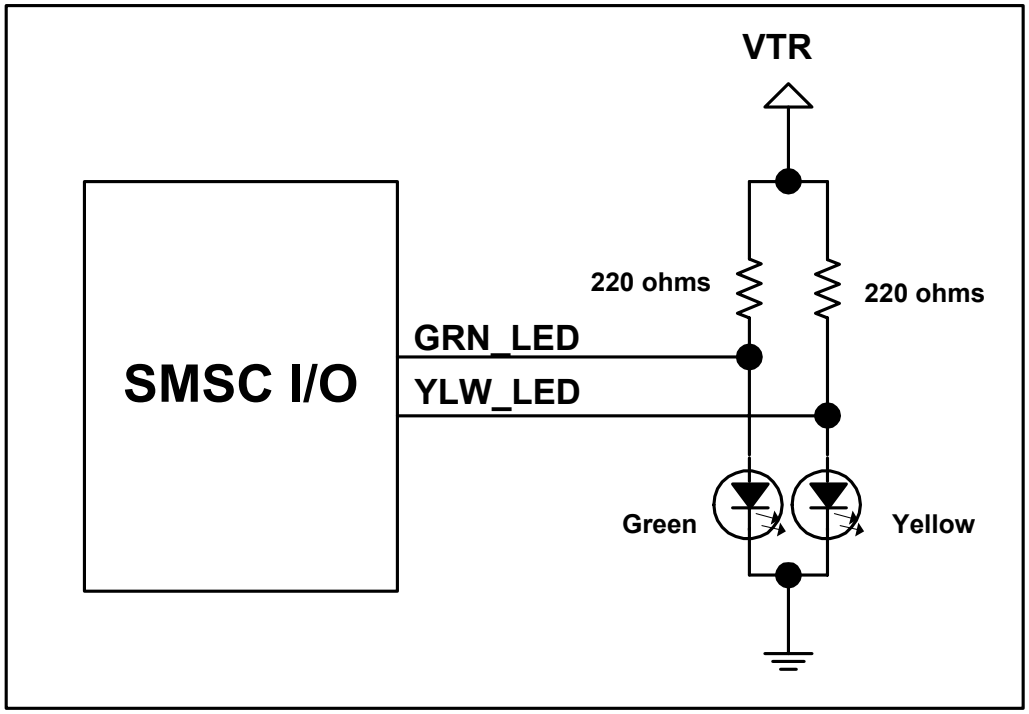


Figure 7.7 – Example Yellow and Green LED Circuit

7.31 Power Generation (5V)

7.31.1 Reference Pins

Table 7.24 – Reference Generation Pins

NAME	BUFFER	MAX OUT CURRENT	POWER WELL	DESCRIPTION
REF5V	AO	3.3mA	VCC	5V Reference Output
REF5V_STBY	AO	3.3mA	VTR	Highest System Standby Voltage

O_{AN}: Analog Output, 5V level.

See DC characteristics see the “Electrical Characteristics” section.

7.31.2 5V Main Reference Generation

REF5V is used to help power-up various system components’ 5V tolerant buffers. This signal is used to guarantee there are no power sequencing requirements at each particular system component.

REF5V is powered by VCC when VCC5V < VCC.

Upon motherboard power-up, REF5V is an analog output signal that tracks either VCC or VCC5V (through an external pull-up resistor), whichever is greater in amplitude. REF5V becomes a high impedance input while tracking the VCC power supply.

Table 7.25 – REF5V

MAIN SUPPLY	REF5V
VCC5V < VCC	VCC
VCC5V > VCC	Hi-Z

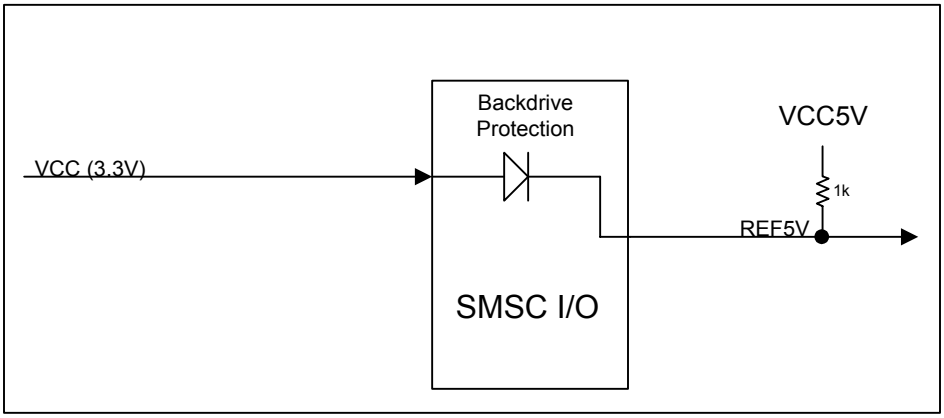


Figure 7.8 – REF5V Circuit

Note: the maximum voltage drop across the diode is 350mV.

7.31.3 5V Standby Reference Generation

REF5V_STBY is generated in the same manner as REF5V, but in reference to V_5P0_STBY and

VTR instead. REF5V_STBY serves the same purpose as REF5V, but tracks different power supplies.

REF5V_STBY is an analog output signal that tracks either VTR or V_5P0_STBY, whichever is greater in amplitude.

Upon motherboard power-up, REF5V_STBY is an analog output signal that tracks either VTR or V_5P0_STBY (through an external pull-up resistor), whichever is greater in amplitude. REF5V_STBY becomes a high impedance input while tracking the V_5P0_STBY power supply.

REF5V_STBY is powered by VTR when VTR > V_5P0_STBY.

Table 7.26 – REF5V_STBY

STANDBY SUPPLY	REF5V_STBY
V_5P0_STBY < VTR	VTR
V_5P0_STBY > VTR	Hi-Z

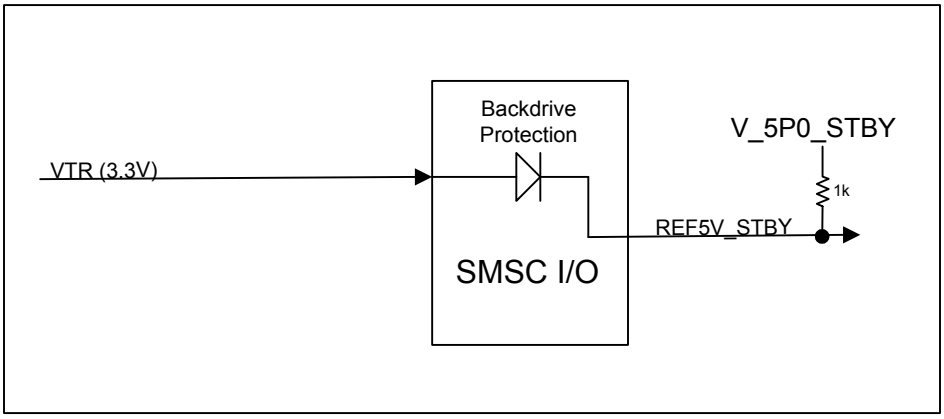


Figure 7.9 – REF5V_STBY

Note: the maximum voltage drop across the diode is 350mV.

7.31.4 Reference Timings

See Figure 13.25 to Figure 13.28 in the “Timing Diagrams” section.

7.32 IDE Reset Output Pin

nIDE_RST is an open drain buffered copy of nPCI_RESET. This signal requires an external 1kohm pull-up to VCC5V.

This signal will be low when VCC5V=0 since it is externally pulled up to VCC5V.

Table 7.27 – nIDE_RSTDRV Pin

NAME	BUFFER	POWER WELL	DESCRIPTION
nIDE_RSTDRV	OD8	VCC	IDE Reset Output

Table 7.28 – nIDE_RSTDRV Truth Table

nPCI_RESET (Input)	nIDE_RSTDRV (Output)
0	0
1	Hi-Z

See Table 13.1 for nIDE_RSTDRV timing.

7.33 PCI Reset Output Pins

The nPCIRST_OUT is 3.3V buffered copy of nPCI_RESET. The nPCIRST_OUT2 is 3.3V buffered copy of nPCI_RESET.

The nPCIRST_OUT and nPCIRST_OUT2 signals will be low when VCC=0.

Table 7.29 – nPCIRST_OUT Pins

NAME	BUFFER	POWER WELL	DESCRIPTION
nPCIRST_OUT	OP14	VTR	Buffered PCI Reset Output
nPCIRST_OUT2	OP14	VTR	Buffered PCI Reset Output

Table 7.30 – nPCIRST_OUT and nPCIRST_OUT2 Truth Table

INPUT	OUTPUTS	
nPCI_RESET	nPCIRST_OUT	nPCIRST_OUT2
0	0	0
1	1	1

See Table 13.2 for nPCI_RSTOUT and nPCI_RSTOUT2 timings.

7.34 Voltage Translation Circuit

Table 7.31 – Voltage Translation DDC Pins

NAME	BUFFER	POWER WELL	DESCRIPTION
DDCSDA_5V/ GP20	IO_SW	VTR	5V DDC Data IOD/ GPIO (Note)
DDCSCL_5V/ GP21	IO_SW	VTR	5V DDC Clock IOD/ GPIO (Note)
DDCSDA_3V/ GP22	IO_SW	VTR	3.3V DDC Data IOD/ GPIO (Note)

NAME	BUFFER	POWER WELL	DESCRIPTION
DDCSCL_3V/ GP23	IO_SW	VTR	3.3V DDC Clock IOD/ GPIO (Note)

Note: The DDC_5V signals require external pull-up to VCC5V. The DDC_3V signals require external pull-up to VCC. If DDC functions are selected on the pins, the pins will tri-state when VCC is removed.

The VGA DDC voltage translation circuitry is used in conjunction with integrated VGA chipsets. Since the chipset operates at 3.3V signal levels and the VGA signals are specified at 5V signal levels, on-board voltage translation is needed for the DDC signals. This is a non-inverting translation. See the Table 7.32 and Table 7.33 for further details on the logic.

The DDC data pins and the DDC clock pins function as inputs shorted together through the isolation resistor. The DDC signals require external pull-up resistors on LPC47M182. See the “Pins That Require External Resistors” section for resistor values. See Figure 7.10 for recommended schematic implementation. Note the switch is always on after the DDC functions are selected on the GPIO pins. That is, the switch is controlled by the GPIO alternate function select bits. Once the DDC functions are selected, the switch is closed and remains closed when VCC is removed. The current flow is controlled by the external signals on the DDC pins. See the tables below for the current flow across the switch based on the voltage levels on the pins. The switch provides a 25ohm resistance to ground.

This circuit requires ESD protection external to the chip to protect the device from hot-plugging on the VGA connector. See the “Electrical Characteristics” section for current and voltage requirements.

Due to the multiplexing with GPIO pins, these pins are powered by VTR. (Without the multiplexing requirement, these pins could be powered by VCC).

Note: If any of the Alternate Function Select bits in GP20 to GP23 registers are set for DDC function, the DDC functions will be selected on all four GP20 to GP23 pins. However, it is recommended that the DDC functions be selected via the Alternate Function Select bits in all of the GP20 to GP23 registers when using the DDC functions.

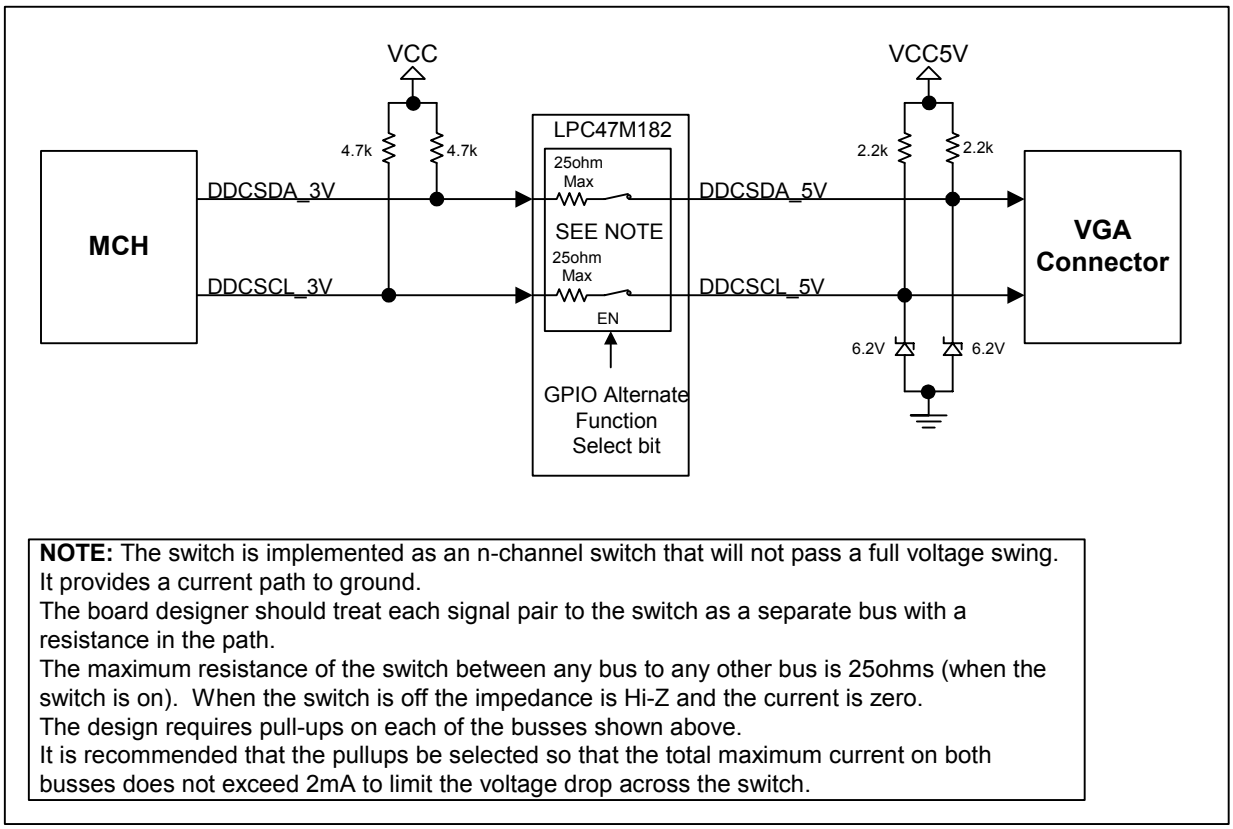
The GP20 to GP23 registers are defined in “GPIO Runtime Registers” section when LD_NUM=0 and “Runtime Register Block Runtime Registers” section when LD_NUM=1.

Table 7.32 – VGA DDCSDA Voltage Translation Logic

DDC VS. GPIO ALTERNATE FUNCTION SELECT BIT/S	DDCSDA_3V	DDCSDA_5V	CURRENT ACROSS THE SWITCH
GPIO/EETI/Reserved	Don’t Care	Don’t Care	No Current flow (0 mA)
DDC (DEFAULT)	0V	0V	Current flows from DDCSDA_5V or DDCSDA_3V
DDC (DEFAULT)	3.6V (max)	5.5V (max)	No Current flow (0 mA)

Table 7.33 – VGA DDCSCL Voltage Translation Logic

DDC Vs. GPIO ALTERNATE FUNCTION SELECT BIT/S	DDCSCL_3V	DDCSCL_5V	CURRENT ACROSS THE SWITCH
GPIO/EETI/Reserved	Don't Care	Don't Care	No Current flow (0 mA)
DDC (DEFAULT)	0V	0V	Current flows from DDCSCL_5V or DDCSCL_3V
DDC (DEFAULT)	3.6V (max)	5.5V (max)	No Current flow (0 mA)



NOTE: The switch is implemented as an n-channel switch that will not pass a full voltage swing. It provides a current path to ground.
The board designer should treat each signal pair to the switch as a separate bus with a resistance in the path.
The maximum resistance of the switch between any bus to any other bus is 25ohms (when the switch is on). When the switch is off the impedance is Hi-Z and the current is zero.
The design requires pull-ups on each of the busses shown above.
It is recommended that the pullups be selected so that the total maximum current on both busses does not exceed 2mA to limit the voltage drop across the switch.

Figure 7.10 – VGA DDC Voltage Translation Circuit

7.35 SMBus Isolation Circuitry

Table 7.34 – SMBus Isolation Pins

NAME	BUFFER	POWER WELL	DESCRIPTION
SMB_CLK_M	IO_SW	VTR	Main Well SMBus Clock
SMB_DAT_M	IO_SW	VTR	Main Well SMBus Data
SMB_CLK_R	IO_SW	VTR	Resume Well SMBus Clock
SMB_DAT_R	IO_SW	VTR	Resume Well SMBus Data

The SMBus Isolation circuitry is used to isolate the main SMBus signals from the resume SMBus signals during power down modes. The SMB data pins and the SMB clock pins function as inputs shorted together through the isolation resistor when the switch is closed. The SMBus signals require external pull-up resistors on LPC47M182. See Figure 7.11 for recommended schematic implementation. The switch is controlled by the PWRGD_PS signal. The switch is closed as long as PWRGD_PS is '1'. The current flow is controlled by the external signals on the SMB pins. See Table 7.35 and Table 7.36 for the current flow across the switch based on the voltage levels on the pins. The switch provides a 25ohm resistance to ground.

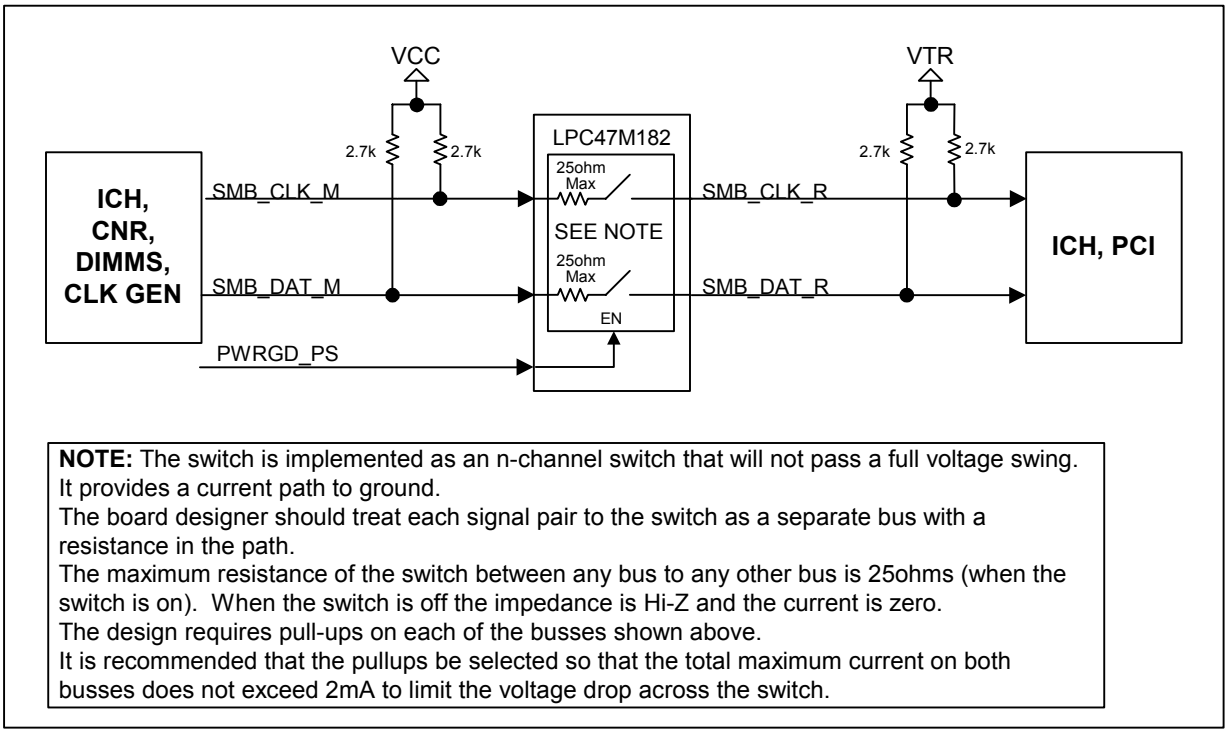
These pins are powered by VTR.

Table 7.35 – SMB_CLK Isolation Logic

PWRGD_PS	SMB_CLK_M	SMB_CLK_R	CURRENT ACROSS THE SWITCH
0	Don't Care	Don't Care	No Current flow (0 mA)
1	0V	0V	Current flows from SMB_CLK_R or SMB_CLK_M
1	3.6V (max)	3.6V (max)	No Current flow (0 mA)

Table 7.36 – SMB_DAT Isolation Logic

PWRGD_PS	SMB_DAT_M	SMB_DAT_R	CURRENT DIRECTION ACROSS THE SWITCH
0	Don't Care	Don't Care	No Current flow (0 mA)
1	0V	0V	Current flows from SMB_DAT_R or SMB_DAT_M
1	3.6V (max)	3.6V (max)	No Current flow (0 mA)



NOTE: The switch is implemented as an n-channel switch that will not pass a full voltage swing. It provides a current path to ground.
The board designer should treat each signal pair to the switch as a separate bus with a resistance in the path.
The maximum resistance of the switch between any bus to any other bus is 25ohms (when the switch is on). When the switch is off the impedance is Hi-Z and the current is zero.
The design requires pull-ups on each of the busses shown above.
It is recommended that the pullups be selected so that the total maximum current on both busses does not exceed 2mA to limit the voltage drop across the switch.

Figure 7.11 – SMBUS Isolation Circuit

7.36 PS_ON Logic

Table 7.37 – nPS_ON, nCPU_PRESENT and nSLP_S3 Pins

NAME	BUFFER	POWER WELL	DESCRIPTION
nPS_ON	OD8	VTR	Power Supply Turn-ON Open Drain Output
nCPU_PRESENT	ISPU_400	VTR	CPU Present Input from Processor
nSLP_S3	I	VTR	S3 Power State Input from South Bridge

The nPS_ON is a function of nSLP_S3 and nCPU_PRESENT according to the truth table below.

The nCPU_PRESENT is the signal from the processor that tells the system whether or not a processor has been plugged in. The nCPU_PRESENT will be pulled to VTR through a 30uA resistor inside the chip.

The nPS_ON is used as the power down signal for the power supply. Since nPS_ON is an open drain output, it may need to be pulled through a 1kohm resistor to V_5P0_STBY external to the chip if such a pull-up is not provided on the power supply. The power supply turn-on circuit behaves according to the table below.

Table 7.38 – nPS_ON Truth Table

INPUTS		OUTPUT
NCPU_PRESENT	**NSLP_S3**	**nPS_ON**
0	0	Hi-Z
0	1	0
1	0	Hi-Z
1	1	Hi-Z

See Table 13.3 for nPS_ON timing.

7.37 PWRGD_PLATFORM Logic

Currently the two signals available for power sequencing control (BF_CUT & LATCHED_BF_CUT) occur ~1ms before nPCI_RESET de-assertion. An option is required to insert more delay from ACPI power sequencing events to software runtime. To do this, the PWRGD_3V signal, needs to be redefined as PWRGD_PLATFORM. The assertion and de-assertion edge is described below, and is summarized in Table 7.39 – PWRGD_PLATFORM Truth Table.

- **Negative edge (S0->S3/S5):** The 1-0 transition of nSLP_S3 input or the 1-0 transition (or 0 level) of PWRGD_PS input would cause an immediate 1-0 transition (or 0 level) of PWRGD_PLATFORM.
- **Positive edge (S3/S5->S0):** The 0-1 transition of PWRGD_PS input would cause a 0-1 transition of PWRGD_3V. The PWRGD_3V transition is either immediate (no delay) or after a 100ms (min) to 120ms (max) delay from the 0-1 transition of PWRGD_PS.

The delay is optional and will be governed by a lockable select bit in the nIO_PME register (located at offset 16h in the in the Power Control Logical Device, when LD_NUM=0, or Runtime Register Block Logical Device, when LD_NUM=1). Default operation selects the delay. An internal delay counter is used to determine whether the 100-120 msec delay time has elapsed.

Table 7.39 – PWRGD_PLATFORM Truth Table

NSLP_S3	PWRGD_PS	PWRGD_PLATFORM SELECT BIT	INTERNAL DELAY ELAPSED? 0 = NO 1= YES	PWRGD_PLATFORM
1-0 transition or 0 level	X	X	X	0
X	1-0 transition or 0 level	X	X	0
1	0-1 transition	0	X	1 (no delay)
1	0-1 transition	1	0	0 (delay time not elapsed)
1	0-1 transition	1	1	1 (after 100-120 msec delay)

A timing diagram for generating the PWRGD_PLATFORM is shown below:

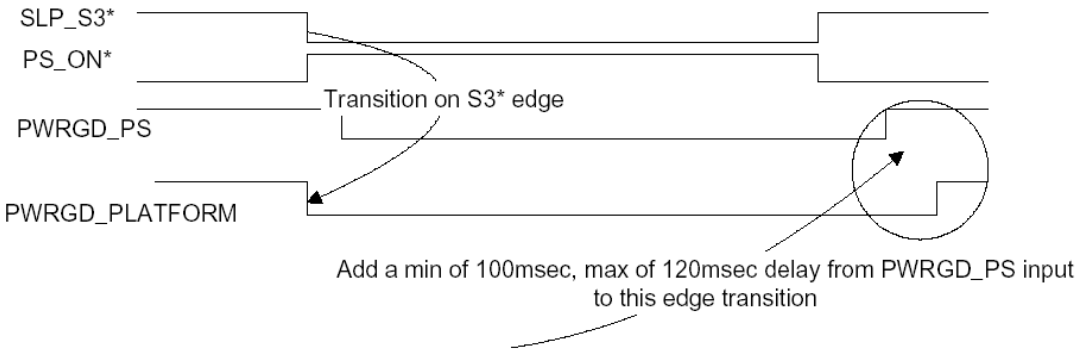


Figure 7.12 – PRWGD_PLATFORM Generation

7.37.1 Selecting the Delay

Bits 3:2 of the nIO_PME register, (located at offset 16h in the in the Power Control Logical Device, when LD_NUM=0, or Runtime Register Block Logical Device, when LD_NUM=1), is used to select the delay.

7.38 SCK_BJT_GATE Output

Table 7.40 – SCK_BJT_GATE Pin

NAME	BUFFER	POWER WELL	DESCRIPTION
SCK_BJT_GATE	OD8	VTR	Open-Drain Gate Output for the SCK_BJT_GATE in S3

Note: The SCK_BJT_GATE requires external pull-up to V_5P0_STBY.

The SCK_BJT_GATE pin is an open drain output that provides the gate signal for SCK_BJT in the S3 power state. This circuit is used for glitch protection on the SCK line when moving in to and out of the S3 power state. This signal is only required for designs utilizing Rambus memory. This output functions according to the table below. See the figure below for the circuit implementation.

Table 7.41 – SCK_BJT_GATE Truth Table

PWRGD_PLATFORM (INPUT)	SCK_BJT_GATE (OUTPUT)
0	Hi-Z
1	0

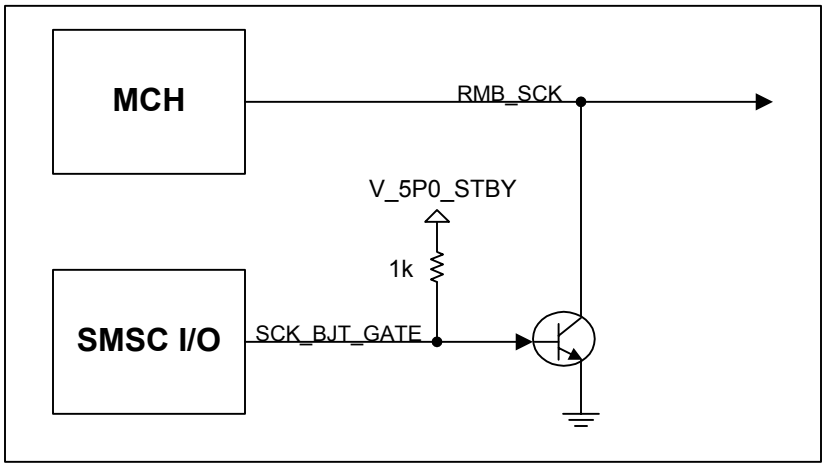


Figure 7.13 - SCK_BJT_GATE Circuit

See Table 13.4 for SCK_BJT_GATE timing.

7.39 Backfeed Cut and Latched Backfeed Cut Circuitry

Table 7.42 – nBACKFEED_CUT and LATCHED_BF_CUT Pins

Name	Buffer	Power Well	Description
nBACKFEED_CUT	OD8	VTR	Open-Drain Output used for STR Circuitry
LATCHED_BF_CUT	OP14	VTR	Latched Backfeed Cut Output for STR Circuitry

Note: The nBACKFEED_CUT requires an external pull-up to V_5P0_STBY.

nBACKFEED_CUT is a signal required by the S3 power state circuitry and is powered by the VTR supply. It is a function PWRGD_PS and nSLP_S3 according to the table below. nBACKFEED_CUT is used to switch between the main voltage regulator and the suspend voltage regulator for various sub-systems when the system is transitioning into the S3 power state.

Table 7.43 – nBACKFEED_CUT Truth Table

INPUTS		OUTPUT
PWRGD_PS	**NSLP_S3**	**nBACKFEED_CUT**
0	0	Hi-Z
0	1	Hi-Z
1	0	Hi-Z
1	1	0

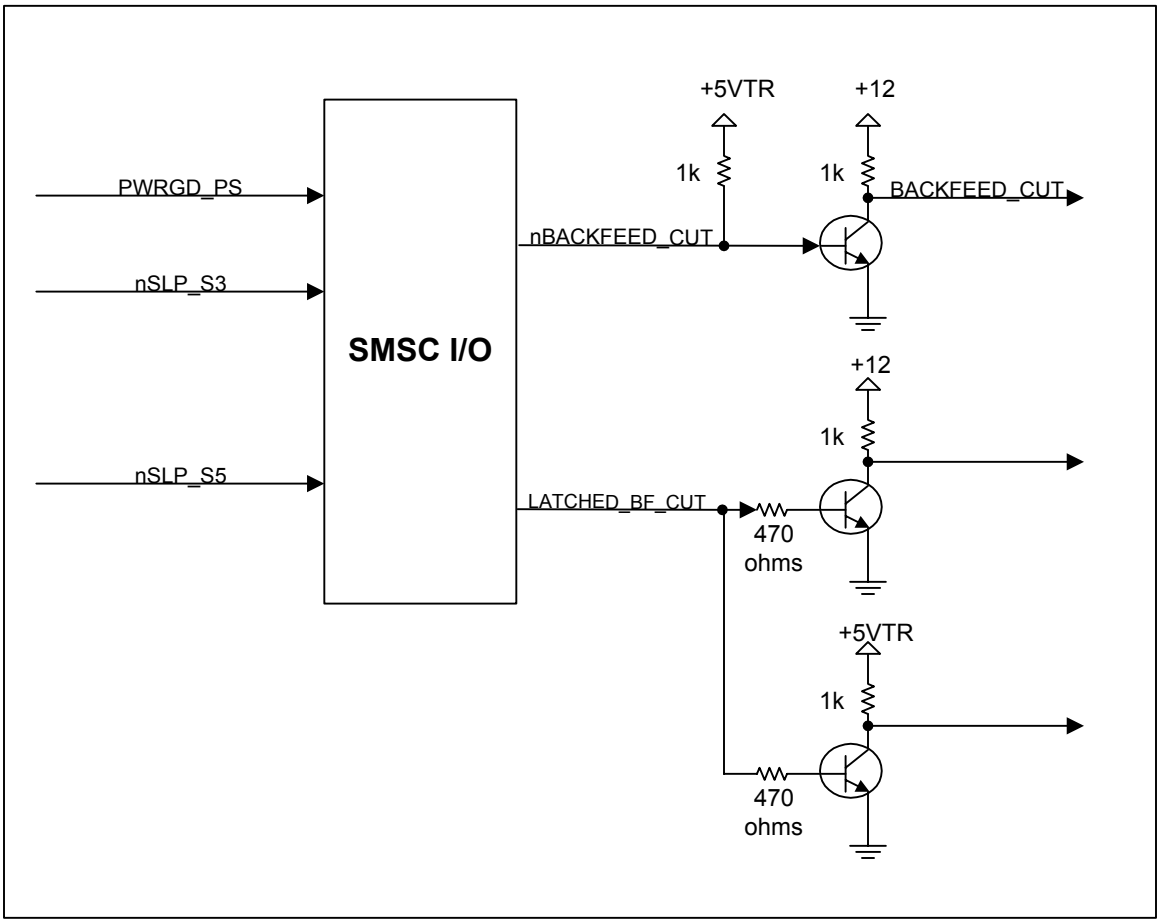


Figure 7.14– Backfeed Cut and Latched Backfeed Cut Circuit

The LATCHED_BF_CUT is generated from nBACKFEED_CUT and nSLP_S5. It is powered by VTR.

Table 7.44 – LATCHED_BF_CUT Truth Table

INPUTS		OUTPUT
NBACKFEED_CUT (INTERNAL SIGNAL)	**NSLP_S5**	**LATCHED_BF_CUT**
0	0	0
0	1	0
1	0	0
0 to 1 (rising edge)	1	1
'1' and no rising edge	1	No Change (Note)

Note: This is the condition when nBACKFEED_CUT stays high and nSLP_S5 goes low and then high again (see Figure 7.17).

APPLICATION NOTE:

The figure below shows the power up sequence. The nBACKFEED_CUT signal follows the power rail up to its final value. The LATCHED_BF_CUT signal stays low and never turns on. The nSLP_S5 goes to its high value when the power rails have stabilized, approximately 25msec after power on. nBACKEED_CUT

is pulled low a period t1 after nSLP_S5 goes high. The period t1 can be as short as 1msec. Typical measured values are approximately 200msec. The t1 and t2 values are guaranteed by the inherent design of the system and are not controlled by the LPC47M182.

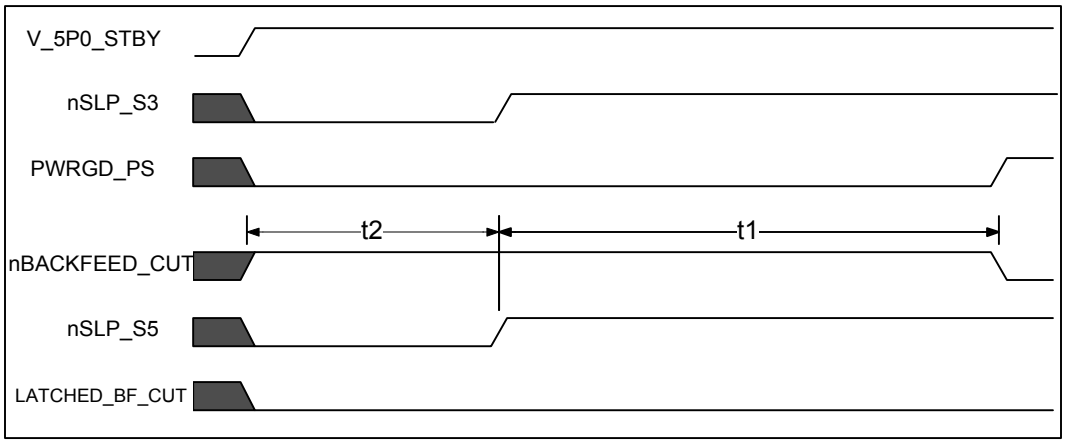


Figure 7.15 – Latched Backfeed Cut Power Up Sequence

Table 7.45 – Latched Backfeed Cut Power Up Sequence Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nSLP_S5 inactive to nBACKFEED_CUT active	1	200		msec
t2	nSLP_S5 inactive after power rails have stabilized		25		msec

Note: Periods t1 and t2 should be guaranteed by the inherent design of the system. These timings are not controlled by the LPC47M182.

There are two possible timing sequences following the power up signal sequencing. The first possible sequence is with nSLP_S5 staying high and nBACKFEED_CUT transitioning from low to high, remaining high for an undetermined period and then going back to low. At this point, the system returns to the end of the power-up sequence.

During these nBACKFEED_CUT transitions, the propagation delays, rise and fall times for LATCHED_BF_CUT are as described in the figure below. The first sequence can start at the end of the power-up sequence at any time.

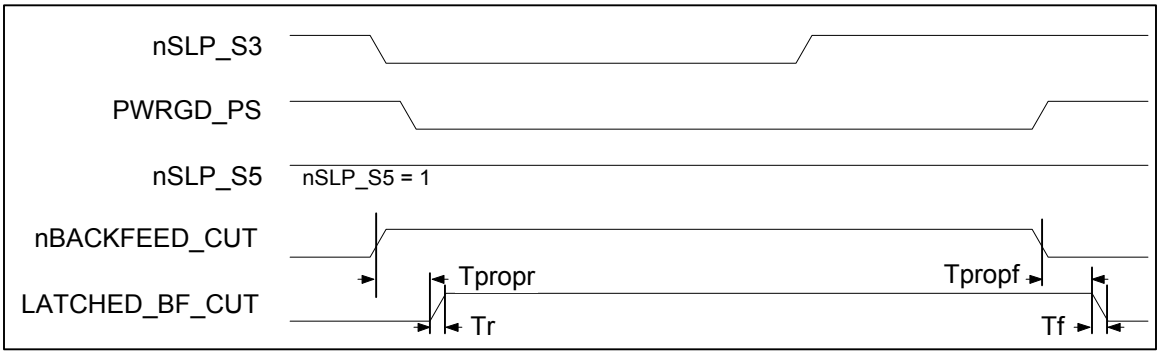


Figure 7.16 – Latched Backfeed Cut Sequence 1

The second possible sequence, shown in the figure below, is a normal powerdown sequence. The nBACKFEED_CUT signal goes from low to high when nSLP_S3 goes low, and nSLP_S5 goes from high to low 30usec to 65usec (t3) later.

The LATCHED_BF_CUT signal goes high when nBACKFEED_CUT goes high and then LATCHED_BF_CUT returns to low when nSLP_S5 goes low.

The nBACKFEED_CUT stays high and nSLP_S5 stays low for an indeterminate time and then nSLP_S5 will go high. A minimum of 1msec (t4) later, nBACKFEED_CUT will go low and the system returns to the end of the power-up sequence when nSLP_S3 and PWRGD_PLATFORM goes high. Typical measured values of t4 are approximately 250msec. During all transitions, the propagation delays, rise and fall times and power regulation times for LATCHED_BF_CUT are as described in Figure 7.17. The first sequence can start at the end of this power-up sequence at any time.

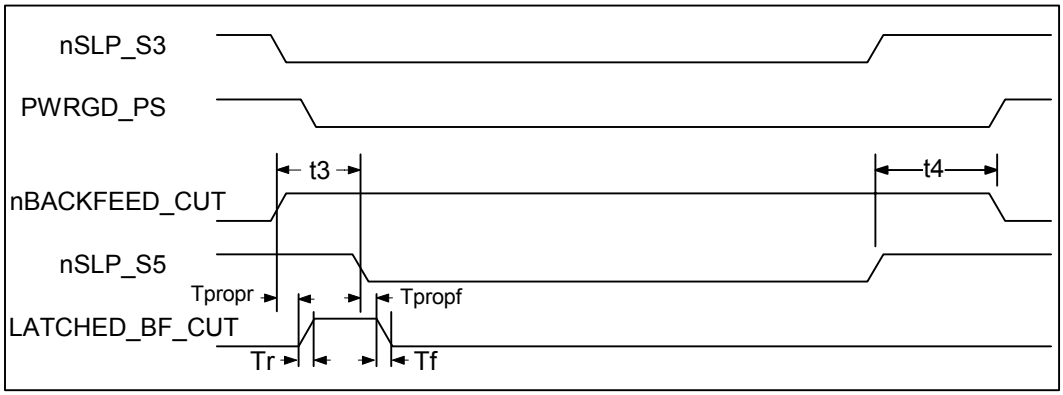


Figure 7.17 – Latched Backfeed Cut Sequence 2

Table 7.46 – Latched Backfeed Cut Sequence 1 and 2 Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
Tr	LATCHED_BF_CUT rise time. Measured from 10% to 90%.			1	us
Tf	LATCHED_BF_CUT fall time. Measured from 90% to 10%.			1	us
Tpropf	LATCHED_BF_CUT high to low propagation delay. Measured from nBACKFEED_CUT/nSLP_S5 threshold to 90% of LATCHED_BF_CUT			50	ns
Tpropr	LATCHED_BF_CUT low to high propagation delay. Measured from nBACKFEED_CUT/nSLP_S5 threshold to 10% of LATCHED_BF_CUT			50	ns
CO	Output Capacitance			25	pF
CL	Load Capacitance			50	pF
t3	nBACKFEED_CUT inactive to nSLP_S5 active	30		60	us
t4	nSLP_S5 inactive to nBACKFEED_CUT active	1	250		ms

The following figure shows a flowchart of the logic.

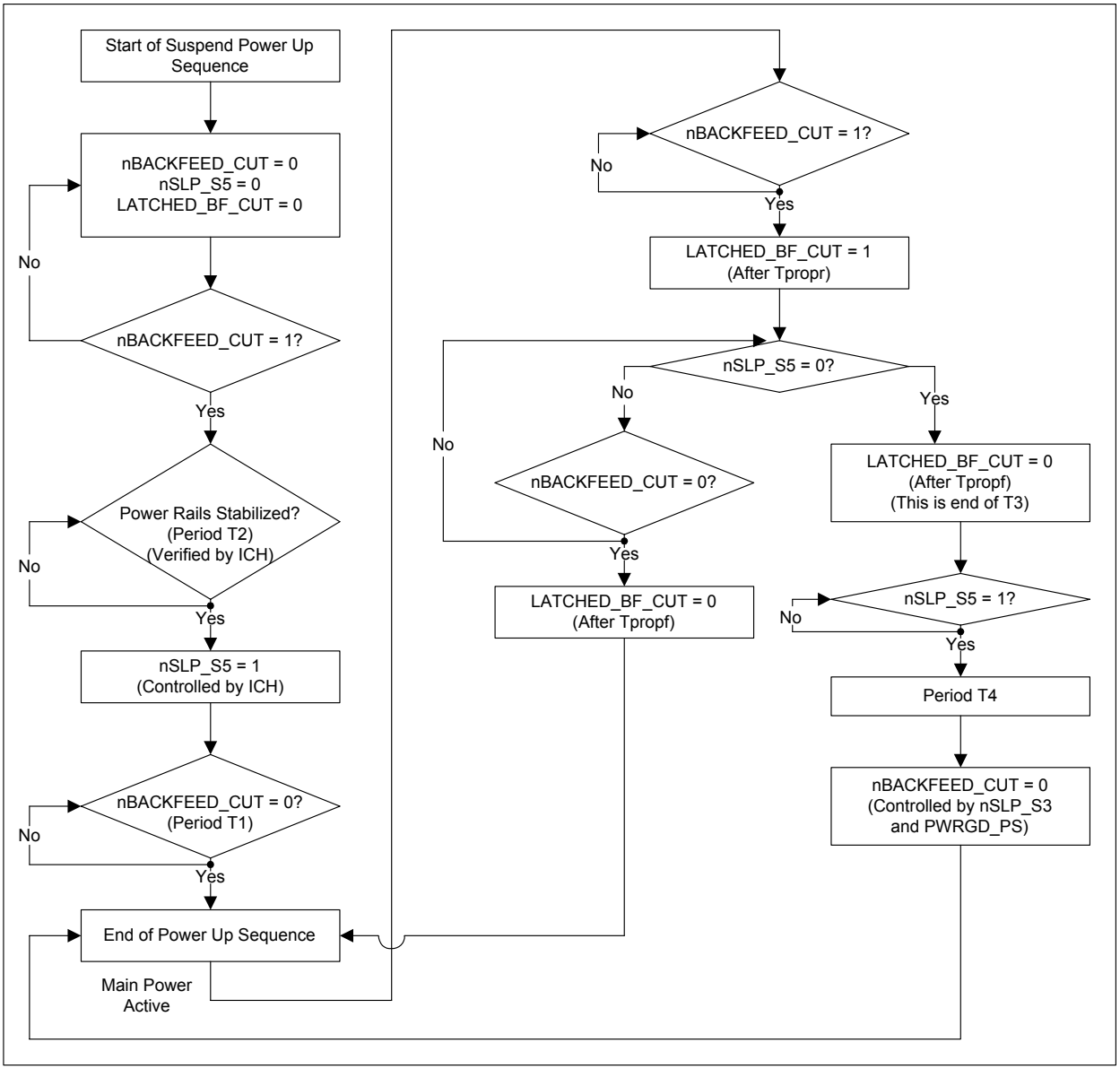


Figure 7.18 – Latched Backfeed Cut Flowchart

7.40 Resume Reset Logic

Table 7.47 – nRSMRST Pin

NAME	BUFFER	POWER WELL	DESCRIPTION
nRSMRST	O8	VTR	Resume Reset Output
V_5P0_STBY	PWR		5V Standby

The nRSMRST signal is the reset output for the ICH resume well. This signal is used as a power on reset signal as well as a brown-out sensor for the ICH.

The rising edge of nRSMRST is a delayed 3.3V buffered copy of V_5P0_STBY. This delay, t_{RESET_DELAY}, nominally 32ms, starts when V_5P0_STBY hits the trip point, V_{TRIP}. Note the nRSMRST will be inactive high after the t_{RESET_DELAY} only if VTR (3.3V) is present. Otherwise, nRSMRST will be active low beyond the t_{RESET_DELAY} – until VTR (3.3V) goes active. On the falling edge there is minimal delay, t_{RESET_FALL}. Note that V_{TRIP} shown in Figure 26 has a V_{TRIP_MIN} and a V_{TRIP_MAX}. See Table below for timing and voltage parameters.

Note that no internal clock is available during nRSMRST generation, so an internally generated delay is required. The requirements are loose enough that an onboard RC delay is permissible. This delay is only required at V_5P0_STBY power on and brown-out recovery.

See Table 13.7 for nRSMRST timing.

7.41 CNR Logic

Table 7.48 – CNR Pins

NAME	TYPE	POWER WELL	DESCRIPTION
nAUD_LNK_RST	I	VTR	Audio Link Reset Input
nCDC_DWN_ENAB/ GP24	IO12	VTR	CODEC Down Enable Input/GPIO
nCDC_DWN_RST	O12	VTR	CODEC Down Reset Output

The CNR CODEC Down Enable Circuitry is used in conjunction with soft audio and motherboards with a CNR slot. This feature allows the Basic Input / Output System (BIOS) to enable an audio CNR board. See figure and table below for implementation and definition of the input and output states. Note that these signals are required in all sleep states. The CNR circuitry is powered from VTR.

The nCDC_DWN_ENAB pin also functions as a GPIO. This allows BIOS to drive the pin to a known state if the motherboard requires it. Note that nCDC_DWN_RST still follows the nCDC_DWN_ENAB pin even when it is functioning as a GPIO output.

The nCDC_DWN_ENAB/GP24 pin functions as follows:

- When the nCDC_DWN_ENAB function is selected on GP24, it will be an input to the CNR logic. The polarity bit will not affect the input.
- If GP24 is programmed as GPIO output the GP data bit will control nCDC_DWN_ENAB input to the CNR logic. The data bit will also be reflected on the GP24 pin as an output under both VCC and VTR

power. The polarity bit will affect the output and input to the CNR logic. The output type select bit will also affect the GP24 pin.

- If GP24 is programmed as GPIO input, it will not affect the nCDC_DWN_ENAB input into the CNR logic. It will function as a normal GPIO input and can be used as a PME event.

Table 7.49 – CNR Logic Truth Table

INPUTS		OUTPUT
NAUD_LNK_RST	**NCDC_DWN_ENAB (NOTE)**	**nCDC_DWN_RST**
0	0	0
0	1	0
1	0	1
1	1	0

Note: If GP24 is programmed as GPIO output the GP data bit will also control nCDC_DWN_ENAB input to the CNR logic.

This follows the boolean equation:

(nAUD_LNK_RST)x($\overline{\text{nCDC\_DWN\_ENAB}}$)=nCDC_DWN_RST

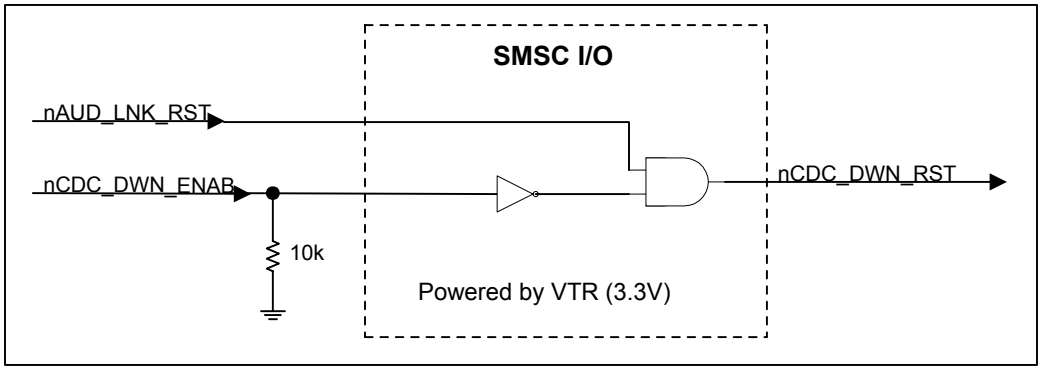


Figure 7.19 – CNR Circuit

See Table 13.6 for CNR timing.

Chapter 8 Power Control Runtime Registers

Table 8.1 shows the runtime registers summary in the Power Control logical Device. Table 8.2 shows the runtime registers description in the Power Control logical device. These runtime registers can only be accessed when LD_NUM bit in the TEST 7 configuration register is '0' (see Table 11.3). The register offsets are from the base address programmed in the Power Control logical device.

Table 8.1 – Power Control Runtime Registers Summary, LD_NUM Bit = 0

REGISTER OFFSET (hex)	TYPE	PCI Reset	VCC POR	VTR POR	SOFT RESET	REGISTER
00	R/W	-	-	0x00	-	PME_STS
01 – 03	R	-	-	-	-	Reserved – reads return 0
04	R/W	-	-	0x00	-	PME_EN
05 – 07	R	-	-	-	-	Reserved – reads return 0
08	R/W	-	-	0x00	-	PME_STS3
09	R/W	-	-	0x00	-	PME_STS2
0A	R/W	-	-	0x00	-	PME_STS1
0B	R	-	-	-	-	Reserved – reads return 0
0C	R/W	-	-	0x00	-	PME_EN3
0D	R/W	-	-	0x00	-	PME_EN2
0E	R/W	-	-	0x00	-	PME_EN1
0F	R	-	-	-	-	Reserved – reads return 0
10	R/W	-	-	0x03	-	LED
11	R/W	-	-	0x00	-	Keyboard Scan Code
12	R	-	-	0x00	-	Tach1 LSB
13	R	-	-	0x00	-	Tach1 MSB
14	R	-	-	0x00	-	Tach2 LSB
15	R	-	-	0x00	-	Tach2 MSB
16	R/W	-	-	0x80	-	nIO_PME Register
17	R/W	-	-	0x00	-	MSC_STS
18	R/W	0x01	0x01	-	-	Force Disk Change
19	R	-	-	-	-	Floppy Data Rate Select Shadow
1A	R	-	-	-	-	UART1 FIFO Control Shadow
1B	R/W	0xFF	0xFF	-	-	Interrupt Generating Register 1
1C	R/W	0xFF	0xFF	-	-	Interrupt Generating Register 2
1D	R	-	-	-	-	UART2 FIFO Control Shadow
1E-1F	R	-	-	-	-	Reserved – reads return 0

Table 8.2 – Power Control Runtime Registers Description, LD_NUM Bit = 0

NAME	REG OFFSET (Type)	DESCRIPTION
PME_STS Default = 0x00 on VTR POR	0x00 (R/W)	Bit[0] PME_Status = 0 (default) = 1 Set when LPC47M182 would normally assert the nIO_PME signal, independent of the state of the PME_En bit. Bit[7:1] Reserved PME_Status is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a "1" to PME_Status will clear it and cause the LPC47M182 to stop asserting nIO_PME, in enabled. Writing a "0" to PME_Status has no effect.
N/A	0x01 – 0x03 (R)	Bits[7:0] Reserved – reads return 0
PME_EN Default = 0x00 on VTR POR	0x04 (R/W)	Bit[0] PME_En = 0 nIO_PME signal assertion is disabled (default) = 1 Enables LPC47M182 to assert nIO_PME signal Bit[7:1] Reserved PME_En is not affected by Vcc POR, SOFT RESET or HARD RESET
N/A	0x05 – 0x07 (R)	Bits[7:0] Reserved – reads return 0
PME_STS3 Default = 0x00 on VTR POR	0x08 (R/W)	PME Wake Status Register 3 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a "1". Bit[0] GP20 Bit[1] GP21 Bit[2] GP22 Bit[3] GP23 Bits[7:4] Reserved The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Wake Status Register has no effect.
PME_STS2 Default = 0x00 on VTR POR	0x09 (R/W)	PME Wake Status Register 2 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a "1". Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Wake Status Register has no effect.

NAME	REG OFFSET (Type)	DESCRIPTION
PME_STS1 Default = 0x00 on VTR POR	0x0A (R/W)	PME Wake Status Register 1 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] Reserved (Note 1) Bit[1] RI2 Bit[2] RI1 Bit[3] KBD Bit[4] MOUSE Bit[5] SPEKEY (Wake on specific key) Bit[6] FAN_TACH1 (Note) Bit[7] FAN_TACH2 (Note) The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect. Note: ➢ When the GP1x/FAN_TACHx pin is configured as a GPIO (GPIO control register bit 2 = 0), the associated PME status bit will never be set. ➢ When the pin is configured for the tachometer function (GPIO control register bit 2 = 1) and then the function is switched to the GPIO function, the associated PME status bit will be cleared.
N/A	0x0B (R)	Bits[7:0] Reserved – reads return 0
PME_EN3 Default = 0x00 on VTR POR	0x0C (R/W)	PME Wake Status Register 3 This register is used to enable individual LPC47M182 PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] GP20 Bit[1] GP21 Bit[2] GP22 Bit[3] GP23 Bits[7:4] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.

NAME	REG OFFSET (Type)	DESCRIPTION
PME_EN2 Default = 0x00 on VTR POR	0x0D (R/W)	PME Wake Enable Register 2 This register is used to enable individual LPC47M182 PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.
PME_EN1 Default = 0x00 on VTR POR	0x0E (R/W)	PME Wake Enable Register 1 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] Reserved (Note 1) Bit[1] RI2 Bit[2] RI1 Bit[3] KBD Bit[4] MOUSE Bit[5] SPEKEY (Wake on specific key) Bit[6] FAN_TACH1 Bit[7] FAN_TACH2 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.
N/A	0x0F (R)	Bits[7:0] Reserved – reads return 0
LED Default = 0x03 on VTR POR	0x10 (R/W)	LED Register Bit[0] GRN_YLW 0 = Select YLW_LED if nSLP_S5 if high 1 = Select GRN_LED if nSLP_S5 is high Bit[1] SDY_BLK 0 = Blink at 0.67 Hz with 39.6% duty cycle (0.59375 sec high, 0.90625 low) if nSLP_S5 is high 1 = Steady if nSLP_S5 is high Bit[7:2] Reserved

NAME	REG OFFSET (Type)	DESCRIPTION
Keyboard Scan Code Default = 0x00 on VTR POR	0x11 (R/W)	Keyboard Scan Code Bit[0] LSB of Scan Code . . . . Bit[7] MSB of Scan Code
Tach1 LSB Default = 0x00 on VTR POR	0x12 (R)	This register is least significant 8-bit of the 16-bit Fan Tachometer 1 reading. Bit[0] FAN_TACH1 Reading Bit 0 … Bit[7] FAN_TACH1 Reading Bit 7
Tach1 MSB Default = 0x00 on VTR POR	0x13 (R)	This register is most significant 8-bit of the 16-bit Fan Tachometer 1 reading. Bit[0] FAN_TACH1 Reading Bit 8 … Bit[7] FAN_TACH1 Reading Bit 15
Tach2 LSB Default = 0x00 on VTR POR	0x14 (R)	This register is least significant 8-bit of the 16-bit Fan Tachometer 2 reading. Bit[0] FAN_TACH2 Reading Bit 0 … Bit[7] FAN_TACH2 Reading Bit 7
Tach2 MSB Default = 0x00 on VTR POR	0x15 (R)	This register is most significant 8-bit of the 16-bit Fan Tachometer 2 reading. Bit[0] FAN_TACH2 Reading Bit 8 … Bit[7] FAN_TACH2 Reading Bit 15
nIO_PME Register Default = 0x84 on VTR POR	0x16 (R/W) except Bits[3:2] are Read Only when Bit[3] set to '1'	Bit[0] nIO_PME Reserved Bit[1]nIO_PME Polarity : =1 Invert, =0 No Invert Bit[2] PWRGD_PLATFORM_SEL 1 = select PWRGD_PLATFORM delay (default) 0 = select no delay for PWRGD_PLATFORM Bit[3] PWRGD_PLAFORM LOCK 1 = When set to one, Bit[2] and Bit[3] of this register become RO. They remain RO until a VTR POR. 0 = no lock operation (Default) Bits[6:4] Reserved Bit[7] nIO_PME Output Type Select 1=Open Drain (default) 0=Push Pull
MSC_STS Default = 0x00 on VTR POR	0x17 (R/W)	Miscellaneous Status Register Bits[1:0] can be cleared by writing a 1 to their position (writing a 0 has no effect). Bit[0] Either Edge Triggered Interrupt Input 0 Status. This bit is set when an edge occurs on the GP21 pin. Bit[1] Either Edge Triggered Interrupt Input 1 Status. This bit is set when an edge occurs on the GP22 pin. Bit[7:2] Reserved. This bit always returns zero.

NAME	REG OFFSET (Type)	DESCRIPTION
Force Disk Change Default = 0x01 on VCC POR	0x18 (R/W)	Force Disk Change Bit[0] Force Disk Change for FDC0 0=Inactive 1=Active Bit[1] Reserved Force Change 0 can be written to 1 but is not clearable by software. Force Change 0 is cleared on nSTEP and nDS0 DSKCHG (FDC DIR Register, Bit 7) = (nDS0 AND Force Change 0) OR nDSKCHG Setting the Force Disk Change bit active '1' forces the FDD nDSKCHG input active. Bit[7:2] Reserved
Floppy Data Rate Select Shadow	0x19 (R)	Floppy Data Rate Select Shadow Bit[0] Data Rate Select 0 Bit[1] Data Rate Select 1 Bit[2] PRECOMP 0 Bit[3] PRECOMP 1 Bit[4] PRECOMP 2 Bit[5] Reserved Bit[6] Power Down Bit[7] Soft Reset
UART1 FIFO Control Shadow	0x1A (R)	UART FIFO Control Shadow 1 Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)
INT_GEN1 Default = 0xFF on VCC POR and HARD RESET	0x1B (R/W)	Interrupt Generating Register 1 (Note 2) 0=Corresponding Interrupt frame driven low in the SER IRQ stream. This must be enabled through the INT_G Configuration Register. Bit[0] Reserved Bit[1] nINT1 Bit[2] nINT2 Bit[3] nINT3 Bit[4] nINT4 Bit[5] nINT5 Bit[6] nINT6 Bit[7] nINT7 ***Note:*** To enable/disable this register see Logical Device A (0xF1)

NAME	REG OFFSET (Type)	DESCRIPTION
INT_GEN2 Default = 0xFF on VCC POR and HARD RESET	0x1C (R/W)	Interrupt Generating Register 2 (Note 2) 0=Corresponding Interrupt frame driven low in the SER IRQ stream. This must be enabled through the INT_G Configuration Register. Bit[0] nINT8 Bit[1] nINT9 Bit[2] nINT10 Bit[3] nINT11 Bit[4] nINT12 Bit[5] nINT13 Bit[6] nINT14 Bit[7] nINT15 ***Note:*** To enable/disable this register see Logical Device A (0xF1)
UART2 FIFO Control Shadow	0x1D (R)	UART FIFO Control Shadow 2 Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)
N/A	0x1E-0x1F (R)	Bits[7:0] Reserved – reads return 0

Note 1: These bits are R/W bit, but have no effect on circuit operation.
Note 2: These bits when read indicate the current bit status. These bits are set to “0” by writing “0” to individual bit locations in this register. Producing an interrupt in the SER_IRQ stream by setting these bits to “0” overrides other interrupt sources for the SER_IRQ stream. No other functional logic in the LPC47M182 sets bits in the register. These bits are only cleared by writing “1” to the bit location.

Chapter 9 GPIO Runtime Registers

Table 9.1 shows the runtime registers summary in the GPIO logical Device. Table 9.2 shows the runtime registers description in the GPIO logical device. These registers can only be accessed when LD_NUM bit in the TEST 7 configuration register is '0' (see Table 11.3). The register offsets are from the base address programmed in the GPIO logical device.

Table 9.1 – GPIO Runtime Registers Summary, LD_NUM = 0

REGISTER OFFSET (hex)	TYPE	PCI Reset	VCC POR	VTR POR	SOFT RESET	REGISTER
00	R/W	-	-	0x01	-	GP10
01	R/W	-	-	0x01	-	GP11
02	R/W	-	-	0x01	-	GP12
03	R/W	-	-	0x01	-	GP13
04	R/W	-	-	0x01	-	GP14
05	R/W	-	-	0x01	-	GP15
06	R/W	-	-	0x01	-	GP16
07	R/W	-	-	0x01	-	GP17
08	R/W	-	-	0x04	-	GP20
09	R/W	-	-	0x04	-	GP21
0A	R/W	-	-	0x04	-	GP22
0B	R/W	-	-	0x04	-	GP23
0C	R/W	-	-	0x05	-	GP24
0D-14	R	-	-	-	-	Reserved – reads return 0
15	R/W	-	-	0x00	-	GP1
16	R/W	-	-	0x00	-	GP2
17-1F	R	-	-	-	-	Reserved – reads return 0

Table 9.2 – GPIO Runtime Registers Description, LD_NUM = 0

NAME	REG OFFSET (Type)	DESCRIPTION
GP10 Default = 0x01 on VTR POR	0x00 (R/W)	General Purpose I/O bit 1.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bits[6:2] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP11 Default = 0x01 on VTR POR	0x01 (R/W)	General Purpose I/O bit 1.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bits[6:2] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP12 Default = 0x01 on VTR POR	0x02 (R/W)	General Purpose I/O bit 1.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bits[6:2] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP13 Default = 0x01 on VTR POR	0x03 (R/W)	General Purpose I/O bit 1.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bits[6:2] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP14 Default = 0x01 on VTR POR	0x04 (R/W)	General Purpose I/O bit 1.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bits[6:2] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP15 Default = 0x01 on VTR POR	0x05 (R/W)	General Purpose I/O bit 1.5 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bits[6:2] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP16 Default = 0x01 on VTR POR	0x06 (R/W)	General Purpose I/O bit 1.6 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=FAN_TACH1 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (Type)	DESCRIPTION
GP17 Default = 0x01 on VTR POR	0x07 (R/W)	General Purpose I/0 bit 1.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity :=1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=FAN_TACH2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP20 Default = 0x04 on VTR POR Note 1	0x08 (R/W)	General Purpose I/0 bit 2.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1= DDCSDA_5V 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP21 Default = 0x04 on VTR POR Note 1	0x09 (R/W)	General Purpose I/O bit 2.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bits[3:2] Alternate Function Select 11=Reserved 10=Either Edge Triggered Input 0 (Note 2) 01= DDCSCL_5V 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP22 Default = 0x04 on VTR POR Note 1	0x0A (R/W)	General Purpose I/O bit 2.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bits[3:2] Alternate Function Select 11=Reserved 10=Either Edge Triggered Input 0 (Note 2) 01= DDCSDA_3V 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP23 Default = 0x04 on VTR POR Note 1	0x0B (R/W)	General Purpose I/O bit 2.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=DDCSCL_3V 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (Type)	DESCRIPTION
GP24 Default = 0x05 on VTR POR	0x0C (R/W)	General Purpose I/O bit 2.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nCDC_DWN_ENAB 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
N/A	0x0D-0x14 (R)	Bits[7:0] Reserved – reads return 0
GP1 Default = 0x00 on VTR POR	0x15 (R/W)	General Purpose I/O Data Register 1 Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17
GP2 Default = 0x00 on VTR POR	0x16 (R/W)	General Purpose I/O Data Register 2 Bit[0] GP20 Bit[1] GP21 Bit[2] GP22 Bit[3] GP23 Bit[4] GP24 Bits[7:5] Reserved
N/A	0x17-0x1F (R)	Bits[7:0] Reserved – reads return 0

Note 1: The In/Out, Polarity and Output Type Select Bits do not apply when DDCSCL/DDCSDA signals are selected.
Note 2: If the EETI function is selected for this GPIO then both a high-to-low and low-to-high edge will set the PME and MSC status bits.

Chapter 10 Runtime Register Block Runtime Registers

Table 10.1 shows the runtime register summary. The Runtime Register Block runtime registers can only be accessed when LD_NUM bit in the TEST 7 configuration register is '1'. See "Power Control Runtime Registers" section and "GPIO Runtime Registers" section for description of these registers. Note these offsets replace the register offsets defined in the Power Control logical device and GPIO logical device when LD_NUM bit is '1'

Table 10.1 – Runtime Register Block Runtime Registers Summary

REGISTER OFFSET (HEX)	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	REGISTER
00	R/W	-	-	0x00	-	PME_STS
01-03	R	-	-	-	-	Reserved – reads return 0
04	R/W	-	-	0x00	-	PME_EN
05-07	R	-	-	-	-	Reserved – reads return 0
08	R/W	-	-	0x00	-	PME_STS3
09	R/W	-	-	0x00	-	PME_STS2
0A	R/W	-	-	0x00	-	PME_STS1
0B	R	-	-	-	-	Reserved – reads return 0
0C	R/W	-	-	0x00	-	PME_EN3
0D	R/W	-	-	0x00	-	PME_EN2
0E	R/W	-	-	0x00	-	PME_EN1
0F	R	-	-	-	-	Reserved – reads return 0
10	R/W	-	-	0x03	-	LED
11	R/W	-	-	0x00	-	Keyboard Scan Code
12	R	-	-	0x00	-	Tach1 LSB
13	R	-	-	0x00	-	Tach1 MSB
14	R	-	-	0x00	-	Tach2 LSB
15	R	-	-	0x00	-	Tach2 MSB
16	R/W	-	-	0x80	-	nIO_PME Register
17	R/W	-	-	0x00	-	MSC_STS
18	R/W	0x01	0x01	-	-	Force Disk Change
19	R	-	-	-	-	Floppy Data Rate Select Shadow
1A	R	-	-	-	-	UART1 FIFO Control Shadow
1B	R/W	0xFF	0xFF	-	-	Interrupt Generating Register 1
1C	R/W	0xFF	0xFF	-	-	Interrupt Generating Register 2
1D	R	-	-	-	-	UART2 FIFO Control Shadow
1F	R	-	-	-	-	Reserved – reads return 0
20	R/W	-	-	0x01	-	GP10
21	R/W	-	-	0x01	-	GP11
22	R/W	-	-	0x01	-	GP12
23	R/W	-	-	0x01	-	GP13
24	R/W	-	-	0x01	-	GP14
25	R/W	-	-	0x01	-	GP15

REGISTER OFFSET (HEX)	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	REGISTER
26	R/W	-	-	0x01	-	GP16
27	R/W	-	-	0x01	-	GP17
28	R/W	-	-	0x04	-	GP20
29	R/W	-	-	0x04	-	GP21
2A	R/W	-	-	0x04	-	GP22
2B	R/W	-	-	0x04	-	GP23
2C	R/W	-	-	0x05	-	GP24
2D-34	R	-	-	-	-	Reserved – reads return 0
35	R/W	-	-	0x00	-	GP1
36	R/W	-	-	0x00	-	GP2
37-3F	R	-	-	-	-	Reserved – reads return 0

Chapter 11 Configuration

The Configuration of the LPC47M182 is very flexible and is based on the configuration architecture implemented in typical Plug-and-Play components. The LPC47M182 is designed for motherboard applications in which the resources required by their components are known. With its flexible resource allocation architecture, the LPC47M182 allows the BIOS to assign resources at POST.

11.1 System Elements

11.1.1 Primary Configuration Address Decoder

After a hard reset (nPCI_RESET pin asserted) or Vcc Power On Reset the LPC47M182 is in the Run Mode with all logical devices disabled. The logical devices may be configured through two standard Configuration I/O Ports (INDEX and DATA) by placing the LPC47M182 into Configuration Mode.

The BIOS uses these configuration ports to initialize the logical devices at POST. The INDEX and DATA ports are only valid when the LPC47M182 is in Configuration Mode.

The CONFIG PORT's I/O address is set to 0x02E at power-up. Once powered up the configuration port base address can be changed through configuration registers CR26 and CR27.

The INDEX and DATA ports are effective only when the chip is in the Configuration State.

PORT NAME	BASE ADDRESS	TYPE
CONFIG PORT (Note)	0x02E	Write
INDEX PORT (Note)	0x02E	Read/Write
DATA PORT	INDEX PORT + 1	Read/Write

Note: The configuration port base address can be relocated through CR26 and CR27.

11.1.2 Entering the Configuration State

The device enters the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0x55>

11.1.3 Exiting the Configuration State

The device exits the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0xAA>

11.1.4 CONFIGURATION SEQUENCE

To program the configuration registers, the following sequence must be followed:

1. Enter Configuration Mode
2. Configure the Configuration Registers
3. Exit Configuration Mode.

11.1.5 Enter Configuration Mode

To place the chip into the Configuration State the Config Key is sent to the chip's CONFIG PORT. The config key consists of 0x55 written to the CONFIG PORT. Once the configuration key is received correctly the chip enters into the Configuration State (The auto Config ports are enabled).

11.1.6 Configuration Mode

The system sets the logical device information and activates desired logical devices through the INDEX and DATA ports. In configuration mode, the INDEX PORT is located at the CONFIG PORT address and the DATA PORT is at INDEX PORT address + 1.

The desired configuration registers are accessed in two steps:

a) Write the index of the Logical Device Number Configuration Register (i.e., 0x00 for FDC) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT

b) Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

Note: If accessing the Global Configuration Registers, step (a) is not required.

11.1.7 Exit Configuration Mode

To exit the Configuration State the system writes 0xAA to the CONFIG PORT. The chip returns to the RUN State.

Note: Only two states are defined (Run and Configuration). In the Run State the chip will always be ready to enter the Configuration State.

11.1.8 Programming Example

The following is an example of a configuration program in Intel 8086 assembly language.

```
;---------------------------------------------.
; ENTER CONFIGURATION MODE   |
;---------------------------------------------‘
MOV     DX,02EH
MOV     AX,055H
OUT     DX,AL
;---------------------------------------------.
; CONFIGURE REGISTER CRE0,   |
; LOGICAL DEVICE 8                  |
;---------------------------------------------‘
MOV     DX,02EH
MOV     AL,07H
OUT     DX,AL ;Point to LD# Config Reg
MOV     DX,02FH
MOV     AL, 08H
OUT     DX,AL;Point to Logical Device 8
;
MOV     DX,02EH
MOV     AL,E0H
OUT     DX,AL    ; Point to CRE0
MOV     DX,02fH
MOV     AL,02H
OUT     DX,AL    ; Update CRE0
;---------------------------------------------.
; EXIT CONFIGURATION MODE    |
;---------------------------------------------‘
MOV     DX,02EH
MOV     AX,0AAH
OUT     DX,AL
```

Notes:

1) HARD RESET: nPCI_RESET pin asserted

2) SOFT RESET: Bit 0 of Configuration Control register set to one

3) All host accesses are blocked for 500µs after Vcc POR (see Power-up Timing Diagram)

LD_NUM Bit

The LD_NUM bit in the TEST 7 global configuration register (0x29) is used to select between the logical device numbering in the LPC47M182. See the TEST 7 register for LD_NUM bit description. Table 11.1 and Table 11.2 summarize the logical device registers when LD_NUM bit is 0 and 1.

Table 11.1– LPC47M182 Configuration Registers Summary, LD_NUM bit = 0

INDEX	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	CONFIGURATION REGISTER
GLOBAL CONFIGURATION REGISTERS						
0x02	W	0x00	0x00	0x00	-	Config Control
0x03	R	-	-	-	-	Reserved – reads return 0
0x07	R/W	0x00	0x00	0x00	0x00	Logical Device Number
0x20	R	0x74	0x74	0x74	0x74	Device ID – hard wired
0x21	R	-	-	-	-	Device Rev – hard wired to current version
0x22	R/W	0x00	0x00	0x00	0x00	Power Control
0x23	R	-	-	-	-	Reserved – reads return 0
0x24	R/W	0x44	0x44	0x44	-	OSC
0x26	R/W	0x2E	0x2E	-	-	Configuration Port Address Byte 0 (Low Byte)
0x27	R/W	0x00	0x00	-	-	Configuration Port Address Byte 1 (High Byte)
0x28	R/W	-	0x00	0x00	-	TEST 8
0x29	R/W	0x00	0x00	0x00	-	TEST 7
0x2A	R/W	-	0x00	0x00	-	TEST 6
0x2B	R/W	-	0x00	0x00	-	TEST 4
0x2C	R/W	-	0x00	0x00	-	TEST 5
0x2D	R/W	-	0x00	0x00	-	TEST 1
0x2E	R/W	-	0x00	0x00	-	TEST 2
0x2F	R/W	-	0x00	0x00	-	TEST 3
LOGICAL DEVICE 0 CONFIGURATION REGISTERS (FDD)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x03	0x03	0x03	0x03	Primary Base I/O Address High Byte
0x61	R/W	0xF0	0xF0	0xF0	0xF0	Primary Base I/O Address Low Byte
0x70	R/W	0x06	0x06	0x06	0x06	Primary Interrupt Select
0x74	R/W	0x02	0x02	0x02	0x02	DMA Channel Select
0xF0	R/W	0x0E	0x0E	0x0E	-	FDD Mode Register
0xF1	R/W	0x00	0x00	0x00	-	FDD Option Register
0xF2	R/W	0xFF	0xFF	0xFF	-	FDD Type Register
0xF4	R/W	0x00	0x00	0x00	-	FDD0
0xF8	R/W	0x24	0x24	0x24	-	FDC Mapping Register
LOGICAL DEVICE 1 CONFIGURATION REGISTERS (Parallel Port)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0x74	R/W	0x04	0x04	0x04	0x04	DMA Channel Select
0xF0	R/W	0x3C	0x3C	0x3C	-	Parallel Port Mode Register
0xF1	R/W	0x00	0x00	0x00	-	Parallel Port Mode Register 2
0xF8	R/W	0x08	0x08	0x08	-	PP Mapping Register
LOGICAL DEVICE 2 CONFIGURATION REGISTERS (Serial Port 2)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate

INDEX	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	CONFIGURATION REGISTER
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 2 Mode Register
0xF1	R/W	0x02	0x02	0x02	-	IR Options Register
0xF2	R/W	0x03	0x03	0x03	-	IR Half Duplex Timeout
LOGICAL DEVICE 3 CONFIGURATION REGISTERS (Serial Port 1)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 1 Mode Register
LOGICAL DEVICE 4 CONFIGURATION REGISTERS (Power Control)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0XF0	R/W	-	-	0X00	-	CLOCKI32
0xF1	R/W	0x00	0x00	0x00	0x00	INT_G Register
LOGICAL DEVICE 5 CONFIGURATION REGISTERS (Mouse)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
LOGICAL DEVICE 6 CONFIGURATION REGISTERS (Keyboard)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00 (Note 1)	-	KRESET and GateA20 Select
LOGICAL DEVICE 7 CONFIGURATION REGISTERS (GPIO)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte

Note: Reserved registers are read-only, reads return 0.

Note 1. Bits[7:5] of this register reset on VTR POR only.

Table 11.2 – LPC47M182 Configuration Register Summary, LD_NUM bit = 1

INDEX	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	CONFIGURATION REGISTER
GLOBAL CONFIGURATION REGISTERS						
0x02	W	0x00	0x00	0x00	-	Config Control
0x03	R	-	-	-	-	Reserved – reads return 0
0x07	R/W	0x00	0x00	0x00	0x00	Logical Device Number
0x20	R	0x74	0x74	0x74	0x74	Device ID – hard wired
0x21	R	-	-	-	-	Device Rev – hard wired to current version
0x22	R/W	0x00	0x00	0x00	0x00	Power Control
0x23	R	-	-	-	-	Reserved – reads return 0
0x24	R/W	0x44	0x44	0x44	-	OSC
0x26	R/W	0x2E	0x2E	-	-	Configuration Port Address Byte 0 (Low Byte)
0x27	R/W	0x00	0x00	-	-	Configuration Port Address Byte 1 (High Byte)
0x28	R/W	-	0x00	0x00	-	TEST 8
0x29	R/W	0x01	0x01	0x01	-	TEST 7
0x2A	R/W	-	0x00	0x00	-	TEST 6
0x2B	R/W	-	0x00	0x00	-	TEST 4
0x2C	R/W	-	0x00	0x00	-	TEST 5
0x2D	R/W	-	0x00	0x00	-	TEST 1
0x2E	R/W	-	0x00	0x00	-	TEST 2
0x2F	R/W	-	0x00	0x00	-	TEST 3
LOGICAL DEVICE 0 CONFIGURATION REGISTERS (FDD)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x03	0x03	0x03	0x03	Primary Base I/O Address High Byte
0x61	R/W	0xF0	0xF0	0xF0	0xF0	Primary Base I/O Address Low Byte
0x70	R/W	0x06	0x06	0x06	0x06	Primary Interrupt Select
0x74	R/W	0x02	0x02	0x02	0x02	DMA Channel Select
0xF0	R/W	0x0E	0x0E	0x0E	-	FDD Mode Register
0xF1	R/W	0x00	0x00	0x00	-	FDD Option Register
0xF2	R/W	0xFF	0xFF	0xFF	-	FDD Type Register
0xF4	R/W	0x00	0x00	0x00	-	FDD0
0xF8	R/W	0x24	0x24	0x24	-	FDC Mapping Register
LOGICAL DEVICE 1 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE 2 CONFIGURATION REGISTERS (Serial Port 2)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 2 Mode Register

INDEX	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	CONFIGURATION REGISTER
0xF1	R/W	0x02	0x02	0x02	-	IR Options Register
0xF2	R/W	0x03	0x03	0x03	-	IR Half Duplex Timeout
LOGICAL DEVICE 3 CONFIGURATION REGISTERS (Parallel Port)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0x74	R/W	0x04	0x04	0x04	0x04	DMA Channel Select
0xF0	R/W	0x3C	0x3C	0x3C	-	Parallel Port Mode Register
0xF1	R/W	0x00	0x00	0x00	-	Parallel Port Mode Register 2
0xF8	R/W	0x08	0x08	0x08	-	PP Mapping Register
LOGICAL DEVICE 4 CONFIGURATION REGISTERS (Serial Port 1)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 1 Mode Register
LOGICAL DEVICE 5 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE 6 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE 7 CONFIGURATION REGISTERS (Keyboard)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0x72	R/W	0x00	0x00	0x00	0x00	Secondary Interrupt Select
0xF0	R/W	0x00	0x00	0x00 (Note 1)	-	KRESET and GateA20 Select
LOGICAL DEVICE 8 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE 9 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE A CONFIGURATION REGISTERS (Runtime Register Block)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0XF0	R/W	-	-	0X00	-	CLOCKI32
0xF1	R/W	0x00	0x00	0x00	0x00	INT_G Register
LOGICAL DEVICE B CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE C CONFIGURATION REGISTERS (Reserved)						

Note: Reserved registers are read-only, reads return 0.

Note 1. Bits[7:6, 5 and 1] of KRESET and GateA20 Select register reset on VTR POR only.

11.2 Chip Level (Global) Control/Configuration Registers[0x00-0x2F]

The chip-level (global) registers lie in the address range [0x00-0x2F]. The design MUST use all 8 bits of the ADDRESS Port for register selection. All unimplemented registers and bits ignore writes and return zero when read.

The INDEX PORT is used to select a configuration register in the chip. The DATA PORT is then used to access the selected register. These registers are accessible only in the Configuration Mode.

Table 11.3 – Chip Level Registers

REGISTER	ADDRESS	DESCRIPTION
CHIP (GLOBAL) CONTROL REGISTERS		
	0x00 - 0x01	Reserved - Writes are ignored, reads return 0.
Config Control Default = 0x00 on VCC POR, VTR POR and HARD RESET	0x02 W	The hardware automatically clears this bit after the write, there is no need for software to clear the bit. Bit 0 = 1: Soft Reset. Bits 7:1 Reserved Refer to the “Configuration Registers” table for the soft reset value for each register.
	0x03 - 0x06	Reserved - Writes are ignored, reads return 0.
Logical Device # Default = 0x00 on VCC POR, VTR POR, SOFT RESET and HARD RESET	0x07 R/W	A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device. Note: The Activate command operates only on the selected logical device.
Card Level Reserved	0x08 - 0x1F	Reserved - Writes are ignored, reads return 0.
CHIP LEVEL, SMSC DEFINED		
Device ID Hard wired = 0x74	0x20 R	A read only register which provides device identification. Bits[7:0] = 0x74 when read.
Device Rev Hard wired = Current Revision	0x21 R	A read only register which provides device revision information. Bits[7:0] = current revision when read.

REGISTER	ADDRESS	DESCRIPTION
CHIP (GLOBAL) CONTROL REGISTERS		
PowerControl Default = 0x00 on VCC POR, VTR POR, SOFT RESET and HARD RESET	0x22 R/W	Bit[0] FDC Power Bit[1] Reserved Bit[2] Reserved Bit[3] Parallel Port Power Bit[4] Serial Port 1 Power Bit[5] Serial Port 2 Power Bit[6] Reserved Bit[7] Reserved 0 = Power Off or Disabled 1 = Power On or Enabled
	0x23 R	Reserved - Writes are ignored, reads return 0.
OSC Default = 0x44, on on VCC POR, VTR POR and HARD RESET	0x24 R/W	Bit[0] Reserved Bit [1] PLL Control = 0 PLL is on (backward Compatible) = 1 PLL is off Bits[3:2] OSC = 01Osc is on, BRG clock is on. = 10Same as above (01) case. = 00Osc is on, BRG Clock Enabled. = 11Osc is off, BRG clock is disabled. Bit [5:4] Reserved, set to zero Bit [6] 16-Bit Address Qualification = 0 12-Bit Address Qualification = 1 16-Bit Address Qualification *Note*: For normal operation, bit 6 should be set. Bit[7] Reserved
Chip Level Vendor Defined	0x25	Reserved - Writes are ignored, reads return 0.
Configuration Address Byte 0 Default =0x2E on VCC POR and HARD RESET	0x26	Bit[7:1] Configuration Address Bits [7:1] Bit[0] = 0
Configuration Address Byte 1 Default = 0x00 on VCC POR and HARD RESET	0x27	Bit[7:0] Configuration Address Bits [15:8] See Note 1
TEST 8 Default = 0x00 on VCC POR and VTR POR	0x28 R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.

REGISTER	ADDRESS	DESCRIPTION
CHIP (GLOBAL) CONTROL REGISTERS		
TEST 7 Default = 0x00 (when pin 117 is NC) 0x01 (when pin 117 is connected to VTR) on VCC POR, VTR POR and HARD RESET	0x29 R/W	Bit[0] LD_NUM = 0 New LD Numbering (selected when pin 117 is NC) = 1 SMSC LD Numbering (selected when pin 117 is connected to VTR) Pin 117 is used to select the mode of the logical device numbering. This pin affects the LD_NUM bit as follows: ▪ The pin has an internal pull-down resistor that selects the non-SMSC mode. To select this mode, the pin should be left unconnected. This configuration clears the LD_NUM bit to '0' and the associated functionality corresponds to the existing functionality in the part when the LD_NUM bit=0. ▪ Connecting this pin to VTR will select the SMSC mode of the logical device numbering. This configuration sets the LD_NUM bit to '1' and the associated functionality corresponds to the existing functionality in the part when the LD_NUM bit=1. Bits[7:1] Reserved
TEST 6 Default = 0x00, on VCC POR and VTR POR	0x2A R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.
TEST 4 Default = 0x00, on VCC POR and VTR POR	0x2B R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.
TEST 5 Default = 0x00, on VCC POR and VTR POR	0x2C R/W	Bit[7] Test Mode: Reserved for SMSC. Users should not write to this bit, may produce undesired results. Bit[6] 8042 Reset: 1 = put the 8042 into reset 0 = take the 8042 out of reset Bits[5:0] Test Mode: Reserved for SMSC. Users should not write to this bit, may produce undesired results.
TEST 1 Default = 0x00, on VCC POR and VTR POR	0x2D R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.
TEST 2 Default = 0x00, on VCC POR and VTR POR	0x2E R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.

REGISTER	ADDRESS	DESCRIPTION
CHIP (GLOBAL) CONTROL REGISTERS		
TEST 3 Default = 0x00, on VCC POR and VTR POR	0x2F R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.

Note 1: To allow the selection of the configuration address to a user defined location, these Configuration Address Bytes are used. There is no restriction on the address chosen, except that A0 is 0, that is, the address must be on an even byte boundary. As soon as both bytes are changed, the configuration space is moved to the specified location with no delay (**Note:** Write byte 0, then byte 1; writing CR27 changes the base address).

11.3 Logical Device Configuration/Control Registers [0x30-0xFF]

These registers are used to access the registers that are assigned to each logical device. The logical devices are Floppy, Parallel, Serial Port, Keyboard Controller, Power Control and GPIO. A separate set (bank) of control and configuration registers exists for each logical device and is selected with the Logical Device # Register (0x07).

The INDEX PORT is used to select a specific logical device register. These registers are then accessed through the DATA PORT.

The Logical Device registers are accessible only when the device is in the Configuration State. The logical register addresses are shown in the table below.

Table 11.4 – Logical Device Registers

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION
Activate Default = 0x00 on VCC POR, VTR POR, HARD RESET and SOFT RESET	(0x30)	Bits[7:1] Reserved, set to zero. Bit[0] = 1 Activates the logical device currently selected through the Logical Device # register. = 0 Logical device currently selected is inactive **Note:** A logical device will be active and powered up according to the following equation unless otherwise specified: DEVICE ON (ACTIVE) = (Activate Bit SET or Pwr/Control Bit SET). The Logical device's Activate Bit and its Pwr/Control Bit are linked such that setting or clearing one sets or clears the other.
Logical Device Control	(0x31-0x37)	Reserved – Writes are ignored, reads return 0.
Logical Device Control	(0x38-0x3F)	Vendor Defined - Reserved - Writes are ignored, reads return 0.
Memory Base Address	(0x40-0x5F)	Reserved – Writes are ignored, reads return 0.

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION
I/O Base Address (see Device Base I/O Address Table) Default = 0x00 on VCC POR, VTR POR, HARD RESET and SOFT RESET	(0x60-0x6F) 0x60,2,... = addr[15:8] 0x61,3,... = addr[7:0]	Registers 0x60 and 0x61 set the base address for the device. If more than one base address is required, the second base address is set by registers 0x62 and 0x63. Unused registers will ignore writes and return zero when read. Note: If the I/O Base Addr of the logical device is not within the Base I/O range as shown in the Logical Device I/O map, then read or write is not valid and is ignored.
Interrupt Select Defaults : 0x70 = 0x00 or 0x06 (Note) on VCC POR, VTR POR, HARD RESET and SOFT RESET 0x72 = 0x00, on VCC POR, VTR POR, HARD RESET and SOFT RESET	(0x70,0x72)	0x70 is implemented for each logical device. Refer to Interrupt Configuration Register description. Only the keyboard controller uses Interrupt Select register 0x72. Unused register (0x72) will ignore writes and return zero when read. Interrupts default to edge high (ISA compatible). Refer to Table 11.5 **Note:** The default value of the Primary Interrupt Select register for logical device 0 is 0x06.
	(0x71,0x73)	Reserved - not implemented. These register locations ignore writes and return zero when read.
DMA Channel Select Default = 0x02 or 0x04 (Note) on VCC POR, VTR POR, HARD RESET and SOFT RESET	(0x74,0x75)	Only 0x74 is implemented for FDC and Parallel port. 0x75 is not implemented and ignores writes and returns zero when read. Refer to Table 11.6. **Note:** The default value of the DMA Channel Select register for logical device 0 (FDD) is 0x02 and for logical device 4 (UART) is 0x04.
32-Bit Memory Space Configuration	(0x76-0xA8)	Reserved - not implemented. These register locations ignore writes and return zero when read.
Logical Device	(0xA9-0xDF)	Reserved - not implemented. These register locations ignore writes and return zero when read.
Logical Device Configuration	(0xE0-0xFE)	Reserved – Vendor Defined (see SMSC defined Logical Device Configuration Registers).
Reserved	0xFF	Reserved

Table 11.5 – Primary Interrupt Select Configuration Register Description

NAME	REG INDEX	DEFINITION
Primary Interrupt Select Default=0x00 or 0x06 (Note 1) on VCC POR, VTR POR, HARD RESET and SOFT RESET	0x70 (R/W)	Bits[3:0] selects which interrupt is used for the primary Interrupt. 0x00= no interrupt selected 0x01= IRQ1 0x02= IRQ2 0x03= IRQ3 0x04= IRQ4 0x05= IRQ5 0x06= IRQ6 0x07= IRQ7 0x08= IRQ8 0x09= IRQ9 0x0A= IRQ10 0x0B= IRQ11 0x0C= IRQ12 0x0D= IRQ13 0x0E= IRQ14 0x0F= IRQ15 **Note:** All interrupts are edge high (except ECP/EPP)

Note:

An Interrupt is activated by setting the Interrupt Request Level Select 0 register to a non-zero value AND:

- For the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register.
- For the PP logical device by setting IRQE, bit D4 of the Control Port and in addition
- For the PP logical device in ECP mode by clearing serviceIntr, bit D2 of the ecr.
- For the Serial Port logical device by setting any combination of bits D0-D3 in the IER
- and by setting the OUT2 bit in the UART's Modem Control (MCR) Register.
- For the KYBD logical device (refer to the KYBD controller section of this spec).
-

IRQs are disabled if not used/selected by any Logical Device. Refer to Note A.
All IRQ's are available in Serial IRQ mode.

Note 1: The default value of the Primary Interrupt Select register for logical device 0 is 0x06.

Table 11.6 – DMA Channel Select Configuration Register Description

NAME	REG INDEX	DEFINITION
DMA Channel Select Default=0x02 or 0x04 (Note 1) on VCC POR, VTR POR, HARD RESET and SOFT RESET	0x74 (R/W)	Bits[2:0] select the DMA Channel. 0x00= Reserved 0x01= DMA1 0x02= DMA2 0x03= DMA3 0x04-0x07= No DMA active

Note: A DMA channel is activated by setting the DMA Channel Select register to [0x01-0x03] AND :

- For the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register.
- For the PP logical device in ECP mode by setting dmaEn, bit D3 of the ecr.

The DMA channel must be disabled if not used/selected by any Logical Device. Refer to Note A.

Note 1: The default value of the DMA Channel Select register for logical device 0 (FDD) is 0x02 and for logical device 3 is 0x04.

Note A. Logical Device IRQ and DMA Operation

1. IRQ and DMA Enable and Disable: Any time the IRQ or DMA channel for a logical block is disabled by a register bit in that logical block, the IRQ and/or DMA channel must be disabled. This is in addition to the IRQ and DMA channel disabled by the Configuration Registers (active bit or address not valid).

A. FDC: For the following cases, the IRQ and DMA channel used by the FDC are disabled.

Digital Output Register (Base+2) bit D3 (DMAEN) set to "0".
The FDC is in power down (disabled).

B. Serial Port:

Modem Control Register (MCR) Bit D2 (OUT2) - When OUT2 is a logic "0", the serial port interrupt is disabled.

C. Parallel Port:

I. SPP and EPP modes: Control Port (Base+2) bit D4 (IRQE) set to "0", IRQ is disabled.
ii. ECP Mode:
(1) (DMA) dmaEn from ecr register. See table.
(2) IRQ - See table.

MODE (FROM ECR REGISTER)		IRQ CONTROLLED BY	DMA CONTROLLED BY
000	PRINTER	IRQE	dmaEn
001	SPP	IRQE	dmaEn
010	FIFO	(on)	dmaEn
011	ECP	(on)	dmaEn
100	EPP	IRQE	dmaEn
101	RES	IRQE	dmaEn
110	TEST	(on)	dmaEn
111	CONFIG	IRQE	dmaEn

D. Keyboard Controller: Refer to the KBD section of this spec.

Logical Device I/O Address

Table 11.7 and Table 11.8 summarize the logical device I/O addresses when LD_NUM bit is 0 and 1.

Table 11.7 – Logical Device I/O Address, LD_NUM Bit = 0

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (NOTE 1)	FIXED BASE OFFSETS
0x00	FDC	0x60,0x61	[0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : SRA +1 : SRB +2 : DOR +3 : TSR +4 : MSR/DSR +5 : FIFO +7 : DIR/CCR
0x01	Parallel Port	0x60,0x61	[0x0100:0x0FFC] ON 4 BYTE BOUNDARIES (EPP Not supported) or [0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : Data/ecpAfifo +1 : Status +2 : Control +400h : cfifo/ecpDfifo/tfifo/cnfgA +401h : cnfgB +402h : ecr
			(all modes supported, EPP is only available when the base address is on an 8-byte boundary)	+3 : EPP Address +4 : EPP Data 0 +5 : EPP Data 1 +6 : EPP Data 2 +7 : EPP Data 3
0x02	Serial Port 2	0x60,0x61	[0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MSR +5 : LSR +6 : MSR +7 : SCR
0x03	Serial Port	0x60,0x61	[0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MSR +5 : LSR +6 : MSR +7 : SCR
0x04	Power Control	0x60,0x61	[0x0000:0x0FE0] on 32-byte boundaries	+00 : PME Status . . . +1F : Reserved (See Table 8.1 for Full List)
0x05	Mouse	n/a	Not Relocatable	+0 : Data Register +4 : Command/Status Reg.
0x06	KYBD	n/a	Not Relocatable Fixed Base Address: 60,64	+0 : Data Register +4 : Command/Status Reg.
0x07	GPIO	0x60,0x61	[0x0000:0x0FE0] on 32-byte boundaries	+00 : GP10 . . +1F : Reserved (See Table 9.1 for Full List)

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (NOTE 1)	FIXED BASE OFFSETS
Config. Port	Config. Port	0x26, 0x27	0x0100:0x0FFE On 2 byte boundaries	See Configuration Register Summary table. Accessed through the index and DATA ports located at the Configuration Port address and the Configuration Port address +1 respectively.

Note 1: This chip uses address bits [A11:A0] to decode the base address of each of its logical devices. Bit 6 of the OSC Global Configuration Register (CR24) must be set to '1' and Address Bits [A15:A12] must be '0' for 16 bit address qualification.

Table 11.8 – Logical Device I/O Address, LD_NUM Bit = 1

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (NOTE 1)	FIXED BASE OFFSETS
0x00	FDC	0x60,0x61	[0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : SRA +1 : SRB +2 : DOR +3 : TSR +4 : MSR/DSR +5 : FIFO +7 : DIR/CCR
0x01	Reserved	n/a	n/a	n/a
0x02	Serial Port 2	0x60,0x61	[0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MSR +5 : LSR +6 : MSR +7 : SCR
0x03	Parallel Port	0x60,0x61	[0x0100:0x0FFC] ON 4 BYTE BOUNDARIES (EPP Not supported) or [0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : Data/ecpAfifo +1 : Status +2 : Control +400h : cfifo/ecpDfifo/tfifo/cnfgA +401h : cnfgB +402h : ecr
			(all modes supported, EPP is only available when the base address is on an 8-byte boundary)	+3 : EPP Address +4 : EPP Data 0 +5 : EPP Data 1 +6 : EPP Data 2 +7 : EPP Data 3
0x04	Serial Port 1	0x60,0x61	[0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MSR +5 : LSR +6 : MSR +7 : SCR
0x05	Reserved	n/a	n/a	n/a
0x06	Reserved	n/a	n/a	n/a
0x07	KYBD	n/a	Not Relocatable Fixed Base Address: 60,64	+0 : Data Register +4 : Command/Status Reg.

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (NOTE 1)	FIXED BASE OFFSETS
0x08	Reserved	n/a	n/a	n/a
0x09	Reserved	n/a	n/a	n/a
0x0A	Runtime Register Block	0x60,0x61	[0x0000:0x0FC0] on 64-byte boundaries	+00 : PME Status . . . +3F : Reserved
0x0B	Reserved	n/a	n/a	n/a
Config. Port	Config. Port	0x26, 0x27	0x0100:0x0FFE On 2 byte boundaries	See Configuration Register Summary table. Accessed through the index and DATA ports located at the Configuration Port address and the Configuration Port address +1 respectively.

Note 1: This chip uses address bits [A11:A0] to decode the base address of each of its logical devices. Bit 6 of the OSC Global Configuration Register (CR24) must be set to '1' and Address Bits [A15:A12] must be '0' for 16 bit address qualification.

11.4 SMSC Defined Logical Device Configuration Registers

The SMSC Specific Logical Device Configuration Registers reset to their default values only on hard resets generated by Vcc or VTR POR (as shown) or the nPCI_RESET signal. These registers are not affected by soft resets.

Table 11.9 – Floppy Disk Controller Logical Device Configuration Registers

NAME	REG INDEX	DEFINITION
FDD Mode Register Default = 0x0E on VCC POR, VTR POR and HARD RESET	0xF0 R/W	**Note:** Bits[0, 2, 3, 7] in this register are mapped to 0xF8 register. Bit[0] Floppy Mode = 0 Normal Floppy Mode (default) = 1 Enhanced Floppy Mode 2 (OS2) Bit[1] FDC DMA Mode = 0 Burst Mode is enabled = 1 Non-Burst Mode (default) Bit[3:2] Interface Mode = 11 AT Mode (default) = 10 (Reserved) = 01 PS/2 = 00 Model 30 **Notes:** • Setting Bit[3:2] to "10" will not change the state of Bit[2] in 0xF8. • Setting Bit[3:2] to "00" will not change the state of Bit[2] in 0xF8; however, Model 30 mode will be selected. Bit[4] FDC_SWAP 0 = Do Not Swap (default) 1 = Swap Drive 0 (nDS, nMTR pins) with Drive 1 (nDS, nMTR pins) Bit[5] Reserved, set to zero Bit[6] FDC Output Type Control = 0 FDC outputs are OD12 open drain (default) = 1 FDC outputs are O12 push-pull Bit[7] FDC Output Control = 0 FDC outputs active (default) = 1 FDC outputs tri-stated

NAME	REG INDEX	DEFINITION
FDD Option Register Default = 0x00 on VCC POR, VTR POR and HARD RESET	0xF1 R/W	**Note:** Bits[0, 2, 3] in this register are mapped to 0xF8 register. Bit[0] Forced Write Protect = 0 Inactive (default) = 1 FDD nWRTPRT input is forced active when either of the drives has been selected. nWRTPRT (to the FDC Core) = WP (FDC SRA register, bit 1) = (nDS0 AND Forced Write Protect) OR (nDS1 AND Forced Write Protect) OR nWRTPRT (from the FDD Interface) Bit[1] Reserved Bits[3:2] Density Select = 00 Normal (default) = 01 Normal (reserved for users) = 10 1 (forced to logic “1”) = 11 0 (forced to logic “0”) **Notes:** • Setting Bits[3:2] to “01” will not change the state of Bit[5] in the 0xF8 will not change. • Setting Bits[3:2] to “10” will not change the state of Bit[5] in 0xF8 register; however, FDC logic will be affected. Bit[7:4] Reserved.
FDD Type Register Default = 0xFF on VCC POR, VTR POR and HARD RESET	0xF2 R/W	Bits[1:0] Floppy Drive A Type Bits[3:2] Reserved (could be used to store Floppy Drive B type) Bits[5:4] Reserved (could be used to store Floppy Drive C type) Bits[7:6] Reserved (could be used to store Floppy Drive D type)
	0xF3 R	Reserved, Read as 0 (read only)
FDD0 Default = 0x00 on VCC POR, VTR POR and HARD RESET	0xF4 R/W	Bits[1:0] Drive Type Select: DT1, DT0 Bits[2] Read as 0 (read only) Bits[4:3] Data Rate Table Select: DRT1, DRT0 Bits[5] Read as 0 (read only) Bits[6] Precompensation Disable PTS =0 Use Precompensation =1 No Precompensation Bits[7] Read as 0 (read only)
	0xF5 R	Reserved, Read as 0 (read only)

NAME	REG INDEX	DEFINITION
FDC Mapping Register Default = 0x24 on VCC POR, VTR POR and HARD RESET	0xF8 R/W	Bit[0] – Tri-state Control. This bit maps to Bit[7] FDC Output Control in the FDC Mode Register (0xF0). = 0 FDC outputs active (default) = 1 FDC outputs tri-Stated Bit[1] Reserved Bit[2] PC-AT or PS/2 Drive Mode Select. This bit maps to Bit[3] Interface Mode in the FDC Mode Register (0xF0). = 0 PS/2 = 1 AT Mode (default) Note: only two out of three modes in the FDC Mode Register are mapped. Although retained, the model 30 mode cannot be selected via 0xF8. Bit[3] Write Protect (Software). This bit maps to Bit[0] Forced Write Protect in the FDD Option Register (0xF1). = 0 Inactive (default) = 1 Write protected Bit[4] Reserved Bit[5] Density Select. This bit maps to Bits[3:2] Density Select in the FDD Option Register (0xF1) with inversion. A write of '0' on Bit[5] will force Bits[3:2] in the FDD Option Register to "11". Similarly, a write of '1' will force Bits[3:2] in the FDD Option Register to "00". = 0 forced to logic "0" = 1 Normal (default) Bit[6] Floppy Mode. This bit maps to Bit[0] Floppy Mode in the FDC Mode Register (0xF0). = 0 Normal Floppy Mode (default) = 1 Enhanced Floppy Mode 2 (OS2) Bit[7] Reserved

Table 11.10 – Serial Port 2 Logical Device Configuration Registers

NAME	REG INDEX	DEFINITION
Serial Port 2 Mode Register Default = 0x00 on VCC POR, VTR POR and HARD RESET	0xF0 R/W	Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed Disabled(default) = 1 High Speed Enabled Bit[7:2] Reserved, set to zero
IR Option Register Default = 0x02 on VCC POR, VTR POR and HARD RESET	0xF1 R/W	Bit[0] Receive Polarity = 0 Active High (Default) = 1 Active Low Bit[1] Transmit Polarity = 0 Active High = 1 Active Low (Default) Bit[2] Duplex Select = 0 Full Duplex (Default) = 1 Half Duplex Bits[5:3] IR Mode = 000 Standard COM Functionality (Default) = 001 IrDA = 010 ASK-IR = 011 Reserved = 1xx Reserved Bit[6] IR Location Mux = 0 Use Serial port TXD2 and RXD2 (Default). The IRTX2 pin is low. = 1 Use alternate IRRX2 and IRTX2 pins. The TXD2 pin is tri-state. Bit[7] Reserved, write 0.
IR Half Duplex Timeout Default = 0x03 on VCC POR, VTR POR and HARD RESET	0xF2	Bits [7:0] These bits set the half duplex time-out for the IR port. This value is 0 to 10msec in 100usec increments. 0= blank during transmit/receive 1= blank during transmit/receive + 100usec . . .

Table 11.11 – Parallel Port Logical Device Configuration Registers

NAME	REG INDEX	DEFINITION
PP Mode Register Default = 0x3C on VCC POR, VTR POR and HARD RESET	0xF0 R/W	**Note:** Bits[2:0] in this register are mapped to 0xF8 register. Bits[2:0] Parallel Port Mode = 100 Printer Mode (default) = 000 Standard and Bi-directional (SPP) Mode = 001 EPP-1.9 and SPP Mode = 101 EPP-1.7 and SPP Mode = 010 ECP Mode = 011 ECP and EPP-1.9 Mode = 111 ECP and EPP-1.7 Mode Note: Setting Bits[2:0] to either “101”, “011” or “111” will not change the state of Bits[3:0] in the 0xF8; however, appropriate Parallel Port mode will be selected. Bit[6:3] ECP FIFO Threshold 0111b (default) Bit[7] PP Interupt Type **Not valid when the parallel port is in the Printer Mode (100) or the Standard & Bi-directional Mode (000).** = 1 Pulsed Low, released to high-Z. = 0 IRQ follows nACK when parallel port in EPP Mode or [Printer,SPP, EPP] under ECP. IRQ level type when the parallel port is in ECP, TEST, or Centronics FIFO Mode.
PP Mode Register 2 Default = 0x00 on VCC POR, VTR POR and HARD RESET	0xF1 R/W	Bits[3:0] Reserved. Set to zero Bit [4] TIMEOUT_SELECT = 0 TMOUT (EPP Status Reg.) cleared on write of ‘1’ to TMOUT. = 1 TMOUT cleared on trailing edge of read of EPP Status Reg. Bits[7:5] Reserved. Set to zero.
PP Mapping Register Default = 0x08 on VCC POR, VTR POR and HARD RESET	0xF8 R/W	Bits[3:0] Parallel Port Mode. The Bits[3:1] map directly to Bits[2:0] in the PP Mode Register (0xF0). = 0001 Standard and Bi-directional (SPP) Mode = 0010 EPP-1.9 and SPP Mode = 0100 ECP Mode = 1000 Printer Mode (default) = others Reserved Bits[7:4] Reserved

Table 11.12 – Serial Port 1 Logical Device Configuration Registers

NAME	REG INDEX	DEFINITION
Serial Port 1 Mode Register Default = 0x00 on VCC POR, VTR POR and HARD RESET	0xF0 R/W	Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed Disabled(default) = 1 High Speed Enabled Bit[6:2] Reserved, set to zero Bit[7] Share IRQ =0 UARTS use different IRQs =1 UARTS share a common IRQ See Note 1 below.

Note 1: To properly share and IRQ,

1. Configure UART1 (or UART2) to use the desired IRQ.
2. Configure UART2 (or UART1) to use No IRQ selected.
3. Set the share IRQ bit.

Note: If both UARTs are configured to use different IRQs and the share IRQ bit is set, then both of the UART IRQs will assert when either UART generates an interrupt.

Table 11.13 – Keyboard Logical Device Configuration Registers

NAME	REG INDEX	DEFINITION
KRST_GA20 Default = 0x00 on VCC POR, VTR POR and HARD RESET Bits[7:5] reset on VTR POR only	0xF0 R/W	KRESET and GateA20 Select Bit[7] ISO_MODE = 0 Mode 1 (default) – Isolate the 8042 in hardware while the nLPCPD signal is active OR when the Keyboard and Mouse isolation bits are set by software. = 1 Mode 2 – Keyboard and mouse isolation bits set by software only. Note: the input path to the 8042 is also isolated while the nLPCPD signal is active. Bit[6] M_ISO. Enables/disables isolation of mouse signals into 8042. Does not affect MDAT signal to mouse wakeup (PME) logic. 1=block mouse clock and data signals into 8042 0= do not block mouse clock and data signals into 8042 Bit[5] K_ISO. Enables/disables isolation of keyboard signals into 8042. Does not affect KDAT signal to keyboard wakeup (PME) logic. 1=block keyboard clock and data signals into 8042 0= do not block keyboard clock and data signals into 8042 Bit[4] MLATCH = 0 MINT is the 8042 MINT ANDed with Latched MINT (default) = 1 MINT is the latched 8042 MINT Bit[3] KLATCH = 0 KINT is the 8042 KINT ANDed with Latched KINT (default) = 1 KINT is the latched 8042 KINT Bit[2] Port 92 Select = 0 Port 92 Disabled = 1 Port 92 Enabled Bit[1] Reserved Bit[0] Reserved

Table 11.14 – Power Control/Runtime Register Block Logical Device Configuration Registers

NAME	REG INDEX	DEFINITION
CLOCKI32 Default = 0x00 on VTR POR	0xF0 (R/W)	Bit[0] (CLK32_PRSN) 0=32kHz clock is connected to the CLKI32 pin (default) 1=32kHz clock is not connected to the CLKI32 pin (pin is grounded) Bit[1] SPEKEY_EN. This bit is used to turn the logic for the "wake on specific key" feature on and off. It will disable the 32kHz clock input to the logic when turned off. The logic will draw no power when disabled. 0= "Wake on specific key" logic is on (default) 1= "Wake on specific key" logic is off Bits[7:2] are reserved
INT_G Default = 0x00 on VCC POR, VTR POR, HARD RESET and SOFT RESET	0xF1 R/W	Bit[7:1] Reserved Bit[0] INT_G Enable 0 = Disable Interrupt Generating Registers (INT_GENx) from affecting the serial IRQ stream 1 = Enable Interrupt Generating Registers to drive one or more frames low in the SER IRQ stream ***Note:*** See Power Control Block runtime registers at offset 0x1B and 0x1C for configuring Interrupt Generating Registers.

Chapter 12 Electrical Characteristics

12.1 Maximum Guaranteed Ratings

Maximum 3.3 Supply ..... +4.1V
Maximum 5V Supply ..... +6.0V
Voltage on any 3.3V pin, with respect to Ground ..... -0.5 to 5.5V
Voltage on any 5V pin, with respect to Ground ..... -0.5 to 5.5V
Operating Temperature Range ..... 0^{o}C to $+70^{o}$C
Storage Temperature Range ..... -55^{o} to $+150^{o}$C
Lead Temperature Range (lead-free, P/N LPC47N182-NW) ..... Refer to JEDEC Spec. J-STD-020B
Lead Temperature Range (leaded, P/N LPC47N182-NR) ..... Refer to JEDEC Spec. J-STD-020

Note: Stresses above those listed above and below could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

12.2 Operational DC Characteristics

Table 12.1 – Operational DC Characteristics

(T_A = 0^{o}C to 70^{o}C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Input Buffer						
Low Input Level	V_{IL}			0.8	V	TTL Levels
High Input Level	V_{IH}	2.0		5.5	V	TTL Levels
IPU Input Buffer						
Low Input Level	V_{IL}			0.8	V	TTL Levels
High Input Level	V_{IH}	2.0		5.5	V	TTL Levels
Pull-Up	PU		30		uA	
IS Input Buffer						
Low Input Level	V_{IL}			0.8	V	Schmitt Trigger
High Input Level	V_{IH}	2.2		5.5	V	Schmitt Trigger
Schmitt Trigger Hystersis	V_{HYS}		250		mV	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IS_400 Input Buffer						
Low Input Level	V_{IL}			0.8	V	Schmitt Trigger
High Input Level	V_{IH}	2.2		5.5	V	Schmitt Trigger
Schmitt Trigger Hystersis	V_{HYS}		400		mV	
ISPU_400 Input Buffer						
Low Input Level	V_{IL}			0.8	V	Schmitt Trigger
High Input Level	V_{IH}	2.2		5.5	V	Schmitt Trigger
Schmitt Trigger Hystersis	V_{HYS}		400		mV	
Pull-Up	PU		30		uA	
Input Low Current	$ILEAK_{IL}$			1	uA	V_{IN} = VTR
Input High Current	$ILEAK_{IH}$	-26		-88	uA	V_{IN} = 0V
AO Analog Output Buffer						
For REF5V_OUT						
Low Output Level	V_{OL}			0.4	V	VCC5V>1.5V, VCC5V>VCC + 0.15;
High Output Level	V_{OH}	VREF3IN -0.15		VREF3IN +0.15	V	VCC>1.5V, VCC>VCC5V + 0.15; I_{OH} = -3.3mA
For REF5V_STBY						
Low Output Level	V_{OL}			0.4	V	V_5P0_STBY>1.5V, V_5P0_STBY>VTR + 0.15;
High Output Level	V_{OH}	VTR-0.15		VTR+ 0.15	V	VTR>1.5V, VTR>V_5P0_STBY + 0.15; I_{OH} = -3.3mA
O8 Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
OD8 Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}			Vcc+10%	V	Open-Drain

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O12 Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
OD12 Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}			Vcc+10%	V	Open-Drain
OP14 Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
OD24 Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24mA
High Output Level	V_{OH}			Vcc+10%	V	Open-Drain
IO8 Input/Output Buffer						
Low Input Level	V_{IL}			0.8	V	TTL Levels
High Input Level	V_{IH}	2.0		5.5	V	TTL Levels
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
ISO8 Input/Output Buffer						
Low Input Level	V_{IL}			0.8	V	Schmitt Trigger
High Input Level	V_{IH}	2.2		5.5	V	Schmitt Trigger
Schmitt Trigger Hystersis	V_{HYS}		250		mV	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4				I_{OH} = -4mA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
ISOD8 Input/Output Buffer						
Low Input Level	V_{IL}			0.8	V	Schmitt Trigger
High Input Level	V_{IH}	2.2		5.5	V	Schmitt Trigger
Schmitt Trigger Hystersis	V_{HYS}		250		mV	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}			Vcc+10%	V	Open-Drain, Vcc = 5V Max
IPDO8 Input Buffer						
Low Input Level	V_{IL}			0.8	V	TTL Levels
High Input Level	V_{IH}	2.0		5.5	V	TTL Levels
Pull-Down	PD		30		uA	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}			Vcc+10%	V	I_{OH} = -4mA
IO12 Input/Output Buffer						
Low Input Level	V_{IL}			0.8	V	TTL Levels
High Input Level	V_{IH}	2.0		5.5	V	TTL Levels
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
IOP14 Input/Output Buffer						
Low Input Level	V_{IL}			0.8	V	TTL Levels
High Input Level	V_{IH}	2.0		5.5	V	TTL Levels
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
IO_SW Input/Output Special Type	Pins of this type are connected in pairs through a switch. The switch provides a 25 ohm (max) resistance to ground when closed. See SMBus Isolation Circuitry and Voltage Translation Circuit sections for a description. **Note**: Vcc=5V max.					

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IOD24 Input/Output Buffer						
Low Input Level	V_{IL}			0.8	V	TTL Levels
High Input Level	V_{IH}	2.0		5.5	V	TTL Levels
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24mA
High Output Level	V_{OH}			Vcc+10%	V	Open-Drain
PCI Type Buffers (PCI_ICLK, PCI_I, PCI_O, PCI_IO)	3.3V PCI 2.1 Compatible.					
Leakage Current (ALL except IS, IS_400, ISPU_400, ISOD8, AO, O8_3V and PCI Buffers)						
Input High Current	$ILEAK_{IH}$			10	uA	V_{IN} = Vcc
Input Low Current	$ILEAK_{IL}$			-10	uA	V_{IN} = 0V
Leakage Current (IS, IS_400, ISPU_400 and ISOD8 Buffers)						
Input High Leakage Current	$ILEAK_{IH}$			1	uA	V_{IN} = Vcc
Input Low Leakage Current	$ILEAK_{IL}$			-1	uA	V_{IN} = 0V
Leakage Current (AO Buffer)						
Input High Leakage Current	$ILEAK_{IH}$			20	uA	V_{IN} = Vcc
Input Low Leakage Current	$ILEAK_{IL}$			-20	uA	V_{IN} = 0V
Leakage Current (PCI Buffers and nRSMRST)						V_{CC} = 0V and V_{CC} = 3.3V
Input High Leakage Current	$ILEAK_{IH}$			10	µA	V_{IN} = 3.6V Max
Input Low Leakage Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
Backdrive Protect/ChiProtect (All except PCI Buffers and nRSMRST)						V_{CC} = 0V
Input High Leakage Current	$ILEAK_{IH}$			10	µA	V_{IN} = 5.5V Max
Input Low Leakage Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
5V Tolerant Pins (All except PCI Buffers and nRSMRST)						V_{CC} = 0V
Input High Leakage Current	$ILEAK_{IH}$			10	µA	V_{IN} = 5.5V Max
Input Low Leakage Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
3.3V Main Supply Voltage	VCC	3.0	3.3	3.6	V	VCC must not be greater than 0.5V above VTR
3.3V Main Supply Current	I_{CC3}		10	15	mA	All outputs open, all inputs transitioning to/from 0V from/to 3.3V
3.3V Standby Supply Current	I_{TR3}		0.2	2	mA	All outputs open, all inputs transitioning to/from 0V from/to 3.3V
5V Standby Supply Voltage	V_5P0_STBY	4.75		5.25	V	
5V Standby Supply Current	I_{TR5}		1	3	mA	

Note: All leakage currents are measured with pins in high impedance.

12.3 Standby Power Requirements

This includes only signals that are outputs and source standby current (no OD outputs). Internal pull-ups are ignored due to their small contribution. External pull-ups are not in this analysis because they do not cause LPC47M182 to draw a discernable amount of additional power.

Table 12.2 – S3-S5 Standby Current

SYMBOL	TYPE	STBY MAX. CURRENT (MA)	NAME AND FUNCTION
REF5V_STBY	AO	3.3	Standby Reference Output
nCDC_DWN_ENAB/GP24	IO12	6	CODEC Down Enable/GPIO
nCDC_DWN_RST	O12	6	CODEC Down Reset
nPCIRST_OUT	OP14	14	3.3V Buffered copy of nPCI_RESET
nPCIRST_OUT2	OP14	14	Second 3.3V Buffered copy of nPCI_RESET
nIO_PME	O8/OD8	4	Power Management Events
LATCHED_BF_CUT	OP14	0	Signal only on for a short period of time
PWRGD_PLATFORM	O8	4	Power Good Signal
nRSMRST	O8	4	Reset for the ICH Resume Well
GP10-GP17, GP20-GP23	IO8	48	12 GPIOs
Total		**103.3**	

12.4 Capacitance Values for Pins

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = 3.3V ±10%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Note: The input capacitance of a port is measured at the connector pins.

Chapter 13 Timing Diagrams

For the Timing Diagrams shown, the following capacitive loads are used on outputs.

NAME	CAPACITANCE TOTAL (pF)
SER_IRQ	50
LAD [3:0]	50
nLDRQ	50
nDIR	240
nSTEP	240
nDS0	240
PD[0:7]	240
nSTROBE	240
nALF	240
KDAT	240
KCLK	240
MDAT	240
MCLK	240
TXD	50
YLW_LED	50
GRN_LED	50
nIDE_RSTDRV	40
nPCIRST_OUT	40
nPCIRST_OUT2	40
PS_ON	50
SCK_BJT_GATE	50
PWRGD_PLATFORM	50
nCDC_DWN_ENAB/ GP24	50
nCDC_DWN_RST	50

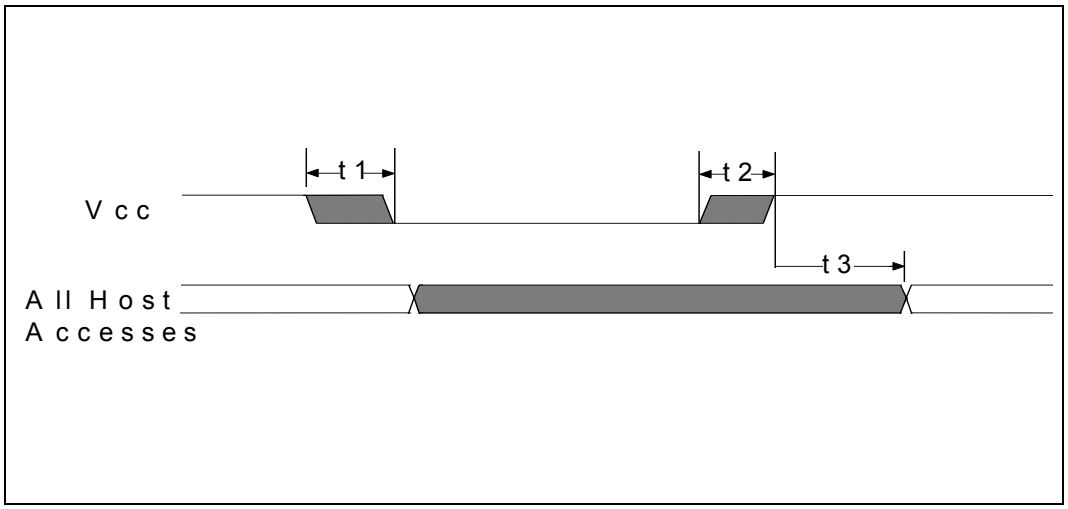


Figure 13.1 - Power-Up Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Vcc Slew from 2.7V to 0V	300			us
t2	Vcc Slew from 0V to 2.7V	100			us
t3	All Host Accesses After Powerup (Note 1)	125		500	us

Note 1: Internal write-protection period after Vcc passes 2.7 volts on power-up

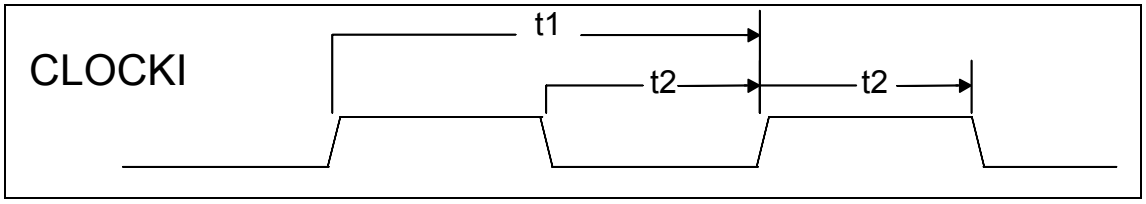


Figure 13.2 - Input Clock Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Clock Cycle Time for 14.318MHZ		69.84		ns
t2	Clock High Time/Low Time for 14.318MHz	20	35		ns
t1	Clock Cycle Time for 32KHZ		31.25		µs
t2	Clock High Time/Low Time for 32KHz		15.63		µs
	Clock Rise Time/Fall Time (not shown)			5	ns

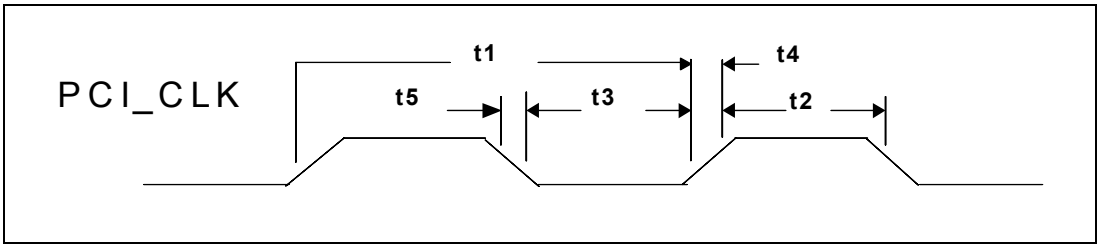


Figure 13.3 - PCI Clock Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Period	30		33.3	nsec
t2	High Time	12			nsec
t3	Low Time	12			nsec
t4	Rise Time			3	nsec
t5	Fall Time			3	nsec

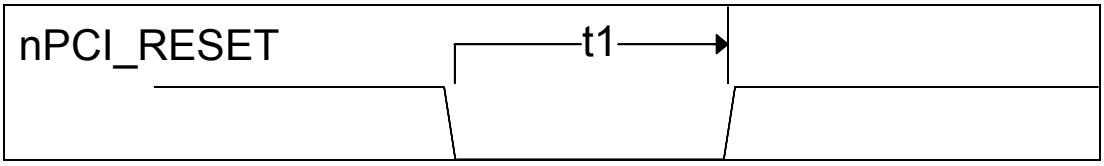


Figure 13.4 - Reset Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nPCI_RESET width	1			ms

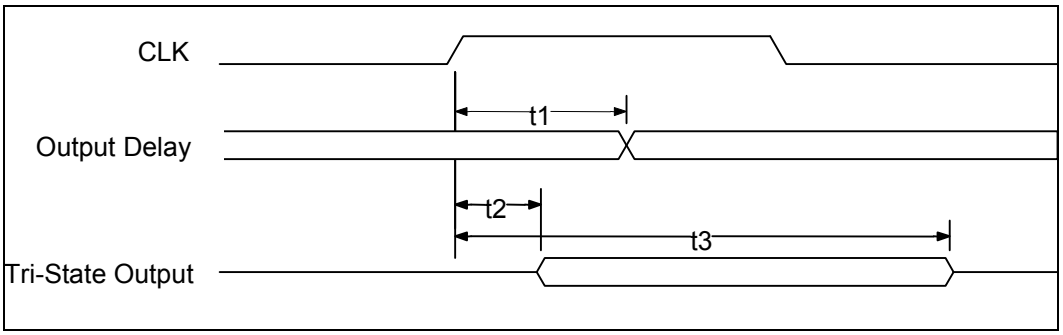


Figure 13.5 - Ouput Timing Measurement Conditions, LPC Signals

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	CLK to Signal Valid Delay – Bused Signals	2		11	ns
t2	Float to Active Delay	2		11	ns
t3	Active to Float Delay			28	ns

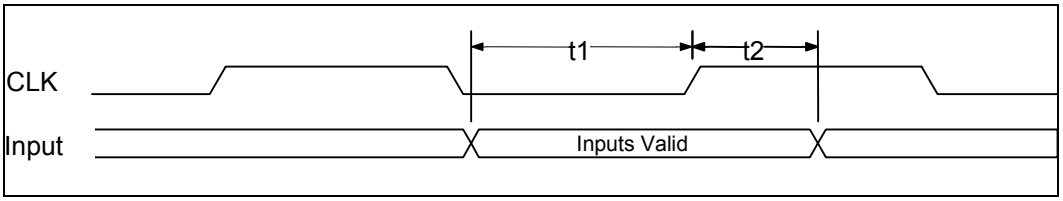
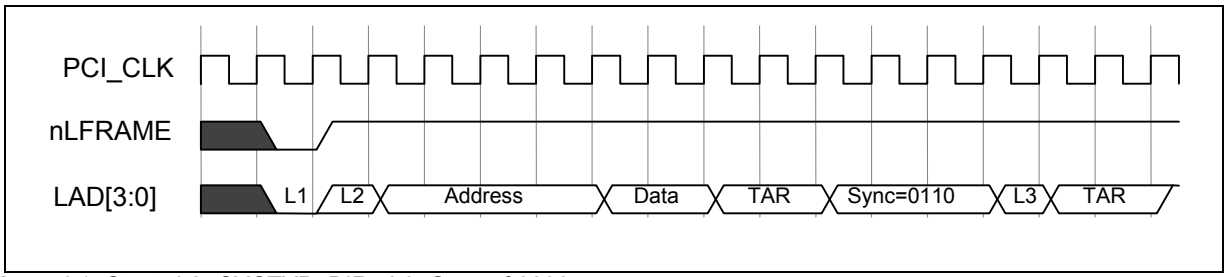


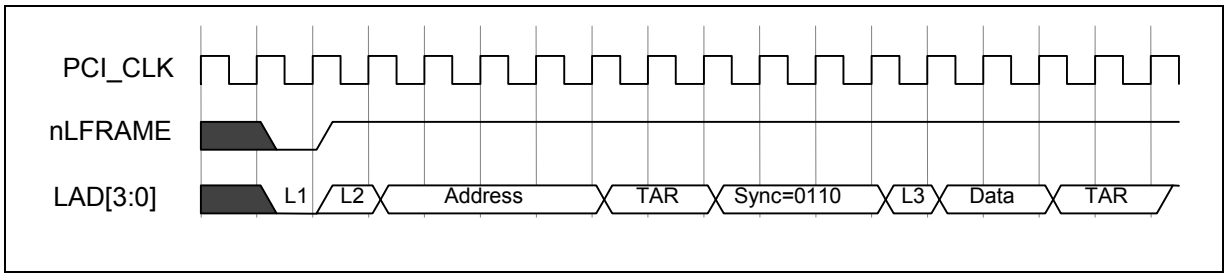
Figure 13.6 - Input Timing Measurement Conditions, LPC Signals

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Input Set Up Time to CLK – Bused Signals	7			ns
t2	Input Hold Time from CLK	0			ns



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

Figure 13.7 - I/O Write



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

Figure 13.8 - I/O Read

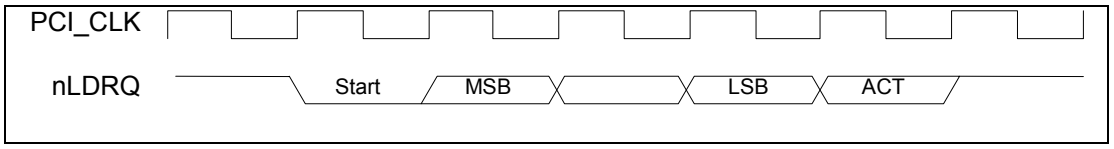
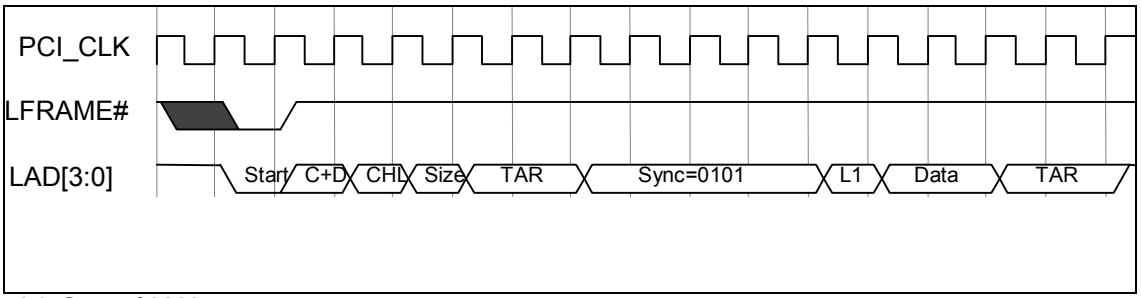
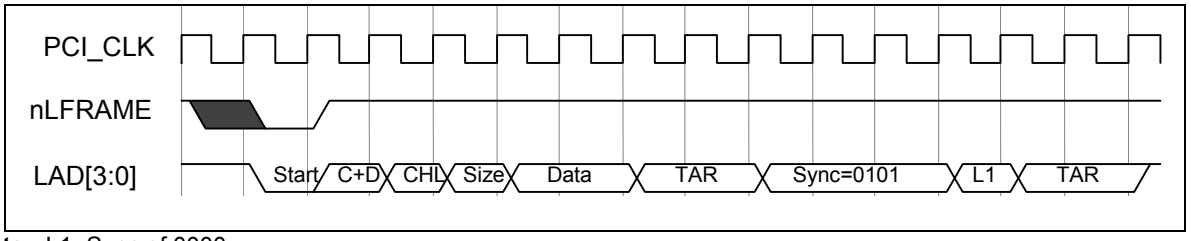


Figure 13.9 – DMA Request Assertion Through NLDRQ



Note: L1=Sync of 0000

Figure 13.10 – DMA Write (First Byte)



Note: L1=Sync of 0000

Figure 13.11 – DMA Read (First Byte)

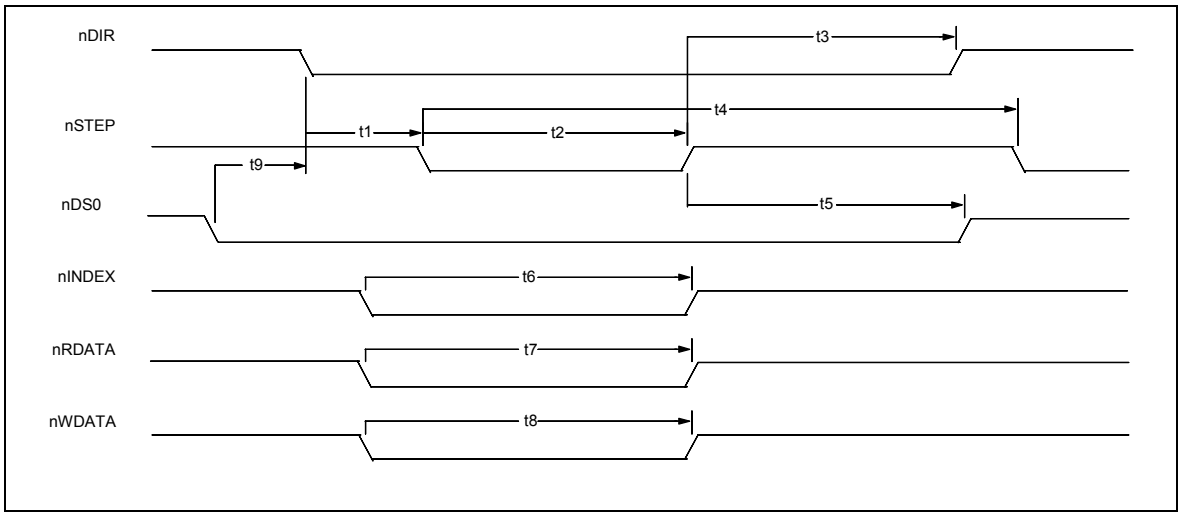


Figure 13.12 – Floppy Disk Drive Timing (At Mode Only)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nDIR Set Up to STEP Low		4		X*
t2	nSTEP Active Time Low		24		X*
t3	nDIR Hold Time after nSTEP		96		X*
t4	nSTEP Cycle Time		132		X*
t5	nDS0 Hold Time from nSTEP Low (Note)		20		X*
t6	nINDEX Pulse Width		2		X*
t7	nRDATA Active Time Low		40		ns
t8	nWDATA Write Data Width Low		.5		Y*
t9	nDS0 Setup Time nDIR Low (Note)	0			ns

***X specifies one MCLK period and Y specifies one WCLK period.**

MCLK = 16 x Data Rate (at 500 kb/s MCLK = 8 MHz)
WCLK = 2 x Data Rate (at 500 kb/s WCLK = 1 MHz)

Note: The DS0 setup and hold time must be met by software.

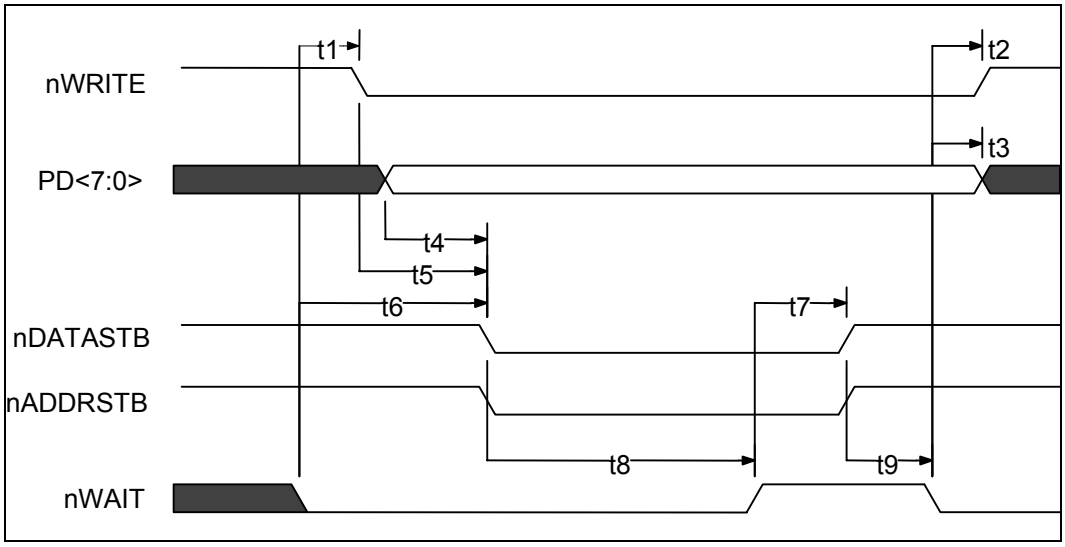


Figure 13.13 – EPP 1.9 Data Or Address Write Cycle

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nWAIT Asserted to nWRITE Asserted (Note 1)	60		185	ns
t2	nWAIT Asserted to nWRITE Change (Note 1)	60		185	ns
t3	nWAIT Asserted to PDATA Invalid (Note 1)	0			ns
t4	PDATA Valid to Command Asserted	10			ns
t5	nWRITE to Command Asserted	5		35	ns
t6	nWAIT Asserted to Command Asserted (Note 1)	60		210	ns
t7	nWAIT Deasserted to Command Deasserted (Note 1)	60		190	ns
t8	Command Asserted to nWAIT Deasserted	0		10	us
t9	Command Deasserted to nWAIT Asserted	0			ns

Note 1: nWAIT must be filtered to compensate for ringing on the parallel bus cable. nWAIT is considered to have settled after it does not transition for a minimum of 50 nsec.

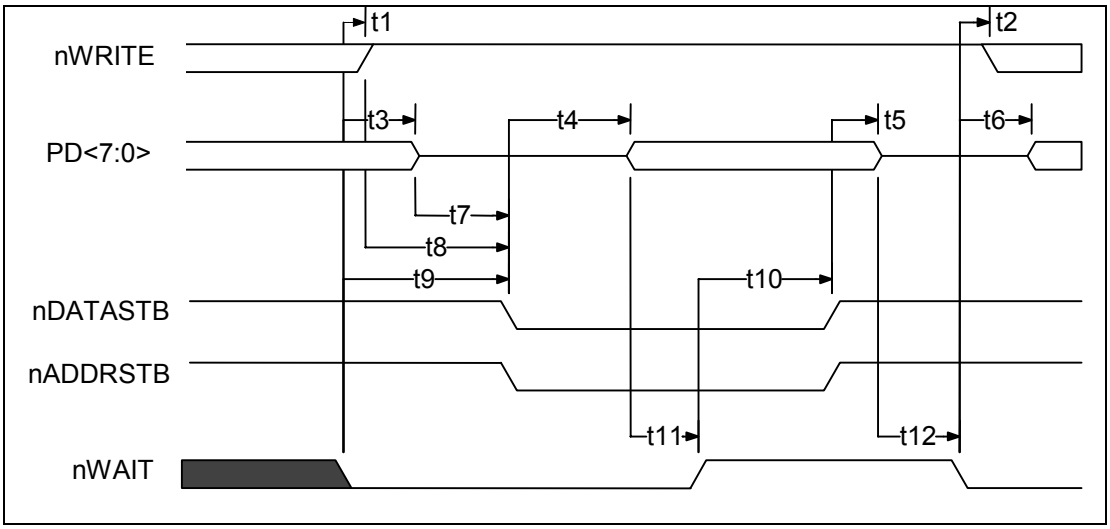


Figure 13.14 – EPP 1.9 Data Or Address Read Cycle

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nWAIT Asserted to nWRITE Deasserted	0		185	ns
t2	nWAIT Asserted to nWRITE Modified (Notes 1,2)	60		190	ns
t3	nWAIT Asserted to PDATA Hi-Z (Note 1)	60		180	ns
t4	Command Asserted to PDATA Valid	0			ns
t5	Command Deasserted to PDATA Hi-Z	0			ns
t6	nWAIT Asserted to PDATA Driven (Note 1)	60		190	ns
t7	PDATA Hi-Z to Command Asserted	0		30	ns
t8	nWRITE Deasserted to Command	1			ns
t9	nWAIT Asserted to Command Asserted	0		195	ns
t10	nWAIT Deasserted to Command Deasserted (Note 1)	60		180	ns
t11	PDATA Valid to nWAIT Deasserted	0			ns
t12	PDATA Hi-Z to nWAIT Asserted	0			µs

Note 1: nWAIT is considered to have settled after it does not transition for a minimum of 50 ns.
Note 2: When not executing a write cycle, EPP nWRITE is inactive high.

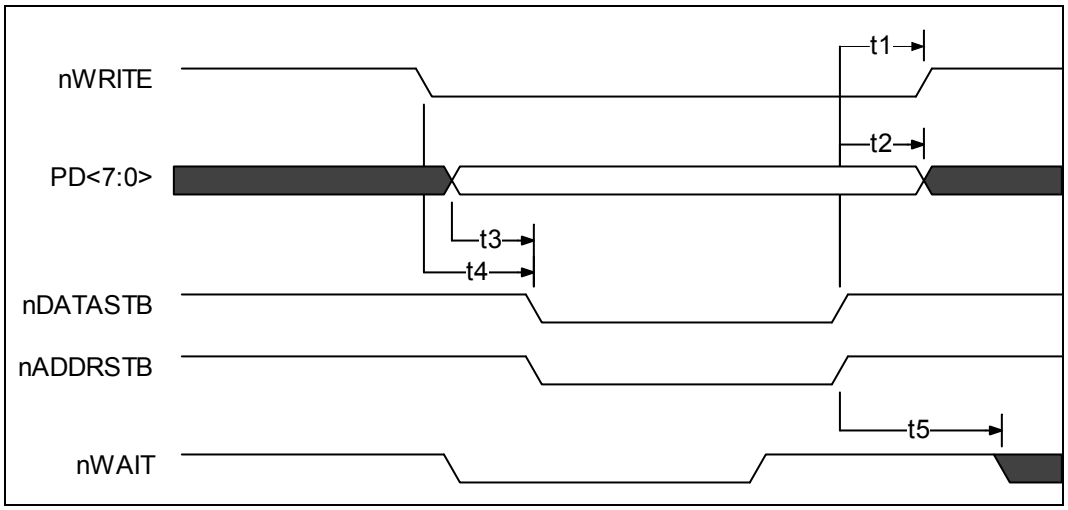


Figure 13.15 – EPP 1.7 Data Or Address Write Cycle

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Command Deasserted to nWRITE Change	0		40	ns
t2	Command Deasserted to PDATA Invalid	50			ns
t3	PDATA Valid to Command Asserted	10		35	ns
t4	nWRITE to Command	5		35	ns
t5	Command Deasserted to nWAIT Deasserted	0			ns

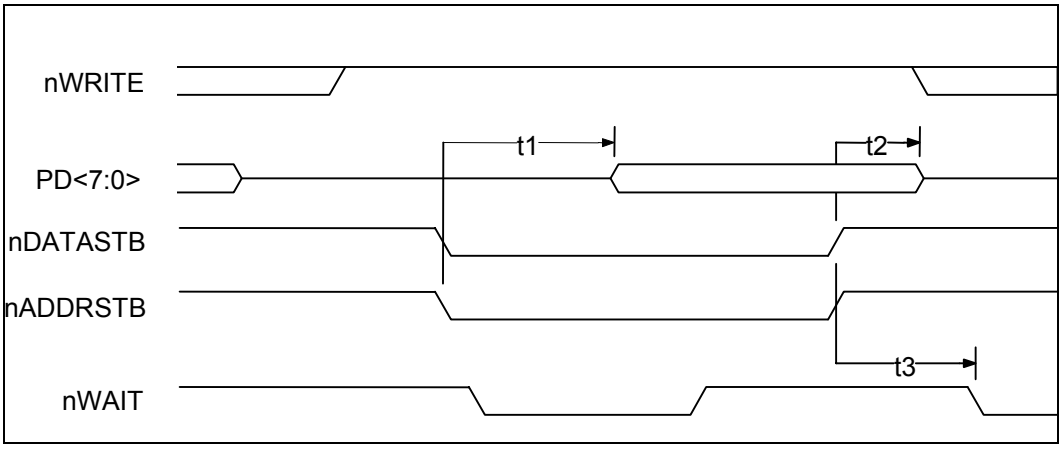


Figure 13.16 – EPP 1.7 Data Or Address Read Cycle

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Command Asserted to PDATA Valid	0			ns
t2	Command Deasserted to PDATA Hi-Z	0			ns
t3	Command Deasserted to nWAIT Deasserted	0			ns

13.1 ECP PARALLEL PORT TIMING

13.1.1 Parallel Port FIFO (Mode 101)

The standard parallel port is run at or near the peak 500KBytes/sec allowed in the forward direction using DMA. The state machine does not examine nACK and begins the next transfer based on Busy. Refer to Figure 13.17.

13.1.2 ECP Parallel Port Timing

The timing is designed to allow operation at approximately 2.0 Mbytes/sec over a 15ft cable. If a shorter cable is used then the bandwidth will increase.

13.1.3 Forward-Idle

When the host has no data to send it keeps HostClk (nStrobe) high and the peripheral will leave PeriphClk (Busy) low.

13.1.4 Forward Data Transfer Phase

The interface transfers data and commands from the host to the peripheral using an interlocked PeriphAck and HostClk. The peripheral may indicate its desire to send data to the host by asserting nPeriphRequest.

The Forward Data Transfer Phase may be entered from the Forward-Idle Phase. While in the Forward Phase the peripheral may asynchronously assert the nPeriphRequest (nFault) to request that the channel be reversed. When the peripheral is not busy it sets PeriphAck (Busy) low. The host then sets HostClk (nStrobe) low when it is prepared to send data. The data must be stable for the specified setup time prior to the falling edge of HostClk. The peripheral then sets PeriphAck (Busy) high to acknowledge the handshake. The host then sets HostClk (nStrobe) high. The peripheral then accepts the data and sets PeriphAck (Busy) low, completing the transfer. This sequence is shown in Figure 13.18.

The timing is designed to provide 3 cable round-trip times for data setup if Data is driven simultaneously with HostClk (nStrobe).

13.1.5 Reverse-Idle Phase

The peripheral has no data to send and keeps PeriphClk high. The host is idle and keeps HostAck low.

13.1.6 Reverse Data Transfer Phase

The interface transfers data and commands from the peripheral to the host using an interlocked HostAck and PeriphClk.

The Reverse Data Transfer Phase may be entered from the Reverse-Idle Phase. After the previous byte has beed accepted the host sets HostAck (nALF) low. The peripheral then sets PeriphClk (nACK) low

when it has data to send. The data must be stable for the specified setup time prior to the falling edge of PeriphClk. When the host is ready to accept a byte it sets HostAck (nALF) high to acknowledge the handshake. The peripheral then sets PeriphClk (nACK) high. After the host has accepted the data it sets HostAck (nALF) low, completing the transfer. This sequence is shown in Figure 13.19.

13.1.7 Output Drivers

To facilitate higher performance data transfer, the use of balanced CMOS active drivers for critical signals (Data, HostAck, HostClk, PeriphAck, PeriphClk) are used in ECP Mode. Because the use of active drivers can present compatibility problems in Compatible Mode (the control signals, by tradition, are specified as open-drain), the drivers are dynamically changed from open-drain to push-pull. The timing for the dynamic driver change is specified in then IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14, July 14, 1993, available from Microsoft. The dynamic driver change must be implemented properly to prevent glitching the outputs.

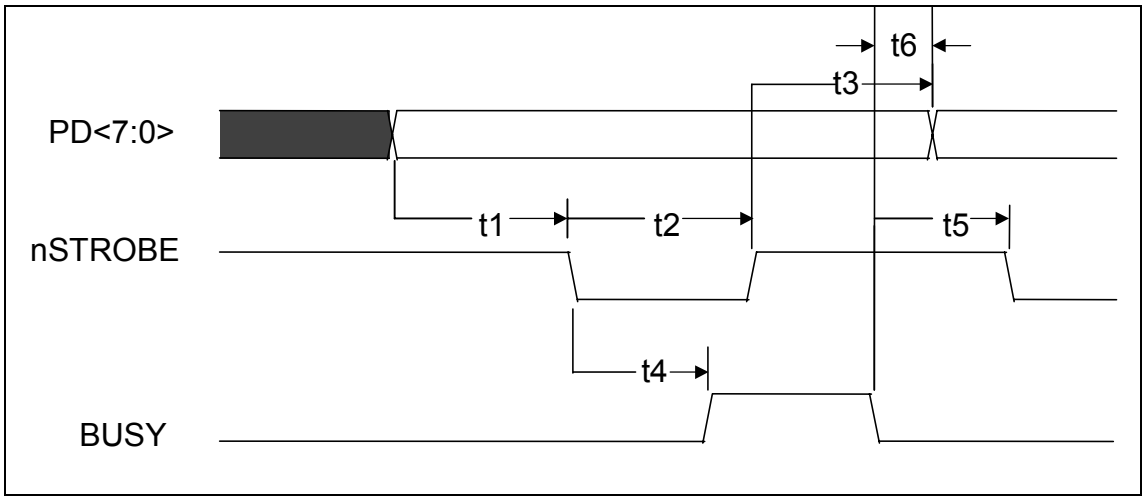


Figure 13.17 – Parallel Port FIFO Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA Valid to nSTROBE Active	600			ns
t2	nSTROBE Active Pulse Width	600			ns
t3	PDATA Hold from nSTROBE Inactive (Note 1)	450			ns
t4	nSTROBE Active to BUSY Active			500	ns
t5	BUSY Inactive to nSTROBE Active	680			ns
t6	BUSY Inactive to PDATA Invalid (Note 1)	80			ns

Note 1: The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.

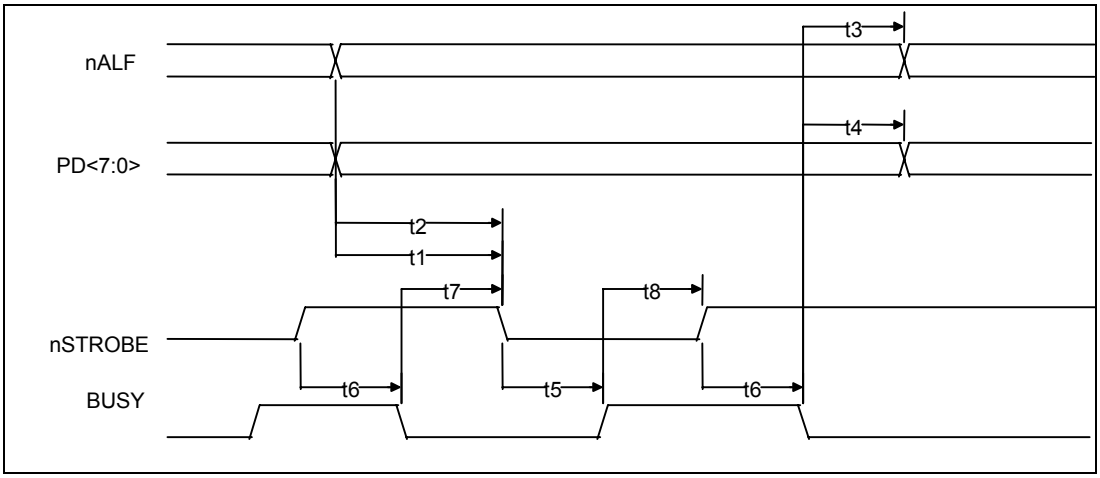


Figure 13.18 - ECP Parallel Port Forward Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nALF Valid to nSTROBE Asserted	0		60	ns
t2	PDATA Valid to nSTROBE Asserted	0		60	ns
t3	BUSY Deasserted to nALF Changed (Notes 1,2)	80		180	ns
t4	BUSY Deasserted to PDATA Changed (Notes 1,2)	80		180	ns
t5	nSTROBE Asserted to Busy Asserted	0			ns
t6	nSTROBE Deasserted to Busy Deasserted	0			ns
t7	BUSY Deasserted to nSTROBE Asserted (Notes 1,2)	80		200	ns
t8	BUSY Asserted to nSTROBE Deasserted (Note 2)	80		180	ns

Note 1: Maximum value only applies if there is data in the FIFO waiting to be written out.
Note 2: BUSY is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

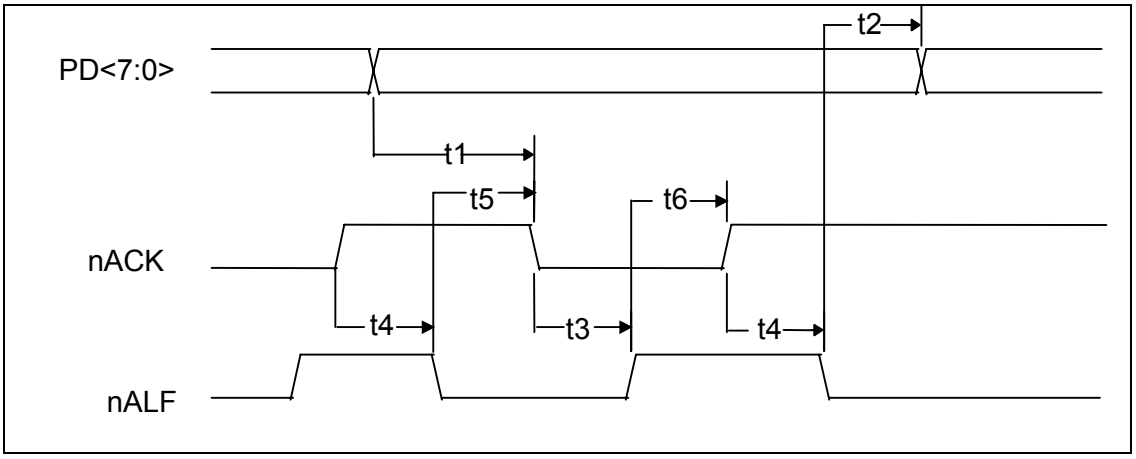


Figure 13.19 – ECP Parallel Port Reverse Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA Valid to nACK Asserted	0			ns
t2	nALF Deasserted to PDATA Changed	0			ns
t3	nACK Asserted to nALF Deasserted (Notes 1,2)	80		200	ns
t4	nACK Deasserted to nALF Asserted (Note 2)	80		200	ns
t5	nALF Asserted to nACK Asserted	0			ns
t6	nALF Deasserted to nACK Deasserted	0			ns

Note 1: Maximum value only applies if there is room in the FIFO and terminal count has not been received. ECP can stall by keeping nALF low.

Note 2: nACK is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

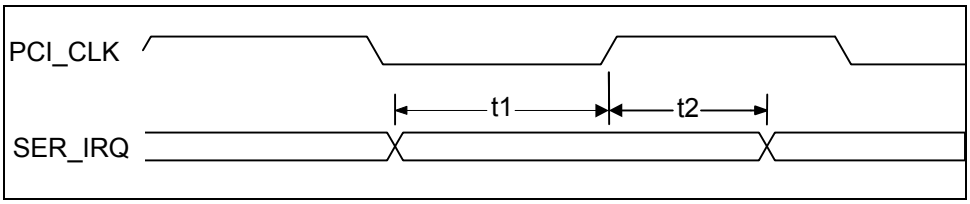


Figure 13.20 – Setup and Hold Time

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SER_IRQ Setup Time to PCI_CLK Rising	7			nsec
t2	SER_IRQ Hold Time to PCI_CLK Rising	0			nsec

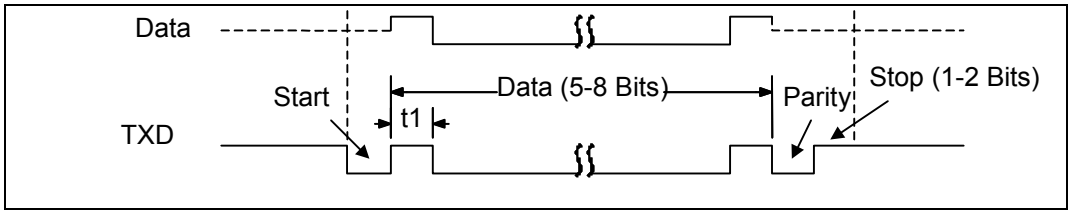


Figure 13.21 – Serial Port Data

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Serial Port Data Bit Time		t_{BR} [1]		nsec

Note 1: t_{BR} is 1/Baud Rate. The Baud Rate is programmed through the divisor latch registers. Baud Rates have percentage errors indicated in the “Baud Rate” table in the “Serial Port” section.

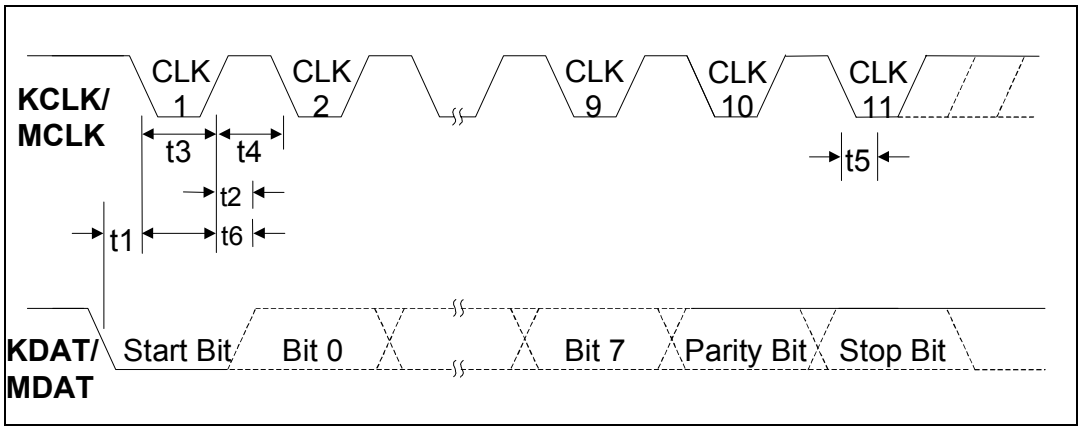


Figure 13.22 – Keyboard/Mouse Receive/Send Data Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Time from DATA transition to falling edge of CLOCK (Receive)	5		25	µsec
t2	Time from rising edge of CLOCK to DATA transition (Receive)	5		T4-5	µsec
t3	Duration of CLOCK inactive (Receive/Send)	30		50	µsec
t4	Duration of CLOCK active (Receive/Send)	30		50	µsec
t5	Time to keyboard inhibit after clock 11 to ensure the keyboard does not start another transmission (Receive)	>0		50	µsec
t6	Time from inactive to active CLOCK transition, used to time when the auxiliary device samples DATA (Send)	5		25	µsec

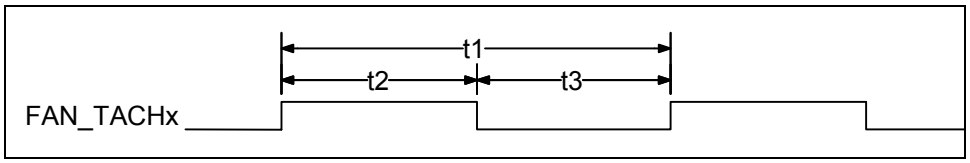


Figure 13.23 – Fan Tachometer Input Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Pulse Time (1/2 Revolution Time=30/RPM)		11.11		µsec
t2	Pulse High Time		5.55		µsec
t3	Pulse Low Time		5.55		µsec

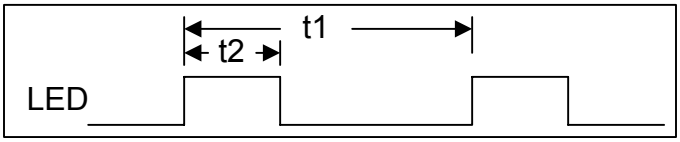


Figure 13.24 – Power LED Output Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Period		1.49		sec
t2	Blink ON Time		0.59		sec

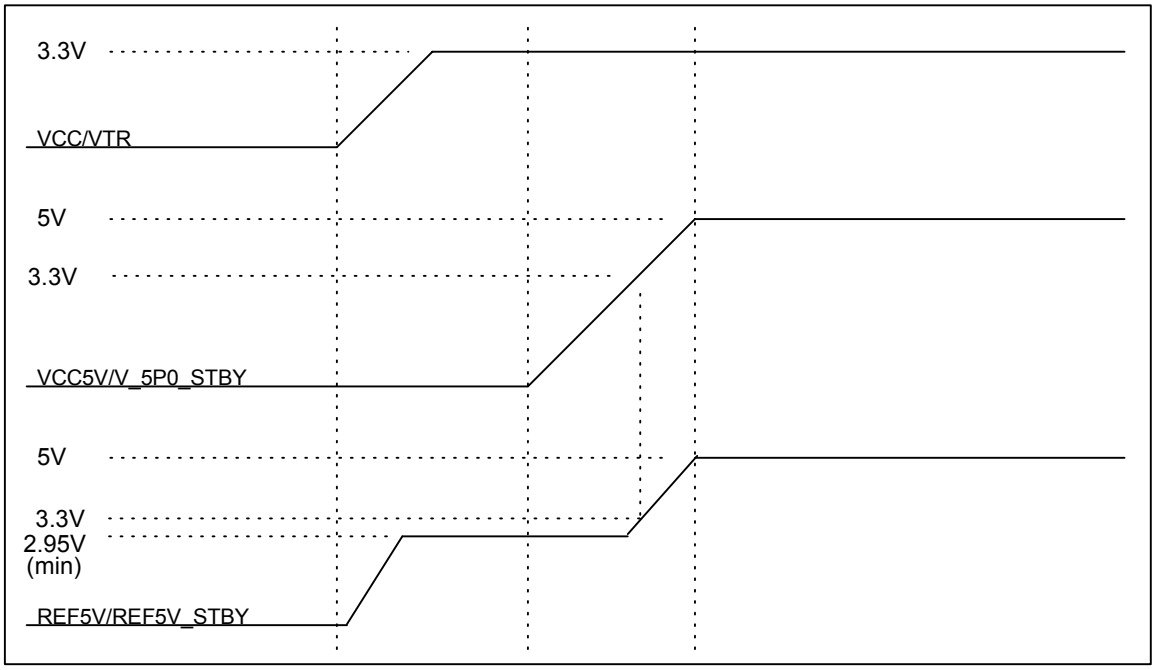


Figure 13.25 – REF5V/REF5V_STBY Output When VCC/VTR Ramps Up Before VCC5V/ V_5P0_STBY

Note: The value 2.95V minimum in Figure 13.25 is (3.3 Supply Voltage – 350 mV).

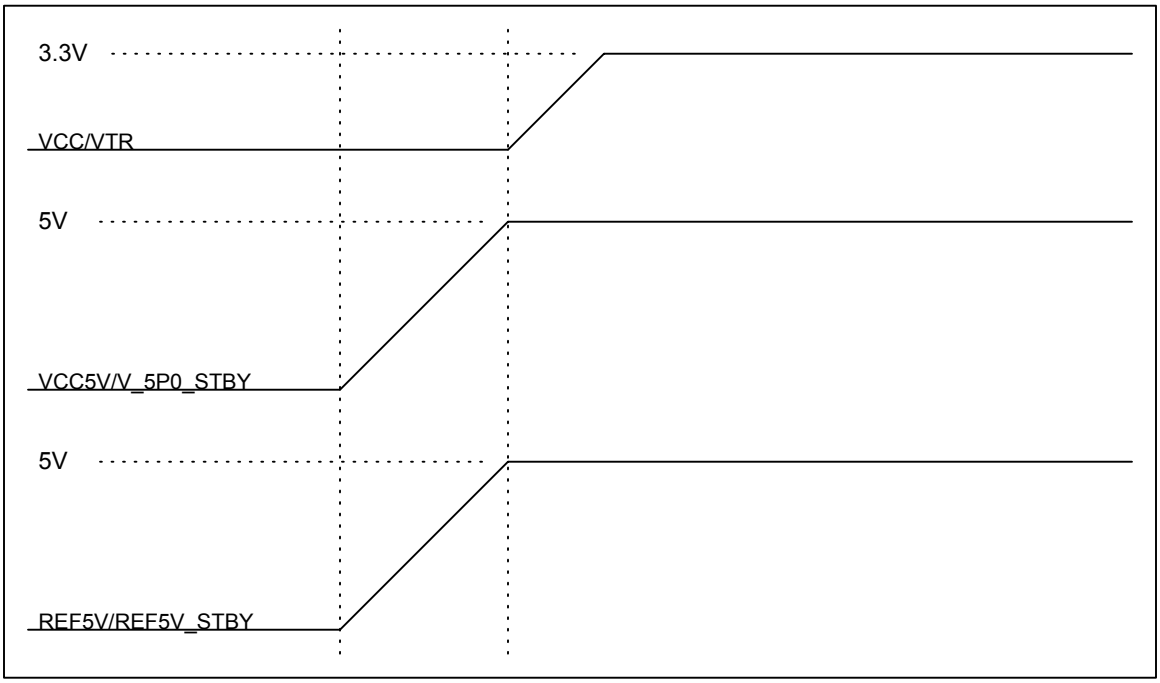


Figure 13.26 – REF5V/REF5V_STBY Output When VCC5V/ V_5P0_STBY Ramps Up Before VCC/VTR

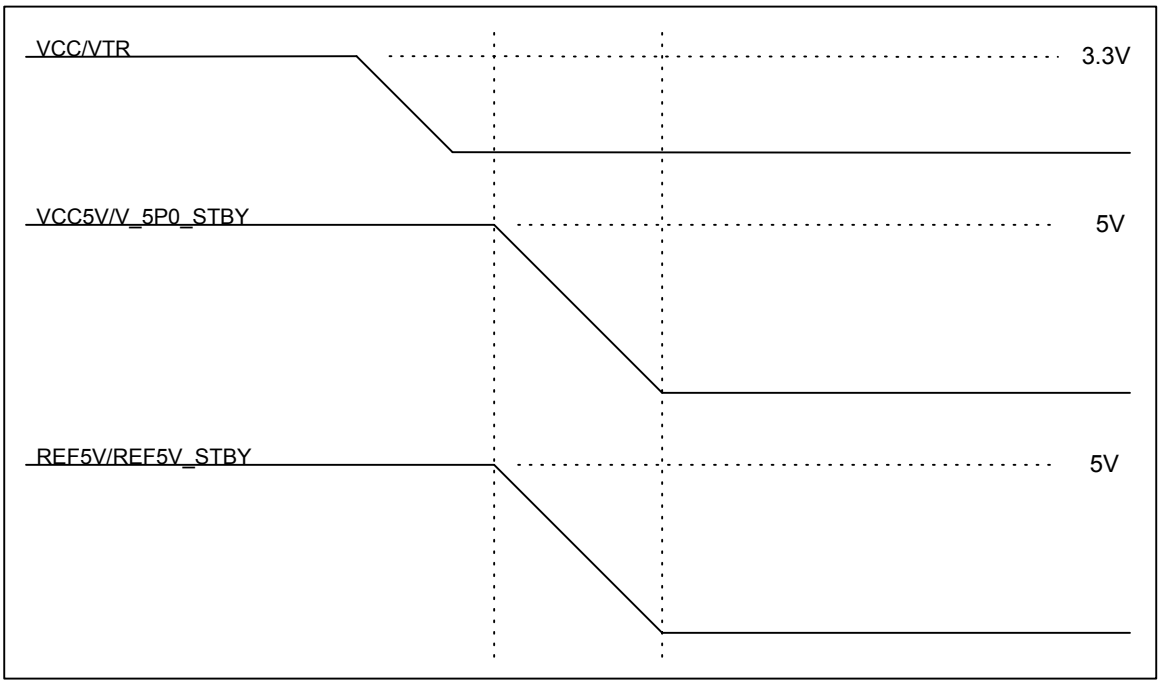


Figure 13.27 – REF5V/REF5V_STBY Output When VCC/VTR Ramps Down Before VCC5V/ V_5P0_STBY

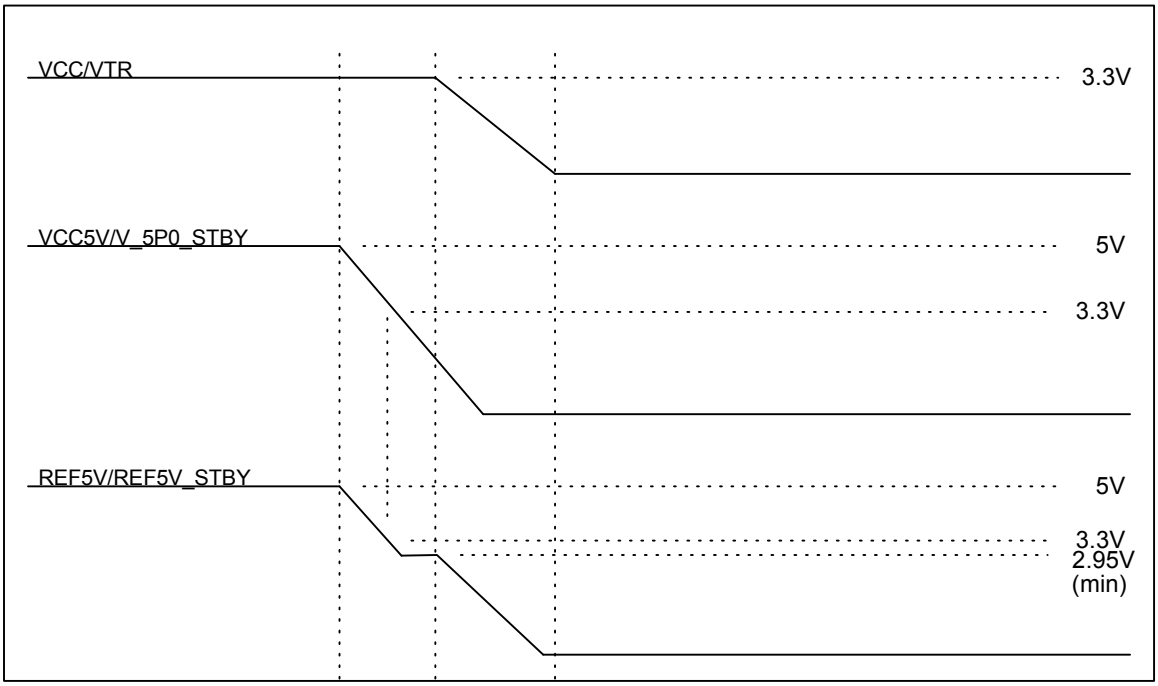


Figure 13.28 – REF5V/REF5V_STBY Output When VCC5V/ V_5P0_STBY Ramps Down Before VCC/VTR

Note: The value 2.95V minimum in Figure 13.28 is (3.3 Supply Voltage – 350 mV).

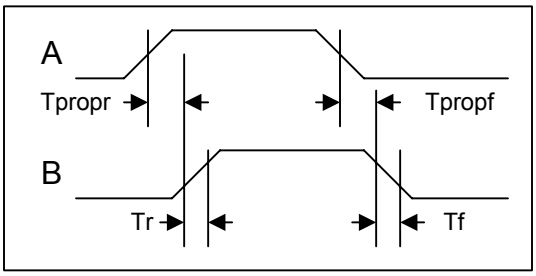


Figure 13.29 – Rise, Fall And Propagation Timings

Table 13.1 – nIDE_RSTDRV Timing

NAME	DESCRIPTION (Refer to Figure 13.29)	MIN	TYP	MAX	UNITS
Tf	nIDE_RSTDRV (B) high to low fall time. Measured form 90% to 10%			15	ns
Tpropf	nIDE_RSTDRV (B) high to low propagation time. Measured from nPCI_RESET (A) to nIDE_RSTDRV (B).			20	ns
CO	Output Capacitance			25	pF
CL	Load Capacitance			40	pF

Table 13.2 – nPCIRST_OUT and nPCIRST_OUT2 Timing

NAME	DESCRIPTION (Refer to Figure 13.29)	MIN	TYP	MAX	UNITS
Tr	nPCIRST_OUT/nPCIRST_OUT2 (B) low to high rise time. Measured form 10% to 90%			53	ns
Tpropr	nPCIRST_OUT/nPCIRST_OUT2 (B) low to high propagation time. Measured from nPCI_RESET (A) to nPCIRST_OUT/nPCIRST_OUT2 (B).			30	ns
CO	Output Capacitance			25	pF
CL	Load Capacitance			40	pF

Table 13.3 – PS_ON Timing

NAME	DESCRIPTION (Refer to Figure 13.29)	MIN	TYP	MAX	UNITS
Tz	nPS_ON (B) low to Hi-Z rise time.			50	ns
Tf	nPS_ON (B) high to low fall time. Measured form 90% to 10%			50	ns
Tpropz	nPS_ON (B) low to Hi-Z propagation time. Measured from nSLP_S3 (A) to nPS_ON (B).			1	us
Tpropf	nPS_ON (B) high to low propagation time. Measured from nSLP_S3 (A) to nPS_ON (B).			1	us
CO	Output Capacitance			25	pF
CL	Load Capacitance			50	pF

Table 13.4 – SCK_BJT_GATE Timing

NAME	DESCRIPTION (Refer to Figure 13.29)	MIN	TYP	MAX	UNITS
Tf	SCK_BJT_GATE (B) low to high fall time. Measured form 90% to 10%			50	ns
Tpropf	SCK_BJT_GATE (B) high to low propagation time. Measured from PWRGD_PLATFORM (A) to SCK_BJT_GATE (B).			1	us
CO	Output Capacitance			25	pF
CL	Load Capacitance			50	pF

Table 13.5 – PWRGD_PLATFORM Timing

NAME	DESCRIPTION (Refer to Figure 13.29)	MIN	TYP	MAX	UNITS
Tr	PWRGD_PLATFORM (B) low to high rise time.			50	ns
Tf	PWRGD_PLATFORM (B) low to high fall time. Measured form 90% to 10%			50	ns
Tpropr	PWRGD_PLATFORM (B) low to high propagation time. Measured from nFPRST (A) to PWRGD_PLATFORM (B).			1	us
Tpropf	PWRGD_PLATFORM (B) high to low propagation time. Measured from nFPRST (A) to PWRGD_PLATFORM (B).			1	us
CO	Output Capacitance			25	pF
CL	Load Capacitance			50	pF

Table 13.6 – CNR CODEC Down Enable Timing

NAME	DESCRIPTION (Refer to Figure 13.29)	MIN	TYP	MAX	UNITS
Tr	nCDC_DWN_RST (B) rise time. Measured from 10% to 90%.			6	us
Tf	nCDC_DWN_RST (B) fall time. Measured from 90% to 10%.			6	us
Tpropr	nCDC_DWN_RST (B) low to high propagation delay. Measured from nAUD_LNK_RST (A) or nCDC_DWN_ENAB (A) to nCDC_DWN_RST (B).			15.3	ns
Tpropf	nCDC_DWN_RST (B) high to low propagation delay. Measured from nAUD_LNK_RST (A) or nCDC_DWN_ENAB (A) to nCDC_DWN_RST (B).			15.3	ns

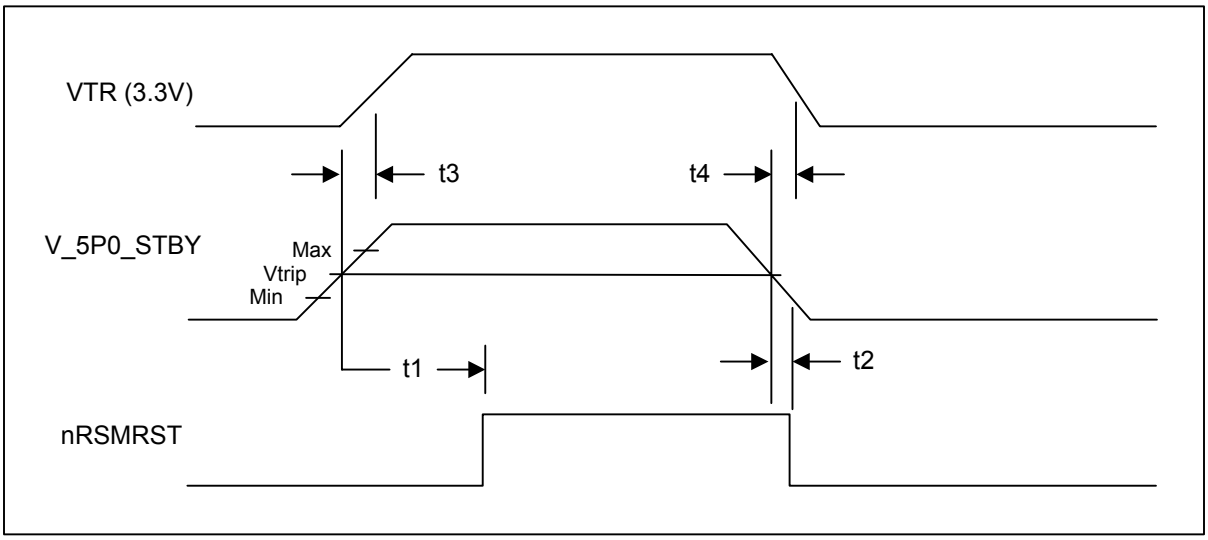


Figure 13.30 – Resume Reset Sequence

Table 13.7 – Resume Reset Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS	Notes
t1	Treset delay. V_5P0_STBY active to nRSMRST inactive	10	32	100	msec	1
t2	Treset_fall. V_5P0_STBY inactive to nRSMRST active (Glitch width allowance)			100	nsec	
	Treset_rise			100	nsec	
t3	V_5P0_STBY active to VTR active	0			msec	2
t4	V_5P0_STBY inactive to VTR inactive	0			msec	2
V_{TRIP}	V_5P0_STBY low trip voltage	4.2		4.5	V	3

Note 1: The nRSMRST will be inactive high max 100 msec after V_5P0_STBY is active assuming the VTR (3.3V) is active. If the VTR (3.3V) is not active within 100 msec, the delay from V_5P0_STBY will be greater than 100 msec and the nRSMRST will go inactive when VTR (3.3V) goes active.

Note 2: The V_5P0_STBY supply must power up before or simultaneous with VTR, and must power down simultaneous with or after VTR (from ICH2 data sheet)

Note 3: The trip point can vary between these limits on a per part basis, but on a given part it should remain relatively stable.

Chapter 14 Package Outline

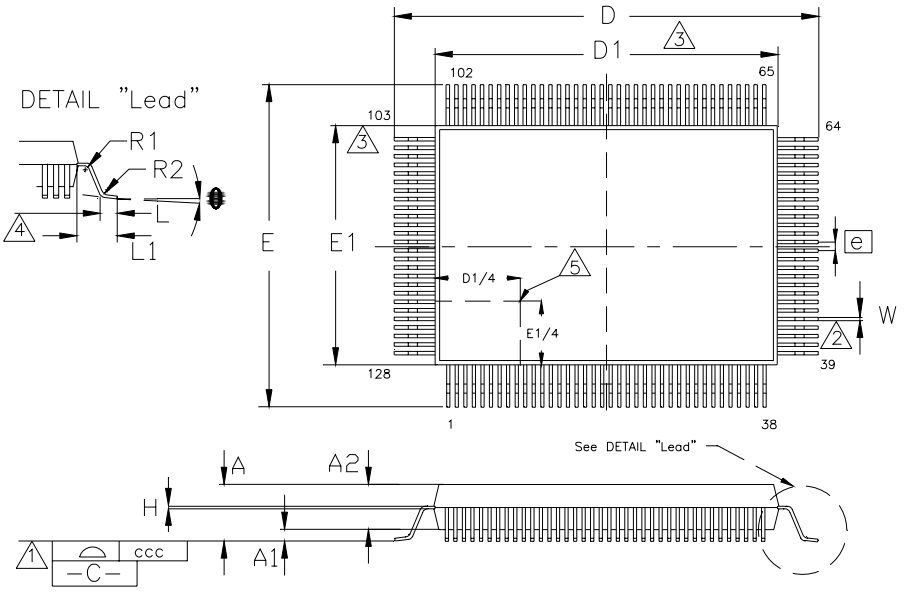


Figure 14.1 - 128 Pin QFP Package Outline, 14x20x2.7 Body, 3.2MM Footprint

Table 14.1 – 128 Pin QFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	3.4	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	2.55	~	3.05	Body Thickness
D	23.00	23.20	23.40	X Span
D1	19.90	20.00	20.10	X body Size
E	17.00	17.20	17.40	Y Span
E1	13.90	14.00	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.73	0.88	1.03	Lead Foot Length
L1	~	1.60	~	Lead Length
e		0.50 Basic		Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.10	~	0.30	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.30	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:
[1] Controlling Unit: millimeter.
[2] Tolerance on the position of the leads is ± 0.04 mm maximum.
[3] Package body dimensions D1 and E1 do not include the mold protrusion.
Maximum mold protrusion is 0.25 mm.
[4] Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
[5] Details of pin 1 identifier are optional but must be located within the zone indicated.

Chapter 15 Board Test Mode

Board level testing is implemented with an XOR Chain. The XOR chain testing allows motherboard manufacturers to check component connectivity (e.g., opens and shorts to VCC or GND).

The TEST_EN pin is used as a strap pin to enter test mode. This pin has an internal 30 µA pull-down resistor to VSS. An external 10 kohm pull-up to V_3P3_STBY is used to put the device in test mode.

Both VCC and VTR supplies are required for the device to operate properly in test mode.

The part enters board test (XOR-chain) mode when the TEST_EN pin is brought high. The part remains in test mode while TEST_EN is high. Bringing TEST_EN low will exit test mode.

When the XOR chain is entered, all output and bi-directional buffers within that chain are tri-stated, except for the XOR chain output. Every signal in the XOR chain (except for the XOR chain's output) functions as an input. Figure 15.1 is a schematic example of XOR chain circuitry.

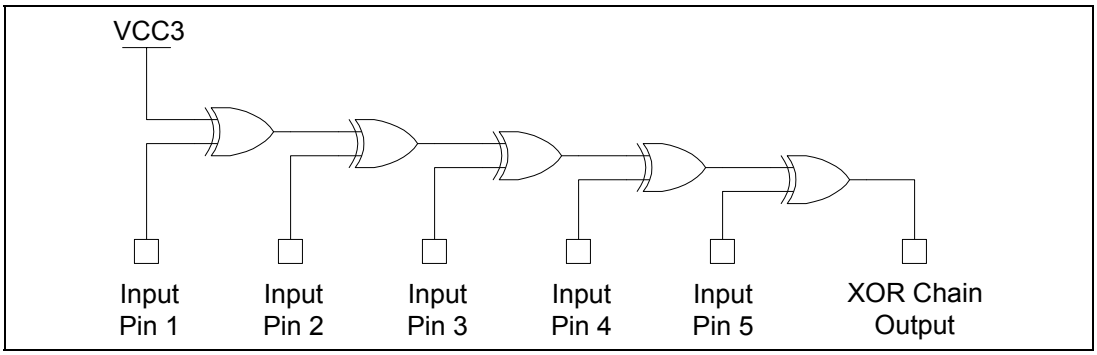


Figure 15.1 – Example XOR Chain Circuitry

The XOR chain output is on pin 30, nDTR1/XOR.

The input pin ordering is as follows: the first input pin in the XOR chain is pin 1 of the chip (MCLK), and the order continues around the chip in increasing pin number order to end at pin 128, skipping those pins that are excluded from the chain (note that pin 117 is excluded from the chain).

The following pins are excluded from the XOR chain.

- nRSMRST pin (1)
- REF5V pin (1)
- REF5V_STBY pin (1)
- VCC pins (5)
- VTR pins (4)
- V_5P0_STBY pin (1)
- VSS pins (7)
- F_CAP pin (1)
- nDTR1/XOR pin (1)
- TEST_EN pin (1)

The total number of pins excluded from the XOR chain is 23; therefore there are an odd number of pins in the XOR chain.

XOR Chain Testability Algorithm Example
An example algorithm for using the XOR chain for board test is shown below.

Table 15.1 – XOR Test Pattern Example

TEST VECTOR	INPUT PIN 1	INPUT PIN 2	INPUT PIN 3	INPUT PIN 4	INPUT PIN 5	XOR OUTPUT
1	0	0	0	0	0	1
2	1	0	0	0	0	0
3	1	1	0	0	0	1
4	1	1	1	0	0	0
5	1	1	1	1	0	1
6	1	1	1	1	1	0

In this example, Vector 1 applies all "0s" to the chain inputs. The outputs being non-inverting, will consistently produce a "1" at the XOR output on a good board. One short to VCC (or open floating to VCC) will result in a "0" at the chain output, signaling a defect.

Likewise, applying Vector 6 (all "1s") to the chain inputs (given that there is an odd number of input signals in the chain) will consistently produce a "0" at the XOR chain output on a good board. One short to VSS (or open floating to VSS) will result in a "1" at the chain output, signaling a defect. It is important to note that the number of inputs pulled to "1" will affect the chain output value. If the number of chain inputs pulled to "1" is even, then a "1" will be seen at the output. If the number of chain inputs pulled to "1" is odd, a "0" will be seen at the output.

Continuing with the example in Table 15.1, as the input pins are driven to "1" across the chain in sequence, the XOR Output will toggle between "0" and "1." Any break in the toggling sequence (e.g., "1011") will identify the location of the short or open.

Chapter 16 Reference Documents

1. IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14, July 14, 1993.
2. Hardware Description of the 8042, Intel 8 bit Embedded Controller Handbook.
3. PCI Bus Power Management Interface Specification, Rev. 1.0, Draft, March 18, 1997.
4. Low Pin Count (LPC) Interface Specification, Revision 1.0, September 29, 1997, Intel Document.
5. Metalious ACPI/Manageability Specification, v1.0, Aril 30, 1999
6. Advanced Configuration and Power Interface Specification, v 1.0
7. SMSC Application Note, AN 8.8: Using the Enhanced Keyboard and Mouse Wakeup Feature in SMSC Super I/O Parts.
8. SMSC Application Note, AN 9.3: Application Considerations When Using the Powerdown Feature of SMSC Floppy Disk Controllers.