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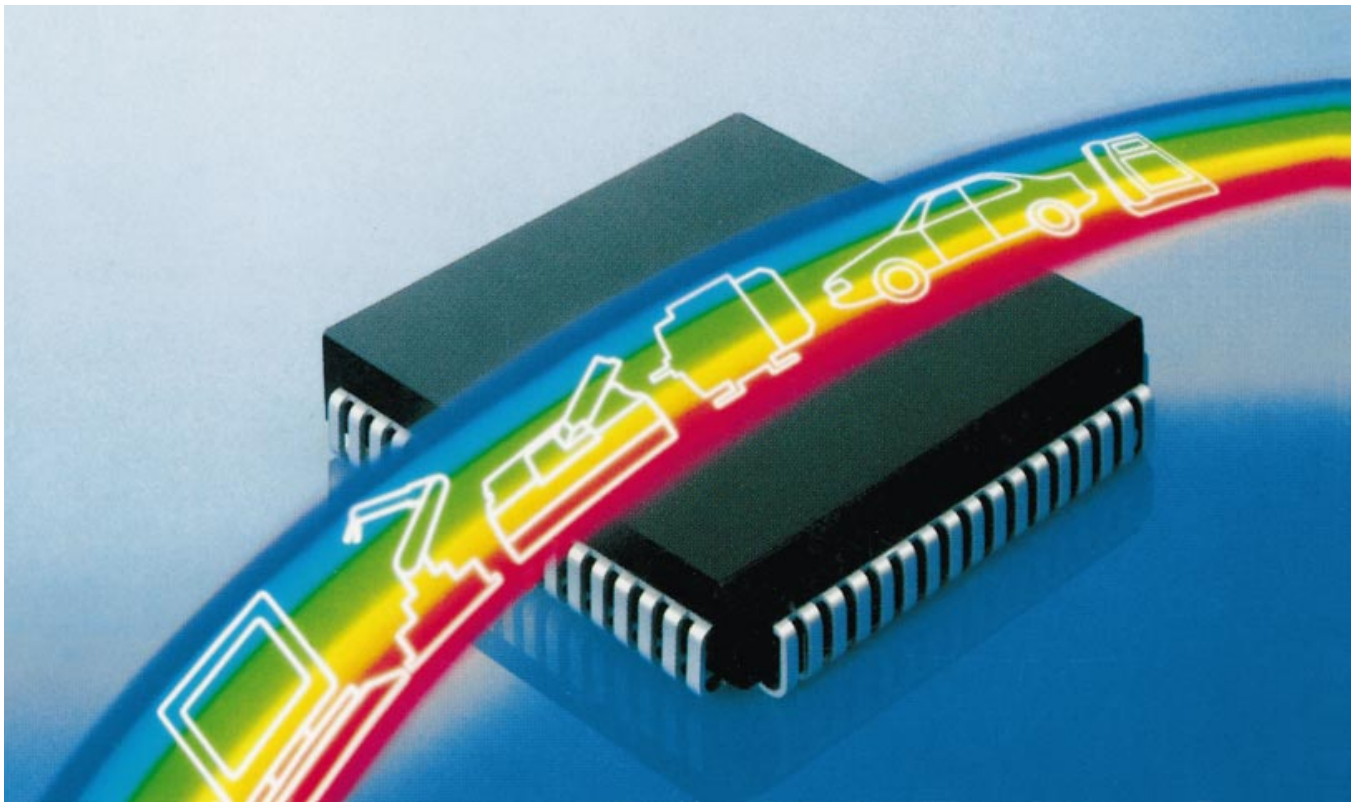

Microcomputer Components

SAB 80C515A/83C515A-5
8-Bit CMOS Single-Chip Microcontroller Family

Addendum to User's Manual SAB 80515/80C515 08.95

SAB 80C515A/83C515A-5 Addendum Revision History:	Current Version: 08.95
Previous Version:	**11.92**
Page	Subjects (major changes since last revision)
3-6 3-16 5-4 5-10	CCH4 / CCL4 deleted Table supplemented (MOVX @Ri, $\overline{EA}$ = 1, 00) Falling edge for P4.0 / $\overline{ADST}$ in figure 5-2 added Formula for SREL added
6-1	New release of SAB 80C515A / 83C515A-5 data sheet inserted

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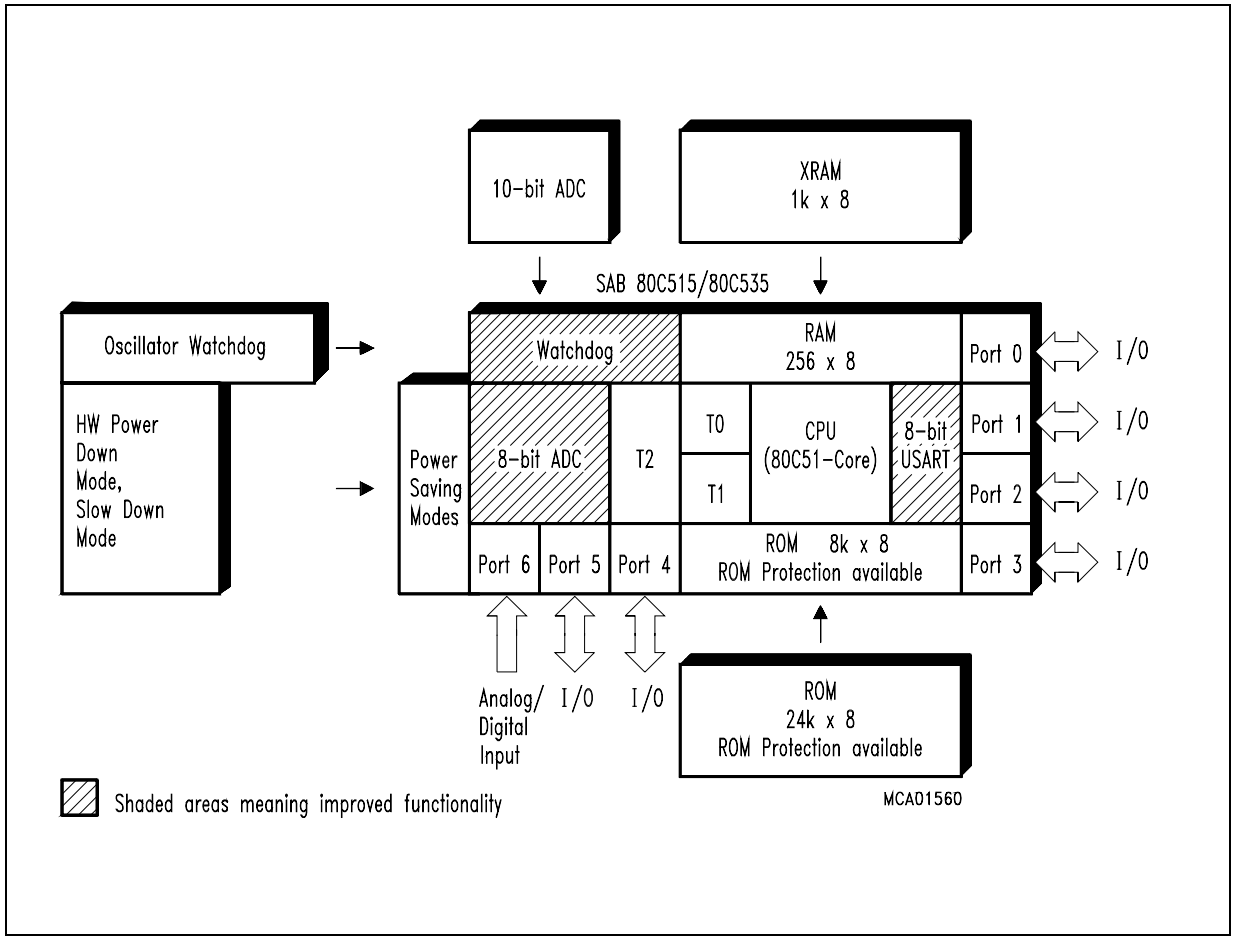
1 Introduction

The SAB 80C515A is a superset of the high end microcontroller SAB 80C515.

While maintaining all architectural and operational characteristics of the SAB 80C515 the SAB 80C515A incorporates more on-chip RAM. A new 10-bit A/D-Converter is implemented as well as an oscillator watchdog unit. Also the operating frequency is higher than at the SAB 80C515.



SAB 80C515A / 83C515A-5

The SAB 80C515A is available in two different versions:

- "ROMless" Version SAB 80C515A. Although this part is called "ROMless" there is an internal ROM of 2 KByte (for Test and Loader Software)
- ROM Version SAB 83C515A-5. This part has 32 KByte on-chip ROM.

With exception of the ROM sizes both parts are identical. Therefore the term SAB 80C515A refers to both versions within this specification unless otherwise noted.

This manual describes only the new features of the SAB 80C515A in addition to the features of the SAB 80C515/80C535. For reference to the SAB 80C515, the user's manual should be used.

Listed below is a summary of the main features of the SAB 80C515A:

- SAB 80C515A/83C515A-5, up to 18 MHz operation frequency
- 32 K × 8 ROM (SAB 83C515A-5 only, ROM-Protection available)
- 256 × 8 on-chip RAM
- additional 1 K × 8 on-chip RAM (XRAM)
- Superset of SAB 80C51 architecture:
  - 1 µs instruction cycle time at 12 MHz
  - 666 ns instruction cycle time at 18 MHz
  - 256 directly addressable bits
- Boolean processor
- 64 Kbyte external data and program memory addressing
- Three 16-bit timer/counters
- Versatile "fail-safe" provisions
- 12 interrupt vectors, four priority levels selectable
- genuine 10-bit A/D converter with 8 multiplexed inputs
- Full duplex serial interface with programmable Baudrate-Generator
- Functionally compatible with SAB 80C515
- Extended power saving modes
- Fast Power-On Reset
- Six ports: 48 I/O lines, 8 input lines
- Three temperature ranges available:
  0 to 70 °C (T1)
  – 40 to + 85 °C (T3)
  – 40 to + 110 °C (T4)
- Plastic package: P-LCC-68

The pin functions of the SAB 80C515A are identical with those of the SAB 80C515 with following exceptions:

	SAB 80C515A	SAB 80C515
Pin 68	$\overline{\text{HWPD}}$	V_{CC}
Pin 1	P4.0/$\overline{\text{ADST}}$	P4.0
Pin 4	$\overline{\text{PE}}$/SWD	$\overline{\text{PE}}$

2 Fundamental Structure

The SAB 80C515A/83C515A-5 is a high-end member of the Siemens SAB 8051 microcontroller family. It is designed in Siemens ACMOS technology and based on the SAB 8051 architecture. ACMOS is a technology which combines high-speed and density characteristics with low-power consumption or dissipation.

While maintaining all the SAB 80C515 features and operating characteristics the SAB 80C515A/ 83C515A-5 contains more on-chip RAM/ROM. Furthermore a new 10-bit A/D-Converter is implemented as well as extended security mechanisms. The SAB 80C515A is identical with the SAB 83C515A-5 except that it lacks the on-chip program memory. The SAB 80C515A/ 83C515A-5 is supplied in a 68-pin plastic leaded chip carrier package (P-LCC-68).

The essential enhancements to the SAB 80C515 are (see also **figure 2-1**):

- Additional 1KByte RAM on chip
- 8-Channel 10-bit A/D Converter
- New baud rate generator for the Serial Channel
- Oscillator Watchdog Unit
- Improved functionality of the Watchdog Timer
- Hardware controlled Power Down Mode
- High speed operation of the device (up to 18 MHz crystal frequency)

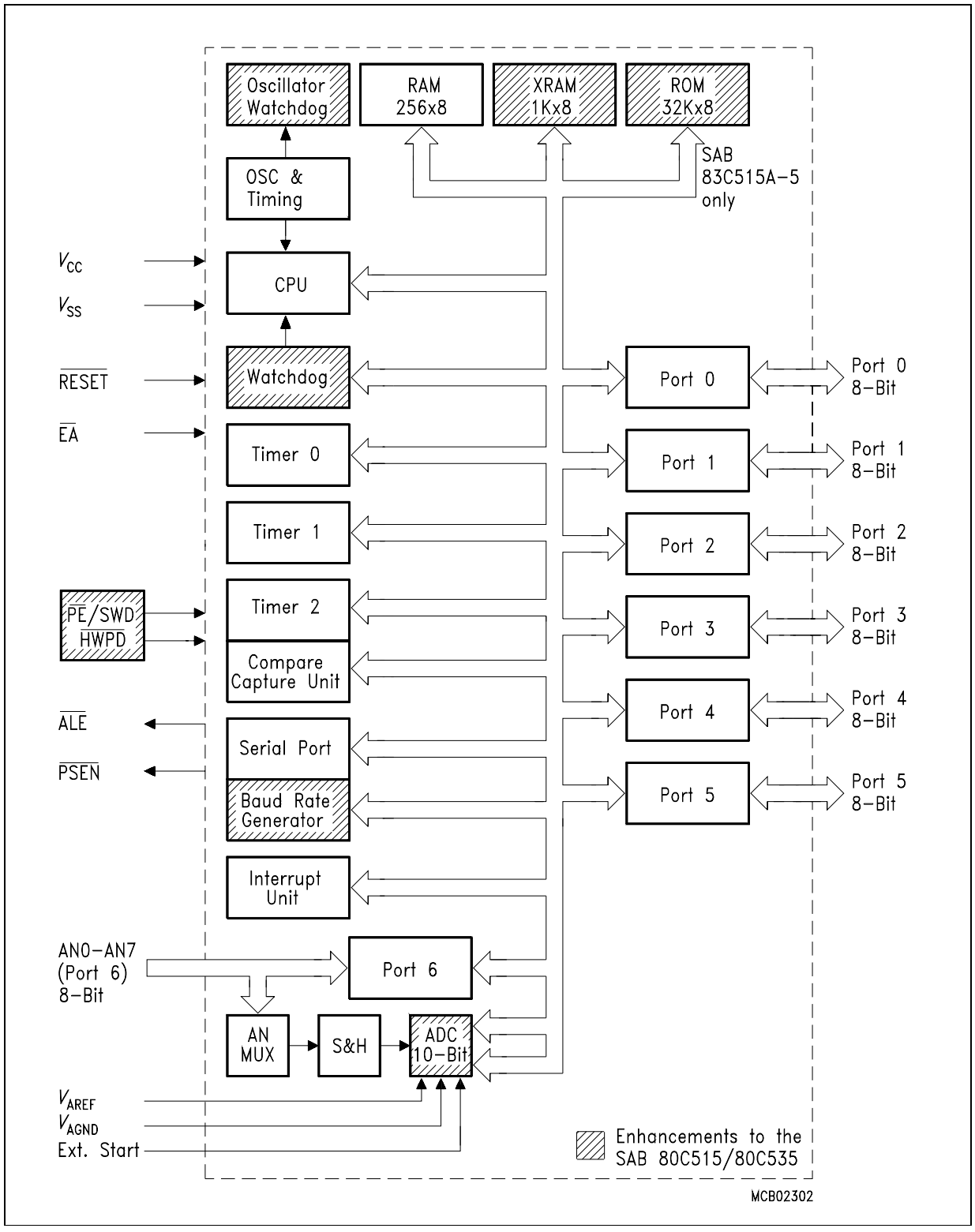


Figure 2-1
Block Diagram of the SAB 80C515A / 83C515A-5

3 Memory Organization

According to the SAB 8051 architecture, the SAB 80C515A has separate address spaces for program and data memory. **Figure 3-1** illustrates the mapping of address spaces.

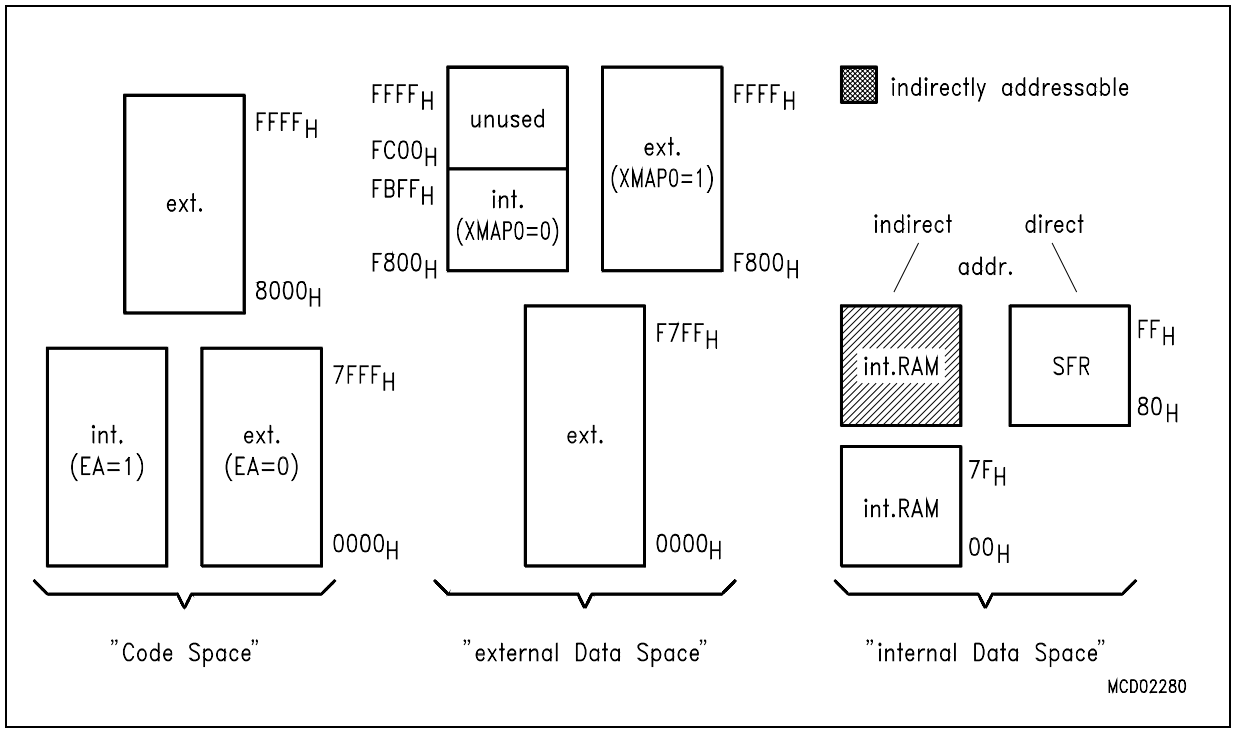


Figure 3-1
Memory Map

3.1 Program Memory, ROM Protection

The SAB 83C515A-5 has 32 Kbyte of on-chip ROM, while the SAB 80C515A has no internal ROM. The program memory can externally be expanded up to 64 Kbyte. Pin $\overline{EA}$ determines whether program fetches below address 8000H are done from internal or external memory.

As a new feature the SAB 83C515A-5 offers the possibility of protecting the internal ROM against unauthorized access. This protection is implemented in the ROM-Mask. Therefore, the decision ROM-Protection 'yes' or 'no' has to be made when delivering the ROM-Code. Once enabled, there is no way of disabling the ROM-Protection.

Effect: The access to internal ROM done by an externally fetched MOVC instruction is disabled. Nevertheless, an access from internal ROM to external ROM is possible.

To verify the read protected ROM-Code a special ROM-Verify-Mode is implemented. This mode also can be used to verify unprotected internal ROM.

ROM-Protection	ROM-Verification Mode (see 'AC Characteristics')	Restrictions
no	ROM-Verification Mode 1 (standard 8051 Verification Mode) ROM-Verification Mode 2	–
yes	ROM-Verification Mode 2	– standard 8051 Verification Mode is disabled – externally applied MOVC accessing internal ROM is disabled

3.2 Data Memory

The data memory space consists of an internal and an external memory space. The SAB 80C515A contains another 1 kByte of On-Chip RAM additional to the 256 Bytes internal RAM of the base type SAB 80C515. This RAM is called XRAM ('eXtended RAM') in this document.

- External Data Memory
  Up to 64 Kbyte external data memory can be addressed by instructions that use 8-bit or 16-bit indirect addressing. For 8-bit addressing MOVX instructions in combination with registers R0 and R1 can be used. A 16-bit external memory addressing is supported by a 16-bit datapointer. Registers XPAGE and SYSCON are controlling whether data fetches at addresses $F800_H$ to $FBFF_H$ are done from internal XRAM or from external data memory.
- Internal Data Memory
  The internal data memory is divided into four physically distinct blocks:
  - the lower 128 bytes of RAM including four register banks containing eight registers each
  - the upper 128 byte of RAM
  - the 128 byte special function register area
  - a 1Kx8 area which is accessed like external RAM (MOVX-instructions), implemented on chip at the address range from $F800_H$ to $FBFF_H$. Special Function Register SYSCON controls whether data is read from or written to XRAM or external RAM.

3.3 Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area.
All special function registers are listed in **table 3-1** and **table 3-2**.

In **table 3-1** they are organized in numeric order of their addresses. In **table 3-2** they are organized in groups which refer to the functional blocks of the SAB 80C515A.

Table 3-1
Special Function Register

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80_H	**P0** [1]	**FF_H**	**$A0_H$**	**P2** [1]	**FF_H**
81_H	SP	07_H	$A1_H$	reserved	XX_H [2]
82_H	DPL	00_H	$A2_H$	reserved	XX_H [2]
83_H	DPH	00_H	$A3_H$	reserved	XX_H [2]
84_H	(WDTL)		$A4_H$	reserved	XX_H [2]
85_H	(WDTH)		$A5_H$	reserved	XX_H [2]
86_H	WDTREL	00_H	$A6_H$	reserved	XX_H [2]
87_H	PCON	00_H	$A7_H$	reserved	XX_H [2]
88_H	**TCON** [1]	**00_H**	**$A8_H$**	**IEN0** [1]	**00_H**
89_H	TMOD	00_H	$A9_H$	IP0	00_H
$8A_H$	TL0	00_H	AA_H	SRELL	$0D9_H$
$8B_H$	TL1	00_H	AB_H	reserved	XX_H [2]
$8C_H$	TH0	00_H	AC_H	reserved	XX_H [2]
$8D_H$	TH1	00_H	AD_H	reserved	XX_H [2]
$8E_H$	reserved	XX_H [2]	AE_H	reserved	XX_H [2]
$8F_H$	reserved	XX_H [2]	AF_H	reserved	XX_H [2]
90_H	**P1** [1]	**FF_H**	**$B0_H$**	**P3** [1]	**FF_H**
91_H	XPAGE	00_H	$B1_H$	SYSCON	$XXXXXX01_B$ [2]
92_H	reserved	XX_H [2]	$B2_H$	reserved	XX_H [2]
93_H	reserved	XX_H [2]	$B3_H$	reserved	XX_H [2]
94_H	reserved	XX_H [2]	$B4_H$	reserved	XX_H [2]
95_H	reserved	XX_H [2]	$B5_H$	reserved	XX_H [2]
96_H	reserved	XX_H [2]	$B6_H$	reserved	XX_H [2]
97_H	reserved	XX_H [2]	$B7_H$	reserved	XX_H [2]
98_H	**SCON** [1]	**00_H**	**$B8_H$**	**IEN1** [1]	**00_H**
99_H	SBUF	XX_H [2]	$B9_H$	IP1	$XX000000_B$ [2]
$9A_H$	reserved	XX_H [2]	BA_H	SRELH	$XXXXXX11_B$ [2]
$9B_H$	reserved	XX_H [2]	BB_H	reserved	XX_H [2]
$9C_H$	reserved	XX_H [2]	BC_H	reserved	XX_H [2]
$9D_H$	reserved	XX_H [2]	BD_H	reserved	XX_H [2]
$9E_H$	reserved	XX_H [2]	BE_H	reserved	XX_H [2]
$9F_H$	reserved	XX_H [2]	BF_H	reserved	XX_H [2]

1) Bit-addressable Special Function Register

2) X means that the value is indeterminate and the location is reserved

Table 3-1, Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$C0_H$	**IRCON** [1]	**00_H**	**$E0_H$**	**ACC** [1]	**00_H**
$C1_H$	CCEN	00_H	$E1_H$	reserved	XX_H [2]
$C2_H$	CCL1	00_H	$E2_H$	reserved	XX_H [2]
$C3_H$	CCH1	00_H	$E3_H$	reserved	XX_H [2]
$C4_H$	CCL2	00_H	$E4_H$	reserved	XX_H [2]
$C5_H$	CCH2	00_H	$E5_H$	reserved	XX_H [2]
$C6_H$	CCL3	00_H	$E6_H$	reserved	XX_H [2]
$C7_H$	CCH3	00_H	$E7_H$	reserved	XX_H [2]
$C8_H$	**T2CON** [1]	**00_H**	**$E8_H$**	**P4** [1]	**FF_H**
$C9_H$	reserved	XX_H [2]	$E9_H$	reserved	XX_H [2]
CA_H	CRCL	00_H	EA_H	reserved	XX_H [2]
CB_H	CRCH	00_H	EB_H	reserved	XX_H [2]
CC_H	TL2	00_H	EC_H	reserved	XX_H [2]
CD_H	TH2	00_H	ED_H	reserved	XX_H [2]
CE_H	reserved	XX_H [2]	EE_H	reserved	XX_H [2]
CF_H	reserved	XX_H [2]	EF_H	reserved	XX_H [2]
$D0_H$	**PSW** [1]	**00_H**	**$F0_H$**	**B** [1]	**00_H**
$D1_H$	reserved	XX_H [2]	$F1_H$	reserved	XX_H [2]
$D2_H$	reserved	XX_H [2]	$F2_H$	reserved	XX_H [2]
$D3_H$	reserved	XX_H [2]	$F3_H$	reserved	XX_H [2]
$D4_H$	reserved	XX_H [2]	$F4_H$	reserved	XX_H [2]
$D5_H$	reserved	XX_H [2]	$F5_H$	reserved	XX_H [2]
$D6_H$	reserved	XX_H [2]	$F6_H$	reserved	XX_H [2]
$D7_H$	reserved	XX_H [2]	$F7_H$	reserved	XX_H [2]
$D8_H$	**ADCON0** [1]	**00_H**	**$F8_H$**	**P5** [1]	**FF_H**
$D9_H$	ADDATH	00_H	$F9_H$	reserved	XX_H [2]
DA_H	ADDATL	00_H	FA_H	reserved	XX_H [2]
DB_H	P6	XX_H [2]	FB_H		
DC_H	ADCON1	$XXXX0000_B$ [2]	FC_H		
DD_H	reserved	XX_H [2]	FD_H		
DE_H	reserved	XX_H [2]	FE_H		
DF_H	reserved	XX_H [2]	FF_H		

1) Bit-addressable Special Function Register

2) X means that the value is indeterminate and the location is reserved

Table 3-2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** [1]	00_H
	B	B-Register	**$F0_H$** [1]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	PSW	Program Status Word Register	$0D0_H$ [1]	00_H
	SP	Stack Pointer	81_H	07_H
A/D-Converter	ADCON0	A/D Converter Control Register 0	**$D8_H$** [1]	00_H
	ADCON1	A/D Converter Control Register 1	$0DC_H$	$0XXX\ 0000_B$ [3]
	ADDATH	A/D Converter Data Register High Byte	$0D9_H$	00_H
	ADDATL	A/D Converter Data Register Low Byte	$0DA_H$	00_H
Interrupt System	IEN0	Interrupt Enable Register 0	**$A8_H$** [1]	00_H
	IEN1	Interrupt Enable Register 1	**$B8_H$** [1]	00_H
	IP0	Interrupt Priority Register 0	$0A9_H$	00_H
	IP1	Interrupt Priority Register 1	$0B9_H$	$XX00\ 0000_B$ [3]
	IRCON	Interrupt Request Control Register	**$C0_H$** [1]	00_H
	TCON [2]	Timer Control Register	**88_H** [1]	00_H
	T2CON [2]	Timer 2 Control Register	**$C8_H$** [1]	00_H
Compare/ Capture-Unit (CCU)	CCEN	Comp./Capture Enable Reg.	$0C1_H$	00_H
	CCH1	Comp./Capture Reg. 1, High Byte	$0C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$0C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$0C7_H$	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$0C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$0C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$0C6_H$	00_H
	CRCH	Com./Rel./Capt. Reg. High Byte	$0CB_H$	00_H
	CRCL	Com./Rel./Capt. Reg. Low Byte	$0CA_H$	00_H
	TH2	Timer 2, High Byte	$0CD_H$	00_H
	TL2	Timer 2, Low Byte	$0CC_H$	00_H
	T2CON	Timer 2 Control Register	**$C8_H$** [1]	00_H
XRAM	XPAGE	Page Addr. Reg. for extended onchip RAM	91_H	00_H
	SYSCON	XRAM Control Reg.	$0B1_H$	$XXXX\ XX01_B$ [3]

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) X means that the value is indeterminate and the location is reserved

Table 3-2, Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80_H** 1)	$0FF_H$
	P1	Port 1	**90_H** 1	$0FF_H$
	P2	Port 2	**$A0_H$** 1)	$0FF_H$
	P3	Port 3	**$B0_H$** 1)	$0FF_H$
	P4	Port 4	**$E8_H$** 1)	$0FF_H$
	P5	Port 5	**$F8_H$** 1)	$0FF_H$
	P6	Port 6, Analog/Digital Input	DB_H	
Power Save Modes	PCON	Power Control Register	87_H	00_H
Serial Channels	ADCON0 2)	A/D Converter Control Reg.	**$0D8_H$** 1)	00_H
	PCON 2)	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Reg.	99_H	$0XX_H$ 3)
	SCON	Serial Channel Control Reg.	**98_H** 1)	00_H
	SRELL	Serial Channel Reload Reg., low byte	AA_H	$D9_H$
	SRELH	Serial Channel Reload Reg., high byte	BA_H	XXXX $XX11_B$ 3)
Timer 0/ Timer 1	TCON	Timer Control Register	**88_H** 1)	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Watchdog	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
	IP0 2)	Interrupt Priority Register 0	$A9_H$	00_H
	IP1 2)	Interrupt Priority Register 1	$B9_H$	XX00 0000_B 3)
	WDTREL	Watchdog Timer Reload Reg.	86_H	00_H

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) X means that the value is indeterminate and the location is reserved

3.4 Architecture of the XRAM

The contents of the XRAM is not affected by a reset or HW Power Down. After power-up the contents is undefined, while it remains unchanged during and after a reset or HW Power Down if the power supply is not turned off.

The additional On-Chip RAM is logically located in the "external data memory" range at the upper end of the 64 KByte address range ($F800_H$ -$FBFF_H$). Nevertheless when XRAM is enabled the address range $F800_H$ to $FFFF_H$ is occupied. This is done to assure software compatibility to SAB 80C517A. It is possible to enable and disable (only by reset) the XRAM. If it is disabled the device shows the same behaviour as the parts without XRAM, i.e. all MOVX accesses use the external bus to physically external data memory.

3.4.1 Accesses to XRAM

Because the XRAM is used in the same way as external data memory the same instruction types must be used for accessing the XRAM.

Note:

If a reset occurs during a write operation to XRAM, the effect on XRAM depends on the cycle which the reset is detected at (MOVX is a 2-cycle instruction):

Reset detection at cycle 1: The new value will not be written to XRAM. The old value is not affected.

Reset detection at cycle 2: The old value in XRAM is overwritten by the new value.

Accesses to XRAM using the DPTR

There are a Read and a Write instruction from and to XRAM which use one of the 16-bit DPTR for indirect addressing. The instructions are:

```
MOVX    A, @DPTR    (Read)
MOVX    @DPTR, A    (Write)
```

Normally the use of these instructions would use a physically external memory. However, in the SAB 80C515A the XRAM is accessed if it is enabled and if the DPTR points to the XRAM address space (DPTR $\geq F800_H$).

Accesses to XRAM using the Registers R0/R1

The 8051 architecture provides also instructions for accesses to external data memory range which use only an 8-bit address (indirect addressing with registers R0 or R1). The instructions are:

MOVX	A, @ Ri	(Read)
MOVX	@Ri, A	(Write)

In application systems, either a real 8-bit bus (with 8-bit address) is used or Port 2 serves as page register which selects pages of 256-Byte. However, the distinction, whether Port 2 is used as general purpose I/0 or as "page address" is made by the external system design. From the device's point of view it cannot be decided whether the Port 2 data is used externally as address or as I/0 data!

Hence, a special page register is implemented into the SAB 80C515A to provide the possibility of accessing the XRAM also with the MOVX @Ri instructions, i.e. XPAGE serves the same function for the XRAM as Port 2 for external data memory.

Special Function Register XPAGE

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr.91H									XPAGE

The reset value of XPAGE is 00_H.

XPAGE can be set and read by software.

Figures 3-2 to **3-4** show the dependencies of XPAGE- and Port 2 - addressing in order to explain the differences in accessing XRAM, ext. RAM or what is to do when Port 2 is used as an I/O-port.

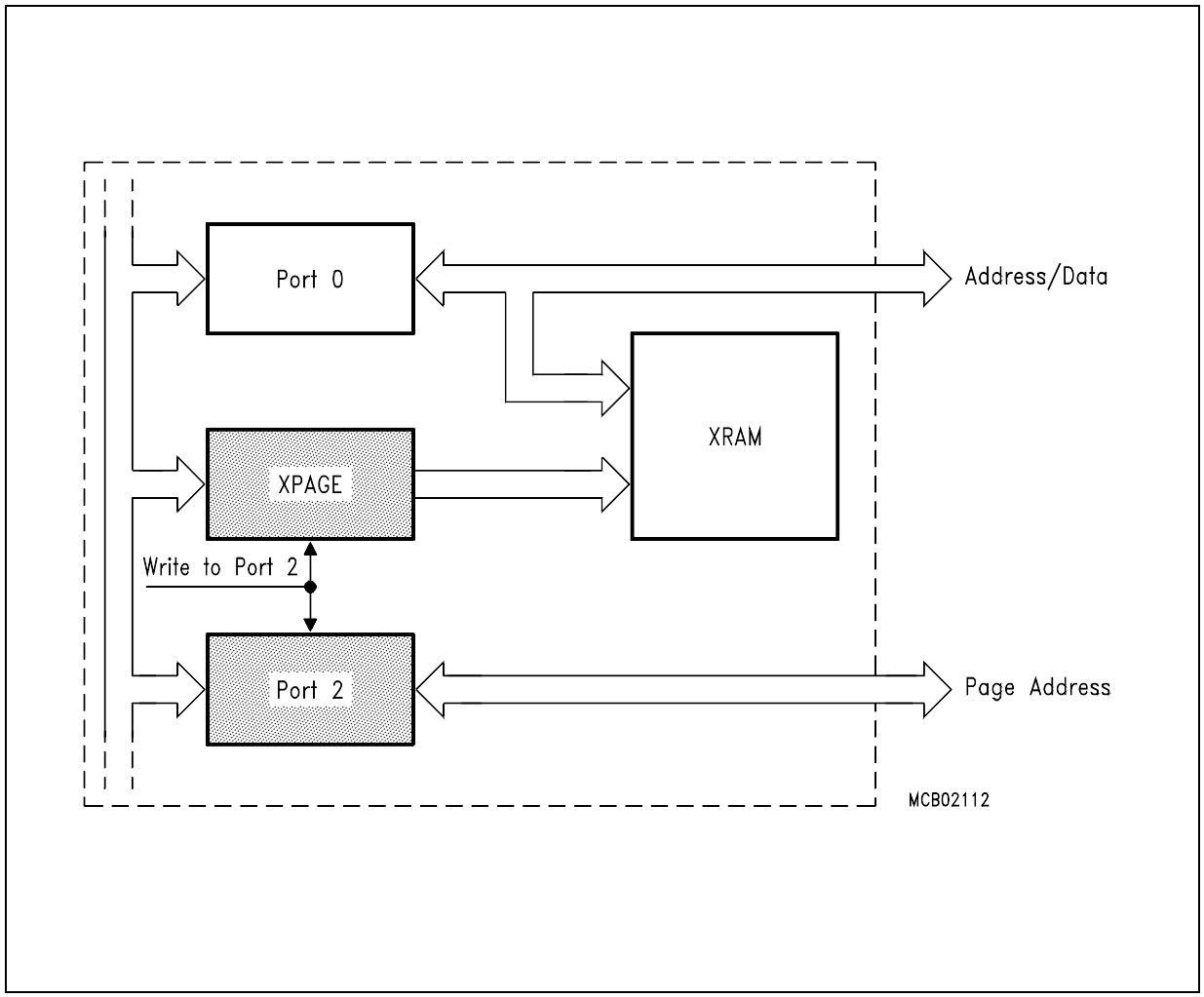


Figure 3-2
Write Page Address to Port 2

MOV P2, pageaddress will write the page address to Port 2 **and** XPAGE-Register.

When external RAM is to be accessed in the XRAM address range ($F800_H$ - $FFFF_H$) XRAM has to be disabled. When additional external RAM is to be addressed in an address range ≤ XRAM ($F800_H$) XRAM may remain being enabled and there is no need to overwrite XPAGE by a second move.

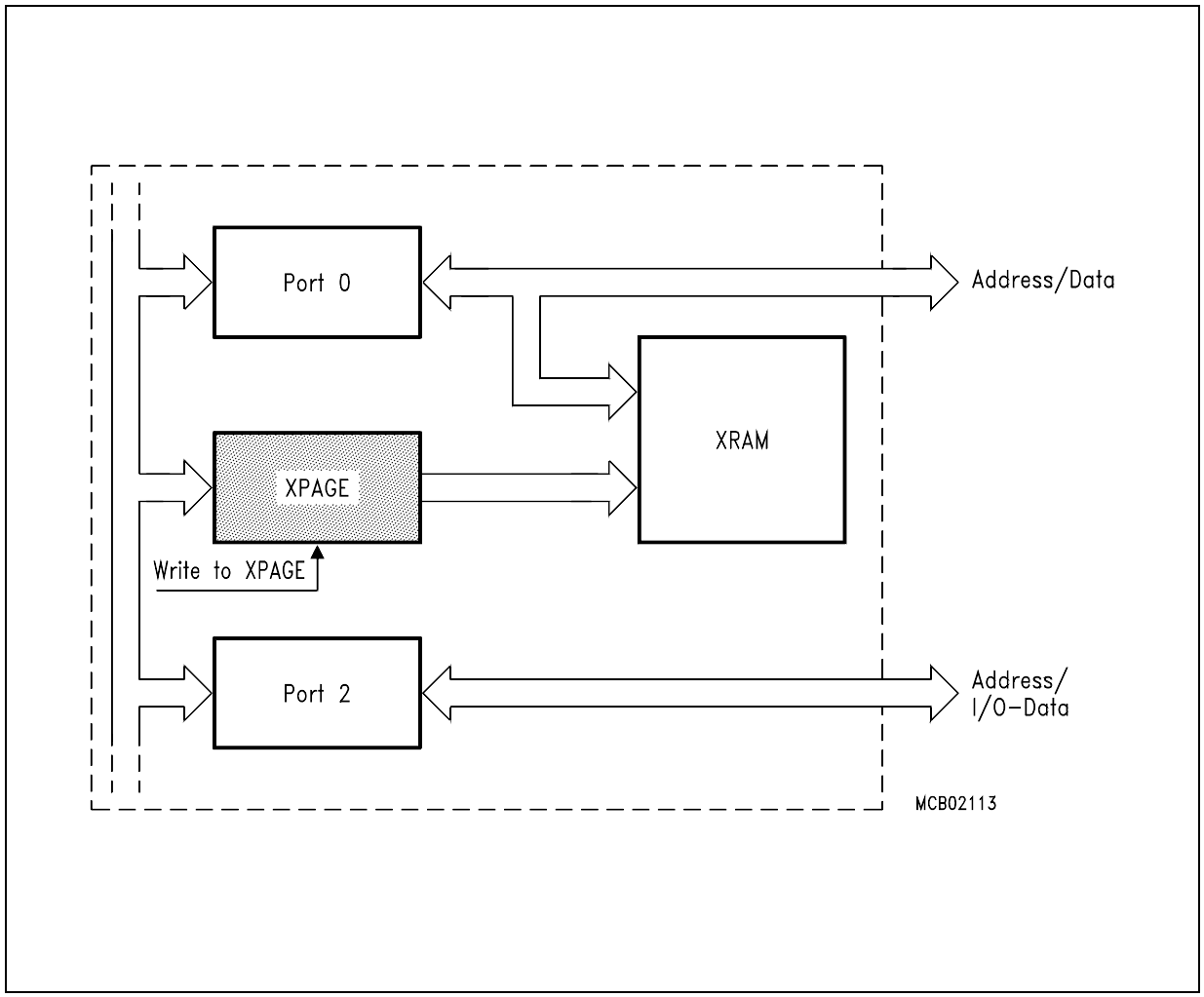


Figure 3-3
Write Page Address to XPAGE

The page address is only written to XPAGE-register. Port 2 is available for addresses or I/O-Data. See **figure 3-4** to see what happens when Port 2 is used as I/O-Port.

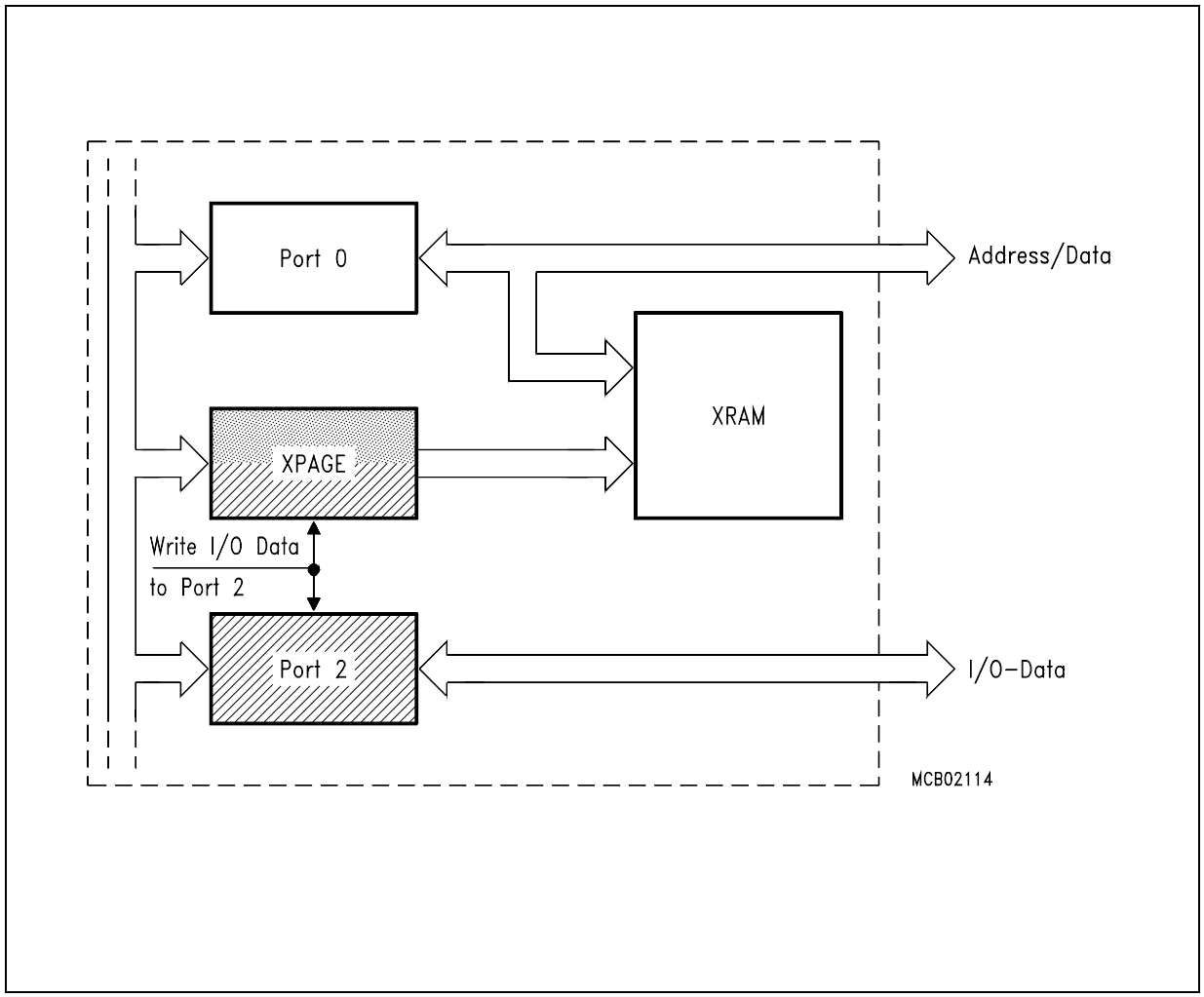


Figure 3-4
Use of Port 2 as I/O-Port

At a write to Port 2, XRAM address in XPAGE-register will be overwritten because of the concurrent write to Port 2 and XPAGE-register. So whenever XRAM is used and the XRAM address differs from the byte written to Port 2 latch it is absolutely necessary to rewrite XPAGE with page address.

Example:

I/O-Data at Port 2 shall be $0AA_H$. A Byte shall be fetched from XRAM at address $0F830_H$

```
MOV R0, #30H
MOV P2, #0AAH        ; P2 shows 0AAH
MOV XPAGE, #0F8H     ; P2 still shows 0AAH but XRAM is addressed
MOVX A, @R0          ; the contents of XRAM at 0F830H is moved to accu
```

The register XPAGE provides the upper address byte for accesses to XRAM with MOVX @Ri instructions. If the address formed from XPAGE and Ri is less than the XRAM address range, then an external access is performed. For the SAB 80C515A the contents of XPAGE must be greater or equal than F8H in order to use the XRAM. Of course, the XRAM must be enabled if it shall be used with MOVX @Ri instructions.

Thus, the register XPAGE is used for addressing of the XRAM; additionally its contents are used for generating the internal XRAM select. If the contents of XPAGE is less than the XRAM address range then an external bus access is performed where the upper address byte is provided by P2 and not by XPAGE!

Therefore, the software has to distinguish two cases, if the MOVX @Ri instructions with paging shall be used:

a) Access to XRAM: The upper address byte must be written to XPAGE or P2; both writes selects the XRAM address range.

b) Access to external memory: The upper address byte must be written to P2; XPAGE will be loaded with the same address in order to deselect the XRAM.

The behaviour of Port0, Port2 and the $\overline{RD}$/$\overline{WR}$ signals depends on the state of pin $\overline{EA}$ and on the control bits XMAP0 and XMAP1 in register SYSCON.

3.4.2 Control of XRAM in the SAB 80C515A

There are two control bits in register SYSCON which control the use and the bus operation during accesses to the additional On-Chip RAM in XDATA range (≙XRAM).

Special Function Register SYSCON

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr.0B1$_H$	–	–	–	–	–	–	XMAP1	XMAP0	SYSCON

Bit	Function
XMAP0	Global enable/disable bit for XRAM memory. XMAP0 = 0: The access to XRAM (= On-Chip XDATA memory) is enabled. XMAP0 = 1: The access to RAM is disabled. All MOVX accesses are performed by the external bus. This bit is hardware protected.
XMAP1	Control bit for $\overline{RD}$/$\overline{WR}$ signals during accesses to XRAM; this bit has no effect if XRAM is disabled (XMAP0 = 1) or if addresses outside the XRAM address range are used for MOVX accesses. XMAP1 = 0: The signals $\overline{RD}$ and $\overline{WR}$ are not activated during accesses to XRAM. XMAP1 = 1: Ports 0, 2 and the signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM.

Reset value of SYSCON is XXXX XX01$_B$.

The control bit XMAP0 is a global enable/disable bit for the additional On-Chip RAM (XRAM). If this bit is set, the XRAM is disabled, all MOVX accesses use external memory via the external bus. In this case the SAB 80C515A can't use the additional On-Chip RAM and is compatible with the types without XRAM.

A hardware protection is done by an unsymmetric latch at XMAP0-bit. A unintentional disabling of XRAM could be dangerous since indeterminate values could be read from external bus. To avoid this the XMAP-bit is forced to '1' only by reset. Additional during reset an internal capacitor is loaded. So the reset state is a disabled XRAM. Because of the load time of the capacitor XMAP0-bit once written to '0' (that is, discharging capacitor) cannot be set to '1' again by software. On the other hand any distortion (software hang up, noise,...) is not able to load this capacitor, too. That is, the stable status is XRAM enabled. The only way to disable XRAM after it was enabled is a reset.

The clear instruction for the XMAP0-bit should be integrated in the program initialization routine before XRAM is used. In extremely noisy systems the user may have redundant clear instructions.

The control bit XMAP1 is relevant only if the XRAM is accessed. In this case the external $\overline{RD}$ and $\overline{WR}$ signals at P3.6 and P3.7 are not activated during the access, if XMAP1 is cleared. For debug purposes it might be useful to have these signals and the Ports 0, 2 available. This is performed if XMAP1 is set.

3.4.3 Behaviour of Port0 and Port2

The behaviour of Port 0 and P2 during a MOVX access depends on the control bits in register SYSCON and on the state of pin $\overline{EA}$. The **table 3-3** lists the various operating conditions. It shows the following characteristics:

a) Use of P0 and P2 pins during the MOVX access.
   Bus: The pins work as external address/data bus. If (internal) XRAM is accessed, the data written to the XRAM can be seen on the bus in debug mode.
   I/0: The pins work as Input/Output lines under control of their latch.
b) Activation of the $\overline{RD}$ and $\overline{WR}$ pin during the access.
c) Use of internal or external XDATA memory.

The shaded areas describe the standard operation as each 80C51 device without on-chip XRAM behaves.

		$\overline{EA}$ = 0			$\overline{EA}$ = 1		
		XMAP1, XMAP0			XMAP1, XMAP0		
		00	10	X1	00	10	X1
MOVX @DPTR	DPTR < XRAM address range	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used
	DPTR ≥ XRAM address range	a)P0/P2→Bus ($\overline{WR}$-Data only) b)$\overline{RD}$/$\overline{WR}$ inactive c)XRAM is used	a)P0/P2→Bus ($\overline{WR}$-Data only) b)$\overline{RD}$/$\overline{WR}$ active c)XRAM is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c) ext.memory is used	a)P0/P2→I/O b)$\overline{RD}$/$\overline{WR}$ inactive c)XRAM is used	a)P0/P2→Bus ($\overline{WR}$-Data only) b)$\overline{RD}$/$\overline{WR}$ active c)XRAM is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c) ext.memory is used
MOVX @ Ri	XPAGE < XRAM addr.page range	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used
	XPAGE ≥ XRAM addr.page range	a)P0→Bus ($\overline{WR}$-Data only) P2→I/O b)$\overline{RD}$/$\overline{WR}$ inactive c)XRAM is used	a)P0→Bus ($\overline{WR}$-Data only) P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)XRAM is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P2→I/O P0/P2→I/O b)$\overline{RD}$/$\overline{WR}$ inactive c)XRAM is used	a)P0→Bus ($\overline{WR}$-Data only) P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)XRAM is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used

modes compatible to 8051-family

Table 3-3
Behaviour of P0/P2 and RD/WR During MOVX Accesses

4 System Reset

4.1 Additional Hardware Power Down Mode in the SAB 80C515A

The SAB 80C515A has an additional Power Down Mode which can be initiated by an external signal at a dedicated pin. This pin is labeled $\overline{\text{HWPD}}$ and is a floating input line (active low). This pin substitutes one of the V_{CC} pins of the base types SAB 80C515 (PLCC68: Pin68). Because this new power down mode is activated by an external hardware signal this mode is referred to as Hardware Power Down Mode in opposite to the program controlled Software Power Down Mode.

Pin $\overline{\text{PE}}$/SWD has no control function for the Hardware Power Down Mode; it enables and disables only the use of all software controlled power saving modes (Idle Mode, Software Power Down Mode).

The function of the new Hardware Power Down Mode is as follows:

The pin $\overline{\text{HWPD}}$ controls this mode. If it is on logic high level (inactive) the part is running in the normal operating modes. If pin $\overline{\text{HWPD}}$ gets active (low level) the part enters the Hardware Power Down Mode; as mentioned above this is independent of the state of pin $\overline{\text{PE}}$/SWD.

$\overline{\text{HWPD}}$ is sampled once per machine cycle. If it is found active, the device starts a complete internal reset sequence. This takes two machine cycles; all pins have their default reset states during this time. This reset has exactly the same effects as a hardware reset; i.e.especially the watchdog timer is stopped and its status flag WDTS is cleared. In this phase the power consumption is not yet reduced. After completion of the internal reset both oscillators of the chip are disabled, the on-chip oscillator as well as the oscillator watchdog's RC oscillator. At the same time the port pins and several control lines enter a floating state as shown in **table 4-1**. In this state the power consumption is reduced to the power down current I_{PD}. Also the supply voltage can be reduced. **Table 4-1** also lists the voltages which may be applied at the pins during Hardware Power Down Mode without affecting the low power consumption.

Table 4-1
Status of all Pins During Hardware Power Down Mode

Pins	Status	Voltage Range at Pin During HW-Power Down
P0, P1, P2, P3, P4, P5, P6	Floating outputs/ Disabled input function	$V_{SS} \le V_{IN} \le V_{CC}$
$\overline{EA}$	Active input	$V_{IN} = V_{CC}$ or $V_{IN} = V_{SS}$
$\overline{PE}$/SWD	Active input, Pull-up resistor Disabled during HW power down	$V_{IN} = V_{CC}$ or $V_{IN} = V_{SS}$
XTAL 1	Active output	pin may not be driven
XTAL 2	Disabled input function	$V_{SS} \le V_{IN} \le V_{CC}$
$\overline{PSEN}$, ALE	Floating outputs/ Disabled input function (for test modes only)	$V_{SS} \le V_{IN} \le V_{CC}$
$\overline{Reset}$	Active input; must be at high level if HWPD is used	$V_{IN} = V_{CC}$
V_{AREF}	ADC reference supply input	$V_{SS} \le V_{IN} \le V_{CC}$

The power down state is maintained while pin $\overline{\text{HWPD}}$ is held active. If HWPD goes to high level (inactive state) an automatic start up procedure is performed:

- First the pins leave their floating condition and enter their default reset state as they had immediately before going to float state.
- Both oscillators are enabled. While the on-chip oscillator (with pins XTAL1 and XTAL2) usually needs a longer time for start-up, if not externally driven (with crystal approx. 1 ms), the oscillator watchdog's RC oscillator has a very short start-up time (typ. less than 2 microseconds).
- Because the oscillator watchdog is active it detects a failure condition if the on-chip oscillator hasn't yet started. Hence, the watchdog keeps the part in reset and supplies the internal clock from the RC oscillator.
- Finally, when the on-chip oscillator has started, the oscillator watchdog releases the part from reset after it performed a final internal reset sequence and switches the clock supply to the on-chip oscillator. This is exactly the same procedure as when the oscillator watchdog detects first a failure and then a recovering of the oscillator during normal operation. Therefore, also the oscillator watchdog status flag is set after restart from Hardware Power Down Mode.
  When automatic start of the watchdog was enabled ($\overline{\text{PE}}$/SWD connected to V_{CC}), the Watchdog Timer will start, too (with its default reload value for time-out period).

The SWD-Function of the $\overline{\text{PE}}$/SWD Pin is sampled only by a hardware reset.Therefore at least one Power On Reset has to be performed.

4.2 Hardware Power Down Reset Timing

Following figures are showing the timing diagrams for entering (**figure 4-1**) and leaving (**figure 4-2**) the Hardware Power Down Mode. If there is only a short signal at pin $\overline{\text{HWPD}}$ (i.e. $\overline{\text{HWPD}}$ is sampled active only once), then a complete internal reset is executed. Afterwards the normal program execution starts again (**figure 4-3**).

Note:

Delay time caused by internal logic is not included.

The $\overline{\text{Reset}}$ pin overrides the Hardware Power Down function, i.e. if reset gets active during Hardware Power Down it is terminated and the device performs the normal reset function. Thus, pin $\overline{\text{Reset}}$ has to be inactive during Hardware Power Down Mode.

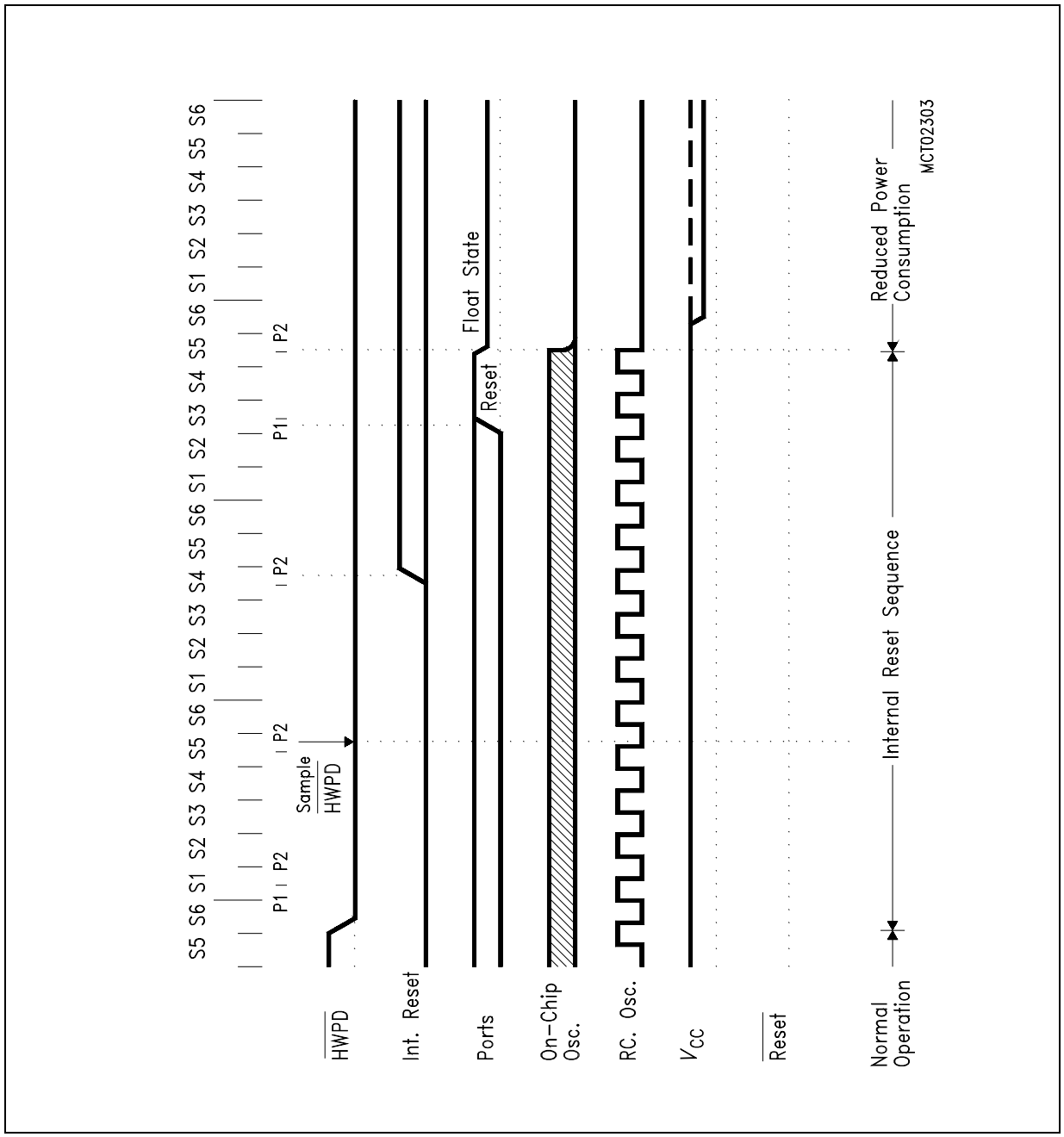


Figure 4-1
Timing Diagram of Entering Hardware Power Down Mode

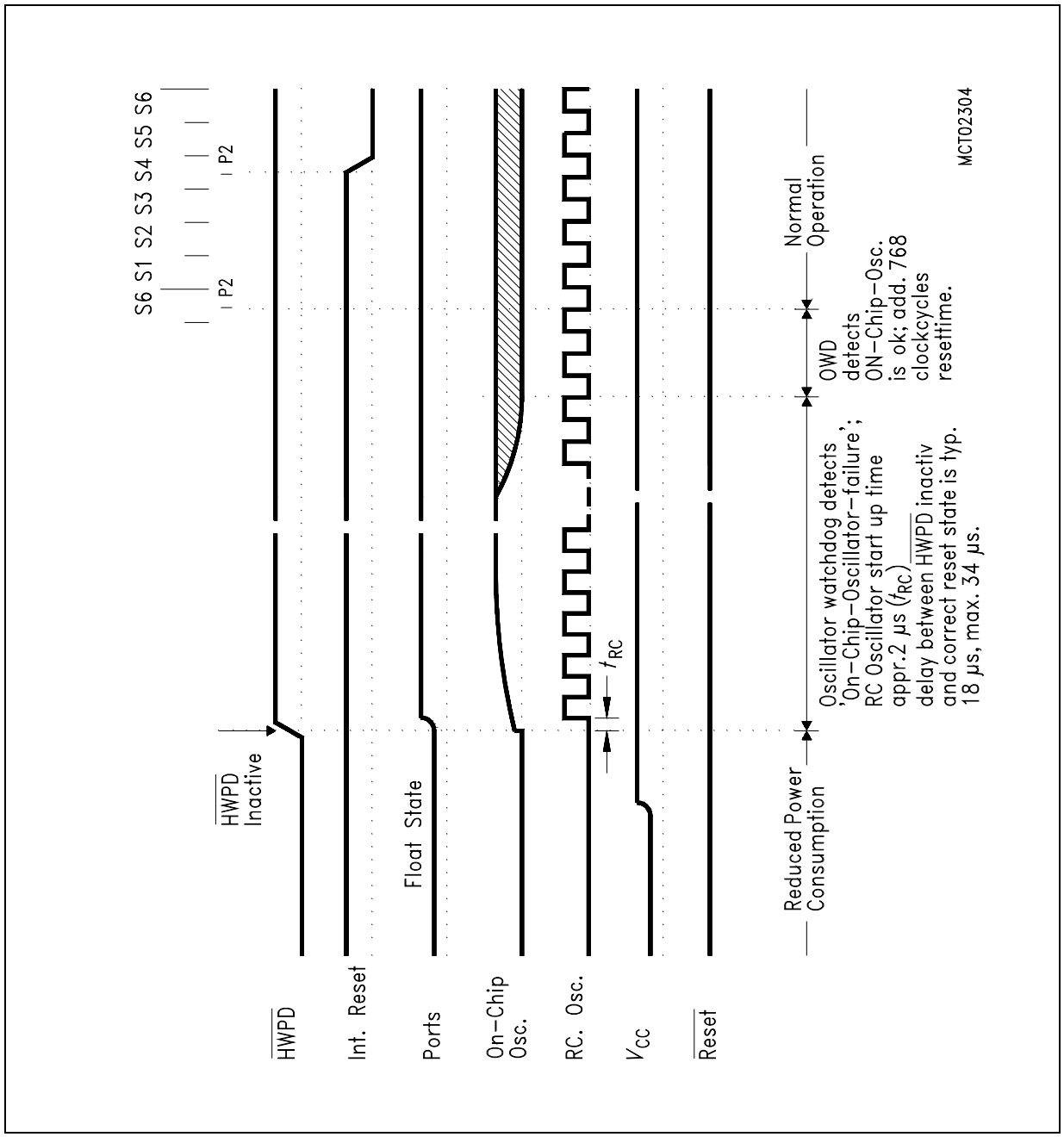


Figure 4-2
Timing Diagram of Leaving Hardware Power Down Mode

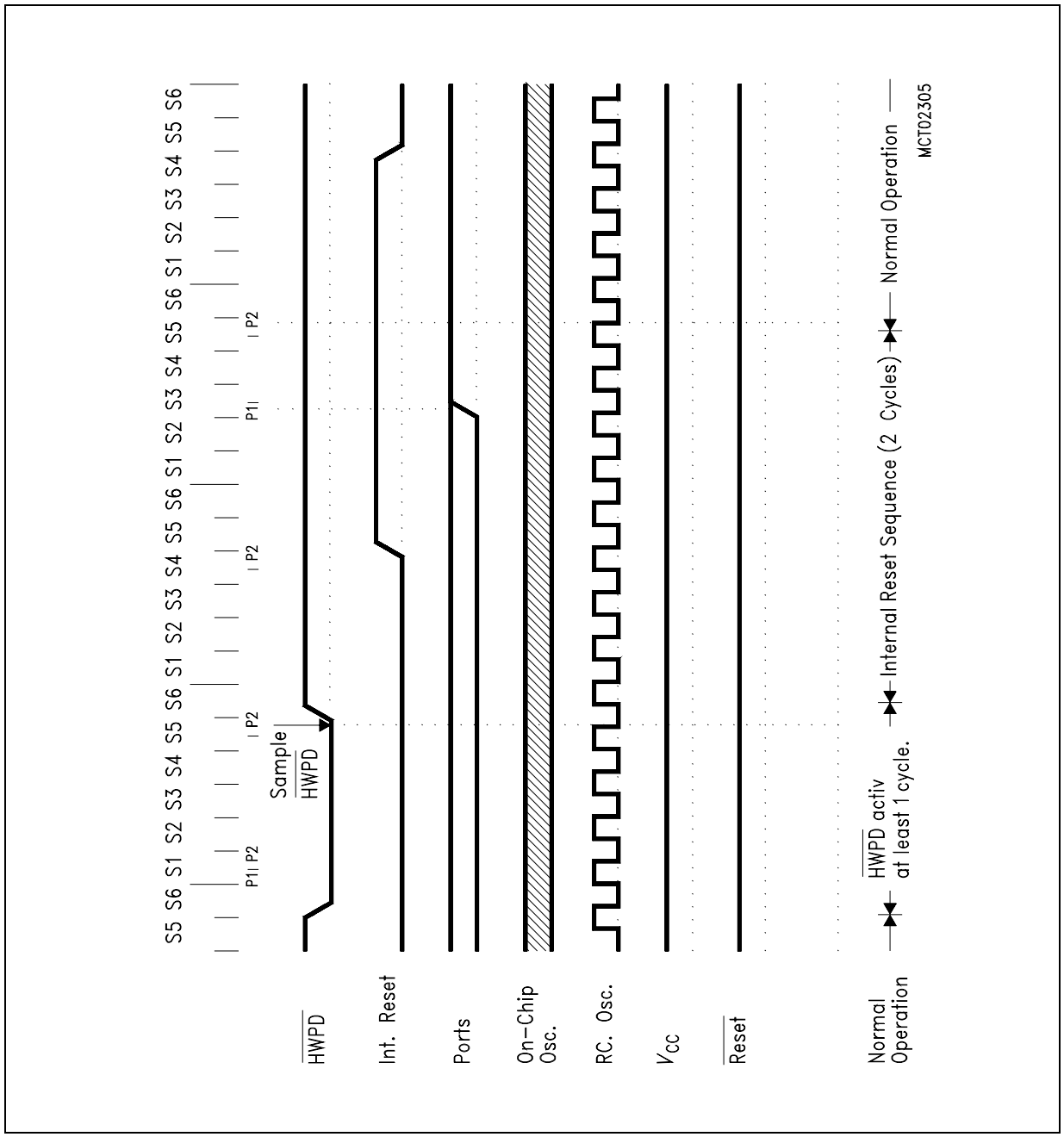


Figure 4-3
Timing Diagram of Hardware Power Down Mode, $\overline{\text{HWPD}}$-Pin is active for only one Cycle

4.3 Fast Internal Reset after Power-On

The SAB 80C515A can use the oscillator watchdog unit for a fast internal reset procedure after power-on.

Figure 4-4 shows the power-on sequence under control of the oscillator watchdog.

Normally the devices of the 8051 family (like the SAB 80C515) enter their default reset state not before the on-chip oscillator starts. The reason is that the external reset signal must be internally synchronized and processed in order to bring the device into the correct reset state. Especially if a crystal is used the start up time of the oscillator is relatively long (typ. 1ms). During this time period the pins have an undefined state which could have severe effects especially to actuators connected to port pins.

In the SAB 80C515A the oscillator watchdog unit can avoid this situation. In this case, after power-on the oscillator watchdog's RC oscillator starts working within a very short start-up time (typ. less than 2 microseconds). In the following the watchdog circuitry detects a failure condition for the on-chip oscillator because this has not yet started (a failure is always recognized if the watchdog's RC oscillator runs faster than the on-chip oscillator). As long as this condition is detected the watchdog uses the RC oscillator output as clock source for the chip rather than the on-chip oscillator's output. This allows correct resetting of the part and brings also all ports to the defined state (see **figure 4-4**). The time period from power-on until reaching the reset state at the ports derives from the following terms:

- RC oscillator start-up < 2 µs
- synchronization of the RC oscillators divider-by-5 < 6T
- synchronization of the state and cycle counters < 6T
- reset procedure till correct port states are reached < 12T

Delay between power-on and correct reset state:

Typ: 18 µs
Max.: 34 µs

After the on-chip oscillator finally has started, the oscillator watchdog detects the correct function; then the watchdog still holds the reset active for a time period of 768 cycles of the RC oscillator in order to allow the oscillation of the on-chip oscillator to stabilize (**figure 4-4**, II). Subsequently the clock is supplied by the on-chip oscillator and the oscillator watchdog's reset request is released (**figure 4-4**, III). However, an externally applied reset still remains active (**figure 4-4**, IV) and the device does not start program execution (**figure 4-4**, V) before the external reset is also released.

Although the oscillator watchdog provides a fast internal reset it is additionally necessary to apply the external reset signal when powering up. The reasons are as follows:

- Termination of Hardware Power Down Mode (a $\overline{\text{HWPD}}$ signal is overridden by reset)
- Termination of Software Power Down Mode
- Reset of the status flag OWDS that is set by the oscillator watchdog during the power up sequence.

The external reset signal must be hold active at least until the on-chip oscillator has started and the internal watchdog reset phase is completed. An external reset time of more than 50 µs should be sufficient in typical applications. If only a capacitor at pin $\overline{\text{Reset}}$ is used a value of less than 100 nF provides the desired reset time.

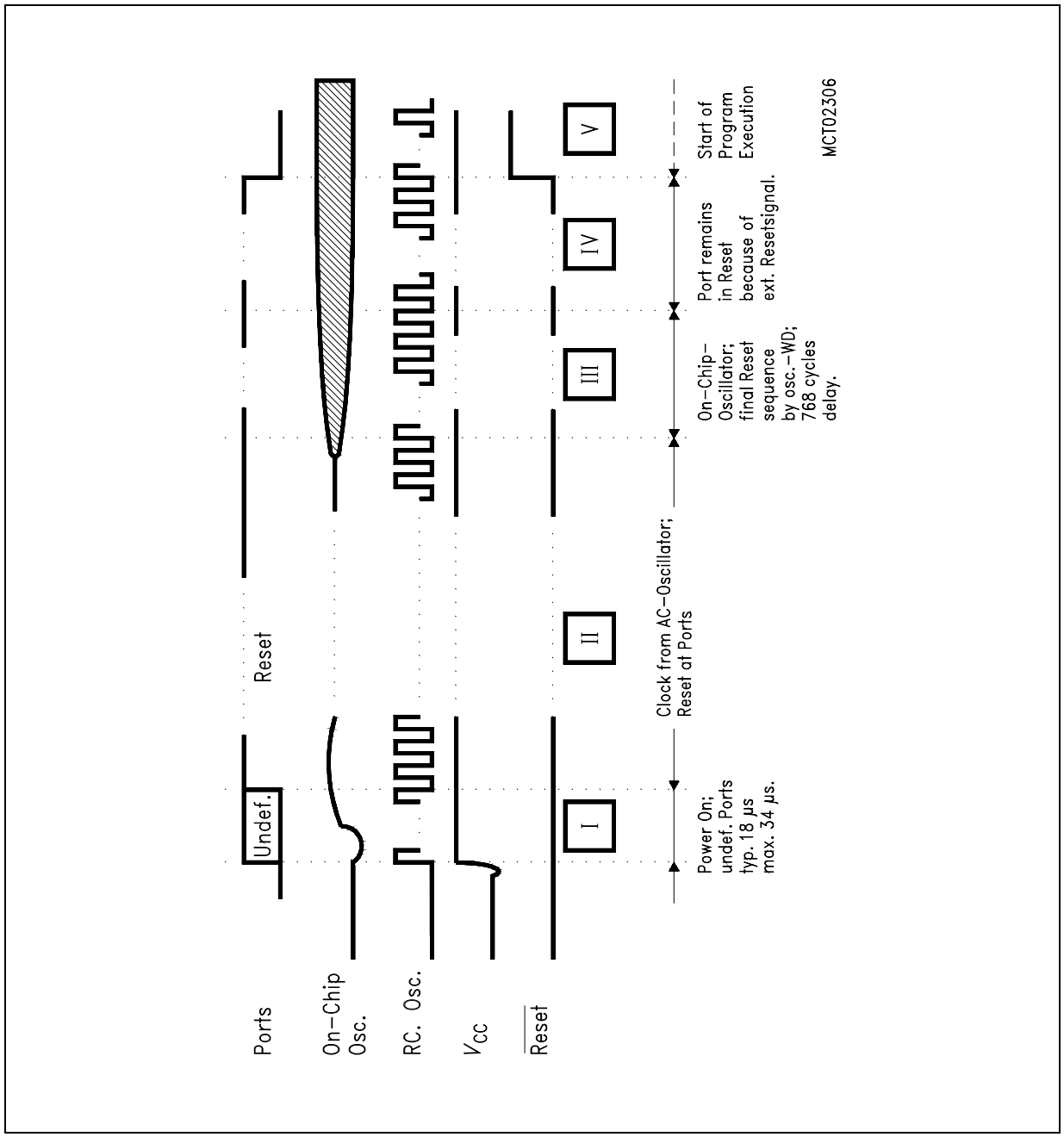


Figure 4-4
Power-on of the SAB 80C515A

5 On-Chip Peripheral Components

Digital I/O Port Circuitry

To realize the Hardware Power Down Mode with floating Port pins in the SAB 80C515A/83C515A-5 the standard port structure used in the 8051 Family is modified (**figure 5-1**).

The FETs p4, p5 and n2 are added. During Hardware Power Down this FETs disconnect the port pins from internal logic.

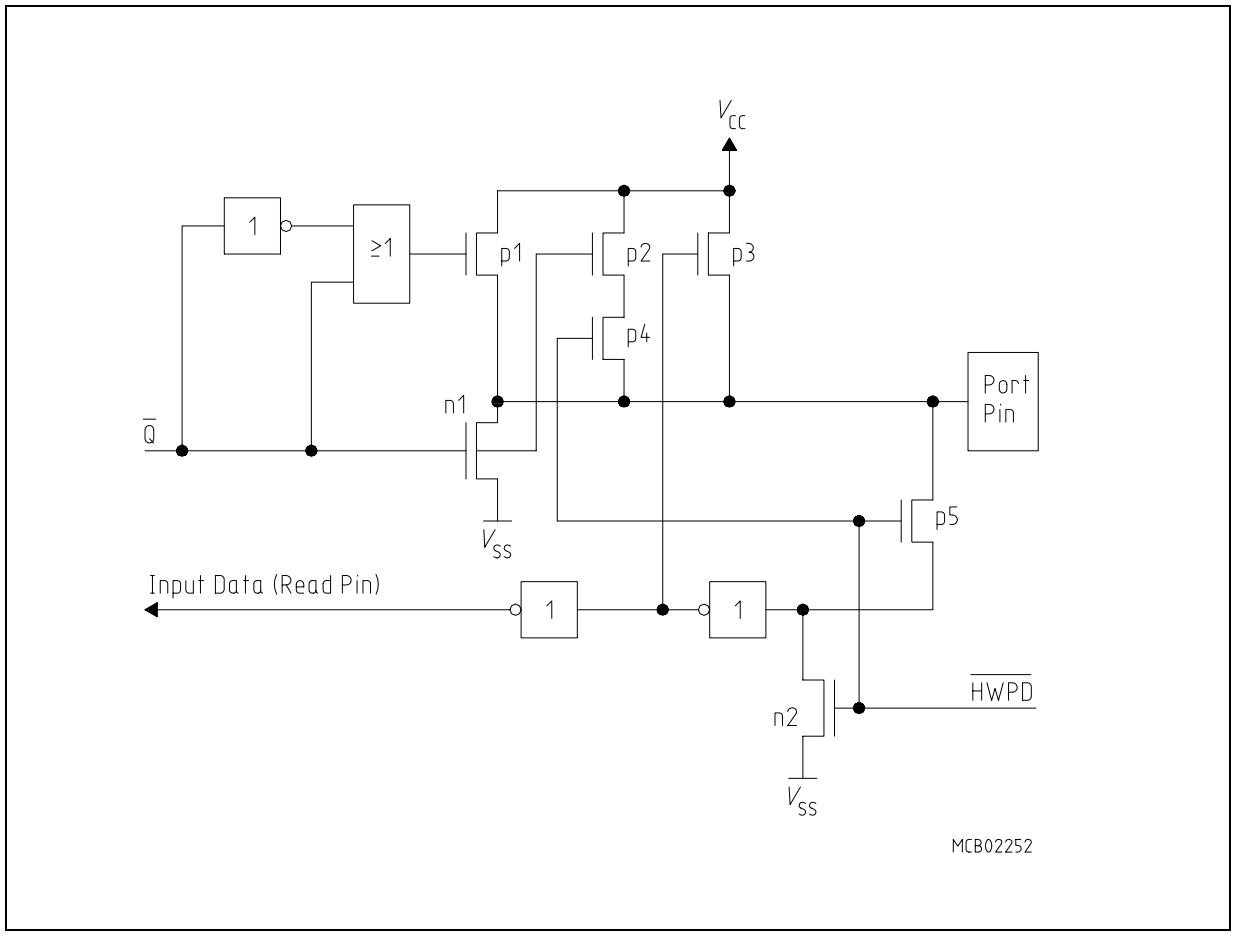


Figure 5-1
Port Structure

P1 and p3 are not active during Hardware Power Down.

P1 is activated only for two oscillator periods if a 0-to-1 transition is programmed to the port pin (not possible during HWPD).

P3 is turned off during reset state (also HWPD).

For detailed description of the port structure please refer to the SAB 80C515/80C535 User's Manual.

5.1 10-Bit A/D-Converter

In the SAB 80C515A a new high performance/high speed 8-channel 10-bit A/D-Converter is implemented. Its successive approximation technique provides 7 µs conversion time (f_{OSC} = 16 MHz). The conversion principle is upward compatible to the one used in the SAB 80C515. The major components are shown in **figure 5-1**.

The comparator is a fully differential comparator for a high power supply rejection ratio and very low offset voltages. The capacitor network is binary weighted providing 10-bit resolution.

The table below shows the sample time T_S and the conversion time T_C (including T_S), which depend on f_{OSC} and the selected prescaler (see also Bit ADCL in SFR ADCON 1).

f_{osc} [MHz]	Prescaler	f_{ADC} [MHz]	T_S [µs]	T_C [µs] (incl. T_S)
12	÷ 8	1.5	2.67	9.33
	÷ 16	0.75	5.33	18.66
16	÷ 8	2.0	2.0	7.0
	÷ 16	1.0	4.0	14.0
18	÷ 8	–	–	–
	÷ 16	1.125	3.555	12.4

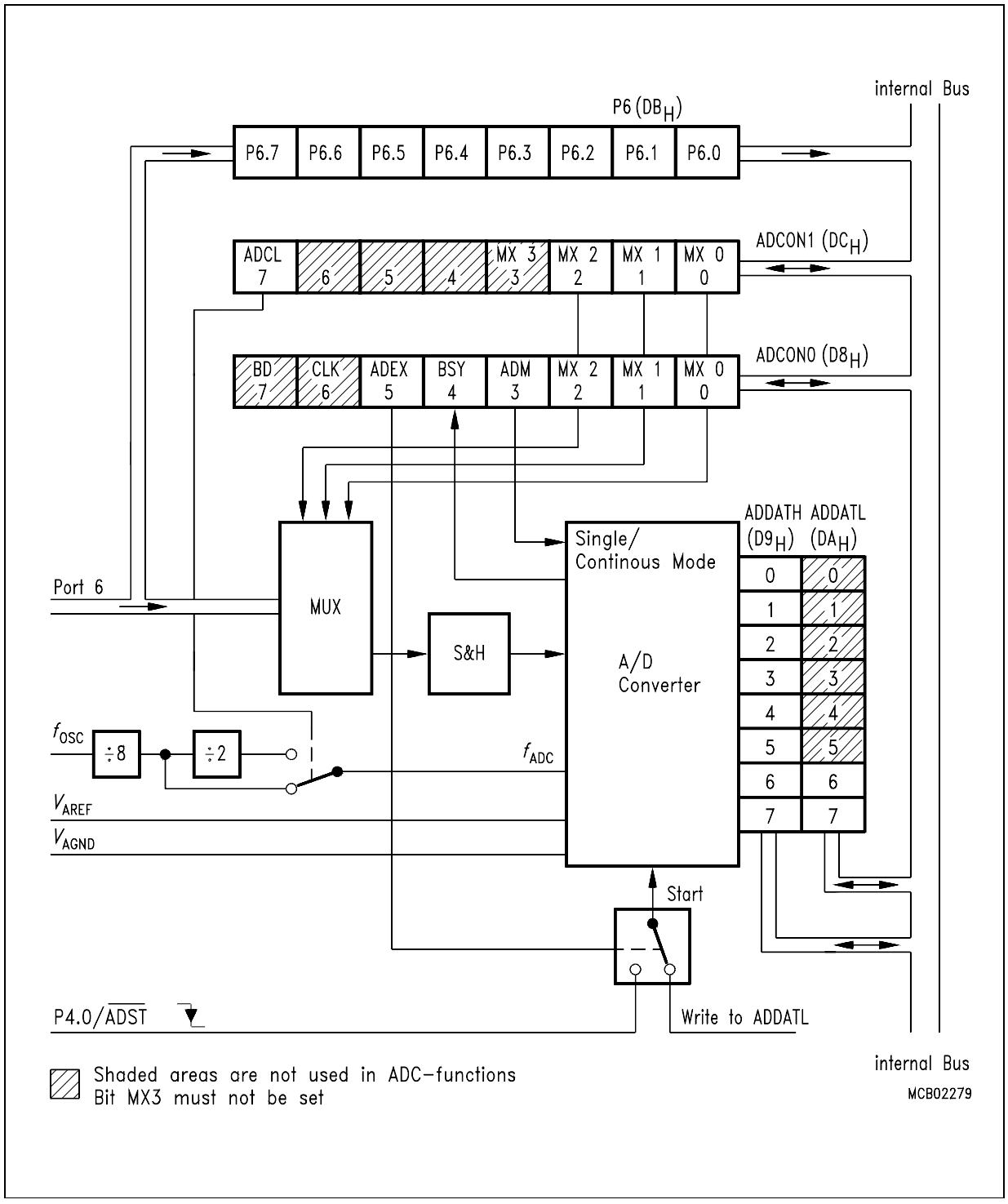
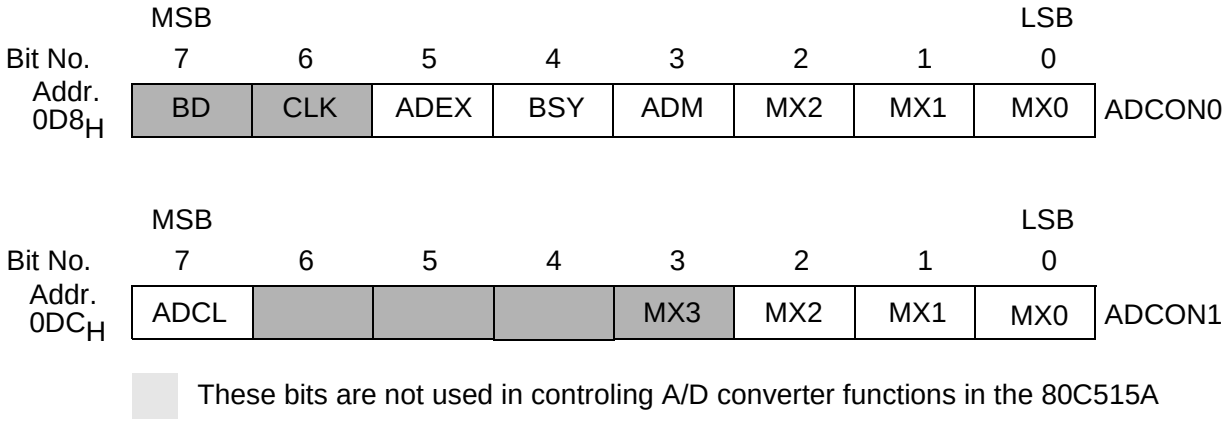


Figure 5-2
10-Bit A/D-Converter

Special Function Registers ADCON0, ADCON1

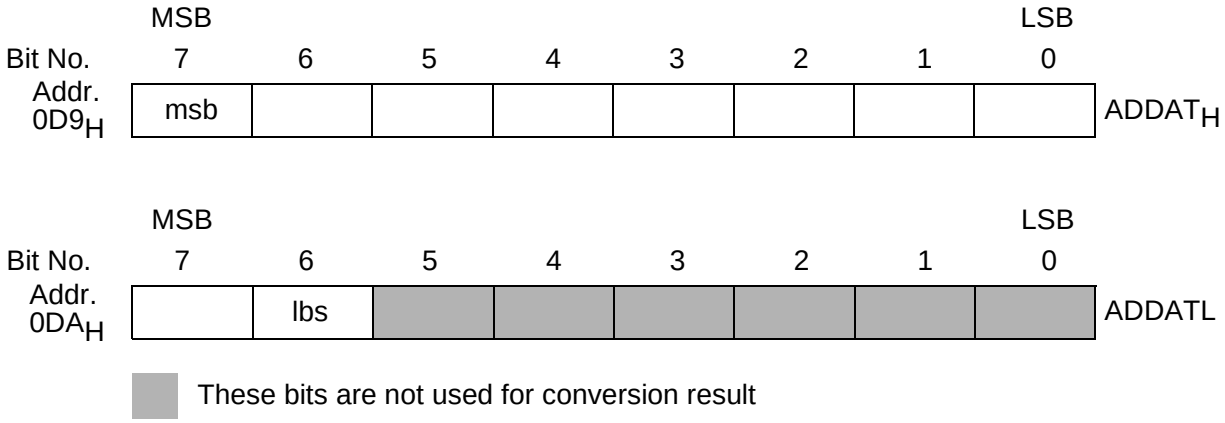


These bits are not used in controling A/D converter functions in the 80C515A

Bit	Function
ADEX	Internal/external start of conversion. When set, the external start of conversion by P4.0 / $\overline{\text{ADST}}$ is enabled
BSY	Busy flag. This flag indicates whether a conversion is in progress (BSY = 1). The flag is cleared by hardware when the conversion is finished.
ADM	A/D Conversion mode. When set, a continuous conversion is selected. If cleared, the converter stops after one conversion.
MX2 - MX0	Select 8 input channels of the ADC. Bits MX0 to MX2 can be written or read either in ADCON0 or in ADCON1
ADCL	ADC Clock. When set $f_{ADC} = f_{OSC} / 16$. Has to be set when $f_{OSC} > 16$ MHz

The reset value of ADCON0 and ADCON1 is 00_H

Special Function Register ADDATH, ADDATL



The reset value of $ADDAT_H$ and ADDATL is 00_H.

The registers **$ADDAT_H$** ($0D9_H$) and **ADDATL** ($0DA_H$) contain the 10-bit conversion result. The data is read as two 8-bit bytes. Data is presented in left justified format (i.e. the msb is the most left-hand bit in a 16-bit word). To get a 10-bit conversion result two READ operations are required. Otherwise $ADDAT_H$ contains the 8-bit conversion result.

A/D Converter Timing

After a conversion has been started (by a write to ADDATL, external start by P4.0/$\overline{\text{ADST}}$ or in continuous mode) the analog input voltage is sampled for 4 clock cycles. The analog source must be capable of charging the capacitor network of appr. 50 pF to full accuracy in this time. During this period the converter is susceptable to spikes and noise at the analog input, which may cause wrong codes at the digital outputs. Therefore RC-filtering at the analog inputs is recommended (see figure below).

Conversion of the sampled analog voltage takes place between the 4th an 14th clock cycle.

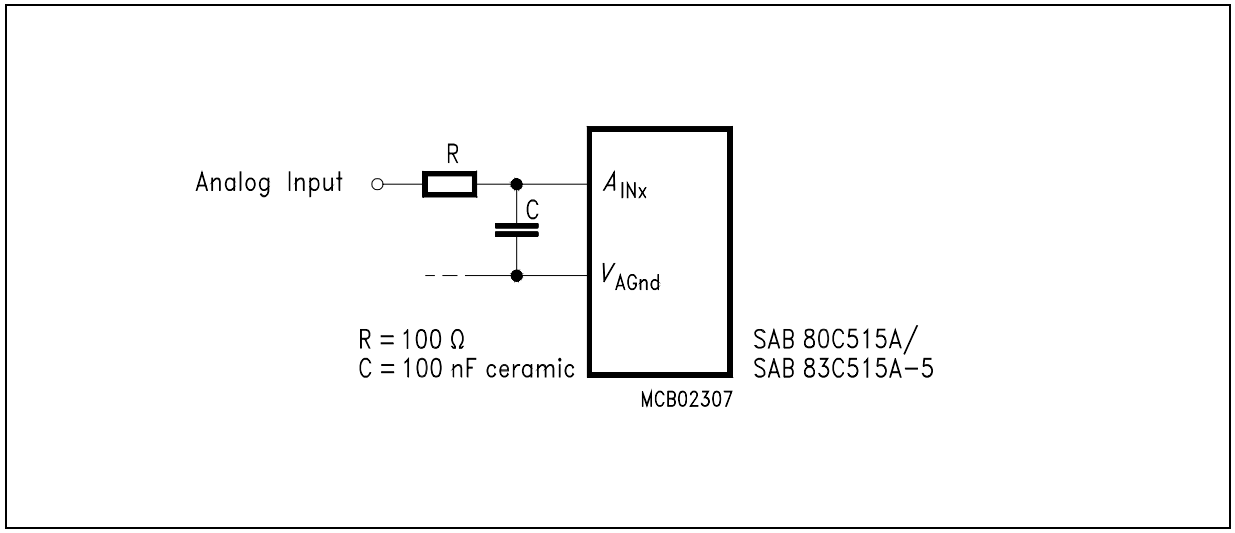


Figure 5-3
Recommended RC-Filtering at the Analog Inputs

5.2 New Baud Rate Generator for Serial Channel

The Serial Channel has a new baud rate generator which provides greater flexibility and better resolution. It substitutes the 80C515's baud rate generator at the Serial Channel which provides only 4.8 kBaud or 9.6 kBaud at 12 MHz crystal frequency. Since the new generator offers greater flexibility it is often possible to use it instead of Timer1 which is then free for other tasks.

Figure 5-3 shows a block diagram of the new baud rate generator for the Serial Channel. It consists of a free running 10-bit timer with f_{OSC} / 2 input frequency. On overflow of this timer there is an automatic reload from the registers SRELL (address AA_H) and SRELH (address BA_H). The lower 8 bits of the timer are reloaded from SRELL, while the upper two bits are reloaded from bit 0 and 1 of register SRELH. The baud rate timer is reloaded by writing to SRELL.

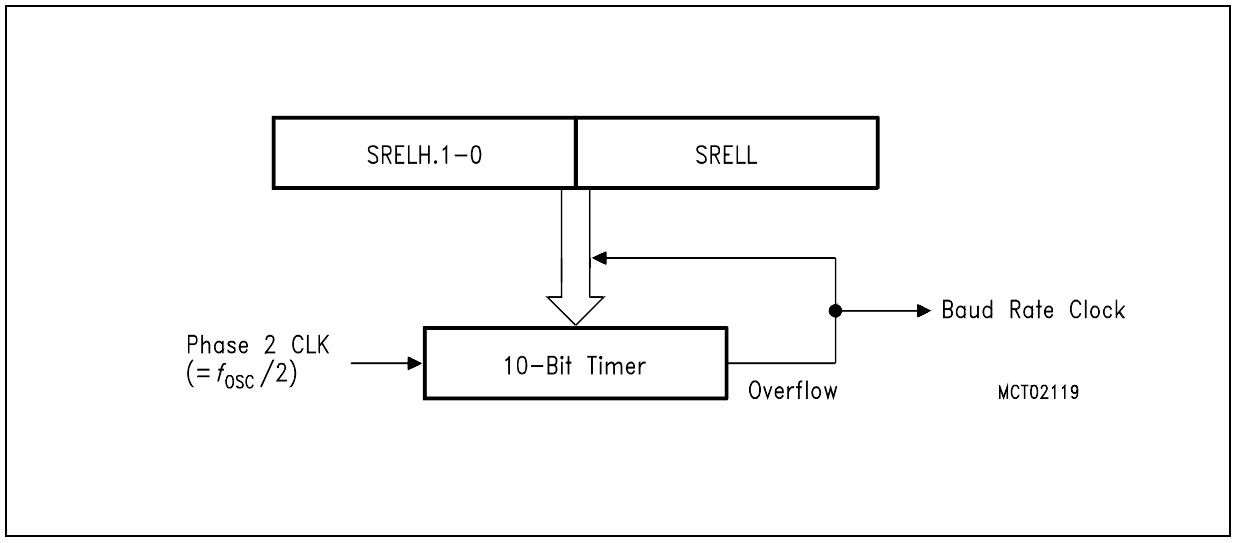
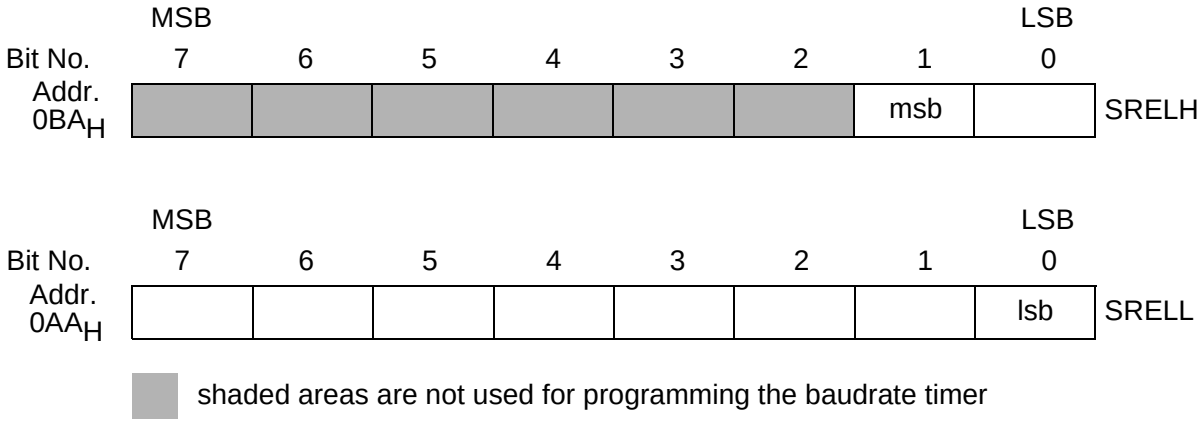


Figure 5-4
Baud Rate Generator for the Serial Interface

Special Function Register S0RELH, S0RELL



Bit	Function
SRELH.0-1	Reload value. Upper two bits of the timer reload value.
SRELL.0-7	Reload value. Lower 8 bit of timer reload value.

Reset value of SRELL is $0D9_H$, SRELH contains XXXX $XX11_B$.

Figure 5-5 shows a block diagram of the options available for baud rate generation of Serial Channel. It is a fully compatible superset of the functionality of the SAB 80C515. The new baud rate generator can be used in modes 1 and 3 of the Serial Channel. It is activated by setting bit BD (ADCON.7). This also starts the baud rate timer. When Timer1 shall be used for baud rate generation, bit BD must be cleared. In any case, bit SMOD (PCON.7) selects an additional divider by two.

The default values after reset in registers SRELL and SRELH provide a baud rate of 4.8 kBaud (with SMOD = 0) or 9.6 kBaud (with SMOD = 1) at 12 MHz oscillator frequency. This guarantees full compatibility to the SAB 80C515.

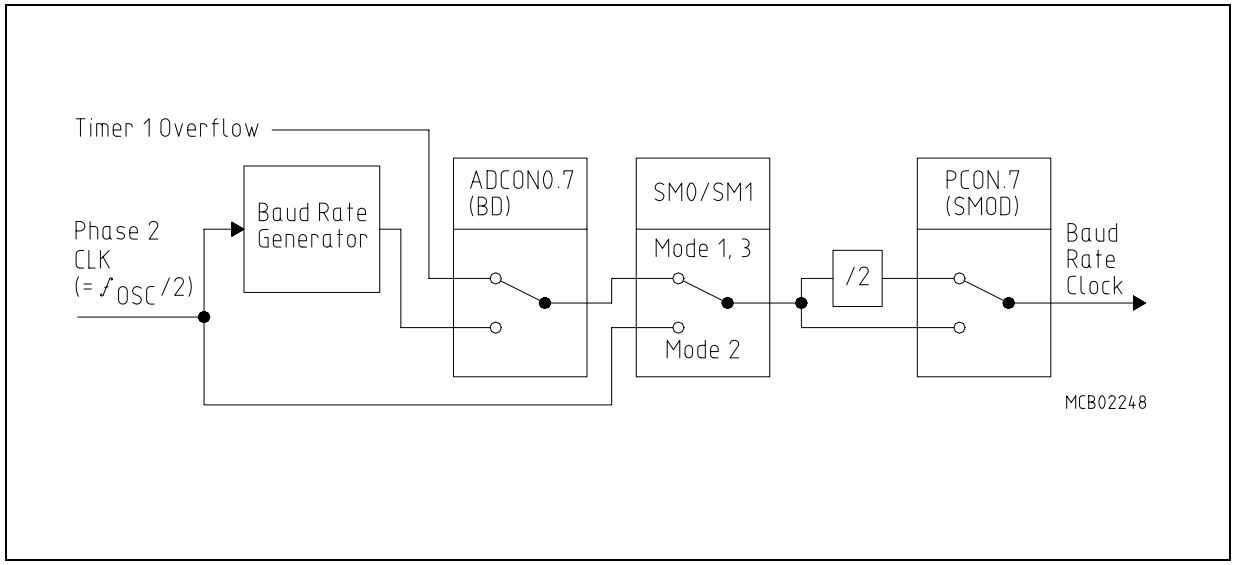


Figure 5-5
Block Diagram of Baud Rate Generation for Serial Interface

If the new baud rate generator is used the baud rate of the Serial Channel in Mode 1 and 3 can be determined as follows:

$$\text{Mode 1, 3 baud rate} = \frac{2^{SMOD} \times \text{oscillator frequency}}{64 \times (2^{10} - \text{SREL})}\ ;\ \text{with SREL = SRELH.1 – 0, SRELL.7 – 0}$$

$$\text{SREL} = 2^{10} - \frac{2^{SMOD} \times f_{OSC}}{64 \times \text{baud rate}}$$

5.3 Fail Save Mechanisms

The SAB 80C515A offers two on-chip peripherals which ensure an automatic ’fail-save’ reaction in cases where the controller’s hardware fails or the software hangs up:

- Programmable Watchdog Timer (WDT) with variable time-out period from 512 µs to approx. 1.1 seconds at 12 MHz. The SAB 80C515A's WDT is compatible to the SAB 80C515's WDT, which is not programmable.
- An Oscillator Watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into the reset state if the on-chip oscillator fails. This unit is new in with respect to the SAB 80C515.

5.3.1 Programmable Watchdog Timer

To protect the system against software upset, the user's program has to clear the watchdog within a previously programmed time period. If the software fails to do this periodical refresh of the Watchdog Timer, an internal hardware reset will be initiated. The software can be designed such that the watchdog times the if the program does not work properly. It also times out if a software error is based on hardware-related problems.

The Watchdog Timer in the SAB 80C515A is a 15-bit timer, which is incremented by a count rate of either $f_{CYCLE}/2$ or $f_{CYCLE}/32$ ($f_{CYCLE} = f_{OSC}/12$). That is, the machine clock is divided by a series of arrangement of two prescalers, a divide-by-two and a divide-by-16 prescaler (**see figure 5-6**). The latter is enabled by setting bit WDTREL.7.

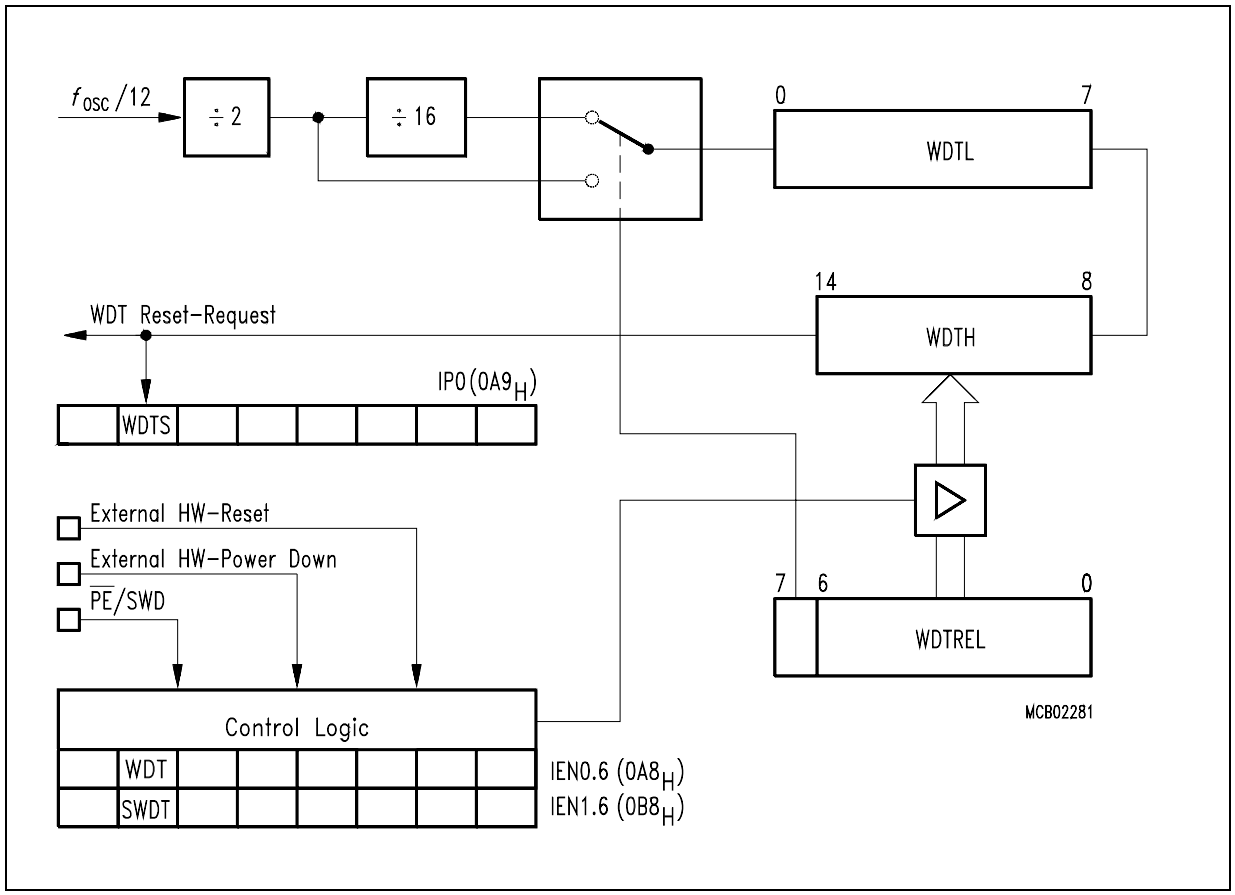
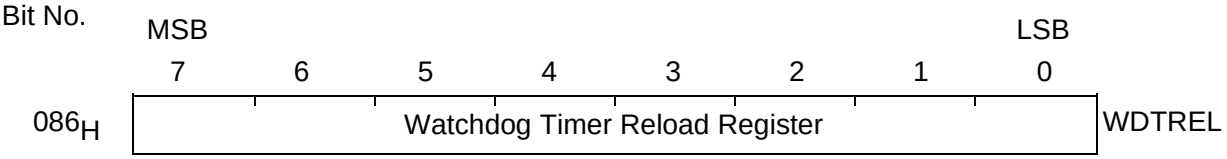


Figure 5-6
Block Diagram of the Programmable Watchdog Timer

Special Function Register WDTREL (Address 086_H)



Bit	Function
WDTREL.7	Prescaler select bit. When set, the watchdog timer is clocked through an additional divide-by-16 prescaler (see figure 12).
WDTREL.6 to WDTREL.0	Seven bit reload value for the high-byte of the watchdog timer. This value is loaded to the WDT when a refresh is triggered by a consecutive setting of bits WDT and SWDT.

Reset value of WDTREL is 00_H.

Immediately after start (see next section for start procedure), the Watchdog Timer is initialized to the reload value programmed to WDTREL.0-WDTREL.6. After an external HW reset (or power-on reset, or HW Power Down) register WDTREL is cleared to 00_H. The lower seven bits of WDTREL can be loaded by software at any time.

Examples (given for 12 and 18 MHz oscillator frequency):

WDTREL	Time-out Period		Comments
	f_{osc} = 12 MHz	f_{osc} = 18 MHz	
00_H	65.535 ms	43.690 ms	This is the default value and coincides with the watchdog period of the SAB 80C515
80_H	1.1 s	0.73 s	maximum time period
$7F_H$	512 µs	341 µs	minimum time period

Starting the Watchdog Timer

There are two ways to start the Watchdog Timer depending on the level applied to the pin $\overline{PE}$/SWD (Power Down Modes enable # / Start Watchdog Timer; pin 4). This pin serves two functions (new for the SAB 80C515A), because it is also used for disabling the software initiated power saving modes. For details concerning software initiated power saving modes see User's Manual SAB 80C515.

Automatic Start of the Watchdog Timer

The automatic start of the Watchdog Timer directly after an external reset or a Hardware Power Down ($\overline{HWPD}$; PLCC68 pin 60, new for SAB 80C515A) is a hardware start initialized by strapping pin 4 ($\overline{PE}$/SWD) to V_{CC}. In this case the power saving modes (Software power-down mode and idle mode) are disabled and cannot be started by software. If pin $\overline{PE}$/SWD is left unconnected, a weak pull-up transistor ensures the automatic start of the Watchdog Timer.

The self-start of the Watchdog Timer by a pin option has been implemented to provide high system security in electrically noisy environments.

Note:

The automatic start of the Watchdog Timer is only performed if $\overline{PE}$/SWD is held at high level while $\overline{RESET}$ or $\overline{HWPD}$ is active. A positive transition at these pins during normal program execution will not start the Watchdog Timer.

Furthermore, when using the hardware start, the Watchdog Timer starts running with its default time-out period. The value in the reload register WDTREL, however can be overwritten at any time to set any time-out period desired.

Software Start of the Watchdog Timer

The Watchdog Timer can also be started by software. This method is compatible to the start procedure in the SAB 80C515. Setting of bit SWDT in SFR IEN1 starts the Watchdog Timer. Using the software start, the time-out period can be programmed before Watchdog Timer starts running.

Note that once started the Watchdog Timer cannot be stopped by anything but an external hardware reset at pin 10 ($\overline{RESET}$) with a low level on pin 4 ($\overline{PE}$/SWD) or a hardware power down at pin 60 ($\overline{HWPD}$, independently of level at $\overline{PE}$/SWD).

Refreshing the Watchdog Timer

At the same time the Watchdog Timer is started, the 7-bit register WDTH is preset by the contents of WDTREL.0 to WDTREL.6. Once started the Watchdog Timer cannot be stopped by software but can be refreshed to the reload value only by first setting bit WDT (IEN0.6) and by the next instruction setting SWDT (IEN1.6). Bit WDT will automatically be cleared during the second machine cycle after having been set [1]. This double-instruction refresh of the Watchdog Timer is implemented to minimize the chance of an unintentional reset of the watchdog unit.

The reload register WDTREL can be written at any time, as already mentioned. Therefore, a periodical refresh of WDTREL can be added to the above mentioned starting procedure of the Watchdog Timer. Thus a wrong reload value caused by a possible distortion during the write operation to WDTREL can be corrected by software.

Watchdog Reset and Watchdog Status Flag (WDTS)

If the software fails to clear the watchdog in time, an internally generated watchdog reset is entered at the counter state 7FFCH. The duration of the reset signal then depends on the prescaler selection (either 8 or 128 cycles). This internal reset differs from an external one in so far as the Watchdog Timer is not disabled and bit WDTS is set. Figure 5-6 shows a block diagram of all reset requests in the SAB 80C515A and the function of the watchdog status flag. The WDTS is a flip-flop, which is set by a Watchdog Timer reset and can be cleared by an external hardware reset. Bit WDTS allows the software to examine from which source the reset was activated. The bit WDTS can also be cleared by software.

[1] (SETB - Instructions have to be used)

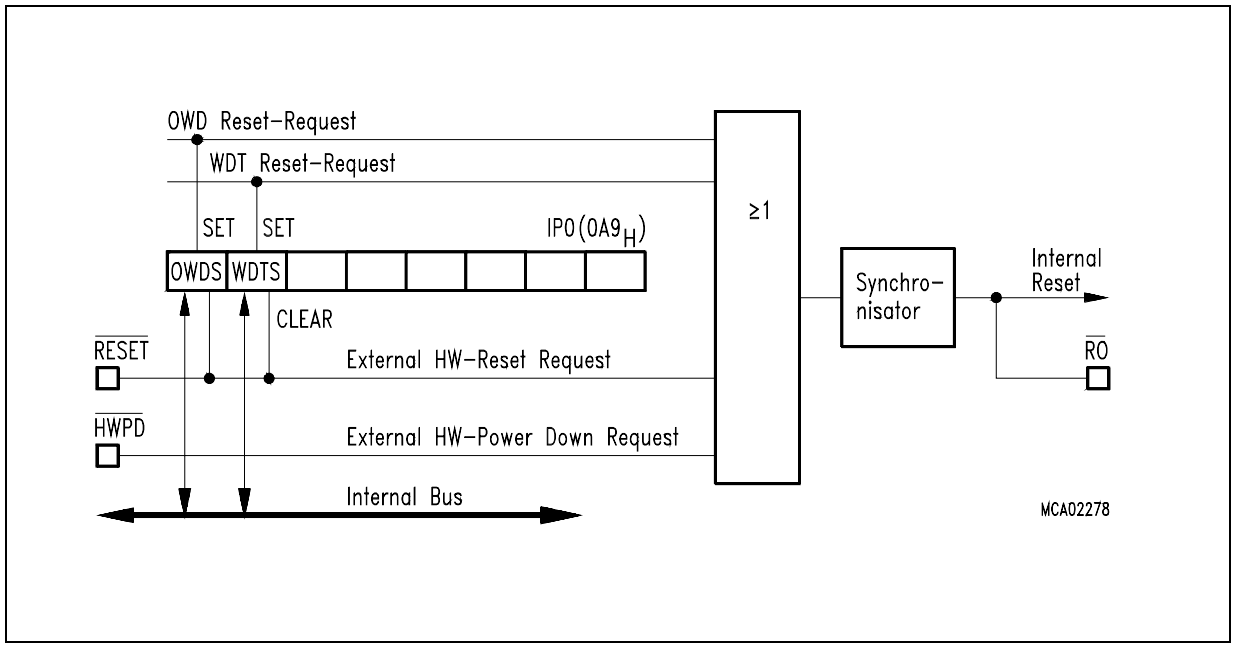


Figure 5-7
Watchdog Status Flags and Reset Requests

Special Function Register IP0 (Address $0A9_H$)

Bit No.

	MSB 7	6	5	4	3	2	1	LSB 0	
086_H	OWDS	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	IPO

These bits are not used for Watchdog Timer

Bit	Function
WDTS	Watchdog timer status flag. Set by hardware e when a Watchdog Timer reset occurred. Can be cleared and set by software.

Reset value of IP0 is 00_H.

5.3.2 Oscillator Watchdog Unit

The unit serves three functions:

- **Monitoring of the on-chip oscillator's function.**
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part executes a final reset phase of appr. 0.5 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.
- **Restart from the Hardware Power Down Mode.**
  If the Hardware Power Down Mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete Hardware Power Down sequence; however, the watchdog works identically to the monitoring function. The Hardware Power Down Mode is discussed in detail in section 4.1, 4.2
- **Fast internal reset after power-on.**
  In this function the oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. In this case the oscillator watchdog unit also works identically to the monitoring function. The power-on is described in section 4.3.

Note:

The oscillator watchdog unit is always enabled.

Detailed Description of the Oscillator Watchdog Unit

Figure 5-8 shows the block diagram of the oscillator watchdog unit. It consists of an internal RC oscillator which provides the reference frequency for the comparison with the frequency of the on-chip oscillator.

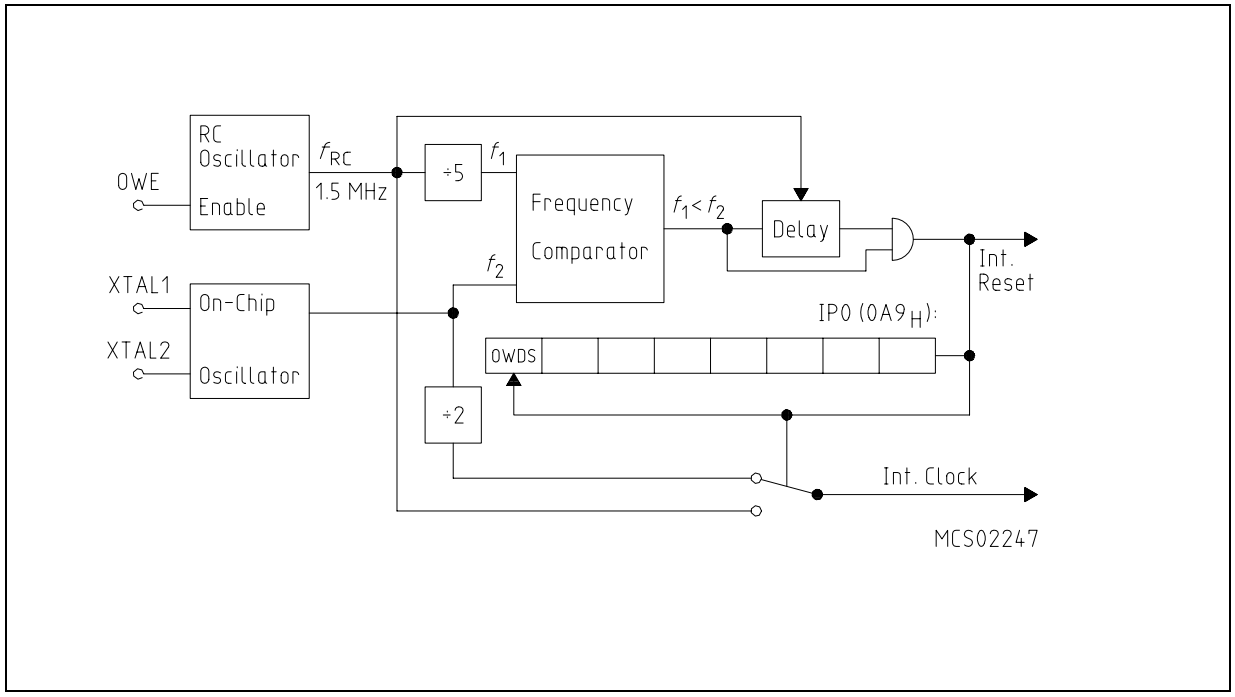


Figure 5-8
Oscillator Watchdog Unit

Special Function Register IP0 (Address $0A9_H$)

Bit No.

	MSB 7	6	5	4	3	2	1	LSB 0	
086_H	OWDS	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	IPO

These bits are not used for Watchdog Timer

Bit	Function
OWDS	Oscillator watchdog timer status flag. Set by hardware when an oscillator watchdog reset occurred. Can be cleared and set by software.

Reset value of IP0 is 00_H.

The frequency coming from the RC oscillator is divided by 5 and compared to the on-chip oscillator's frequency. If the frequency coming from the on-chip oscillator is found lower than the frequency derived from the RC oscillator the watchdog detects a failure condition (the oscillation at the on-chip oscillator could stop because of crystal damage etc.). In this case it switches the input of the internal clock system to the output of the RC oscillator. This means that the part is being clocked even if the on-chip oscillator has stopped or has not yet started. At the same time the watchdog activates the internal reset in order to bring the part in its defined reset state. The reset is performed because clock is available from the RC oscillator. This internal watchdog reset has the same effects as an externally applied reset signal with the following exceptions: The Watchdog Timer Status flag WDTS (IP0.6) is not reset; (the Watchdog Timer however is stopped) and bit OWDS is set. This allows the software to examine error conditions detected by the Watchdog Timer even if meanwhile an oscillator failure occurred.

The oscillator watchdog is able to detect a recovery of the on-chip oscillator after a failure. If the frequency derived from the on-chip oscillator is again higher than the reference the watchdog starts a final reset sequence which takes typ. 1 ms. Within that time the clock is still supplied by the RC oscillator and the part is held in reset. This allows a reliable stabilization of the on chip oscillator. After that, the watchdog toggles the clock supply back to the on-chip oscillator and releases the reset request. If no external reset is applied in this moment the part will start program execution. If an external reset is active, however, the device will keep the reset state until also the external reset request disappears.

Furthermore, the status flag OWDS (IP0.7) is set if the oscillator watchdog was active. The status flag can be evaluated by software to detect that a reset was caused by the oscillator watchdog. The flag OWDS can be set or cleared by software. An external reset request, however, also resets OWDS (and WDTS).

SIEMENS

High-Performance 8-Bit CMOS Single-Chip Microcontroller

SAB 80C515A / 83C515A-5

Preliminary

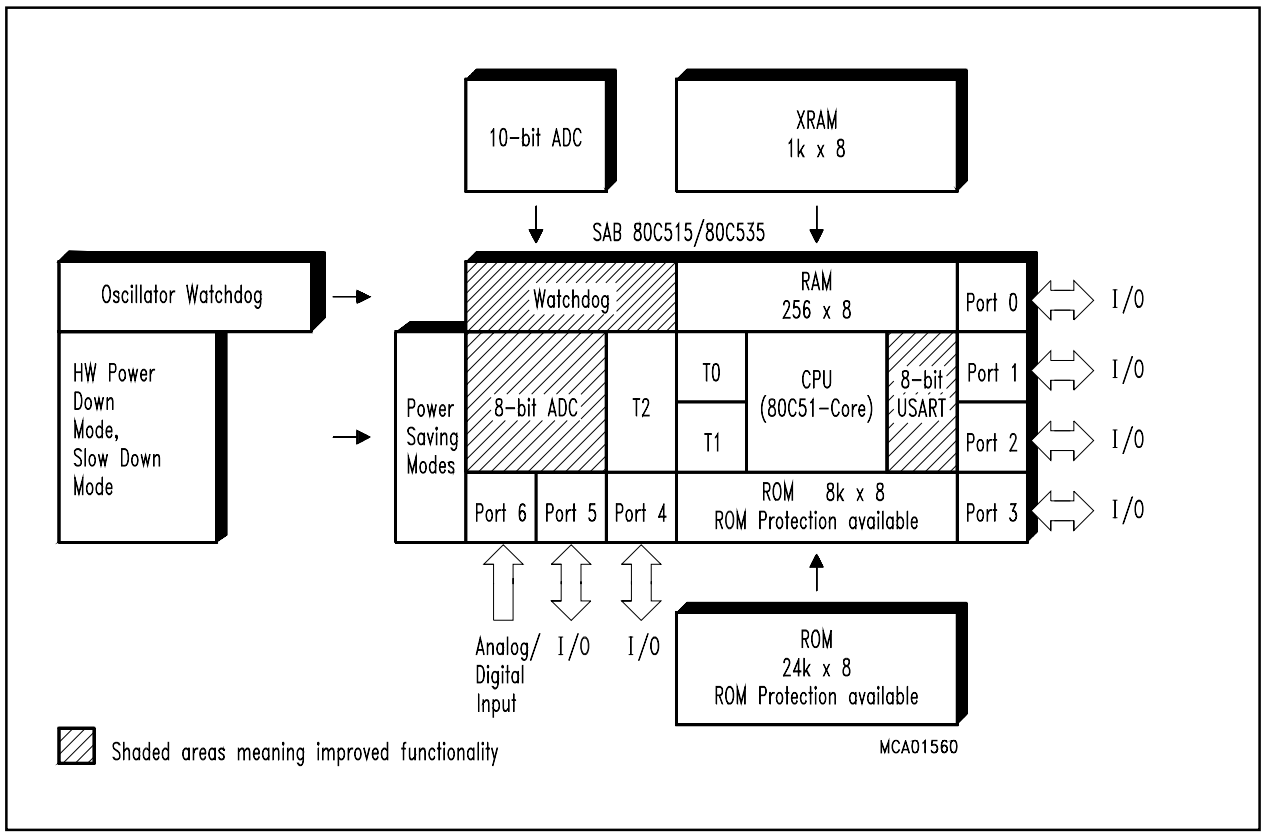
SAB 83C515A-5	Microcontroller with factory mask-programmable ROM
SAB 80C515A	Microcontroller for external ROM

- SAB 80C515A / 83C515A-5, up to 18 MHz operation frequency
- 32 K × 8 ROM (SAB 83C515A-5 only, ROM-Protection available)
- 256 × 8 on-chip RAM
- Additional 1 K × 8 on-chip RAM (XRAM)
- Superset of SAB 80C51 architecture:
  1 µs instruction cycle time at 12 MHz
  666 ns instruction cycle time at 18 MHz
  256 directly addressable bits
  Boolean processor
  64 Kbyte external data and program memory addressing
- Three 16-bit timer/counters
- Versatile "fail-safe" provisions
- Twelve interrupt vectors, four priority levels selectable
- Genuine 10-bit A/D converter with 8 multiplexed inputs
- Full duplex serial interface with programmable Baudrate-Generator
- Functionally compatible with SAB 80C515
- Extended power saving mode
- Fast Power-On Reset
- Seven ports: 48 I/O lines, 8 input lines
- Two temperature ranges available:
  0 to 70 °C (T1)
  – 40 to 85 °C (T3)
- Plastic packages: P-LCC-68 and P-MQFP-80

The SAB 80C515A/83C515A-5 is a high-end member of the Siemens SAB 8051 microcontroller family. It is designed in Siemens ACMOS technology and based on the SAB 8051 architecture. ACMOS is a technology which combines high-speed and density characteristics with low-power consumption or dissipation.

While maintaining all the SAB 80C515 features and operating characteristics the SAB 80C515A/83C515A-5 contains more on-chip RAM/ROM. Furthermore a new 10-bit A/D-Converter is implemented as well as extended security mechanisms. The SAB 80C515A is identical with the SAB 83C515A-5 except that it lacks the on-chip program memory. The SAB 80C515A / 83C515A-5 is supplied in a 68-pin plastic leaded chip carrier package (P-LCC- 68) and in a 80-pin plastic metric quad flat package (P-MQFP-80).

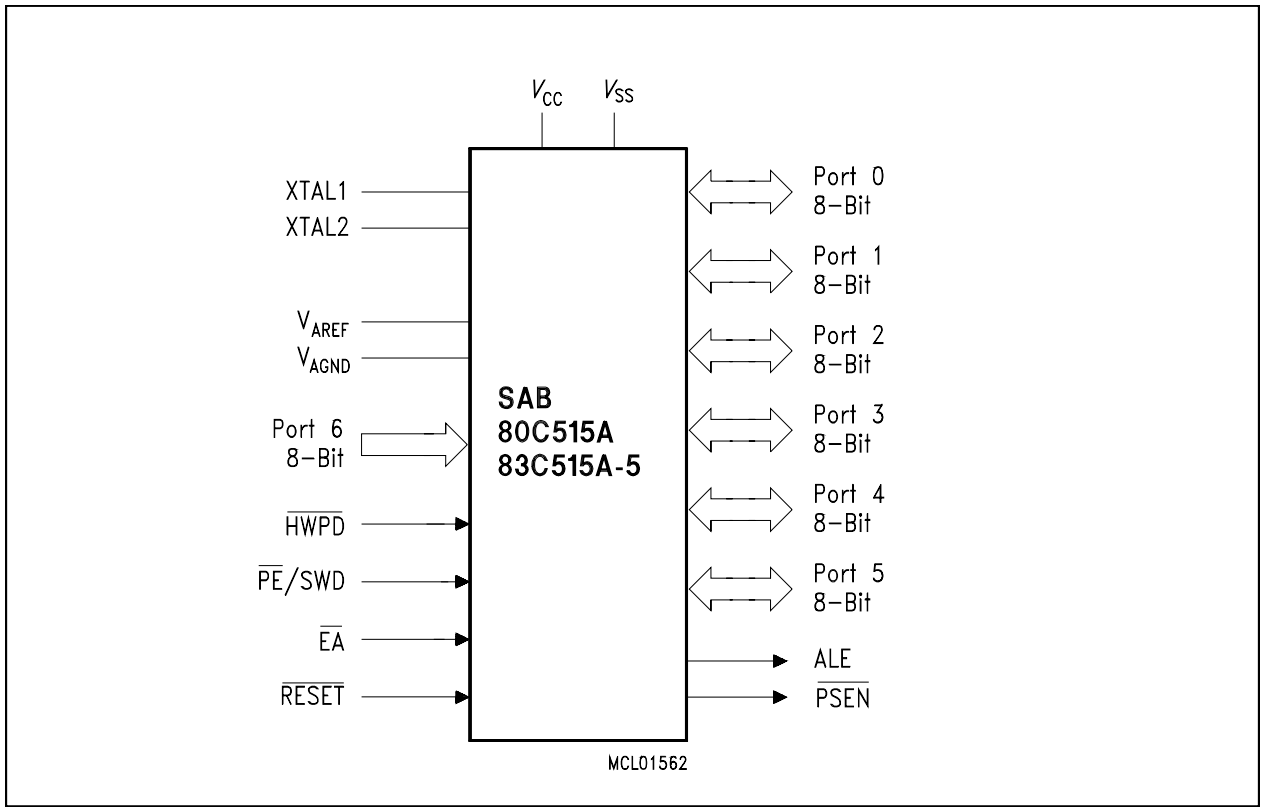
Versions for extended temperature range – 40 to + 110 ∞C are available on request.



Ordering Information

Type	Ordering Code	Package	Description 8-Bit CMOS microcontroller
SAB 80C515A-N18	Q67120-C0581	P-LCC-68	for external memory, 18 MHz
SAB 83C515A-5N18	Q67120-DXXXX	P-LCC-68	with mask-programmable ROM, 18 MHz
SAB 80C515A-N18-T3	Q67120-C0784	P-LCC-68	for external memory, 18 MHz ext. temperature – 40 to + 85 °C
SAB 83C515A-5N18-T3	Q67120-DXXXX	P-LCC-68	with mask-programmable ROM, 18 MHz ext. temperature – 40 to + 85 °C
SAB 80C515A-M18-T3	Q67120-C0851	P-MQFP-80	for external memory, 18 MHz ext. temperature – 40 to + 85 °C
SAB 83C515A-5M18-T3	Q67120-DXXXX	P-MQFP-80	with mask-programmable ROM, 18 MHz ext. temperature – 40 to + 85 °C

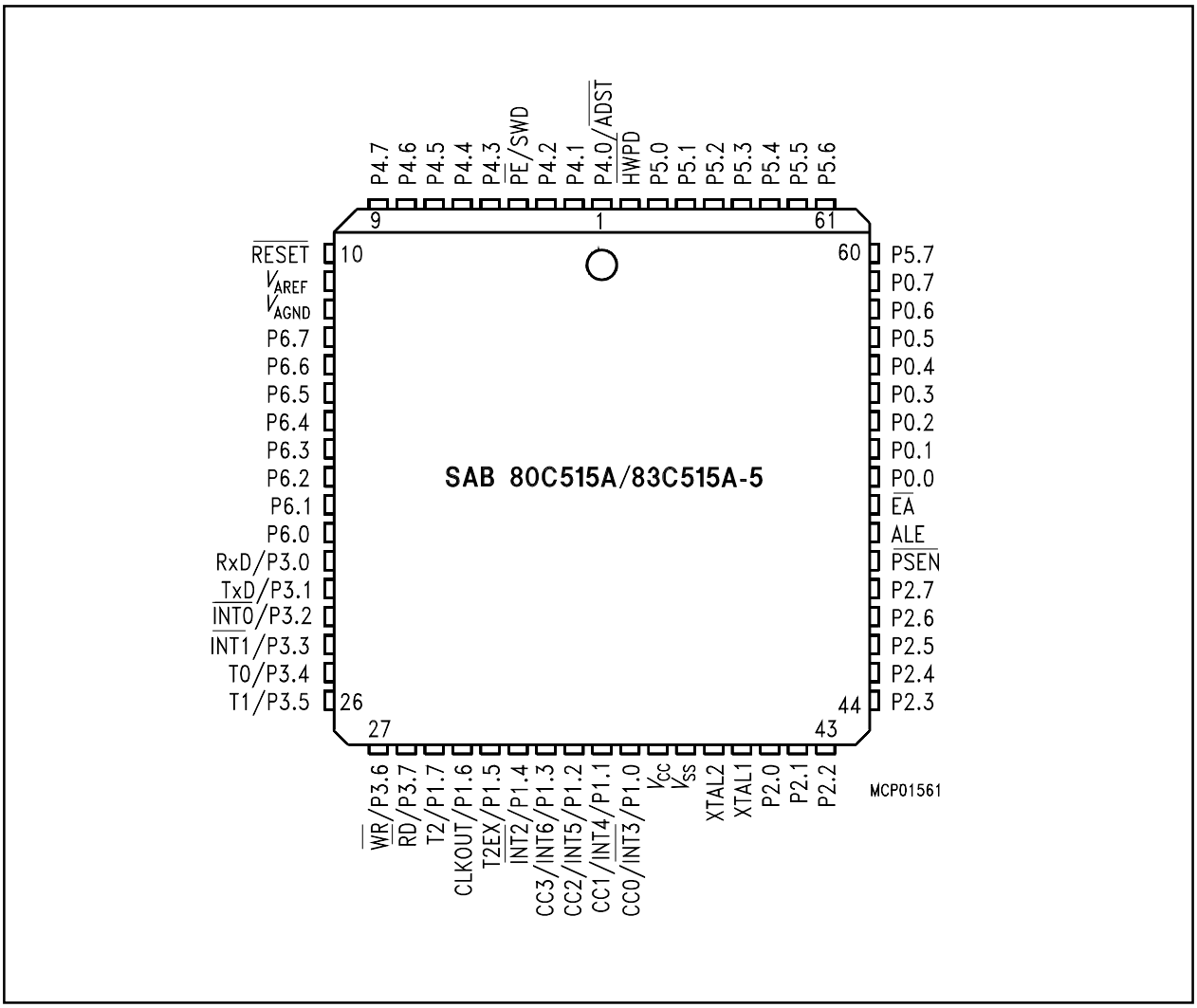
Notes: Versions for extended temperature range – 40 to + 110 °C on request.
The ordering number of ROM types (DXXXX extension) is defined after program release (verification) of the customer.



Logic Symbol

The pin functions of the SAB 80C515A are identical with those of the SAB 80C515 with following exception:

Pin	SAB 80C515A	SAB 80C515
68	$\overline{\text{HWPD}}$	V_{CC}
1	P0.4/$\overline{\text{ADST}}$	P4.0
4	$\overline{\text{PE}}$/SWD	$\overline{\text{PE}}$



Pin Configuration
(P-LCC-68)

N.C. pins must not be connected.

Pin Configuration
(P-MQFP-80)

Pin Definitions and Functions

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	72-74, 76-80	I/O	**Port 4** is an 8-bit bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1's written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. P4 also contains the external A/D converter control pin. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary function assigned to port 6: – $\overline{ADST}$(P4.0): external A/D converter start pin
$\overline{PE}$/SWD	4	75	I	**Power saving mode $\overline{enable}$/Start Watchdog Timer** A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor.
$\overline{RESET}$	10	1	I	**$\overline{Reset}$ pin** A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80C515A. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}
V_{AREF1}	11	3		**Reference voltage** for the A/D converter
V_{AGND}	12	4		**Reference ground** for the A/D converter

Pin Definitions and Functions (cont'd)

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
P6.7-P6.0	13-20	5-12	I	**Port 6** is an 8-bit unidirectional input port to the A/D converter. Port pins can be used for digital input, if voltage levels simultaneously meet the specifications high/low input voltages, and for the eight multiplexed analog inputs.
P3.0-P3.7	21-28	15-22	I/O	**Port 3** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – R × D (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – T × D (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{INT0}$(P3.2): interrupt 0 input/timer 0 gate control input – $\overline{INT1}$(P3.3): interrupt 1 input/timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{WR}$(P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{RD}$(P3.7): the read control signal enables the external data memory to port 0

Pin Definitions and Functions (cont'd)

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
P1.7 - P1.0	29-36	24-31	I/O	**Port 1** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors. The port is used for the low-order address byte during program verification. Port 1 also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{INT3}$/CC0 (P1.0): interrupt 3 input / compare 0 output / capture 0 input – INT4/CC1 (P1.1): interrupt 4 input / compare 1 output / capture 1 input – INT5/CC2 (P1.2): interrupt 5 input / compare 2 output / capture 2 input – INT6/CC3 (P1.3): interrupt 6 input / compare 3 output / capture 3 input – $\overline{INT2}$(P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reloadtrigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
XTAL2	39	36	–	**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.

Pin Definitions and Functions (cont'd)

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
XTAL1	40	37	-	**XTAL1** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clokking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times and rise/fall times specified in the AC characteristics must be taken into account.
P2.0-P2.7	41-48	38-45	I/O	**Port 2** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current ($I_{IL,}$ in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1's. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	49	47	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. The signal remains high during internal program execution.
ALE	50	48	O	The **Address Latch enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods, except during an external data memory access.

Pin Definitions and Functions (cont'd)

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
$\overline{EA}$	51	49	I	**$\overline{External\ Access\ Enable}$** When held high, the SAB 80C515A executes instructions from the internal ROM as long as the PC is less than 32768. When held low, the SAB 80C515A fetches all instructions from external program memory. For the SAB 80C515A this pin must be tied low.
P0.0-P0.7	52-59	52-59	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the SAB 80C515A. External pullup resistors are required during program verification.
P5.7-P5.0	60-67	60-67	I/O	**Port 5** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors.
$\overline{HWPD}$	68	69	I	**$\overline{Hardware\ Power\ Down}$** A low level on this pin for the duration of one machine cycle while the oscillator is running resets the SAB 80C515A. A low level for a longer period will force the part to Power Down Mode with the pins floating. (**see table 5**)
V_{CC}	37	32, 33	–	**Supply voltage** during normal, idle, and power-down operation.
V_{SS}	38	34, 35	–	**Ground** (0 V)
N.C.	–	2, 13, 14, 23, 46, 50, 51, 68, 70, 71	–	Not connected These pins of the P-MQFP-80 package must not be connected.

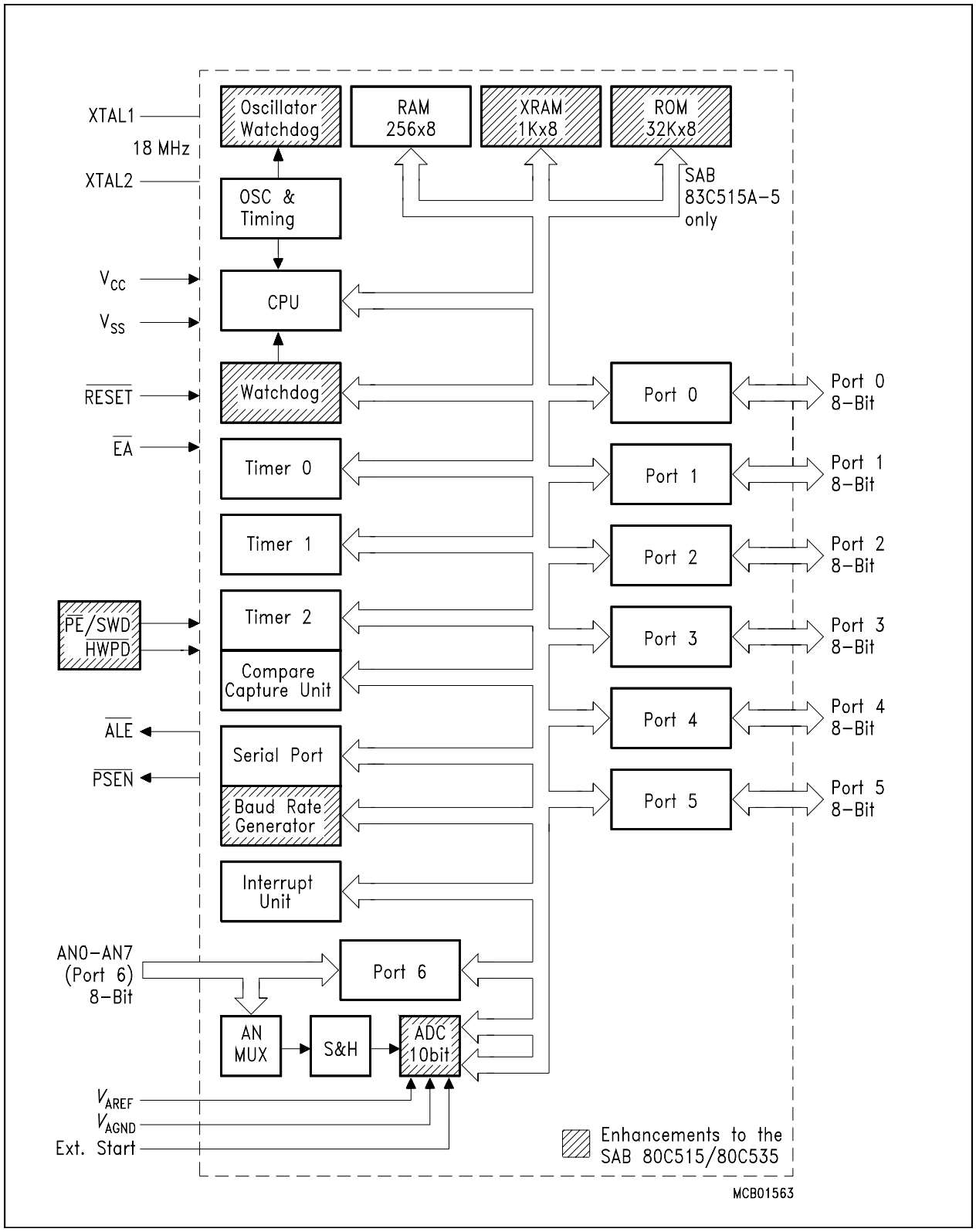


Figure 1
Block Diagram

Functional Description

The SAB 80C515A is based on 8051 architecture. It is a fully compatible member of the Siemens SAB 8051/80C51 microcontroller family being an significantly enhanced SAB 80C515. The SAB 80C515A is therefore code compatible with the SAB 80C515.

Having an 8-bit CPU with extensive facilities for bit-handling and binary BCD arithmetics the SAB 80C515A is optimized for control applications. With a 18 MHz crystal, 58 % of the instructions are executed in 666.67 ns.

While maintaining all architectural and operational characteristics of the SAB 80C515 the SAB 80C515A incorporates more on-chip RAM. A new 10-bit A/D-Converter is implemented as well as an oscillator watchdog unit. Also the maximum operating frequency of 18 MHz is higher than at the SAB 80C515.

With exception of the ROM sizes both parts are identical. Therefore the therm SAB 80C515A refers to both versions within this specification unless otherwise noted.

Memory Organisation

According to the SAB 8051 architecture, the SAB 80C515A has separate address spaces for program and data memory. Figure 2 illustrates the mapping of address spaces.

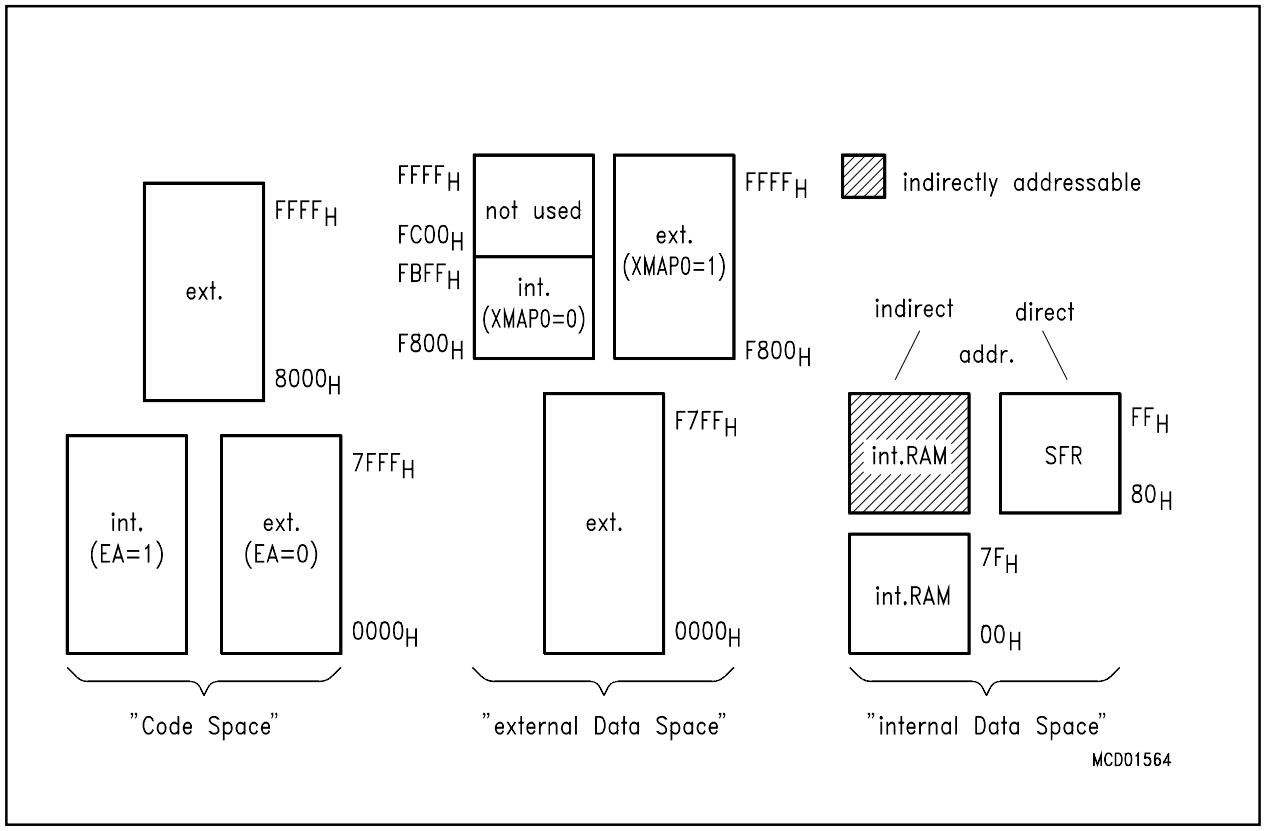


Figure 2
Memory Map

Program Memory ('Code Space')

The SAB 83C515A-5 has 32 Kbyte of on-chip ROM, while the SAB 80C515A has no internal ROM. The program memory can externally be expanded up to 64 Kbyte. Pin $\overline{EA}$ determines whether program fetches below address 8000_H are done from internal or external memory.

As a new feature the SAB 83C515A-5 offers the possibility of protecting the internal ROM against unauthorized access. This protection is implemented in the ROM-Mask. Therefore, the decision ROM-Protection 'yes' or 'no' has to be made when delivering the ROM-Code. Once enabled, there is no way of disabling the ROM-Protection.

Effect: The access to internal ROM done by an externally fetched MOVC instruction is disabled. Nevertheless, an access from internal ROM to external ROM is possible.

To verify the read protected ROM-Code a special ROM-Verify-Mode is implemented. This mode also can be used to verify unprotected internal ROM.

ROM -Protection	ROM-Verification Mode (see 'AC Characteristics')	Restrictions
no	ROM-Verification Mode 1 (standard 8051 Verification Mode) ROM-Verification Mode 2	–
yes	ROM-Verification Mode 2	– standard 8051 Verification Mode is disabled – externally applied MOVC accessing internal ROM is disabled

Data Memory ('Data Space')

The data memory space consists of an internal and an external memory space.The SAB 80C515A contains another 1 Kbyte on On-Chip RAM additional to the 256-bytes internal RAM of the base type SAB 80C515. This RAM is called XRAM ('extended RAM') in this document.

External Data Memory

Up to 64 Kbyte external data memory can be addressed by instructions that use 8-bit or 16-bit indirect addressing. For 8-bit addressing MOVX instructions in combination with registers R0 and R1 can be used. A 16-bit external memory addressing is supported by a 16-bit datapointer. Registers XPAGE and SYSCON are controlling whether data fetches at addresses $F800_H$ to $FBFF_H$ are done from internal XRAM or from external data memory.

Internal Data Memory

The internal data memory is divided into four physically distinct blocks:

– the lower 128 bytes of RAM including four register banks containing eight registers each

– the upper 128 byte of RAM

– the 128 byte special function register area.

– a 1 K $\times$ 8 area which is accessed like external RAM (MOVX-instructions), implemented on chip at the address range from $F800_H$ to $FBFF_H$. Special Function Register SYSCON controls whether data is read from or written to XRAM or external RAM.

A map of the internal data memory is shown in figure 2. The overlapping address spaces of the standard internal data memory (256 byte) are accessed by different addressing modes (see User's Manual SAB 80C515). The stack can be located anywhere in the internal data memory.

Architecture of the XRAM

The contents of the XRAM is not affected by a reset or HW Power Down. After power-up the contents is undefined, while it remains unchanged during and after a reset or HW Power Down if the power supply is not turned off.

The additional On-Chip RAM is logically located in the "external data memory" range at the upper end of the 64 Kbyte address range ($F800_H$-$FBFF_H$). Nevertheless when XRAM is enabled the address range $F800_H$ to $FFFF_H$ is occupied. This is done to assure software compatibility to SAB 80C517A. It is possible to enable and disable (only by reset) the XRAM. If it is disabled the device shows the same behaviour as the parts without XRAM, i.e. all MOVX accesses use the external bus to physically external data memory.

Accesses to XRAM

Because the XRAM is used in the same way as external data memory the same instruction types must be used for accessing the XRAM.

Note: *If a reset occurs during a write operation to XRAM, the effect on XRAM depends on the cycle which the reset is detected at (MOVX is a 2-cycle instruction):*

Reset detection at cycle 1: *The new value will not be written to XRAM. The old value is not affected.*

Reset detection at cycle 2: *The old value in XRAM is overwritten by the new value.*

Accesses to XRAM using the DPTR

There are a Read and a Write instruction from and to XRAM which use one of the 16-bit DPTR for indirect addressing. The instructions are:

MOVX A, @DPTR (Read)

MOVX @DPTR, A (Write)

Normally the use of these instructions would use a physically external memory. However, in the SAB 80C515A the XRAM is accessed if it is enabled and if the DPTR points to the XRAM address space (DPTR $\geq F800_H$).

Accesses to XRAM using the Registers R0/R1

The 8051 architecture provides also instructions for accesses to external data memory range which use only an 8-bit address (indirect addressing with registers R0 or R1). The instructions are:

MOVX A, @Ri (Read)

MOVX @Ri, A (Write)

In application systems, either a real 8-bit bus (with 8-bit address) is used or Port 2 serves as page register which selects pages of 256-byte. However, the distinction, whether Port 2 is used as general purpose I/O or as "page address" is made by the external system design. From the device's point of view it cannot be decided whether the Port 2 data is used externally as address or as I/O data!

Hence, a special page register is implemented into the SAB 80C515A to provide the possibility of accessing the XRAM also with the MOVX @Ri instructions, i.e. XPAGE serves the same function for the XRAM as Port 2 for external data memory.

Special Function Register XPAGE

Addr. 91_H									XPAGE

The reset value of XPAGE is 00_H.
XPAGE can be set and read by software.

The register XPAGE provides the upper address byte for accesses to XRAM with MOVX @Ri instructions. If the address formed from XPAGE and Ri is less than the XRAM address range, then an external access is performed. For the SAB 80C515A the contents of XPAGE must be greater or equal than $F8_H$ in order to use the XRAM. Of course, the XRAM must be enabled if it shall be used with MOVX @Ri instructions.

Thus, the register XPAGE is used for addressing of the XRAM; additionally its contents are used for generating the internal XRAM select. If the contents of XPAGE is less than the XRAM address range then an external bus access is performed where the upper address byte is provided by P2 and not by XPAGE!

Therefore, the software has to distinguish two cases, if the MOVX @Ri instructions with paging shall be used:

a) Access to XRAM:	The upper address byte must be written to XPAGE or P2; both writes selects the XRAM address range.
b) Access to external memory:	The upper address byte must be written to P2; XPAGE will be loaded with the same address in order to deselect the XRAM.

Control of XRAM in the SAB 80C515A

There are two control bits in register SYSCON which control the use and the bus operation during accesses to the additional On-Chip RAM (XRAM).

Special Function Register SYSCON

Addr. $0B1_H$							XMAP1	XMAP0	SYSCON

Bit	Function
XMAP0	Global enable/disable bit for XRAM memory. XMAP0 =0: The access to XRAM (= On-Chip XDATA memory) is enabled. XMAP0 = 1: The access to XRAM is disabled. All MOVX accesses are performed by the external bus (reset state).
XMAP1	Control bit for / $\overline{RD}$/$\overline{WR}$signals during accesses to XRAM; this bit has no effect if XRAM is disabled (XMAP0 = 1) or if addresses exceeding the XRAM address range are used for MOVX accesses. XMAP1 = 0: The signals $\overline{RD}$ and $\overline{WR}$ are not activated during accesses to XRAM. XMAP1 = 1: The signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM.

Reset value of SYSCON is XXXX XX01B.

The control bit XMAP0 is a global enable/disable bit for the additional On-Chip RAM (XRAM). If this bit is set, the XRAM is disabled, all MOVX accesses use external memory via the external bus. In this case the SAB 80C515A does not use the additional On-Chip RAM and is compatible with the types without XRAM.

XMAP0 is hardware protected by an unsymmetric latch. An unintentional disabling of XRAM could be dangerous since indeterminate values would be read from external bus. To avoid this the XMAP-bit is forced to '1' only by reset. Additionally, during reset an internal capacitor is loaded. So after reset state XRAM is disabled. Because of the load time of the capacitor XMAP0-bit once written to '0' (that is, discharging capacitor) cannot be set to '1' again by software. On the other hand any distortion (software hang up, noise, ...) is not able to load this capacitor, too. That is, the stable status is XRAM enabled. The only way to disable XRAM after it was enabled is a reset.

The clear instruction for XMAP0 should be integrated in the program initialization routine before XRAM is used. In extremely noisy systems the user may have redundant clear instructions.

The control bit XMAP1 is relevant only if the XRAM is accessed. In this case the external $\overline{RD}$ and $\overline{WR}$ signals at P3.6 and P3.7 are not activated during the access, if XMAP1 is cleared. For debug purposes it might be useful to have these signals and the addresses at Ports 0.2 available. This is performed if XMAP1 is set.

The behaviour of Port 0 and P2 during a MOVX access depends on the control bits in register SYSCON and on the state of pin $\overline{EA}$. The table 1 lists the various operating conditions. It shows the following characteristics:

a) Use of P0 and P2 pins during the MOVX access.

   Bus: The pins work as external address/data bus. If (internal) XRAM is accessed, the data written to the XRAM can be seen on the bus in debug mode.

   I/0: The pins work as Input/Output lines under control of their latch.

b) Activation of the $\overline{RD}$ and $\overline{WR}$ pin during the access.

c) Use of internal or external XDATA memory.

The shaded areas describe the standard operation as each 80C51 device without on-chip XRAM behaves.

Table 1:
Behaviour of P0/P2 and $\overline{RD}/\overline{WR}$ during MOVX accesses

		$\overline{EA}$ = 0			$\overline{EA}$ = 1		
		XMAP1, XMAP0			XMAP1, XMAP0		
		00	10	X1	00	10	X1
MOVX @DPTR	DPTR < XRAM address range	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
	DPTR ≥ XRAM address range	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
MOVX @Ri	XPAGE < XRAM addr. page range	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
	XPAGE ≥ XRAM addr. page range	a) P0/P2→BUS ($\overline{WR}$ -Data only) P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0→BUS ($\overline{WR}$ -Data only) P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used

(shaded) modes compatible to 8051 - family

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area. All special function registers are listed in table 2 and table 3.

In table 2 they are organized in numeric order of their addresses. In table 3 they are organized in groups which refer to the functional blocks of the SAB 80C515A.

Table 2
Special Function Register

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80_H	**P0** [1]	**$0FF_H$**	**98_H**	**S0CON** [1]	**00_H**
81_H	SP	07_H	99_H	SBUF	XX_H [2]
82_H	DPL	00_H	$9A_H$	reserved	XX_H [2]
83_H	DPH	00_H	$9B_H$	reserved	XX_H [2]
84_H	(WDTL)		$9C_H$	reserved	XX_H [2]
85_H	(WDTH)		$9D_H$	reserved	XX_H [2]
86_H	WDTREL	00_H	$9E_H$	reserved	XX_H [2]
87_H	PCON	00_H	$9F_H$	reserved	XX_H [2]
88_H	**TCON** [1]	**00_H**	**$A0_H$**	**P2** [1]	**$0FF_H$**
89_H	TMOD	00_H	$A1_H$	reserved	XX_H [2]
$8A_H$	TL0	00_H	$A2_H$	reserved	XX_H [2]
$8B_H$	TL1	00_H	$A3_H$	reserved	XX_H [2]
$8C_H$	TH0	00_H	$A4_H$	reserved	XX_H [2]
$8D_H$	TH1	00_H	$A5_H$	reserved	XX_H [2]
$8E_H$	reserved	XX_H [2]	$A6_H$	reserved	XX_H [2]
$8F_H$	reserved	XX_H [2]	$A7_H$	reserved	XX_H [2]
90_H	**P1** [1]	**$0FF_H$**	**$A8_H$**	**IEN0** [1]	**00_H**
91_H	XPAGE	XX_H [2]	$A9_H$	IP0	00_H
92_H	reserved	XX_H [2]	AA_H	SRELL	$0D9_H$
93_H	reserved	XX_H [2]	AB_H	reserved	XX_H [2]
94_H	reserved	XX_H [2]	AC_H	reserved	XX_H [2]
95_H	reserved	XX_H [2]	AD_H	reserved	XX_H [2]
96_H	reserved	XX_H [2]	AE_H	reserved	XX_H [2]
97_H	reserved	XX_H [2]	AF_H	reserved	XX_H [2]

[1] Bit-addressable special function registers

[2] X means that the value is indeterminate and the location is reserved

Table 2: Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$B0_H$	**P3** [1]	**$0FF_H$**	**$D0_H$**	**PSW** [1]	**00_H**
$B1_H$	SYSCON	$XXXX\ XX01_B$ [2]	$D1_H$	reserved	XX_H [2]
$B2_H$	reserved	XX_H [2]	$D2_H$	reserved	XX_H [2]
$B3_H$	reserved	XX_H [2]	$D3_H$	reserved	XX_H [2]
$B4_H$	reserved	XX_H [2]	$D4_H$	reserved	XX_H [2]
$B5_H$	reserved	XX_H [2]	$D5_H$	reserved	XX_H [2]
$B6_H$	reserved	XX_H [2]	$D6_H$	reserved	XX_H [2]
$B7_H$	reserved	XX_H [2]	$D7_H$	reserved	XX_H [2]
$B8_H$	**EN1** [1]	**00_H**	**$D8_H$**	**ADCON0**[1]	**00_H**
$B9_H$	IP1	$XX00\ 0000_B$ [2]	$D9_H$	ADDATH	00_H
BA_H	SRELH	$XXXX\ XX11_B$ [2]	DA_H	ADDATL	00_H
BB_H	reserved	XX_H [2]	DB_H	P6	XX_H[2]
BC_H	reserved	XX_H [2]	DV_H	ADCVON1	$XXXX\ 0000_B$ [2]
BD_H	reserved	XX_H [2]	DD_H	reserved	XX_H[2]
BE_H	reserved	XX_H [2]	DE_H	reserved	XX_H[2]
BF_H	reserved	XX_H [2]	DF_H	reserved	XX_H[2]
$C0_H$	**IRCON** [1]	**00_H**	**$E0_H$**	**ACC** [1]	**00_H**
$C1_H$	CCEN	00_H	$E1_H$	reserved	XX_H [2]
$C2_H$	CCL1	00_H	$E2_H$	reserved	XX_H [2]
$C3_H$	CCH1	00_H	$E3_H$	reserved	XX_H [2]
$C4_H$	CCL2	00_H	$E4_H$	reserved	XX_H [2]
$C5_H$	CCH2	00_H	$E5_H$	reserved	XX_H [2]
$C6_H$	CCL3	00_H	$E6_H$	reserved	XX_H [2]
$C7_H$	CCH3	00_H	$E7_H$	reserved	XX_H [2]
$C8_H$	**T2CON** [1]	**00_H**	**$E8_H$**	**P4** [1]	**$0FF_H$**
$C9_H$	reserved	XX_H [2]	$E9_H$	reserved	XX_H [2]
CA_H	CRCL	00_H	EA_H	reserved	XX_H [2]
CB_H	CRCH	00_H	EB_H	reserved	XX_H [2]
CC_H	TL2	00_H	EC_H	reserved	XX_H [2]
CD_H	TH2	00_H	ED_H	reserved	XX_H [2]
CE_H	reserved	XX_H [2]	EE_H	reserved	XX_H [2]
CF_H	reserved	XX_H [2]	EF_H	reserved	XX_H [2]

[1] Bit-addressable special function registers

[2] X means that the value is indeterminate and the location is reserved

Table 2: Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$F0_H$	**B** [1]	**00_H**	**$F8_H$**	P5 [1]	**$00F_H$**
$F1_H$	reserved	XX_H [2]	$F9_H$	reserved	XX_H [2]
$F2_H$	reserved	XX_H [2]	FA_H	reserved	XX_H [2]
$F3_H$	reserved	XX_H [2]	FB_H		
$F4_H$	reserved	XX_H [2]	FC_H		
$F5_H$	reserved	XX_H [2]	FD_H		
$F6_H$	reserved	XX_H [2]	FE_H		
$F7_H$	reserved	XX_H [2]	FF_H		

[1] Bit-addressable special function registers

[2] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$0E0_H$** [1]	00_H
	B	B-Register	**$0F0_H$** [1]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	PSW	Program Status Word Register	**$0D0_H$** [1]	00_H
	SP	Stack Pointer	81_H	07_H
A/D-Converter	ADCON0	A/D Converter Control Register 0	**$0D8_H$** [1]	00_H
	ADCON1	A/D Converter Control Register 1	$0DC_H$	$0XXX\ 0000_B$ [3]
	ADDATH	A/D Converter Data Reg. High Byte	$0D9_H$	00_H
	ADDATL	A/D Converter Data Reg. Low Byte	$0DA_H$	00_H
Interrupt System	EN0	Interrupt Enable Register 0	**$0A8_H$** [1]	00_H
	IEN1	Interrupt Enable Register 1	**$0B8_H$** [1]	00_H
	IP0	Interrupt Priority Register 0	$0A9_H$	00_H
	IP1	Interrupt Priority Register 1	$0B9_H$	$XX00\ 0000_B$
	IRCON0	Interrupt Request Control Register	**$0C0_H$** [1]	00_H
	TCON [2]	Timer Control Register	**88_H** [1]	00_H
	T2CON [2]	Timer 2 Control Register	**$0C8_H$**	00_H
Compare/ Capture-Unit (CCU)	CCEN	Comp./Capture Enable Reg.	$0C1_H$	00_H
	CCH1	Comp./Capture Reg. 1, High Byte	$0C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$0C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$0C7_H$	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$0C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$0C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$0C6_H$	00_H
	CRCH	Com./Rel./Capt. Reg. High Byte	$0CB_H$	00_H
	CRCL	Com./Rel./Capt. Reg. Low Byte	$0CA_H$	00_H
	TH2	Timer 2, High Byte	$0CD_H$	00_H
	TL2	Timer 2, Low Byte	$0CC_H$	00_H
	T2CON	Timer 2 Control Register	**$0C8_H$** [1]	00_H
XRAM	XPAGE	Page Address Register for Extended On Chip RAM	91_H	00_H
	SYSCON	XRAM Control Register	$0B1_H$	$XXXX\ XX01_B$ [3]

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80_H** 1)	$0FF_H$
	P1	Port 1	**90_H** 1)	$0FF_H$
	P2	Port 2	**$0A0_H$** 1)	$0FF_H$
	P3	Port 3	**$0B0_H$** 1)	$0FF_H$
	P4	Port 4	**$0E8_H$** 1)	$0FF_H$
	P5	Port 5	**$0F8_H$** 1)	$0FF_H$
	P6	Port 6, Analog/Digital Input	$0DB_H$	
Pow.Sav.Mode	PCON	Power Control Register	87_H	00_H
Serial Channels	ADCON0 2)	A/D Converter Control Reg.	**$0D8_H$** 1)	00_H
	PCON 2)	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Reg.	99_H	$0XX_H$ 3)
	SCON	Serial Channel Control Reg.	**98_H** 1)	00_H
	SRELL	Serial Channel Reload Reg., low byte	AA_H	$D9_H$
	SRELH	Serial Channel Reload Reg., high byte	BA_H	$XXXX\ XX11_B$ 3)
Timer 0/ Timer 1	TCON	Timer Control Register	**88_H** 1)	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Watchdog	IEN0 2)	Interrupt Enable Register 0	**$0A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$0B8_H$** 1)	00_H
	IP0 2)	Interrupt Priority Register 0	$0A9_H$	00_H
	IP1 2)	Interrupt Priority Register 1	$0B9_H$	$XX00\ 0000_B$
	WDTREL	Watchdog Timer Reload Reg.	86_H	00_H

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) X means that the value is indeterminate and the location is reserved

A/D Converter

In the SAB 80C515A a new high performance / high-speed 8-channel 10-bit A/D-Converter (ADC) is implemented. Its successive approximation technique provides 7 µs conversion time (f_{OSC} = 16 MHz). The conversion principle is upward compatible to the one used in the SAB 80C515. The main functional blocks are shown in figure 3.

The comparator is a fully differential comparator for a high power supply rejection ratio and very low offset voltages. The capacitor network is binary weighted providing genuine10-bit resolution.

The table below shows the sample time T_S and the conversion time T_C, which are dependend on f_{OSC} and a new prescaler.

f_{OSC} [MHz]	Prescaler	f_{ADC} [MHz]	Sample Time T_S [µs]	Conversion Time (incl. sample time) T_C [µs]
12	÷ 8	1.5	2.67	9.3
	÷ 16	0.75	5.33	18.66
16	÷ 8	2.0	2.0	7.0
	÷ 16	1.0	1.0	14.0
18	÷ 8	–	–	–
	÷ 16	1.125	3.55	12.4

The ADC is clocked (f_{ADC}) with f_{OSC}/8. Because of the ADC's maximum clock frequency of 2 MHz the prescaler (divide-by-2) has to be enabled (set Bit ADCL in SFR ADCON 1) when the oscillator frequency (f_{OSC}) is higher than 16 MHz.

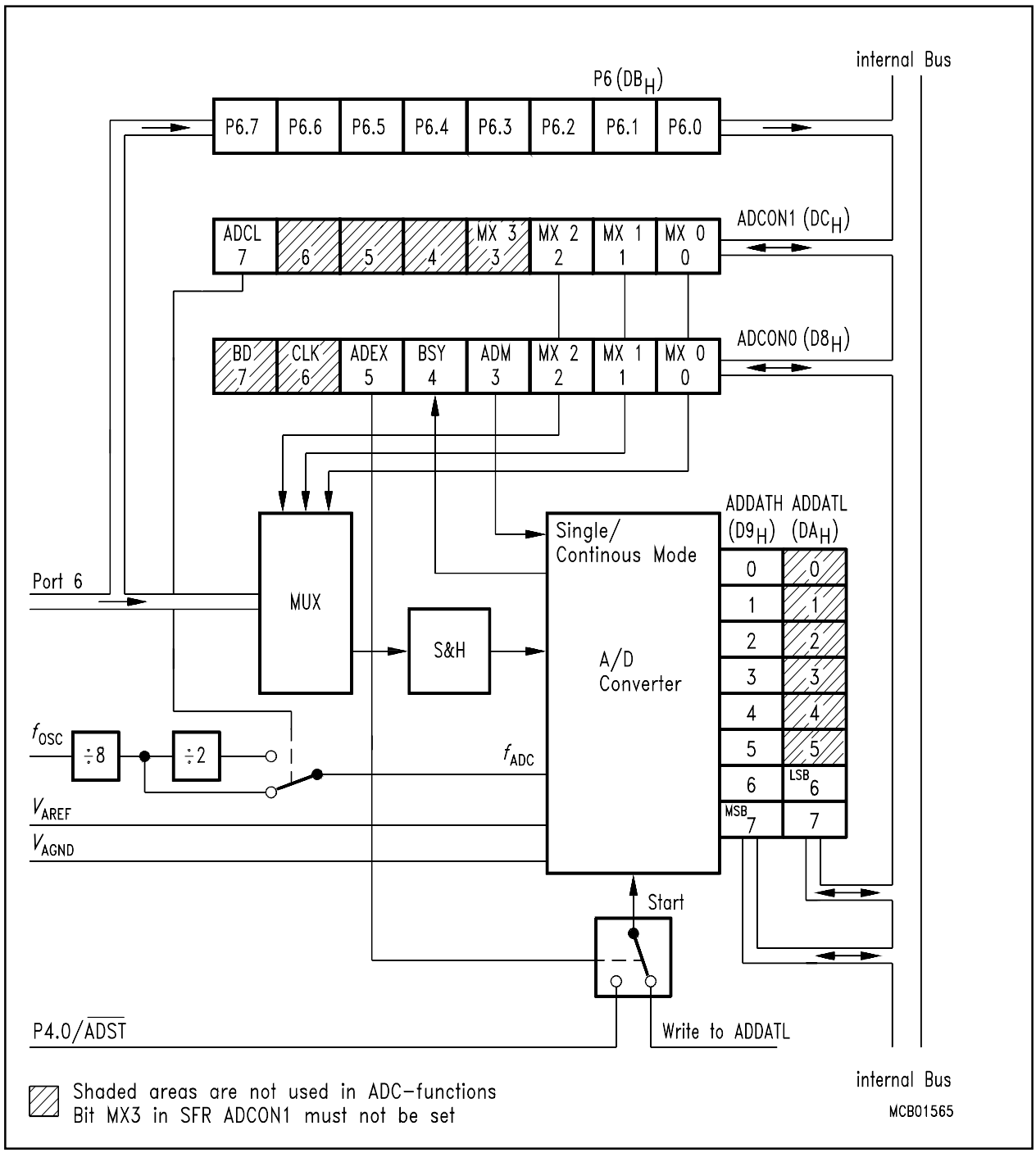


Figure 3
Block Diagram A/D Converter

Timers /Counters

The SAB 80C515A contains three 16-bit timers/counters wich are useful in many applications for timing and counting. the input clock for wach timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

– Timer/Counter 0 and 1

These timers/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; Timer/counter 1 in this mode holds its count.

External inputs $\overline{\text{INTO}}$ and $\overline{\text{INT1}}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

– Timer/Counter 2

Timer/counter 2 of the SAB 80C515A is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.

Figure 4 shows a block diagram of timer/counter 2.

Reload

A 16-bit reload can be performed with the 16-bit CRC register consisting of CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Capture

This feature permits saving of the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value of timer 2 registers TL2 and TH2 into a dedicated capture register.

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Compare

In compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

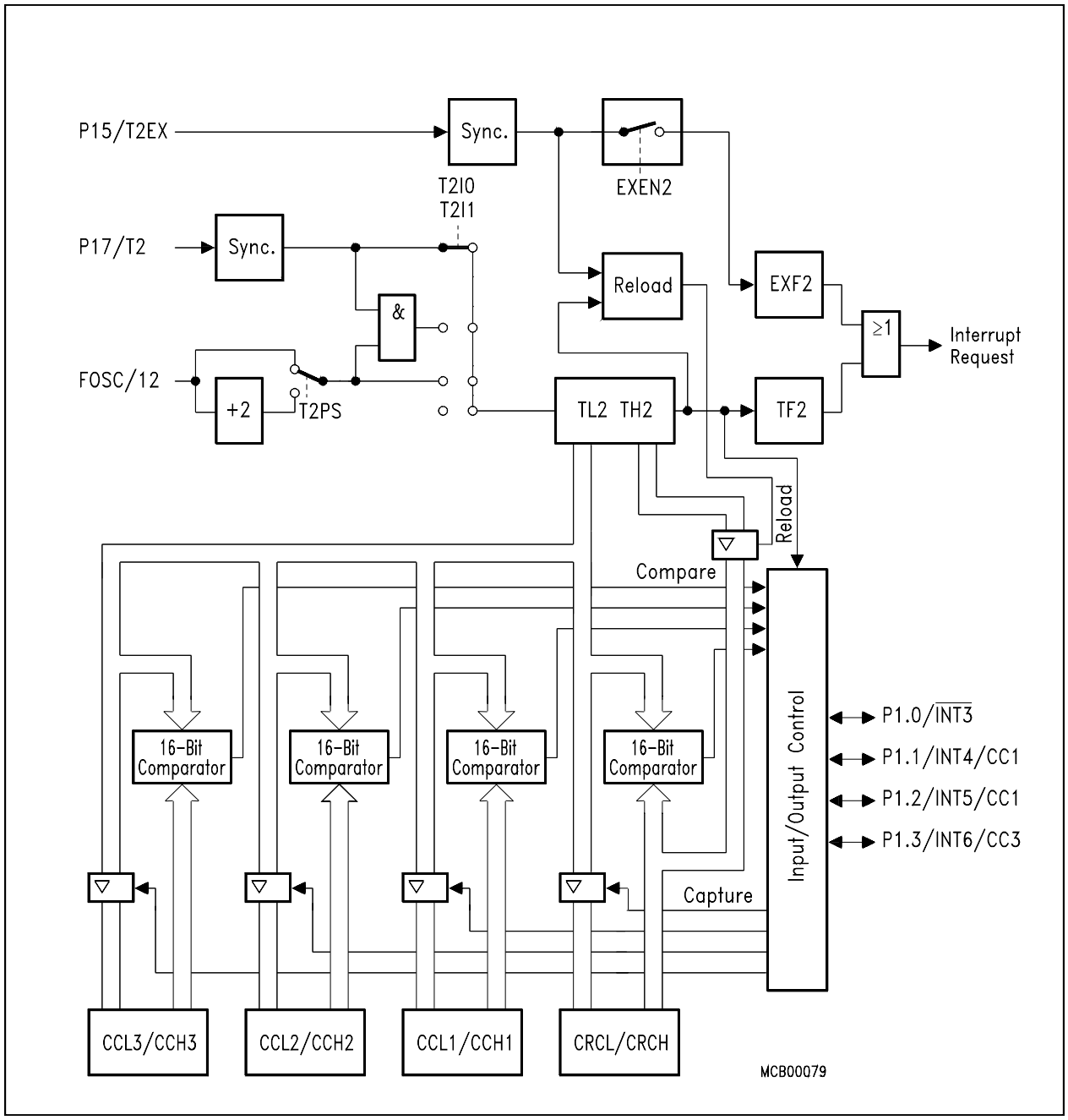


Figure 4
Block Diagram of Timer/Counter 2

Interrupt Structure

The SAB 80C515A has 12 interrupt vectors with the following vector addresses and request flags.

Table 4
Interrupt Sources and Vectors

Source (Request Flags)	Vector Address	Vector
IE0	0003_H	External interrupt 0
TF0	$000B_H$	Timer 0 interrupt
IE1	0013_H	External interrupt 1
TF1	$001B_H$	Timer 1 interrupt
RI + TI	0023_H	Serial port interrupt
TF2 + EXF2	$002B_H$	Timer 2 interrupt
IADC	0043_H	A/D converter interrupt
IEX2	$004B_H$	External interrupt 2
IEX3	0053_H	External interrupt 3
IEX4	$005B_H$	External interrupt 4
IEX5	0063_H	External interrupt 5
IEX6	$006B_H$	External interrupt 6

Each interrupt vector can be individually enabled/disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles, if no other interrrupt of the same or a higher priority level is in process.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 or 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in special function register IP0 and one in IP1.

Figure 6 shows the priority level structure.

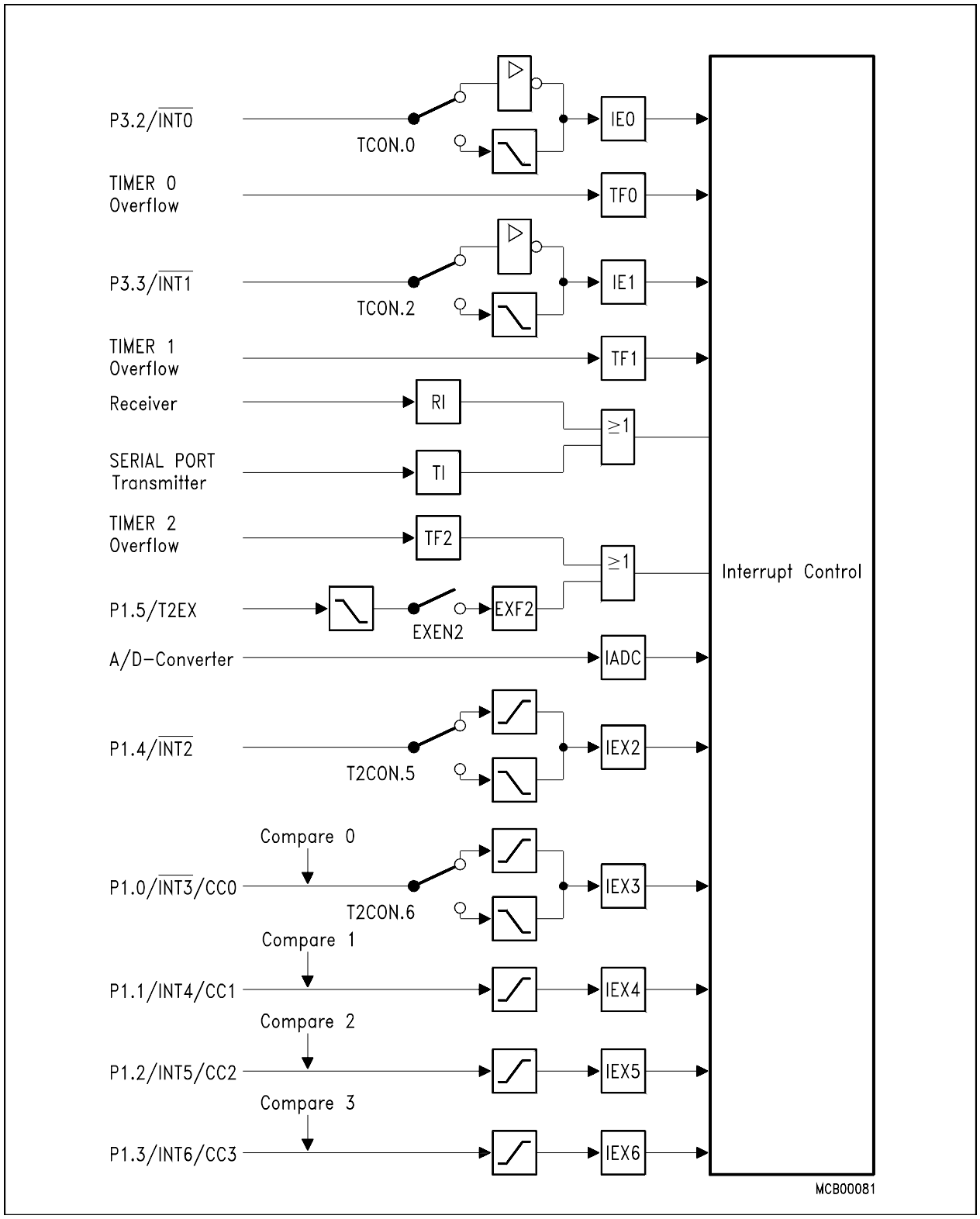


Figure 5
Interrupt Request Sources

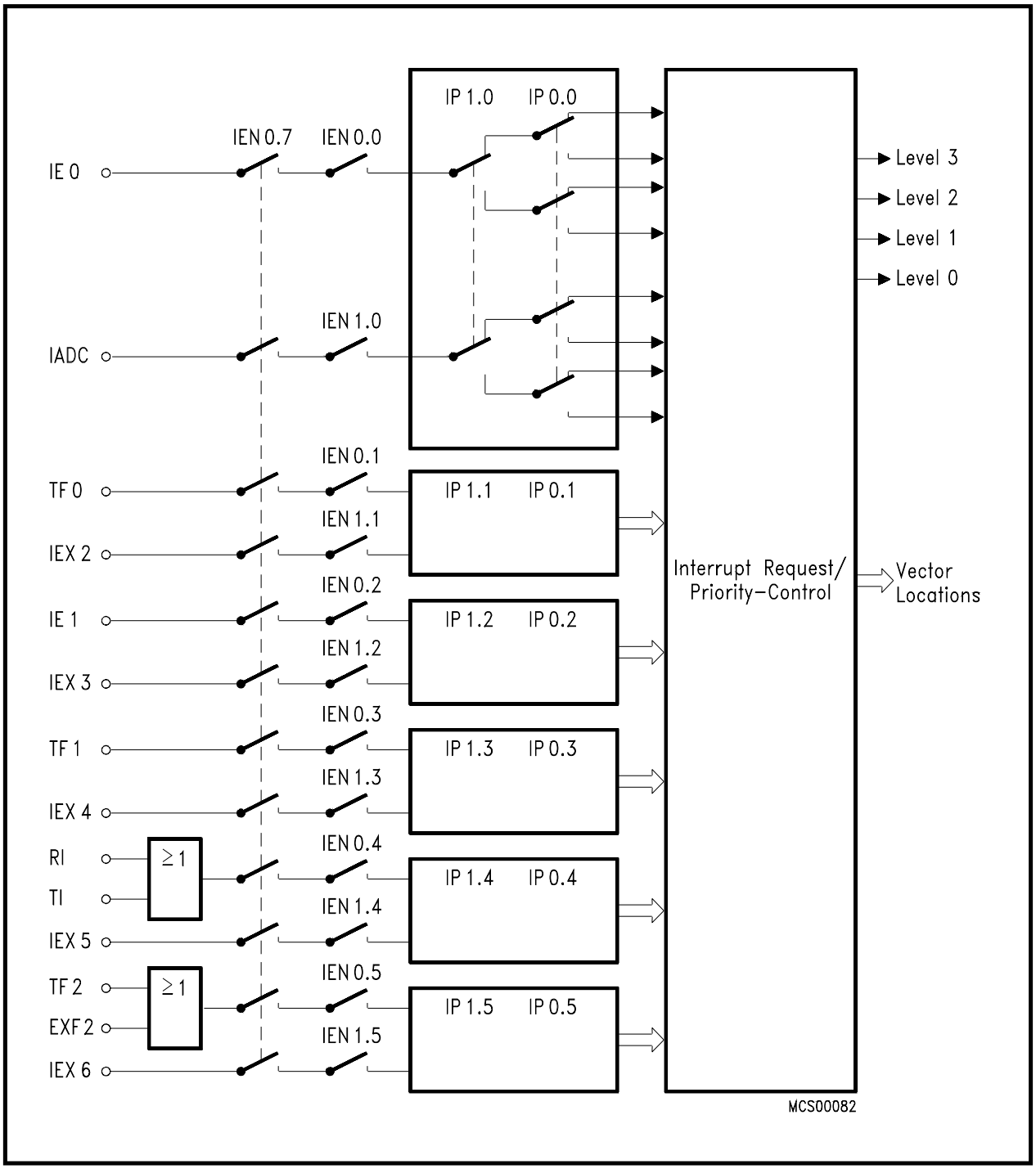


Figure 6
Interrupt Priority Level Structure

I/O Ports

The SAB 80C515A has six 8-bit I/O ports and one input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pull-up FET. Ports 1, 3 and 4 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{\text{INT3}}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{\text{INT2}}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external count or gate input
P3.0	RxD	Serial port's receiver data input (asynchronous) or data input /output (synchronous)
P3.1	TxD	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	INT0	External interrupt 0 input, timer 0 gate control
P3.3	INT1	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	WR	External data memory write strobe
P3.7	RD	External data memory read strobe
P4.0	$\overline{\text{ADST}}$	A/D Converter, external start of conversion

The SAB 80C515A has one dual-purpose input port. The ANx lines of port 6 in the SAB 80C515 can individually be used as analog or digital inputs. Reading the special function register P6 allows the user to input the digital values currently applied to the port pins. It is not necessary to select these modes by software; the voltages applied at port 6 pins can be converted to digital values using the A/D converter and at the same time the pins can be read via SFR P6. It must be noted, however, that the results in port P6 bits will be indeterminate if the levels at the corresponding pins are not within their V_{IL}/V_{IH} specifications. Furthermore, it is not possible to use port P6 as an output port. Special function register P6 is located at address $0DB_H$.

In Hardware Power Down Mode the port pins and several control lines enter a floating state. For more details see the section about Hardware Power Down Mode.

Power Saving Modes

The SAB 80C515A provides – due to Siemens ACMOS technology – four modes in which power consumption can be significantly reduced.

– The **Slow Down Mode**
  The controller keeps up the full operating functionality, but is driven with one eight of its normal operating frequency. Slowing down the frequency remarkable reduces power consumption.

– The **Idle Mode**
  The CPU is gated off from the oscillator, but all peripherals are still supplied with the clock and continue working.

– The **Software Power Down Mode**
  Operation of the SAB 80C515A is stopped, the on-chip oscillator and the RC-oscillator are turned off. This mode is used to save the contents of the internal RAM with a very low standby current and is fully compatible to the Power Down Mode of the SAB 80C515.

– The **Hardware Power Down Mode**
  Operation of the SAB 80C515A is stopped, the on-chip oscillator and the RC-oscillator are turned off. The pin $\overline{\text{HWPD}}$ controls this mode. Port pins and several control lines enter a floating state. The Hardware Power Down Mode is new in the SAB 80C515A and is independent of the state of pin $\overline{\text{PE}}$/SWD (which enables only the software initiated power reduction modes).

Hardware Enable for Software controlled Power Saving Modes

A dedicated pin $\overline{\text{PE}}$/SWD of the SAB 80C515A allows to block the Software controlled power saving modes. Since this pin is mostly used in noise-critical application it is combined with an automatic start of the Watchdog Timer.

$\overline{\text{PE}}$/SWD = V_{IH} (logic high level):	Using of the power saving modes is not possible. The watchdog timer starts immediately after reset. The instruction sequences used for entering of power saving modes will not affect the normal operation of the device.
$\overline{\text{PE}}$/SWD = V_{IL} (logic low level):	All power saving moes can be activated by software. The watchdog timer can be started by software at any time.

When left unconnected, pin $\overline{\text{PE}}$/SWD is pulled high by a weak internall pull-up. This is done to provide system protection on default.

The logic-level applied to pin $\overline{\text{PE}}$/SWD can be changed during program execution to allow or to block the use of the power saving modes without any effect on the on-chip watchdog circuitry.

Requirements for Hardware Power Down Mode

There is no dedicated pin to enable the Hardware Power Down Mode. The control pin $\overline{PE}$/SWD has no control function in this mode. It enables and disables only the use of software controlled power saving modes.

Software Controlled Power Saving Modes

All of these modes are entered by software. Special function register PCON (power control register, address is 87_H) is used to select one of these modes.

Slow Down Mode

During slow down operation all signal frequencies that are derived from the oscillator clock, are divided by eight, also the clockout signal and and the watchdog timer count.

The slow down mode is enabled by setting bit SD. The controller actually enters the slow down mode after a short synchronisation period (max. 2 machine cycles).

The slow down mode is disabled by clearing bit SD.

Idle Mode

During idle mode all peripherals of the SAB 80C515A (except for the watchdog timer) are still supplied by the oscillator clock. Thus the user has to take care which peripheral should continue to run and which has to be stopped during Idle.

The procedure to enter the Idle mode is similar to the one entering the power down mode. The two bits IDLE and IDLS must be set by two consecutive instructions to minimize the chance of unintentional activating of the idle mode.

There are two ways to terminate the idle mode:

– The idle mode can be terminated by activating any enabled interrupt. This interrupt will be serviced and the instruction to be executed following the RETI instruction will be the one following the instruction that set the bit IDLS.

– The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. The control signals ALE and $\overline{PSEN}$ hold at logic high levels (see table 5).

Software Power Down Mode

The power down mode is entered by two consecutive instructions directly following each other. The first instruction has to set the flag PDE (power down enable) and must not set PDS (power down set). The following instruction has to set the start bit PDS. Bits PDE and PDS will automatically be cleared after having been set.

The instruction that sets bit PDS is the last instruction executed before going into power down mode. The only exit from power down mode is a hardware reset.

The status of all output lines of the controller can be looked up in table 5.

Hardware Controlled Power Down Mode

The pin $\overline{\text{HWPD}}$ controls this mode. If it is on logic high level (inactive) the part is running in the normal operating modes. If pin $\overline{\text{HWPD}}$ gets active (low level) the part enters the Hardware Power Down Mode; this is independent of the state of pin $\overline{\text{PE}}$/SWD.

$\overline{\text{HWPD}}$ is sampled once per machine cycle. If it is found active, the device starts a complete internal reset sequence. The watchdog timer is stopped and its status flag WDTS is cleared exactly the same effects as a hardware reset. In this phase the power consumption is not yet reduced. After completion of the internal reset both oscillators of the chip are disabled. At the same time the port pins and several control lines enter a floating state as shown in table 5. In this state the power consumption is reduced to the power down current IPD. Also the supply voltage can be reduced. Table 5 also lists the voltages which may be applied at the pins during Hardware Power Down Mode without affecting the low power consumption.

Termination of HWPD Mode:

This power down state is maintained while pin $\overline{\text{HWPD}}$ is held active. If HWPD goes to high level (inactive state) an automatic start up procedure is performed:

- First the pins leave their floating condition and enter their default reset state (as they had immediately before going to float state).
- Both oscillators are enabled. The oscillator watchdog's RC oscillator starts up very fast (typ. less than 2 ms).
- Because the oscillator watchdog is active it detects a failure condition if the on-chip oscillator hasn't yet started. Hence, the watchdog keeps the part in reset and supplies the internal clock from the RC oscillator.
- Finally, when the on-chip oscillator has started, the oscillator watchdog releases the part from reset with oscillator watchdog status flag set.
  When automatic start of the watchdog was enabled ($\overline{\text{PE}}$/SWD connected to V_{CC}), the Watchdog Timer will start, too (with its default reload value for time-out period).
- The $\overline{\text{Reset}}$ pin overrides the Hardware Power Down function, i.e. if reset gets active during Hardware Power Down it is terminated and the device performs the normal resetfunction.(Thus, pin $\overline{\text{Reset}}$ has to be inactive during Hardware Power Down Mode). function.(Thus, pin $\overline{\text{Reset}}$ has to be inactive during Hardware Power Down Mode).

Table 5
Status of all pins during Idle Mode, Power Down Mode and Hardware Power Down Mode

Pins	Idle Mode Last instruction executed from		Power Down Mode Last instruction executed from		Hardware Power Down
	internal ROM	external ROM	internal ROM	external ROM	Status
P0	Data	float	Data	float [1]	floating [1]
P1	Data alt outputs	Dat alt outputsa	Data last outputs	Data last outputs	
P2	Data	Address	Data	Data	
P3	Data alt outputs	Data alt outputs	Data last output	Data last output	outputs
P4	Data alt outputs	Data alt outputs	Data last outputs	Data last output	disabled
P5	Data alt output	Data alt output	Data last output	Data last output	input
P6	[1]	[1]	[1]	[1]	function
$\overline{EA}$					active input [2]
$\overline{PE}$/SWD					active input pull-up disabled [2]
XTAL1					active output
XTAL2					disabled input function [1]
$\overline{PSEN}$	high	high	low	low	floating output
ALE	high	high	low	low	
V_{AREF} V_{AGND}					active supply pins [3]
$\overline{RESET}$					active input must be high

[1] Applied voltage range at pin $V_{SS} \leq V_{IN} \leq V_{CC}$
[2] $V_{IN} = V_{SS}$ or $V_{IN} = V_{CC}$
[3] $V_{SS} \leq V_{IN} \leq V_{CC}$; $V_{AREF} \geq V_{AGND}$

Serial Interface

The SAB 80C515A has a full duplex and receive buffered serial interface. It is functionally identical with the serial interface of the SAB 8051.

Table 6 shows possible configurations and the according baud rates.

Table 6
Baud Rate Generation

	Mode		Mode 0		
8-Bit synchronous channel	Baudrate	f_{OSC} =12 MHz	1 MHz		
		f_{OSC} =16 MHz	1.33 MHz		
		f_{OSC} =18 MHz	1.5 MHz		
	derived from		f_{OSC}		
	Mode		**Mode 1**		
8-Bit UART	Baudrate	f_{OSC} =12 MHz	1 Baud – 62.5 kBaud		183 Baud – 375 kBaud
		f_{OSC} =16 MHz	1 Baud – 83 kBaud		244 Baud – 500 kBaud
		f_{OSC} =18 MHz	1 Baud – 93.7 kBaud		2375 Baud – 562.5 kBaud
	derived from		Timer 1		10-Bit Baudrate Generator
	Mode		**Mode 2**	**Mode 3**	
9-Bit UART	Baudrate	f_{OSC} =12 MHz	187.5 kBaud/ 375 kBaud	1 Baud – 62.5 kBaud	183 Baud –75 kBaud
		f_{OSC}=16 MHz	250 Baud/ 500 kBaud	1 Baud – 83.3 kBaud	244 Baud – 500 kBaud
		f_{OSC} =18 MHz	281.2 kBaud/ 562.5 kBaud	1 Baud – 93.7 kBaud	275 Baud – 562.5 kBaud
	derived from		$f_{OSC}/2$	Timer 1	10-Bit Baudrate Generator

The Serial Interface can operate in 4 modes:

Mode 0: Shift register mode:
Serial data enters and exits through R × D. T × D outputs the shift clock 8 data bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 8-bit UART, variable baud rate:
10-bit are transmitted (through T × D) or received (through R × D): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB80 in special function register SCON. The baud rate is variable.

Mode 2: 9-bit UART, fixed baud rate:
11-bit are transmitted (through T × D) or received (through R × D): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9th data bit (TB80 in SCON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB80 or a second stop bit by setting TB80 to 1. On reception the 9th data bit goes into RB80 in special function register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 9-bit UART, variable baud rate:
11-bit are transmitted (through T × D) or received (through R × D): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). In fact, mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

Variable Baud Rates for Serial Interface

Variable baud rates for modes 1 and 3 of serial interface can be derived from either timer 1 or a new dedicated Baudrate Generator.

The baud rate is generated by a free running 10-bit timer with programmable reload register.

$$\text{Mode 1.3 baud rate} = \frac{2^{\text{SMOD}} * f_{OSC}}{64 * (2^{10} - \text{SREL})}$$

The default value after reset in the reload registers SRELL and SRELH provides a baud rate of 4.8 kBaud (SMOD = 0) or 9.6 kBaud (SMOD = 1) at 12 MHz oscillator frequency. This guarantees full compatibility to the SAB 80C515.

Fail Safe Units

The SAB 80C515A offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure:

– a programmable watchdog timer (WDT), with variable time-out period from 512 µs up to appr. 1.1 s @12 MHz. Upward compatible to SAB 80C515 watchdog timer.

– an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state, in case the on-chip oscillator fails; it also controls the restart from the Hardware Power Down Mode and provides the clock for a fast internal reset after power-on.

Programmable Watchdog Timer

The WDT can be activated by hardware or software.

Hardware initialization is done when pin $\overline{PE}$/SWD (Pin 4) is held high during RESET. The SAB 80C515A then starts program execution with the WDT running. Since pin $\overline{PE}$/SWD is only sampled during Reset, the WDT cannot be started externally during normal operation.

Software initialization is done by setting bit SWDT in SFR IEN1.

A refresh of the watchdog timer is done by setting bits WDT (SFR IEN0) and SWDT consecutively. This double instruction sequence has been implemented to increase system security.

When a watchdog timer reset occurs, the watchdog timer keeps on running, but a status flag WDTS (SFR IP0) is set. This flag can also be cleared by software.

Figure 7 shows the block diagram of the programmable Watchdog Timer.

Oscillator Watchdog

The unit serves three functions:

– Monitoring of the on-chip oscillator's function.
The watchdog monitors the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is forced into reset; if the failure condition disappears (i.e. the on-chip oscillator has again a higher frequency than the RC oscillator), the part executes a final reset phase of appr. 0.25 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.

– Restart from the Hardware Power Down Mode.
If the Hardware Power Down Mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete Hardware Power Down sequence; however, the watchdog works identically to the monitoring function.

– Fast internal reset after power-on.
In this function the oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. In this case the oscillator watchdog unit also works identically to the monitoring function.

Figure 8 shows the block diagram of the oscillator watchdog unit. It consists of an internal RC oscillator which provides the reference frequency for the frequency comparator.

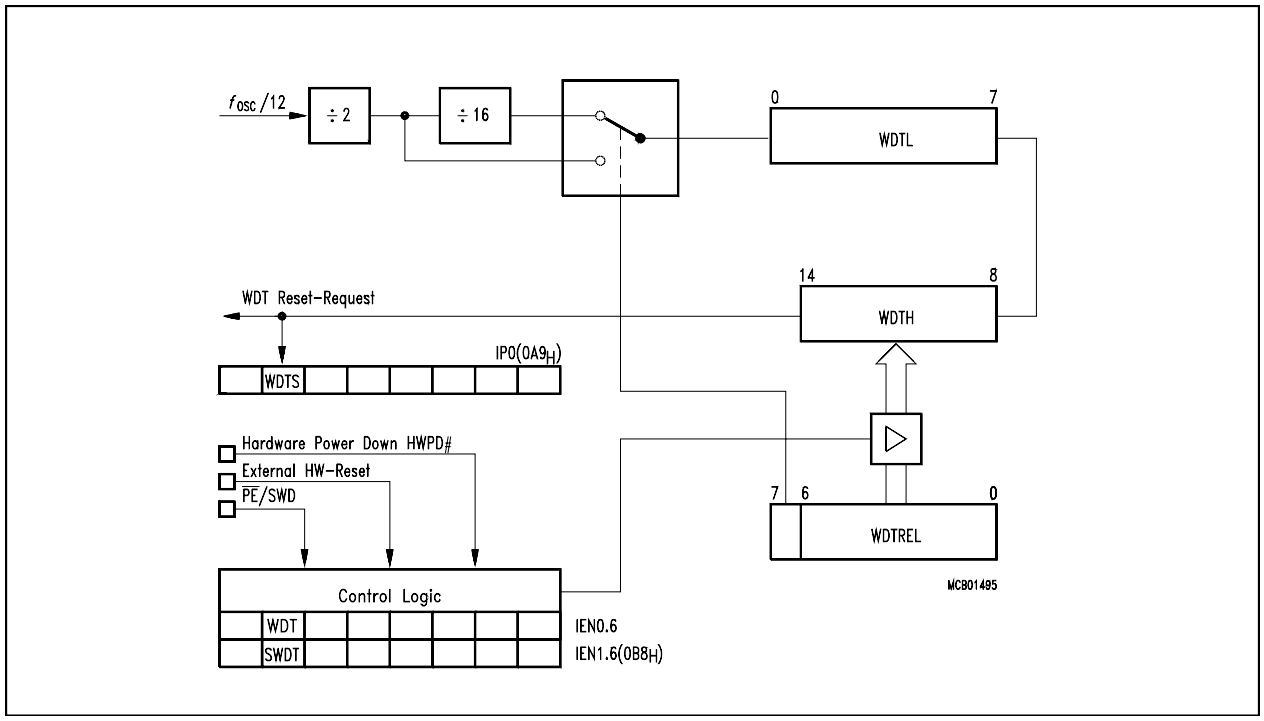


Figure 7
Block Diagram of the Programmable Watchdog Timer

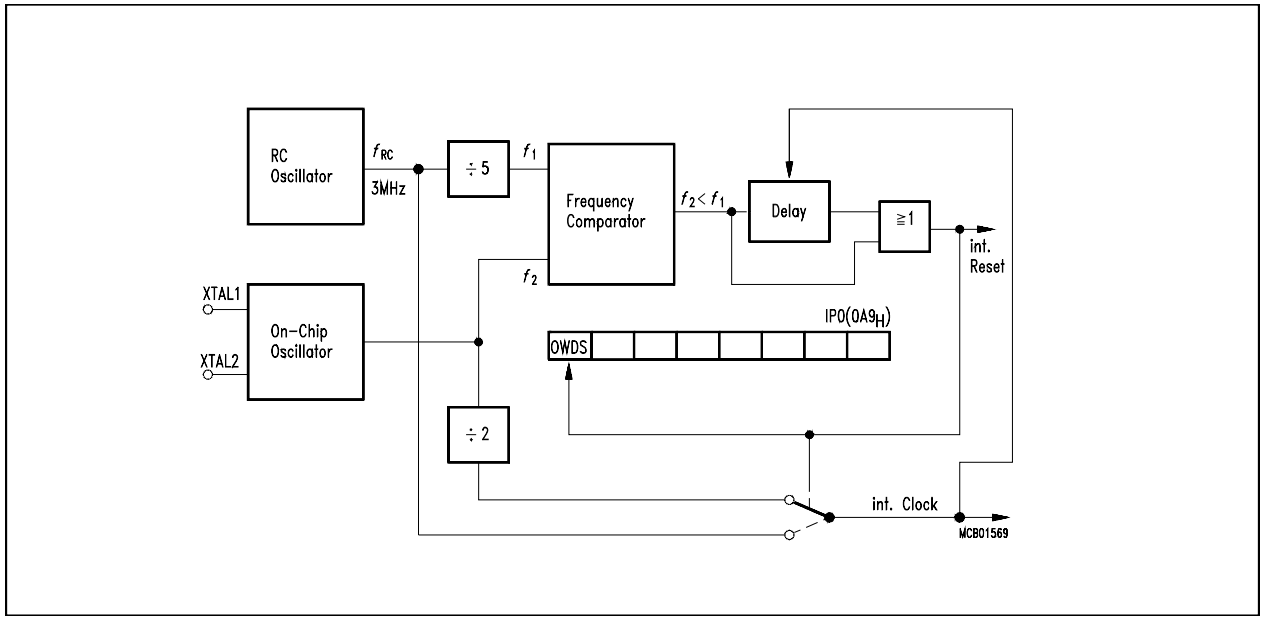


Figure 8
Functional Block Diagram of the Oscillator Watchdog

Fast internal reset after power-on

The SAB 80C515A can use the oscillator watchdog unit for a fast internal reset procedure after power-on.

Normally members of the 8051 family (like the SAB 80C515) enter their default reset state not before the on-chip oscillator starts. The reason is that the external reset signal must be internally synchronized and processed in order to bring the device into the correct reset state. Especially if a crystal is used the start up time of the oscillator is relatively long (typ. 1 ms). During this time period the pins have an undefined state which could have severe effects e.g. to actuators connected to port pins.

In the SAB 80C515A the oscillator watchdog unit avoids this situation. After power-on the oscillator watchdog's RC oscillator starts working within a very short start-up time (typ. less than 2 ms). In the following the watchdog circuitry detects a failure condition for the on-chip oscillator because this has not yet started (a failure is always recognized if the watchdog's RC oscillator runs faster than the on-chip oscillator). As long as this condition is valid the watchdog uses the RC oscillator output as clock source for the chip rather than the on-chip oscillator's output. This allows correct resetting of the part and brings also all ports to the defined state.

Delay time between power-on and correct reset state:

Typ.: 18 µs
Max.: 34 µs

Instruction Set

The SAB 80C515A / 83C515A-5 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-H6497-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias	– 40 to 85 °C
Storage temperature	– 65 to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS})	– 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to V_{CC} + 0.5 V
Input current on any pin during overload condition	– 10mA to + 10 mA
Absolute sum of all input currents during overload condition	|100 mA|
Power dissipation	1 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) theVoltage on V_{CC} pins with respect to ground (V_{SS}) must not exeed the values defined by the absolute maximum ratings.*

DC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
T_A = 0 to 70 °C for the SAB 80C515A
T_A = – 40 to 85 °C for the SAB 80C515A-T3

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Input low voltage (exept $\overline{EA}$,$\overline{RESET}$, $\overline{HWPD}$)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage $\overline{EA}$	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage ($\overline{HWPD}$, $\overline{RESET}$)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (exept $\overline{RESET}$, XTAL2 and $\overline{HWPD}$)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to $\overline{RESET}$ and $\overline{HWPD}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Output low voltage (ports 1, 2, 3, 4, 5)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (ports 0, ALE, $\overline{RESET}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage, (ports1, 2, 3, 4, 5)	V_{OH}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 80 µA I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode,- ALE, $\overline{PSEN}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 800 µA I_{OH} = – 80 µA [2]
Logic 0 input current (ports 1, 2, 3, 4, 5)	I_{IL}	– 10	– 70	µA	V_{IN} = 2 V
Logical 1-to-0 transition current, ports 1, 2, 3, 4, 5	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$, P6, $\overline{HWPD}$)	I_{LI}	– –	± 100 ± 150	nA nA	0.45 < V_{IN} < V_{CC} 0.45 < V_{IN} < V_{CC} T_A > 100 °C
Input low current to $\overline{RESET}$ for reset	I_{IL2}	– 10	– 100	µA	V_{IN} = 0.45 V
Input low current ($\overline{XTAL2}$)	I_{IL3}	–	– 15	µA	V_{IN} = 0.45 V
Input low current ($\overline{PE}$/SWD)	I_{IL4}	–	– 20	µA	V_{IN} = 0.45 V
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25 °C
Power-supply current:					
Active mode, 12 MHz [7]	– I_{CC}	–	26	mA	V_{CC} = 5 V [4]
Active mode, 18 MHz [7]	– I_{CC}	–	35	mA	V_{CC} = 5 V [4]
Idle mode, 12 MHz [7]	– I_{CC}	–	11.8	mA	V_{CC} = 5 V [5]
Idle mode, 18 MHz [7]	– I_{CC}	–	14.2	mA	V_{CC} = 5 V [5]
Slow down mode, 12 MHz	– I_{CC}	–	9	mA	V_{CC} = 5 V [6]
Slow down mode, 18 MHz	– I_{CC}	–	10	mA	V_{CC} = 5 V [6]
Power Down Mode	– I_{PD}	–	50	µA	V_{CC} = 2 ... 5.5 V [3]

Notes see page 43.

Notes for page 44:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4 and 5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Software Power Down Mode) is measured under following conditions:
$\overline{EA}$ = $\overline{RESET}$ = V_{CC}; Port0 = Port6 = V_{CC}; XTAL1 = N.C.; XTAL2 = V_{SS};
$\overline{PE}$/SWD = V_{SS}; $\overline{HWPD}$ = V_{CC}; V_{AGND} = V_{SS}; V_{ARef} = V_{CC}; all other pins are disconnected.
I_{PD} (Hardware Power Down Mode): independent of any particular pin connection.

4) I_{CC} (active mode) is measured with:
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.;
$\overline{EA}$ = $\overline{PE}$/SWD = V_{CC}; Port0 = Port6 = V_{CC}; $\overline{HWPD}$ = V_{CC}; $\overline{RESET}$ = V_{SS};
all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.; $\overline{RESET}$ = V_{CC}; $\overline{HWPD}$ = V_{CC}; Port0 = Port6 = V_{CC}; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}; all other pins are disconnected;

6) I_{CC} (slow down mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.; $\overline{RESET}$ = V_{CC}; $\overline{HWPD}$ = V_{CC}; Port6 = V_{CC}; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}; all other pins are disconnected;

7) I_{CC} Max at other frequencies is given by:
active mode: I_{CC} (max) = 1.5 * f_{OSC} + 8
idle mode: I_{CC} (max)= 0.4 * f_{OSC} + 7
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

A/D Converter Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
V_{AREF} = V_{CC} ± 5 %; V_{AGND} = V_{SS} ± 0.2 V;
T_A = 0 to 70 °C for the SAB 80C515A/83C515A-5
T_A = – 40 to 85 °C for the SAB 80C515A-T3/83C515A-5-T3

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input capacitance	C_I		25	70	pF	
Sample time (inc. load time)	T_S			4 t_{CY} [1]	µs	[2]
Conversion time (inc. sample time)	T_C			14 t_{CY} [1]	µs	[3]
Total unadjusted error	TUE			± 2	LSB	V_{AREF} = V_{CC} V_{AGND} = V_{SS}
V_{AREF} supply current	I_{REF}		± 20		µA	

1) $t_{CY} = (8*2^{ADCL}) / f_{OSC}$; ($t_{CY} = 1/f_{ADC}$; $f_{ADC} = f_{OSC}/(8*2^{ADCL})$)
2) This parameter specifies the time during the input capacitance C_I, can be charged/discharged by the external source. It must be guaranteed, that the input capacitance C_I, is fully loaded within this time. 4TCY is 2 µs at the f_{OSC}= 16 MHz. After the end of the sample time T_S, changes of the analog input voltage have no effect on the conversion result.
3) This parameter includes the sample time T_S. 14TCY is 7 µs at f_{OSC} = 16 MHz.

AC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB 80C515A/83C515A-5

T_A = – 40 to 85 °C for the SAB 80C515A-T3/83C515A-5-T3

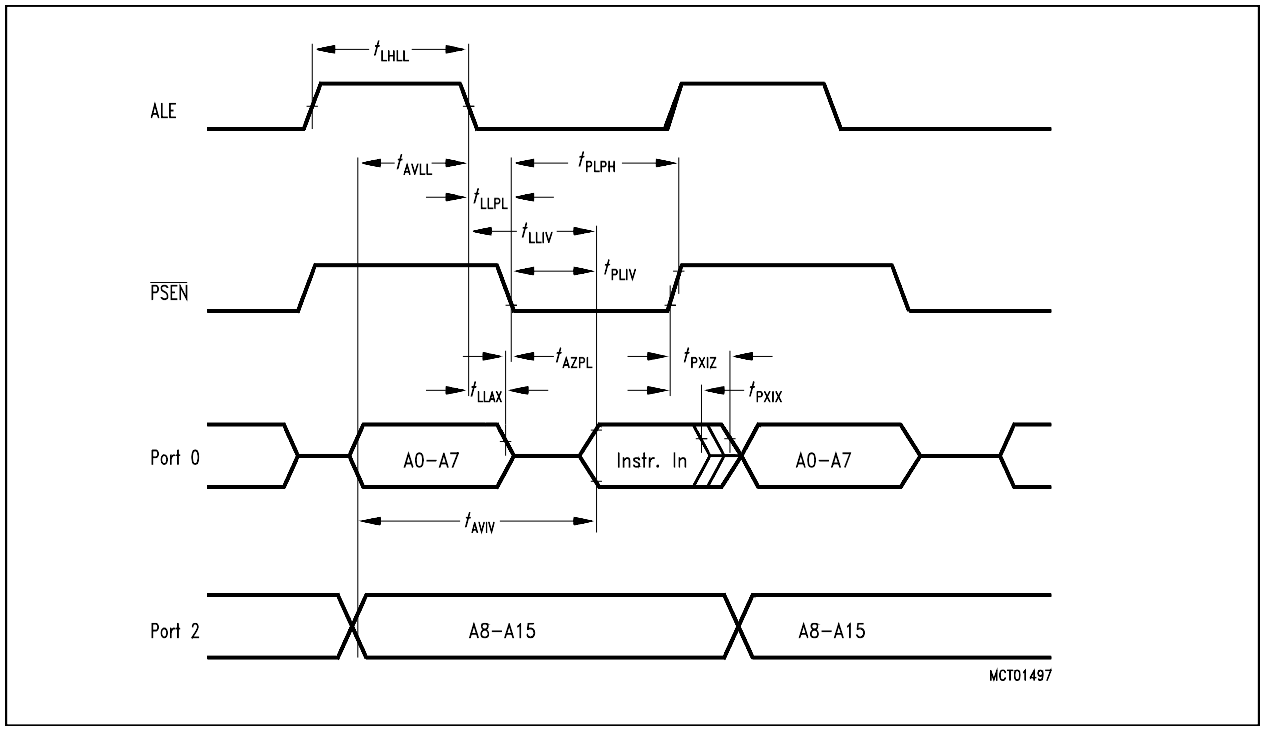
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	71	–	$2\,t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	26	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	26	–	$t_{CLCL} - 30$	–	ns
ALE to valid instruction in	t_{LLIV}	–	122	–	$4\,t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	31	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	132	–	$3\,t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	92	–	$3\,t_{CLCL} - 75$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} *)	–	46	–	$t_{CLCL} - 10$	ns
Address valid after $\overline{PSEN}$	t_{PXAV} *)	48	–	$t_{CLCL} - 8$	–	ns
Address to valid instruction in	t_{AVIV}	–	218	–	$5\,t_{CLCL} - 60$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

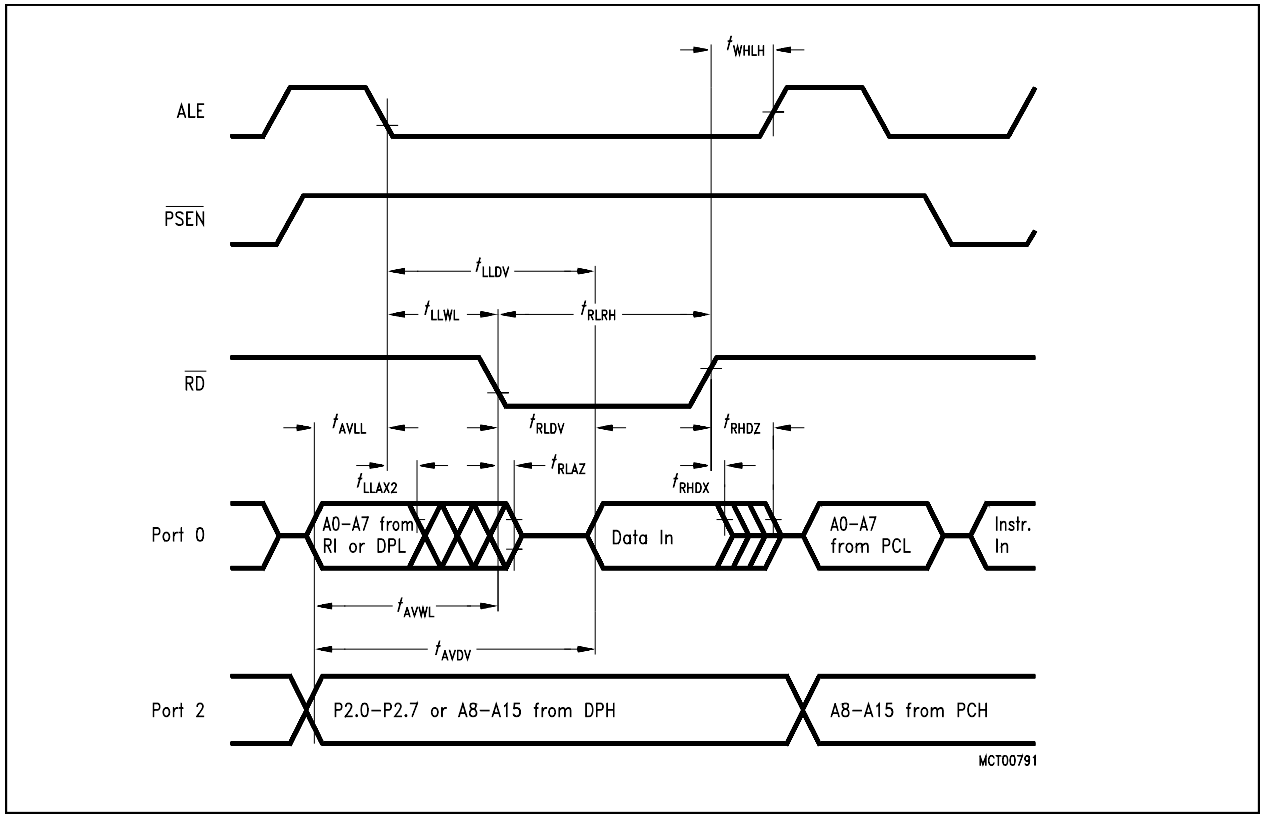
*) Interfacing the SAB 80C515A to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

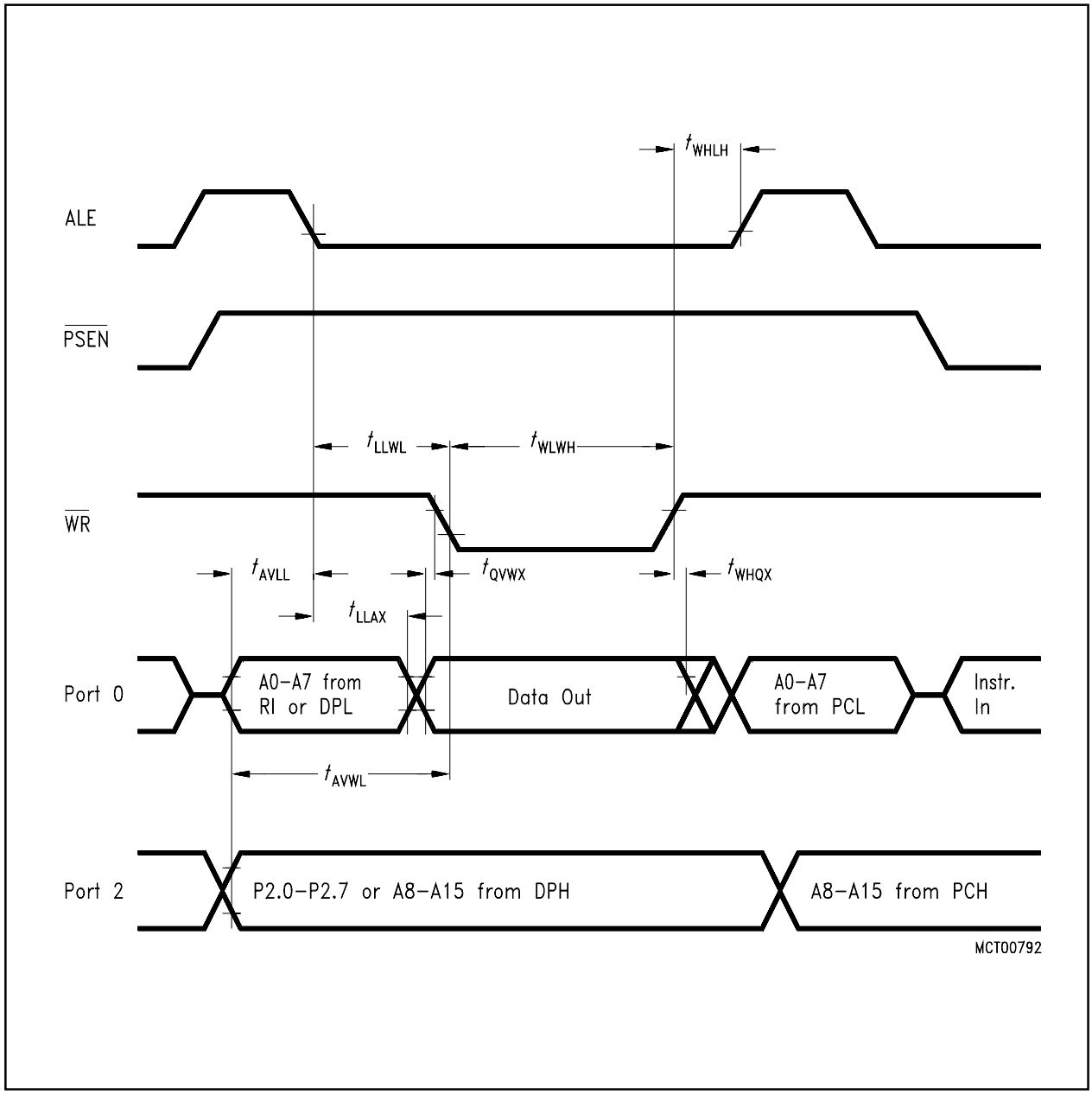
Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	233	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	233	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	81	–	2 t_{CLCL} – 30	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	128	–	5 t_{CLCL} – 150	ns
DATA hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	51	–	2 t_{CLCL} – 60	ns
ALE to valid data in	t_{LLDV}	–	294	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	335	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	117	217	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	16	96	t_{CLCL} – 40	t_{CLCL} + 40	ns
Address valid to $\overline{WR}$	t_{AVWL}	92	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	11	–	t_{CLCL} – 45	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	239	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	16	–	t_{CLCL} – 40	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns



Program Memory Read Cycle



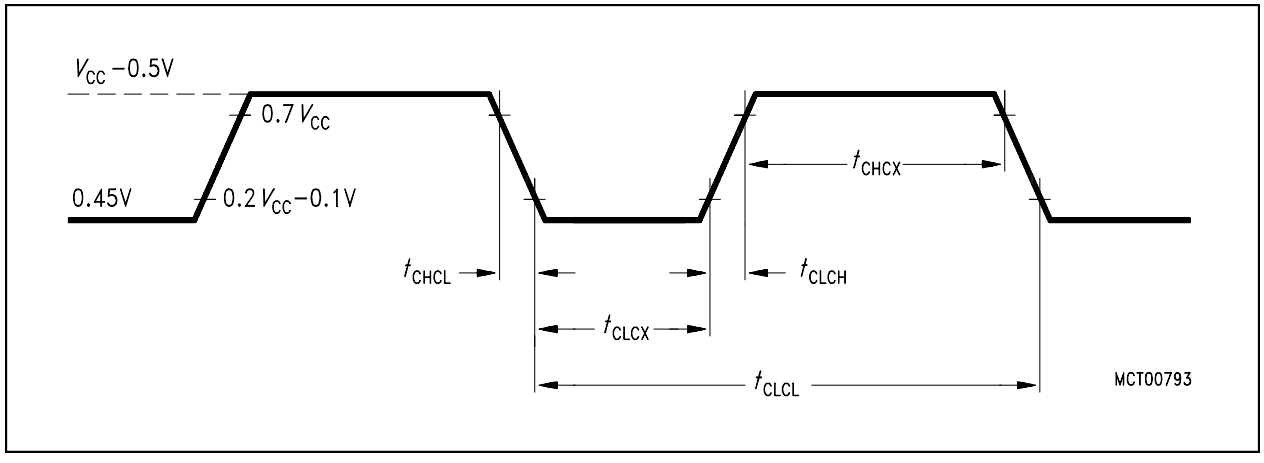
Data Memory Read Cycle



Data Memory Write Cycle

AC Characteristics (cont'd)

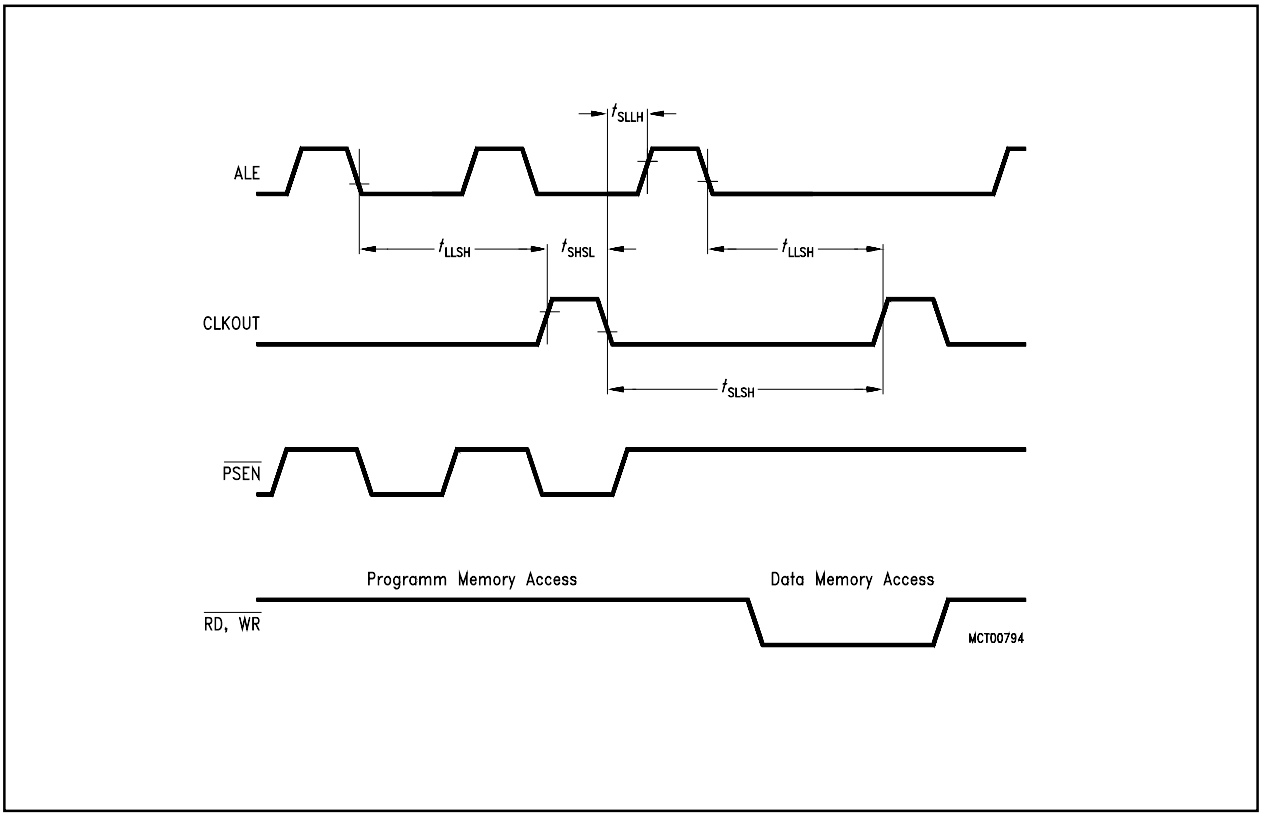
Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 3.5 MHz to 18 MHz		
		min.	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	55.6	285	ns
High time	t_{CHCX}	20	t_{CLCL}-t_{CLCX}	ns
Low time	t_{CLCX}	20	t_{CLCL}-t_{CHCX}	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns
Oscillator frequency	$1/t_{CLC}$	3.5	18	MHz



External Clock Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	349	–	7 t_{CLCL} – 40	–	ns
CLKOUT high time	t_{SHSL}	71	–	2 t_{CLCL} – 40	–	ns
CLKOUT low time	t_{SLSH}	516	–	10 t_{CLCL} – 40	–	ns
CLKOUT low to ALE high	t_{SLLH}	16	96	t_{CLCL} – 40	t_{CLCL} + 40	ns



System Clock Timing

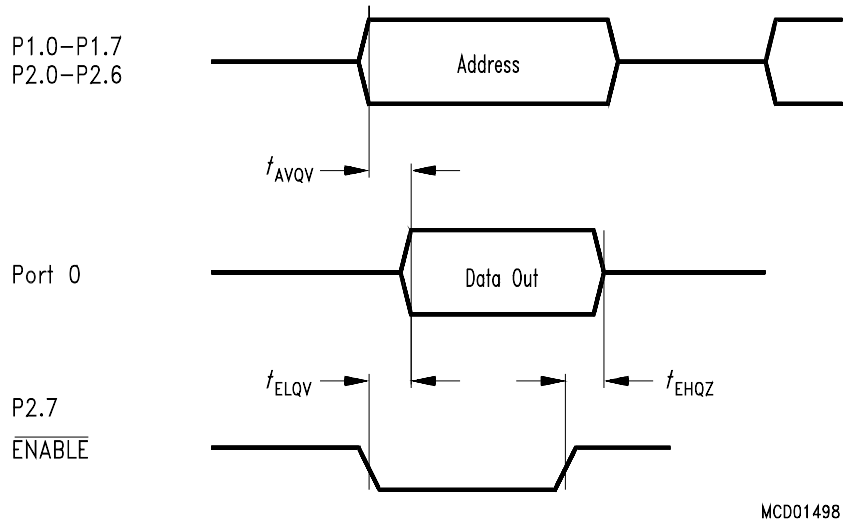
ROM Verification Characteristics

T_A = 25 °C ± 5 °C; V_{CC} = 5 V +10 %, – 15 %; V_{SS} = 0 V

Parameter	Symbol	Limit values		Unit
		min.	max.	

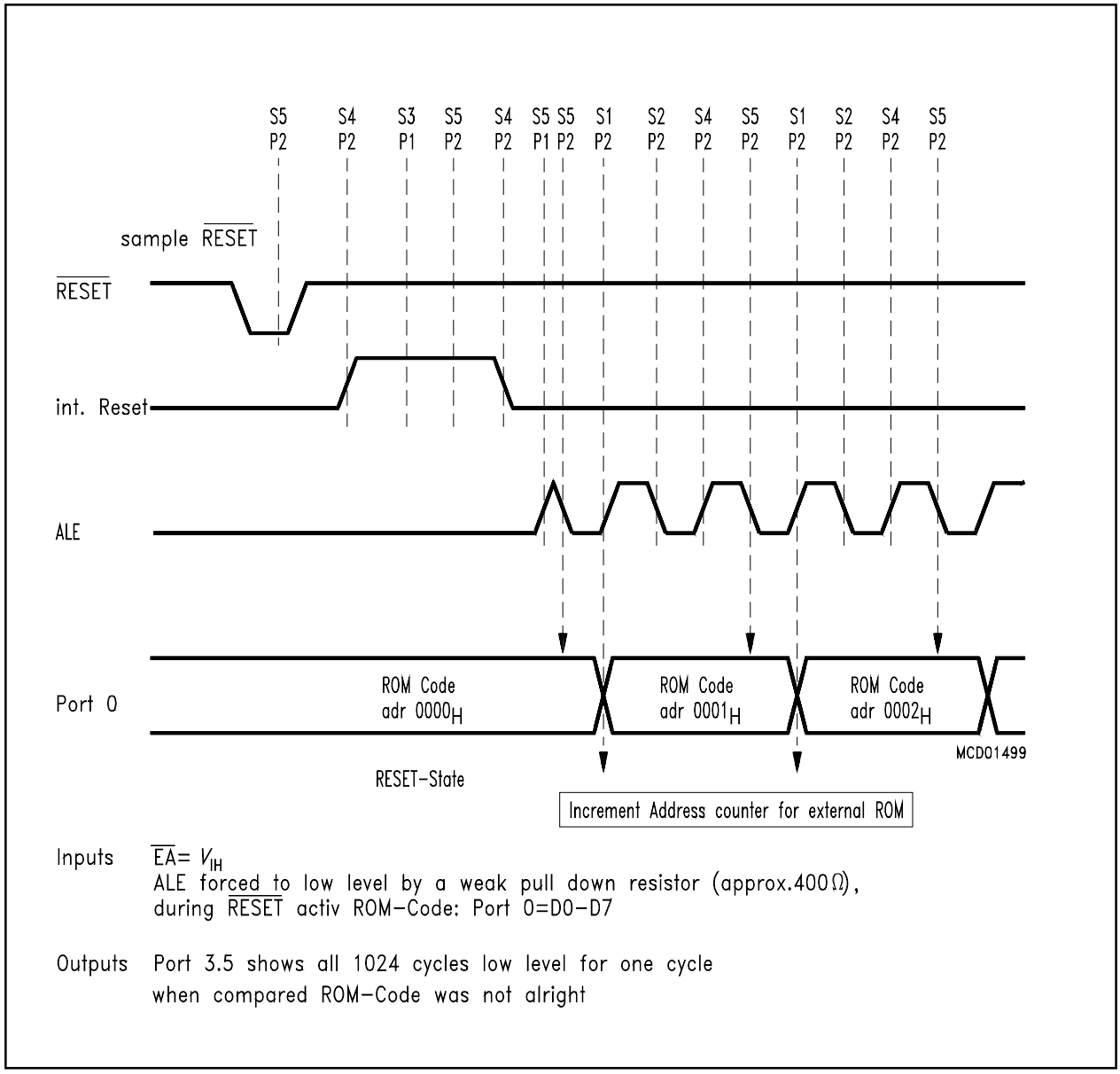
ROM Verification Mode 1 (Standard Verify Mode for not Read Protected ROM)

Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE	t_{EHOZ}	0	48 t_{CLCL}	ns
Oscillator frequency	1/t_{CLCL}	4	6	MHz

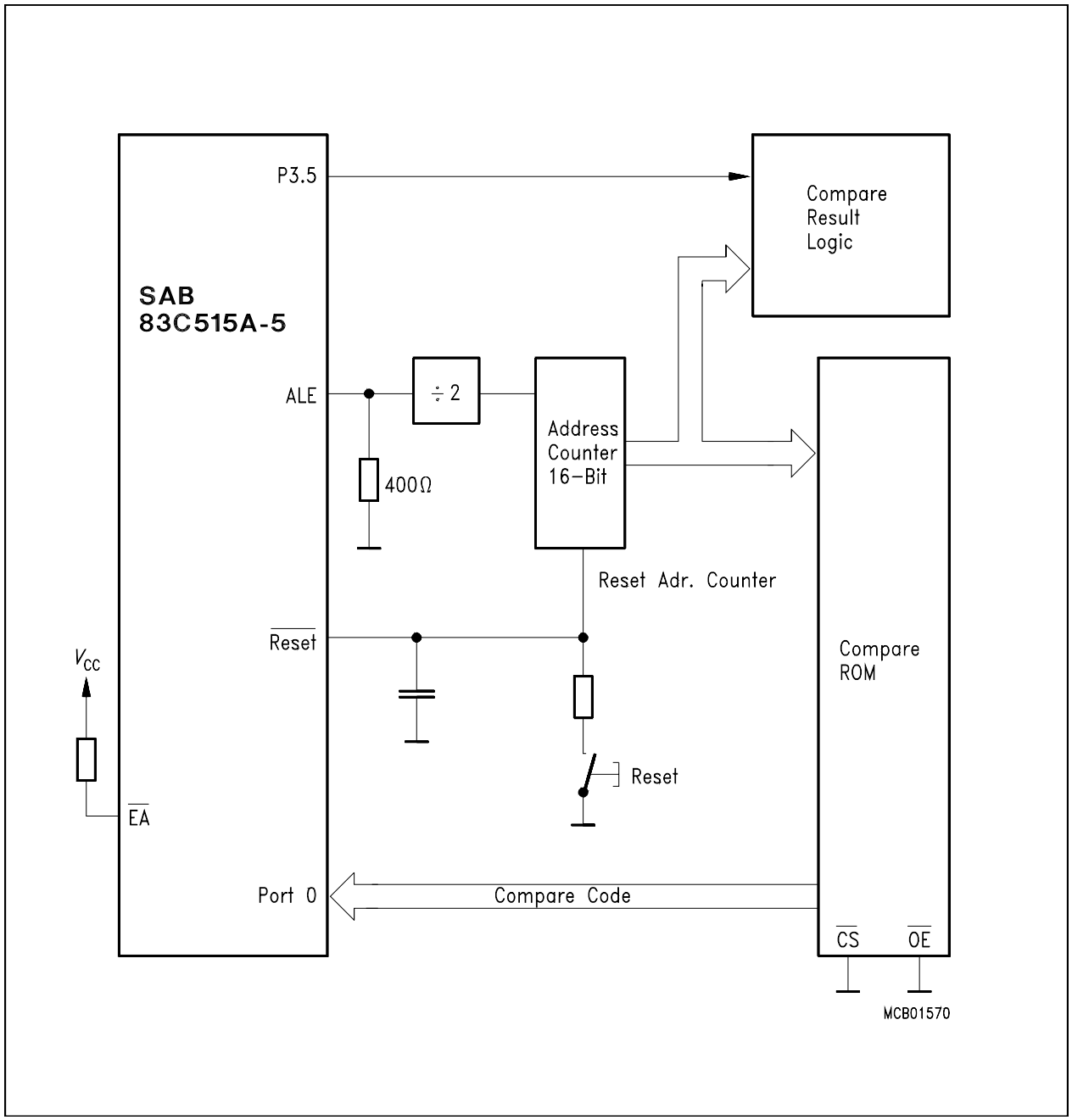


ROM Verification Mode 1

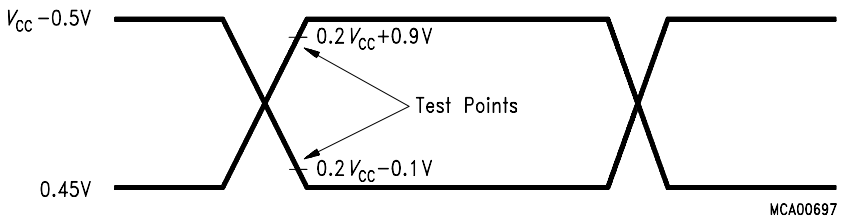
ROM Verification Mode 2 (New Verify Mode for Protected and not Protected ROM)



ROM Verification Mode 2

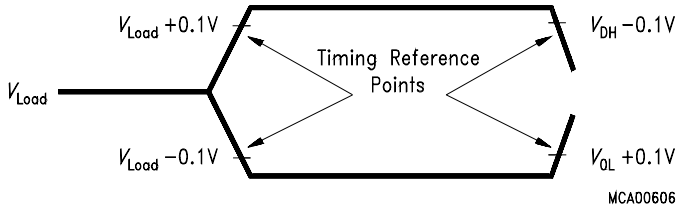


Application Example for Verifying the Internal ROM with ROM Verify Mode 2



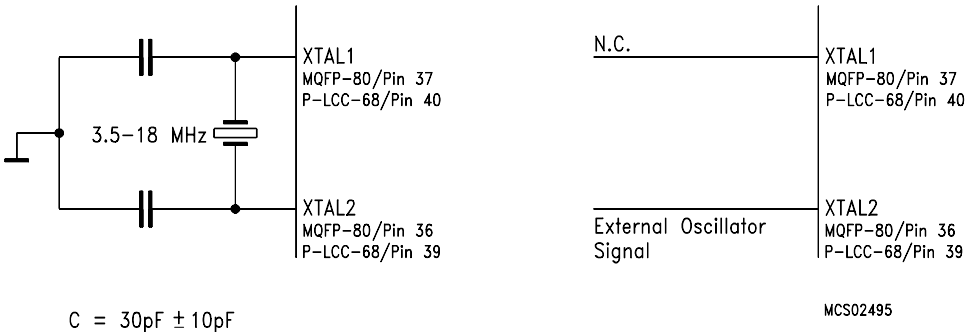
AC Inputs during testing are driven at V_{CC} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

AC Testing: Float Waveforms



Recommended Oscillator Circuits