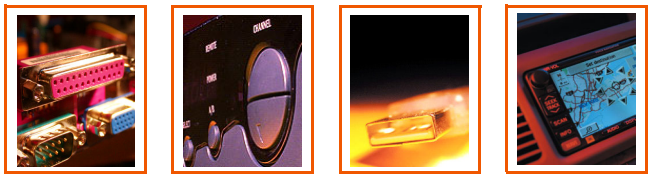
LPC47M10x



100 Pin Enhanced Super I/O Controller with LPC Interface for Consumer Applications

PRODUCT FEATURES

Data Brief

- 3.3 Volt Operation (5 Volt Tolerant)
- LPC Interface
- ACPI 1.0 Compliant
- Fan Control
  - — Fan Speed Control Outputs
  - — Fan Tachometer Inputs
- Programmable Wake-up Event Interface
- PC98, PC99 Compliant
- Dual Game Port Interface
- MPU-401 MIDI Support
- General Purpose Input/Output Pins
- ISA Plug-and-Play Compatible Register Set
- Intelligent Auto Power Management
- System Management Interrupt
- 2.88MB Super I/O Floppy Disk Controller
  - — Licensed CMOS 765B Floppy Disk Controller
  - — Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - — Supports Two Floppy Drives Directly
  - — Configurable Open Drain/Push-Pull Output Drivers
  - — Supports Vertical Recording Format
  - — 16-Byte Data FIFO
  - — 100% IBM Compatibility
  - — Detects All Overrun and Underrun Conditions
  - — Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - — DMA Enable Logic
  - — Data Rate and Drive Control Registers
  - — 480 Address, Up to Eight IRQ and Three DMA Options
- Enhanced Digital Data Separator
  - — 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - — Programmable Precompensation Modes
- Keyboard Controller
  - — 8042 Software Compatible
  - — 8 Bit Microcomputer
  - — 2k Bytes of Program ROM
  - — 256 Bytes of Data RAM
  - — Four Open Drain Outputs Dedicated for Keyboard/Mouse Interface
  - — Asynchronous Access to Two Data Registers and One Status Register
  - — Supports Interrupt and Polling Access
  - — 8 Bit Counter Timer
  - — Port 92 Support
  - — Fast Gate A20 and KRESET Outputs
- Serial Ports
  - — Two Full Function Serial Ports
  - — High Speed NS16C550A Compatible UARTs with Send/Receive 16-Byte FIFOs
  - — Supports 230k and 460k Baud
  - — Programmable Baud Rate Generator
  - — Modem Control Circuitry
  - — 480 Address and 15 IRQ Options
- Infrared Port
  - — Multiprotocol Infrared Interface
  - — IrDA 1.0 Compliant
  - — SHARP ASK IR
  - — 480 Addresses, Up to 15 IRQ
- Multi-Mode Parallel Port with ChiProtect
  - — Standard Mode IBM PC/XT®, PC/AT, and PS/2 Compatible Bidirectional Parallel Port
  - — Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - — IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - — ChiProtect Circuitry for Protection
  - — 960 Address, Up to 15 IRQ and Three DMA Options
- LPC Interface
  - — Multiplexed Command, Address and Data Bus
  - — Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - — PME Interface
- 100 Pin QFP package, green, lead-free packages also available

ORDER NUMBER(S):

LPC47M102S-MC FOR AMI BIOS IN 100 PIN QFP PACKAGE (LEADED)

LPC47M102S-MS FOR AMI BIOS IN 100 PIN QFP PACKAGE (GREEN, LEAD-FREE)

LPC47M107S-MC FOR PHOENIX BIOS IN 100 PIN QFP PACKAGE (LEADED)

LPC47M107S-MS FOR PHOENIX BIOS IN 100 PIN QFP PACKAGE (GREEN, LEAD-FREE)

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PRODUCT PREVIEW

General Description

The LPC47M10x* is a 3.3V (5V tolerant) PC98/PC99 compliant Super I/O controller. The LPC47M10x implements the LPC interface, a pin reduced ISA bus interface which provides the same or better performance as the ISA/X-bus with a substantial savings in pins used. The LPC47M10x provides fan control through two fan speed control output pins and two fan tachometer input pins. It also provides 37 general purpose input/output (GPIO) pins, a dual game port interface and MPU-401 MIDI support.

The LPC47M10x incorporates a keyboard interface, SMSC's true CMOS 765B floppy disk controller, advanced digital data separator, two 16C550A compatible UARTs, one Multi-Mode parallel port which includes ChiProtect circuitry plus EPP and ECP, on-chip 12 mA AT bus drivers, one floppy direct drive support, and Intelligent Power Management including PME support. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC's patented data separator technology, allowing for ease of testing and use. Both on-chip UARTs are compatible with the NS16C550A. The parallel port is compatible with IBM PC/AT architecture, as well as IEEE 1284 EPP and ECP. The LPC47M10x incorporates sophisticated power control circuitry (PCC) which includes support for keyboard and mouse wake-up events. The PCC supports multiple low power-down modes.

The LPC47M10x supports the ISA Plug-and-Play Standard register set (Version 1.0a) and provides the recommended functionality to support Windows '95. The I/O Address, DMA Channel and hardware IRQ of each logical device in the LPC47M10x may be reprogrammed through the internal configuration registers. There are 480 (960 for Parallel Port) I/O address location options, a Serialized IRQ interface, and three DMA channels.

The LPC47M10x does not require any external filter components and is therefore easy to use and offers lower system costs and reduced board area. The LPC47M10x is software and register compatible with SMSC's proprietary 82077AA core.

*The “x” in the part number is a designator that changes depending upon the particular BIOS used inside the specific chip. “2” denotes AMI Keyboard BIOS and “7” denotes Phoenix 42i Keyboard BIOS.

Block Diagram

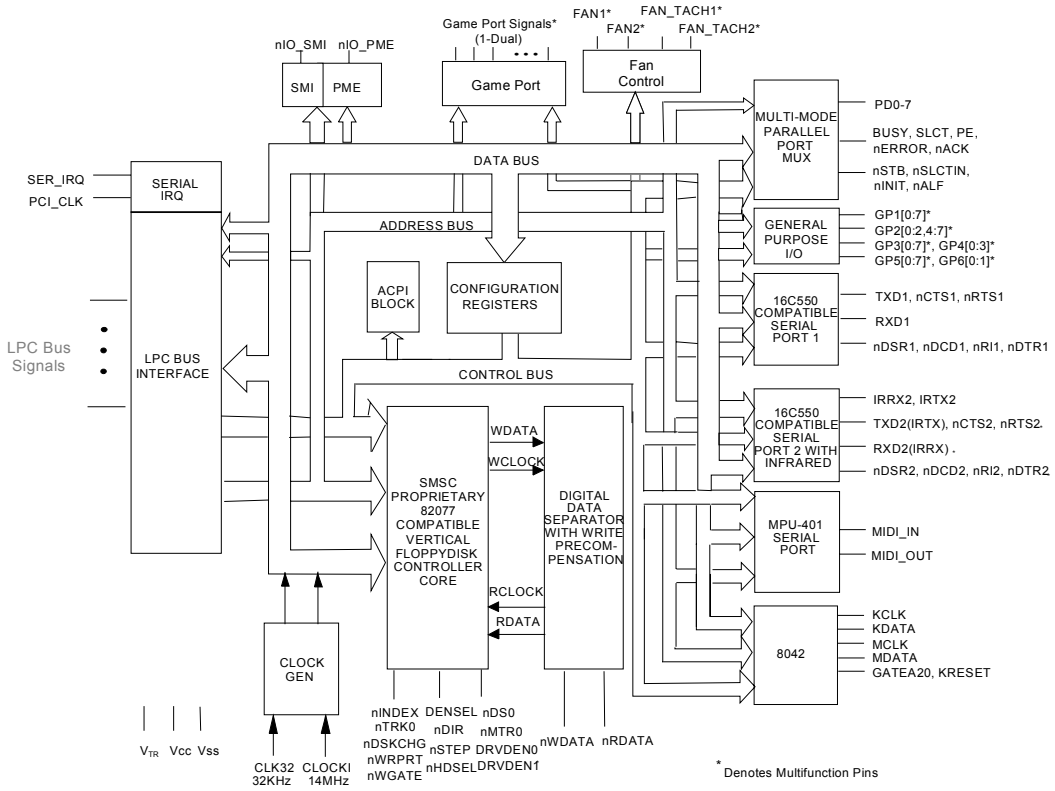

Figure 1 LPC47M10x Block Diagram

PRODUCT PREVIEW

Package Outline

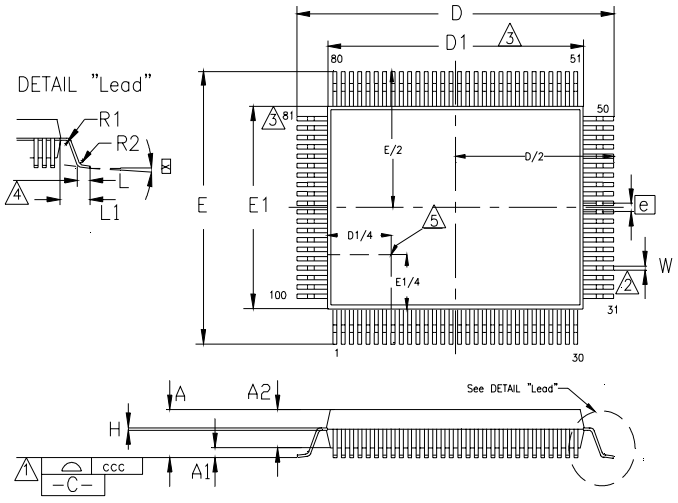

Figure 2 LPC47M10x 100 Pin QFP and 100 Pin QFP (Lead-Free) Package Outline

Table 1 LPC47M10x 100 Pin QFP and 100 Pin QFP (Lead-Free) Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	3.4	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	2.57	~	2.87	Body Thickness
D	23.65	~	24.15	X Span
D/2	11.825	11.95	12.075	$^1/_2$ X Span Measured from Centerline
D1	19.90	~	20.10	X body Size
E	17.65	~	18.15	Y Span
E/2	8.825	8.95	9.075	$^1/_2$ Y Span Measured from Centerline
E1	13.90	~	14.10	Y body Size
H	0.11	~	0.23	Lead Frame Thickness
L	0.73	0.88	1.03	Lead Foot Length
L1	~	1.95	~	Lead Length
e		0.65 Basic		Lead Pitch
q	0^o	~	7^o	Lead Foot Angle
W	0.20	~	0.40	Lead Width
R1	0.10	~	0.25	Lead Shoulder Radius
R2	0.15	~	0.40	Lead Foot Radius
ccc	~	~	0.09	Coplanarity *(Assemblers)*
ccc	~	~	0.10	Coplanarity *(Test House)*

Notes:

1. Controlling Unit: millimeter
2. Tolerance on the position of the leads is ± 0.065 mm maximum
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated