

TMC2250A

Matrix Multiplier

12 x 10 bit, 50 MHz

Features

- Four user-selectable filtering and transformation functions:
 - Triple dot product (3 x 3) matrix multiply
 - Cascadeable 9-tap systolic FIR filter
 - Cascadeable 3 x 3-pixel image convolver
 - Cascadeable 4 x 2-pixel image convolver
- 50 MHz (20ns) pipelined throughput
- 12-bit input and output data, 10-bit coefficients
- 6-bit cascade input and output ports in all filter modes
- Onboard coefficient storage, with three-cycle updating of all nine coefficients

Description

The TMC2250A is a flexible high-performance nine-multiplier array VLSI circuit which can execute a cascadeable 9-tap FIR filter, a cascadeable 4 x 2 or 3 x 3-pixel image convolution, or a 3 x 3 color space conversion. All configurations offer throughput at up to the maximum guaranteed 50 MHz clock rate with 12-bit data and 10-bit coefficients. All inputs and outputs are registered on the rising edges of the clock.

The 3 x 3 matrix multiply or color conversion configuration can perform video standard conversion (YIQ or YUV to RGB, etc.) or three-dimensional perspective translation at real-time video rates.

The 9-tap FIR filter configuration, useful in Video, Telecommunications, and Signal Processing, features a 16-bit cascade input to allow construction of longer filters.

Applications

- Image filtering and manipulation
- Video effects generation
- Video standards conversion and encoding/decoding
- Three-dimensional image manipulation
- Medical image processing
- Edge detection for object recognition
- FIR filtering for communications systems

The cascadeable 3 x 3 and 4 x 2-pixel image convolver functions allow the user to perform numerous image processing functions, including static filters and edge detectors. The 16-bit cascade input port facilitates two-chip 50 MHz cubic convolution (4 x 4-pixel kernel).

The TMC2250A is fabricated in a sub-micron CMOS process and operates at clock speeds of up to 50 MHz over the full commercial (0°C to 70°C) temperature and supply voltage ranges. It is available in 120-pin Plastic Pin Grid Array (PPGA) packages, 120-lead Ceramic Pin Grid Array package (CPGA), 120-lead PQFP to PPGA package (MPGA) and 120-lead Plastic Quad FlatPack (PQFP). All input and output signals are TTL compatible.

Functional Description

The TMC2250A is a nine-multiplier array with the internal bus structure and summing adders needed to implement a 3 x 3 matrix multiplier (triple dot product) a cascadeable 9-tap FIR filter, a 3 x 3-pixel convolver, or a 4 x 2-pixel convolver all in one monolithic circuit. With a 50MHz guaranteed maximum clock rate, this device offers video and imaging system designers a single-chip solution to numerous common image and signal-processing problems.

The three data input ports (A, B, C) accept 12-bit two's complement integer data, which is also the format for the output ports (X, Y, Z) in the matrix multiply mode (Mode 00). In the filter configurations (Modes 01, 10, and 11) the cascade ports assume 12-bit integer, 4-bit fractional two's complement data on both input and output. The coefficient input ports (KA, KB, KC) are always 10-bit two's complement fractional. Table 1 details the bit weighting of the input and output data in all configurations.

Operating Modes

The TMC2250A can implement four different digital filter architectures. Upon selection of the desired function by the user (MODE₁₋₀), the device reconfigures its internal data paths and input and output buses appropriately. The output ports (XC, YC and ZC) are configured in all filter modes a 16-bit Cascade In and Cascade Out ports so that multiple devices can be connected to build larger filters. These modes are described individually below. The I/O function configurations for all four modes are shown in Table 1.

Definitions

The calculations performed by the TMC2250A in each mode are also shown below, utilizing the following notation:

A(1), B(5), C(2), CASIN(3)

Indicates the data word presented to that input port during the specified clock rising edge(x). Applies to all input ports A₁₁₋₀, B₁₁₋₀, C₁₁₋₀, and CASIN₁₅₋₀.

KA1(1), KB3(4)

Indicates coefficient data stored in the specified one of the nine onboard coefficient registers KA1 through KC3, as shown in the block diagram for that mode, input during or before the specified clock rising edge (x).

X(1), Y(4), Z(6), CASOUT (6)

Indicated data available at that output port t_{DO} after that specified clock rising edge (x). Applies to all output ports X₁₁₋₀, Y₁₁₋₀, Z₁₁₋₀, and CASOUT₁₅₋₀.

Numeric Format

Table 2 shows the binary weightings of the input and output ports of the TMC2250A. Although the internal sums of products could grow to 23 bits, in the matrix multiply mode (Mode 00) the outputs X, Y and Z are rounded to yield 12-bit integer words. Thus the output format is identical to the input data format. In the filter configurations (Modes 01, 10, and 11) the cascade output is always half-LSB rounded to 16 bits, specifically 12 integer bits and 4 fractional guard bits, with no overflow "headroom". The user is of course free to half-LSB round the output word to any size less than 16 bits by forcing a 1 into the bit position of the cascade input immediately below the desired LSB. In all modes, bit weighting is easily adjusted if desired by applying the same scaling correction factor to both input and output data words. If the coefficients are rescaled, the relative weightings of the CASIN and CASOUT ports will differ accordingly.

Data Overflow

As shown in Table 2, the TMC2250A's matched input and output data formats accommodate 0dB (unity) gain. Therefore, the user must be aware of input conditions that could lead to numeric overflow. Maximum input data and coefficient word sizes must be taken into account with the specific algorithm performed to ensure that no overflow occurs.

Table 1. Data Port Formatting by Mode

Mode	Inputs						Inputs/Output		Outputs		
	A ₁₁₋₀	B ₁₁₋₀	C ₁₁₋₀	KA ₉₋₀	KB ₉₋₀	KC ₉₋₀	XC ₁₁₋₀	YC ₁₁₋₈	Y ₇₋₄	YC ₃₋₀	ZC ₁₁₋₀
00	A ₁₁₋₀	B ₁₁₋₀	C ₁₁₋₀	KA ₉₋₀	KB ₉₋₀	KC ₉₋₀	X ₁₁₋₀	Y ₁₁₋₈	Y ₇₋₄	Y ₃₋₀	Z ₁₁₋₀
01	A ₁₁₋₀	B ₁₁₋₀	NC	KA ₉₋₀	KB ₉₋₀	KC ₉₋₀	CASIN ₁₅₋₄	CASIN ₃₋₀	NC	CASOUT ₃₋₀	CASOUT ₁₅₋₄
10	A ₁₁₋₀	B ₁₁₋₀	C ₁₁₋₀	KA ₉₋₀	KB ₉₋₀	KC ₉₋₀	CASIN ₁₅₋₄	CASIN ₃₋₀	NC	CASOUT ₃₋₀	CASOUT ₁₅₋₄
11	A ₁₁₋₀	B ₁₁₋₀	NC	KA ₉₋₀	KB ₉₋₀	KC ₉₋₀	CASIN ₁₅₋₄	CASIN ₃₋₀	NC	CASOUT ₃₋₀	CASOUT ₁₅₋₄

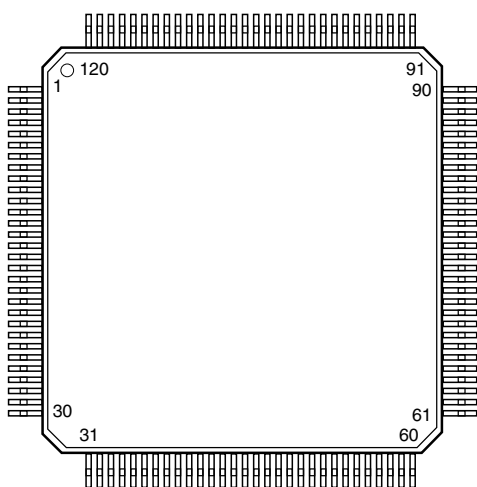
Table 2. Bit Weightings for Input and Output Data Words

Bit Weights	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	
Inputs																							
All Modes Data A, B, C	$-I_{11}$	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	.										
Coefficients KA, KB, KC														$-K_9$	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0
Modes 01, 10, 11 CASIN	$-Cl_{15}$	Cl_{14}	Cl_{13}	Cl_{12}	Cl_{11}	Cl_{10}	Cl_9	Cl_8	Cl_7	Cl_6	Cl_5	Cl_4	.	Cl_3	Cl_2	Cl_1	Cl_0						
Internal Sum	X_{20}	X_{19}	X_{18}	X_{17}	X_{16}	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	.	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	
Outputs																							
Mode 00 X, Y, Z	$-O_{11}$	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	.										
Modes 01, 10, 11 CASOUT	-	CO_1	CO_1	CO_1	CO_1	CO_1	CO	CO	CO	CO	CO	CO_4	.	CO	CO	CO	CO						
	CO_{15}	4	3	2	1	0	9	8	7	6	5			3	2	1	0						

Note: A minus sign indicates a two's complement sign bit.

Pin Assignments

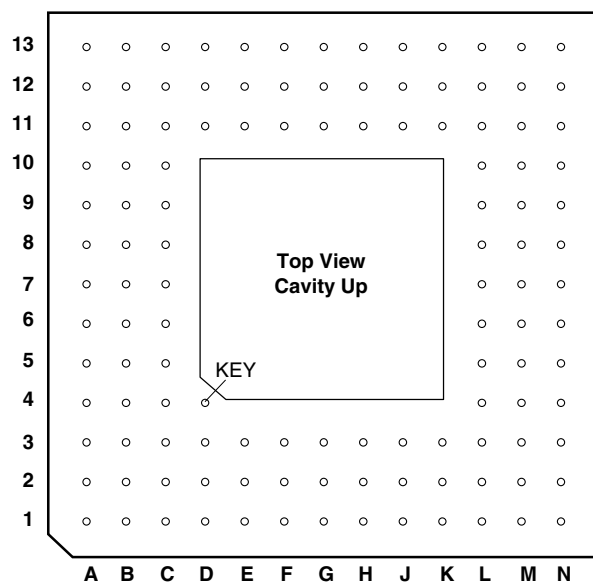
120 Pin Plastic Quad Flat Pack (MQFP), KE Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	XC6	31	ZC6	61	KA1	91	B5
2	XC5	32	ZC7	62	KA2	92	B6
3	XC4	33	ZC8	63	KA3	93	B7
4	XC3	34	GND	64	KA4	94	B8
5	XC2	35	ZC9	65	KA5	95	B9
6	XC1	36	ZC10	66	KA6	96	B10
7	XC0	37	ZC11	67	KA7	97	B11
8	GND	38	KC0	68	KA8	98	C0
9	YC11	39	KC1	69	KA9	99	C1
10	YC10	40	KC2	70	CWE1	100	C2
11	YC9	41	KC3	71	CWE0	101	C3
12	VDD	42	GND	72	GND	102	VDD
13	YC8	43	KC4	73	A0	103	C4
14	Y7	44	KC5	74	A1	104	C5
15	Y6	45	KC6	75	A2	105	C6
16	GND	46	VDD	76	A3	106	GND
17	Y5	47	KC7	77	A4	107	C7
18	Y4	48	KC8	78	A5	108	C8
19	YC0	49	KC9	79	A6	109	C9
20	VDD	50	KB0	80	A7	110	C10
21	YC1	51	KB1	81	A8	111	C11
22	YC2	52	KB2	82	A9	112	MODE1
23	YC3	53	KB3	83	A10	113	MODE0
24	GND	54	KB4	84	A11	114	GND
25	ZC0	55	KB5	85	B0	115	XC11
26	ZC1	56	KB6	86	B1	116	XC10
27	ZC2	57	KB7	87	B2	117	XC9
28	ZC3	58	KB8	88	CLK	118	VDD
29	ZC4	59	KB9	89	B3	119	XC8
30	ZC5	60	KA0	90	B4	120	XC7

Pin Assignments (continued)

120 Pin Plastic Pin Grid Array, H5 Package and 120 Pin Ceramic Pin Grid Array, G1 Package and 120 Pin Plastic Quad Flatpack to 120-Pin Pin Grid Array (MPGA)



Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	XC ₇	C5	GND	G11	A ₃	L10	KB ₈
A2	XC ₉	C6	C ₁₀	G12	A ₂	L11	KA ₁
A3	XC ₁₀	C7	GND	G13	A ₃	L12	KA ₅
A4	MODE ₀	C8	VDD	H1	Y ₄	L13	KA ₆
A5	C ₁₁	C9	C ₀	H2	YC ₀	M1	ZC ₂
A6	C ₈	C10	B ₈	H3	VDD	M2	ZC ₇
A7	C ₇	C11	B ₅	H11	GND	M3	ZC ₉
A8	C ₅	C12	B ₃	H12	A ₀	M4	ZC ₁₁
A9	C ₃	C13	B ₁	H13	A ₁	M5	KC ₂
A10	C ₁	D1	YC ₁₁	J1	YC ₁	M6	KC ₄
A11	B ₁₀	D2	XC ₀	J2	YC ₂	M7	KC ₆
A12	B ₇	D3	XC ₀	J3	GND	M8	KC ₉
A13	B ₄	D11	CLK	J11	KA ₈	M9	KB ₂
B1	XC ₄	D12	B ₀	J12	CWE ₁	M10	KB ₅
B2	XC ₅	D13	A ₁₀	J13	CWE ₀	M11	KB ₉
B3	XC ₈	E1	YC ₉	K1	YC ₃	M12	KA ₂
B4	XC ₁₁	E2	YC ₁₀	K2	ZC ₀	M13	KA ₃
B5	MODE ₁	E3	GND	K3	ZC ₃	N1	ZC ₅
B6	C ₉	E11	A ₁₁	K11	KA ₄	N2	ZC ₈
B7	C ₆	E12	A ₉	K12	KA ₇	N3	ZC ₁₀
B8	C ₄	E13	A ₈	K13	KA ₉	N4	KC ₁
B9	C ₂	F1	Y ₇	L1	ZC ₁	N5	KC ₃
B10	B ₁₁	F2	YC ₈	L2	ZC ₄	N6	KC ₅
B11	B ₉	F3	VDD	L3	ZC ₆	N7	KC ₇
B12	B ₆	F11	A ₇	L4	GND	N8	KC ₈
B13	B ₂	F12	A ₆	L5	KC ₀	N9	KB ₁
C1	XC ₁	F13	A ₅	L6	GND	N10	KB ₃
C2	XC ₂	G1	Y ₅	L7	VDD	N11	KB ₆
C3	XC ₆	G2	Y ₆	L8	KB ₀	N12	KB ₇
C4	VDD	G3	GND	L9	KB ₄	N13	KA ₀

Pin Descriptions

Pin Name	Pin Number		Function	Pin Description
	CPGA/PPGA/MPGA	MQFP		
Power				
V _{DD}	F3, H3, L7, C8, C4	12, 20, 46, 102, 118	Supply Voltage	The TMC2250A operates from a single +5V supply. All pins must be connected.
GND	E3, G3, J3, L4, L6, H11, C7, C5	8, 16, 24, 34, 42, 72, 106, 114	Ground	The TMC2250A operates from a single +5V supply. All pins must be connected.
Clock				
CLK	D11	88	System Clock	The TMC2250A operates from a single system clock input. All timing specifications are referenced to the rising edge of clock.
Controls				
MODE _{1,0}	B4, A4	112, 113	Mode Control	The TMC2250A will switch to the configuration selected by the user (as shown in Table 3) on the next clock. This registered control is usually static; however, should the user wish to switch between modes, the internal pipeline latencies of the device must be taken into account. Valid data will not be available at the outputs in the new configuration until enough clocks in the new mode have passed to flush the internal registers.
CWE _{1,0}	J12, J13	70, 71	Coefficient Write Enable	Data presented to the coefficient input ports (KA, KB, and KC) will update three of the internal coefficient storage registers, as indicated by the simultaneous Coefficient Write Enable select, on the next clock. See Table 4 and the Functional Block Diagram.
Input/Output				
A ₁₁₋₀	E11, D13, E12, E13, F11, F12, F13, G13, G11, G12, H13, H12	84, 83, 82, 81, 80, 79, 78, 77, 76, 75, 74, 73	Data Input A	Data presented to the 12-bit registered data input ports A, B, and C are latched into the multiplier input registers for the currently selected configuration (Table 3). In all modes except Mode 00, new data are internally right-shifted to the next filter tap on each rising edge of CLK.
B ₁₁₋₀	B10, A11, B11, C10, A12, B12, C11, A13, C12, B13, C13, D12	97, 96, 95, 94, 93, 92, 91, 90, 89, 87, 86, 85	Data Input B	
C ₁₁₋₀	A5, C6, B6, A6, A7, B7, A8, B8, A9, B9, A10, C9	111, 110, 109, 108, 107, 105, 104, 103, 101, 100, 99, 98	Data Input C	

Pin Descriptions (continued)

Pin Name	Pin Number		Function	Pin Description
	CPGA/PPGA/MPGA	MQFP		
KA ₉₋₀	K13, J11, K12, L13, L12, K11, M13, M12, L11, N13	69, 68, 67, 66, 65, 64, 63, 62, 61, 60	Coefficient Input A1, A2, A3	Data presented to the 10-bit registered coefficient input ports KA, KB and KC are latched three at a time into the internal coefficient storage register set indicated by the Coefficient Write Enable $CWE_{1,0}$ on the next clock, as shown in Table 4.
KB ₉₋₀	M11, L10, N12, N11, M10, L9, N10, M9, N9, L8	59, 58, 57, 56, 55, 54, 53, 52, 51, 50	Coefficient Input B1, B2, B3	
KC ₉₋₀	M8, N8, N7, M7, N6, M6, N5, M5, N4, L5	49, 48, 47, 45, 44, 43, 41, 40, 39, 38	Coefficient Input B1, B2, B3	
XC ₁₁₋₀	B4, A3, A2, B3, A1, C3, B2, B1, D3, C2, C1, D2	115, 116, 117, 119, 120, 1, 2, 3, 4, 5, 6, 7	CASIN ₁₅₋₄ / Output X	In all modes except Mode 00, the x port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Input port CASIN ₁₅₋₀ . Data presented to this input will be added to the weighted sums of the data words which were presented to the input ports (A, B and C). In the matrix multiply mode, data are available at the 12-bit registered output ports X, Y AND Z t_{DO} after every clock. These ports are reconfigured in the filtering modes as 16-bit Cascade Input and Output ports. CASOUT ₁₅₋₀ In all modes except Mode 00, the Z port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Output port CASOUT ₁₅₋₀ .
YC ₁₁₋₈	D1, E2, E1, F2	9, 10, 11, 13	CASIN ₃₋₀ / Output Y ₁₁₋₀	
Y ₇₋₄	F1, G2, G1, H1	14, 15, 17, 18	Output ₇₋₄ only	
YC ₃₋₀	K1, J2, J1, H2	23, 22, 21, 19	CASOUT ₃₋₀ / Output Y ₃₋₀	
ZC ₁₁₋₀	M4, N3, M3, N2, M2, L3, N1, L2, K3, M1, L1, K2	37, 36, 35, 33, 32, 31, 30, 29, 28, 27, 26, 25	CASOUT ₁₅₋₄ / Output Z ₁₁₋₀	

Notes:

1. The output ports X, Y, Z and CASOUT, and input port CASIN are internally reconfigured by the device as required for each mode of the device. The multiple-function pins have names which are combinations of these titles, as appropriate.
2. The output drivers on pins XC₁₁₋₀ and YC₁₁₋₈ are not necessarily disabled until after the first rising edge of CLK following power-up. If these pins are to be tied to other output drivers, to each other, or to ground or V_{DD} , the user should ensure that a clock pulse arrives within a few seconds of power-up, to avoid bus contention.

Table 3. Configuration Mode Word

MODE _{1,0}	Configuration Mode
00	3 x 3 Matrix Multiply
01	9-Tap One Dimensional FIR
10	3 x 3 -Pixel Convolver
11	4 x 2 -Pixel Convolver

Table 4. Coefficient Write Enable Word

CWE _{1,0}	Coefficient Set Selected
00	Hold all registers
01	Update KA1, KB1, KC1
10	Update KA2, KB2, KC2
11	Update KA3, KB3, KC3

Table 5. Coefficient Input Ports

Input Port	Registers Available
KA	KA1, KA2, KA3
KB	KB1, KB2, KB3
KC	KC1, KC2, KC3

3 x 3 Matrix Multiplier (Mode 00)

This mode utilizes all six input and output ports in the basic configuration to realize a "triple dot product", in which each output is the sum of all three input words in that column

multiplied by the appropriate stored coefficients. The three corresponding sums of products are available at the outputs five clock cycles after the input data are latched, and three new data words half-LSB rounded to 12 bits are then available every clock cycle.

$$X(5)=A(1)KA1(1)+B(1)KB1(1)+C(1)KC1(1)$$

$$Y(5)=A(1)KA2(1)+B(1)KB2(1)+C(1)KC2(1)$$

$$Z(5)=A(1)KA3(1)+B(1)KB3(1)+C(1)KC3(1)$$

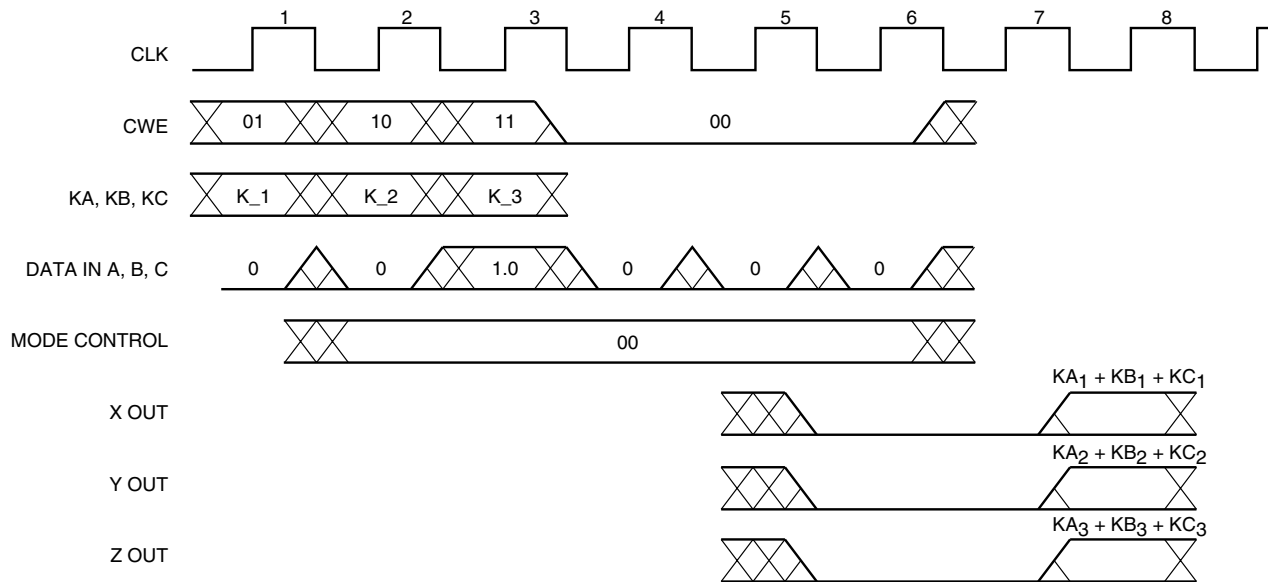


Figure 1. 3 x 3 Matrix Multiplier Impulse Response (Mode 00)

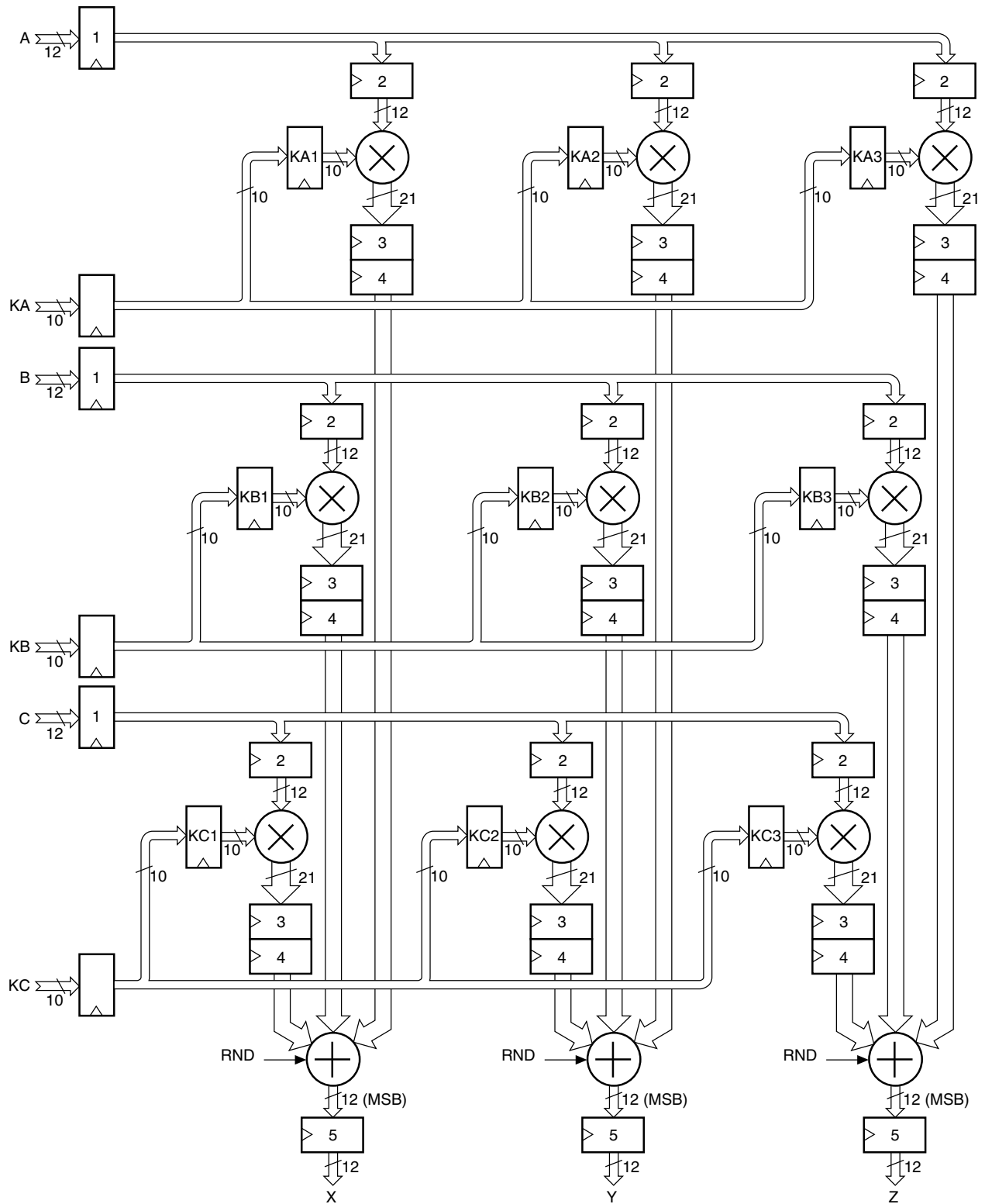


Figure 2. 3 x 3 Matrix Multiplier Configuration (Mode 00)

9-Tap FIR Filter Mode (01)

The architecture for this configuration is shown in Figure 4. The user loads the desired coefficient set, presents input data to ports A and B simultaneously (most applications will wire the A and B inputs together), and receives the resulting 9-sample response, half-LSB rounded to 16 bits, 5 to 13 clock cycles later. A new output data word is available every clock cycle.

The figure shows that the input data are automatically right-shifted by one position through the row of multiplier input registers on every clock in anticipation of a new input data word.

$$\begin{aligned} \text{CASOUT}(13) = & A(9)KA3(9)+A(8)KA2(8)+A(7)KA1(7) \\ & +B(6)KB3(9)+B(5)KB2(8)+B(4)KB1(7) \\ & +B(3)KC3(9)+B(2)KC2(8)+B(1)KC1(7) \\ & +\text{CASIN}(10) \end{aligned}$$

Latency: Impulse in to center of 9-tap response =9 registers.
Cascade In to Cascade Out=4 registers.

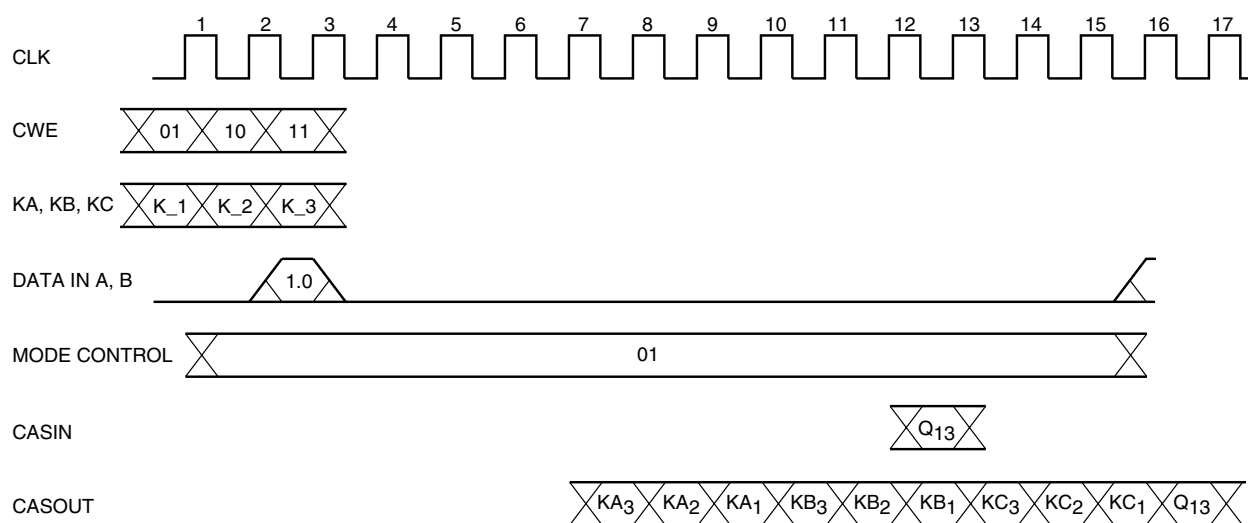


Figure 3. 9-Tap FIR Filter Impulse Response (Mode 01)

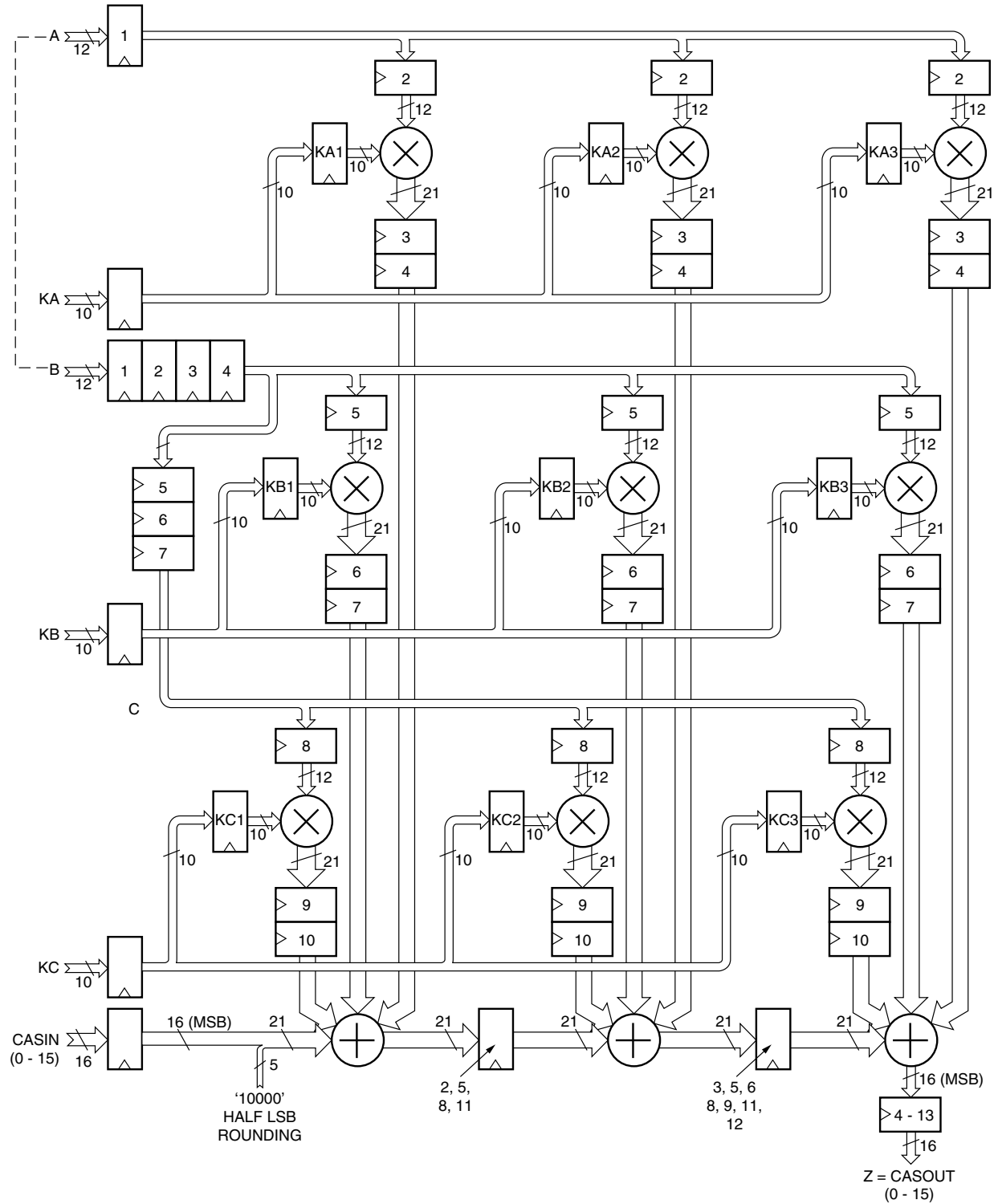


Figure 4. 9-Tap FIR Filter Configuration (Mode 01)

3 x 3 Pixel Convolver (Mode 10)

This filter configuration accepts a 3 pixel-square neighborhood, side-loaded three pixels at a time through input ports A, B and C, and multiplies the 9 most recent pixel values by the coefficient set currently stored in the registers. These products are summed with the data presented to the cascade input, and a new 3-cycle impulse response, rounded to 16 bits, is available at the output port 5 to 7 clocks later, with a new output available on every clock cycle.

The input pixel data are automatically shifted one location to the right through the three rows of multiplier input registers on every clock in anticipation of three new input data words, effectively sliding the convolutional window over one column in an image plane.

$$\text{CASOUT}(7)=$$

$$\begin{aligned} &A(3)KA3(3)+A(2)KA2(2)+A(1)KA1(1) \\ &+B(3)KB3(3)+B(2)KB2(2)+B(1)KB1(1) \\ &+C(3)KC3(3)+C(2)KC2(2)+C(1)KC1(1) \\ &\quad +\text{CASIN}(4) \end{aligned}$$

Latency: Impulse in to center of 3-tap response = 6 registers.
Cascade In to Cascade Out=4 registers.

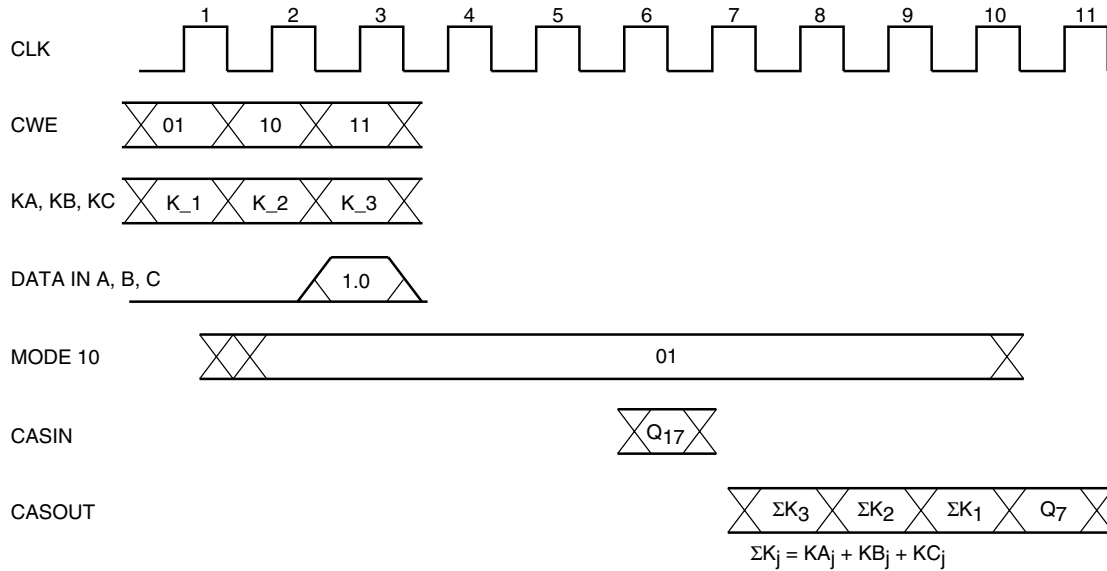


Figure 5. 3 x 3-Pixel Convolver Impulse Response (Mode 10)

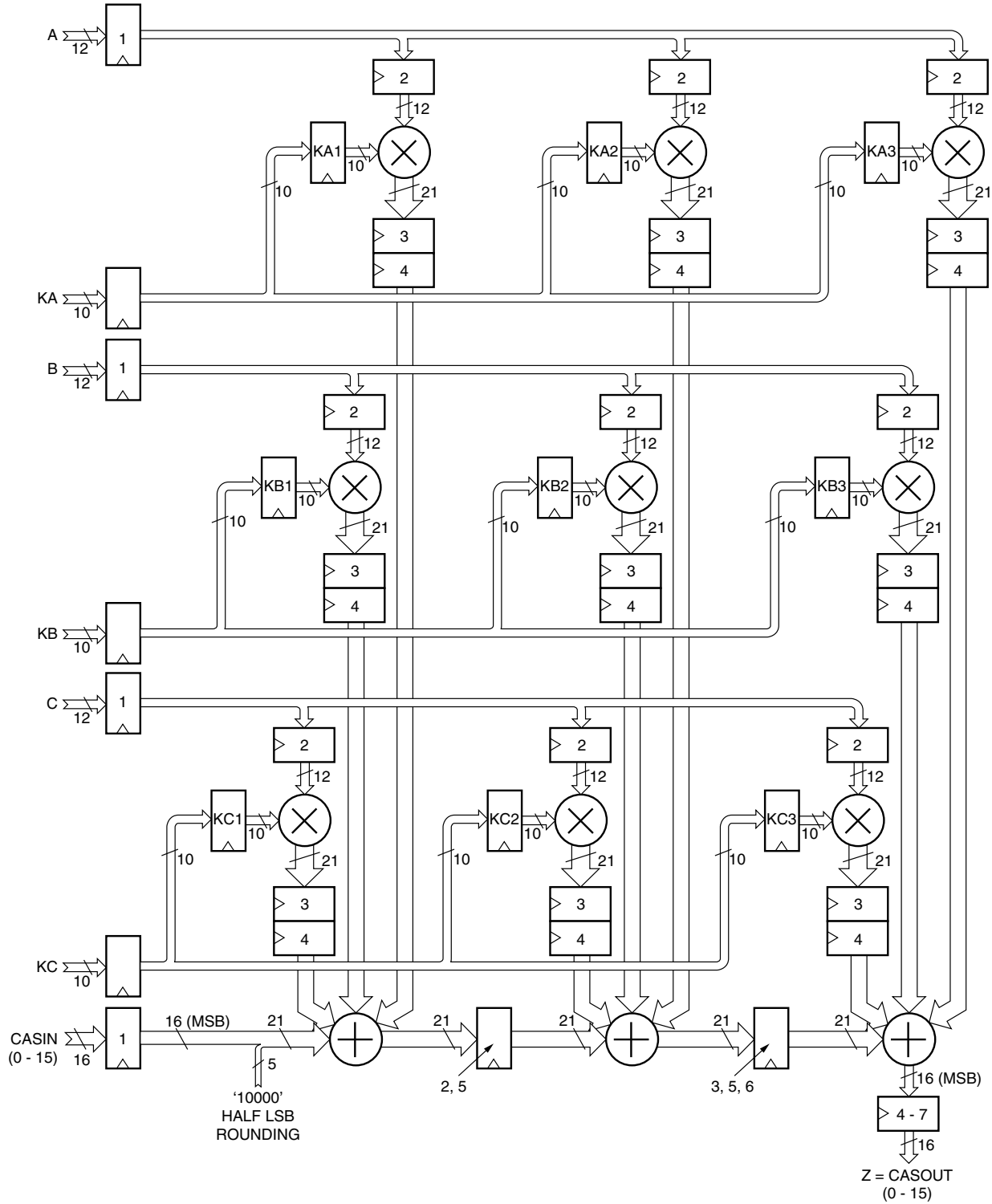


Figure 6. 3 x 3-Pixel Convolver Configuration (Mode 10)

4 x 2-Pixel Cascadeable Convolver (Mode 11)

Similar to Mode 10, the 4 x 2-Pixel convolver allows the use to perform full-speed cubic convolution with only two TMC2250A devices and the TMC2111A Pipeline Delay Register to synchronize the cascade ports (see the Applications Discussion section).

Pixel data are side-loaded into ports A and B, multiplied by the onboard coefficients, summed with the cascade input, and half-LSB rounded to 16 bits. The four-cycle impulse response emerges at the cascade output port 5 to 8 clock cycles later. A new output word is available on every clock cycle. Note that Multiplier KC2 is not used in this mode and that its stored coefficient is ignored.

As shown below, the column of input pixel data is automatically shifted one location to the right through the two rows of multiplier input registers on every clock in anticipation of two new input data words, effectively sliding the convolutional window over one column in an image plane.

$$\begin{aligned} \text{CASOUT}(8) = & \\ & A(4)KA3(4)+A(3)KA2(3)+A(2)KA1(2) \\ & +A(1)KB3(4)+B(4)KB3(4)+B(3)KB2(3) \\ & +B(2)KB1(2)+B(1)KC1(2)+\text{CASIN}(5) \end{aligned}$$

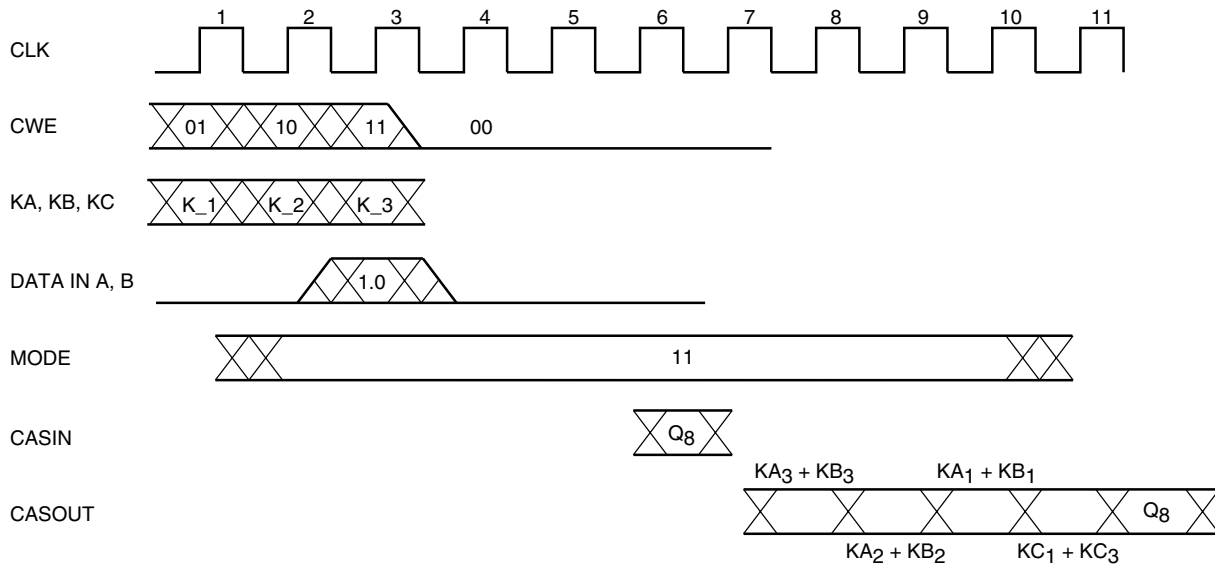


Figure 7. 4 x 2-Pixel Convolver Impulse Response (Mode 11)

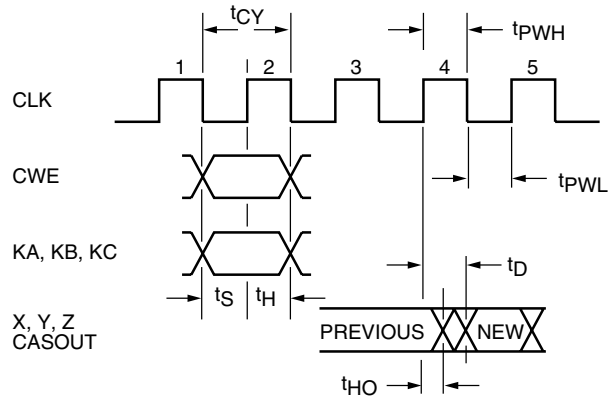


Figure 9. Input/Output Timing Diagram

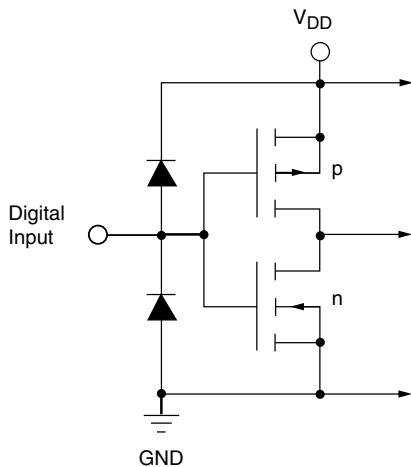


Figure 10. Equivalent Digital Input Circuit

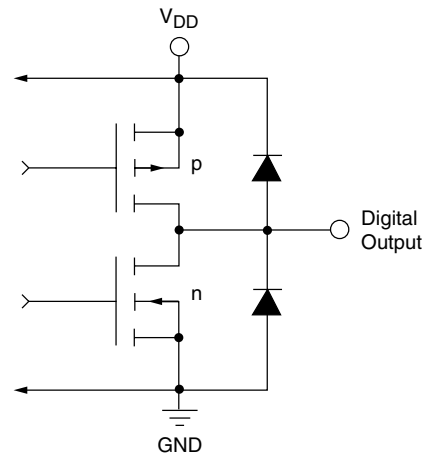


Figure 11. Equivalent Digital Output Circuit

Absolute Maximum Ratings (beyond which the device may be damaged)¹

Parameter	Min	Typ	Max	Unit
Supply Voltage	-0.5		7.0	V
Input Voltage	-0.5		V _{DD} + 0.5	V
Applied Voltage ²	-0.5		V _{DD} + 0.5	V
Externally Forced Current ^{3,4}	-3.0		6.0	mA
Short Circuit Duration (single output in HIGH state to ground)			1	sec
Operating, Ambient Temperature	-20		110	°C
Junction Temperature			140	°C
Storage Temperature	-65		150	°C
Lead Soldering Temperature (10 seconds)			300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Min	Nom	Max	Units
V _{DD}	Power Supply Voltage	4.75	5.0	5.25	V
f _{CLK}	Clock Frequency	TMC2250A		30	MHz
		TMC2250A-2		40	MHz
		TMC2250A-3		50	MHz
t _{PWH}	CLK pulse width, HIGH	6			ns
t _{PWL}	CLK pulse width, LOW	8			ns
t _S	Input Data Setup Time	6			ns
t _H	Input Data Hold Time	2			ns
V _{IH}	Input Voltage, Logic HIGH	2.0			V
V _{IL}	Input Voltage, Logic LOW			0.8	V
I _{OH}	Output Current, Logic HIGH			-2.0	mA
I _{OL}	Output Current, Logic LOW			4.0	mA
T _A	Ambient Temperature, Still Air	0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I _{DD}	Total Power Supply Current	V _{DD} = Max, C _{LOAD} = 25pF, f _{CLK} = Max				
		TMC2250A			125	mA
		TMC2250A-2			140	mA
		TMC2250A-3			155	mA
I _{DDU}	Power Supply Current, Unloaded	V _{DD} = Max, \overline{OE} = HIGH, f _{CLK} = Max				
		TMC2250A			120	mA
		TMC2250A-2			135	mA
		TMC2250A-3			150	mA
I _{DDQ}	Power Supply Current, Quiescent	V _{DD} = Max, CLK = LOW			12	mA
C _{PIN}	I/O Pin Capacitance		5			pF
I _{IH}	Input Current, HIGH ¹	V _{DD} = Max, V _{IN} = V _{DD}			±5	μA
I _{IL}	Input Current, LOW ¹	V _{DD} = Max, V _{IN} = 0 V			±5	μA
I _{OZH}	Hi-Z Output Leakage Current, Output HIGH ²	V _{DD} = Max, V _{IN} = V _{DD}			±10	μA
I _{OZL}	Hi-Z Output Leakage Current, Output LOW ²	V _{DD} = Max, V _{IN} = 0 V			±10	μA
I _{OS}	Short-Circuit Current		-20		-80	mA
V _{OH}	Output Voltage, HIGH	I _{OH} = Max, V _{DD} = Min	2.4			V
V _{OL}	Output Voltage, LOW	I _{OL} = Max, V _{DD} = Min			0.4	V

Notes:

1. Except pins XC₁₁₋₀, YC₁₁₋₈.
2. Pins XC₁₁₋₀, YC₁₁₋₈.

Switching Characteristics

Parameter	Conditions	Min	Typ	Max	Units
t_{DO}	Output Delay Time			15	ns
t_{HO}	Output Hold Time	3			ns

Application Notes

Performing Large-Kernel Pixel Interpolation

The Cascade Input and Output Ports of the TMC2250A allow the user to stack multiple devices to perform larger interpolation kernels with no decrease in pixel throughput. Figure 12 illustrates a basic application utilizing Mode 11 to realize a 4 x 4-pixel kernel, also called Cubic Convolution. This example utilizes the TMC2011A Variable-Length Shift Register to compensate for the internal latency of each TMC2250A. Alternatively, some applications may utilize RAM, FIFO's, or other methods to store multiple-line pixel data. In these cases the user may compensate for latency by simply offsetting the access sequencing of the storage devices.

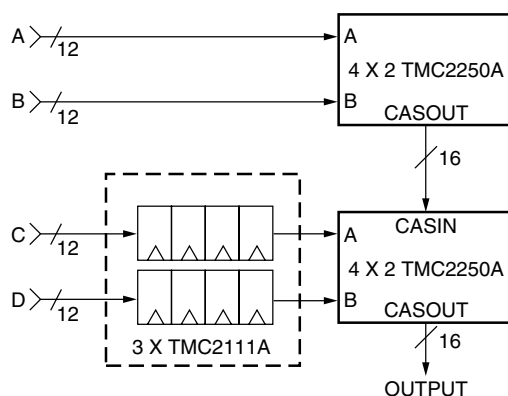


Figure 12. Figure 12. Performing Cubic Convolution with Two TMC2250A's

Related Products

- TMC2301 Image Resampling Sequencer
- TMC2302A Image Manipulation Sequencer
- TMC2249A Video Mixer
- TMC2242B Half-Band Filter

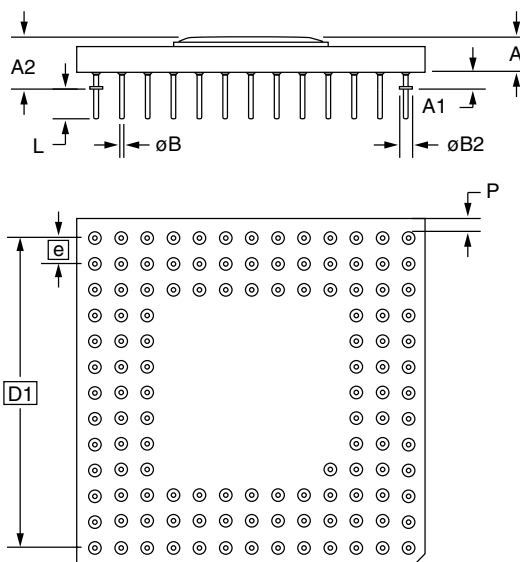
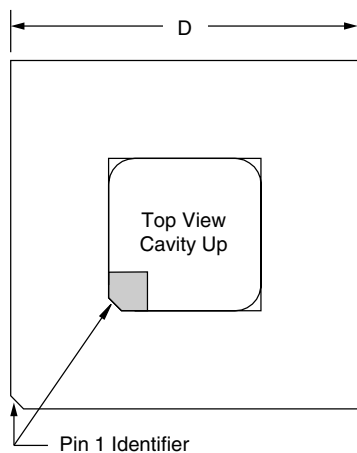
Mechanical Dimensions

120-Lead CPGA Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
ϕB	.016	.020	0.40	0.51	2
$\phi B2$.050 NOM.		1.27 NOM.		2
D	1.340	1.380	33.27	35.05	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
L1	.170	.190	4.31	4.83	
M	13		13		3
N	120		120		4
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



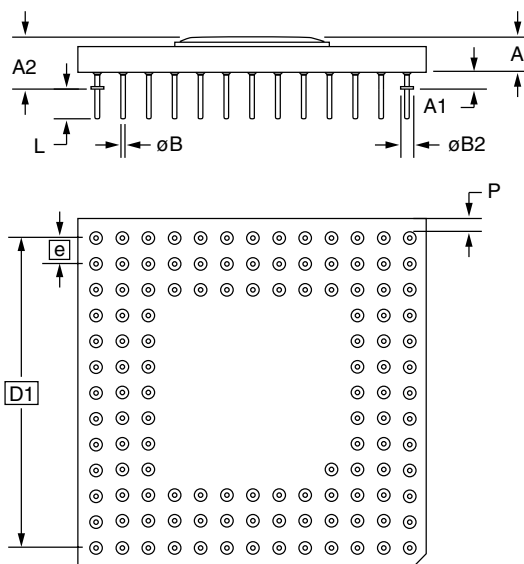
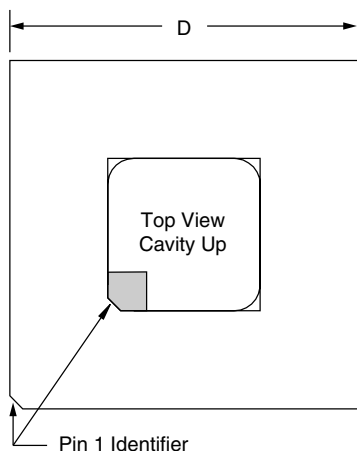
Mechanical Dimensions

120-Lead PPGA Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.340	1.380	33.27	35.05	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
L1	.170	.190	4.31	4.83	
M	13		13		3
N	120		120		4
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



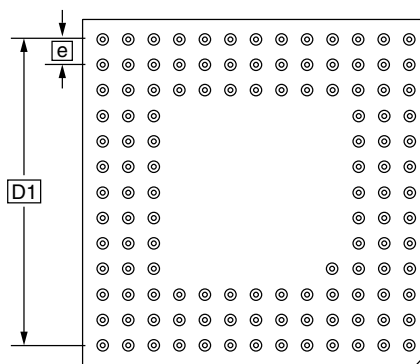
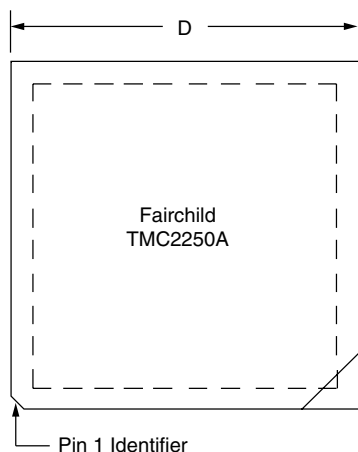
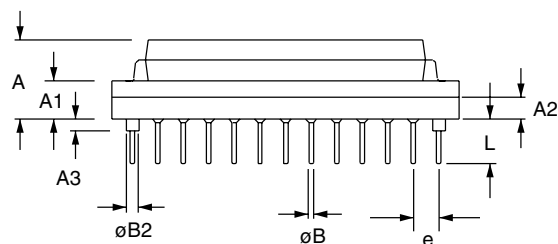
Mechanical Dimensions

120-Lead Metric Quad Flat Package to Pin Grid Array Package (MPGA)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.309	.311	7.85	7.90	
A1	.145	.155	3.68	3.94	
A2	.080	.090	2.03	2.29	
A3	.050 TYP.		1.27 TYP.		
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.355	1.365	34.42	34.67	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.175	.185	4.45	4.70	
M	13		13		3
N	120		120		4

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



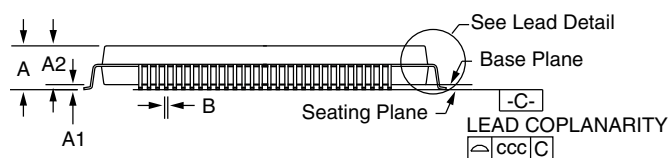
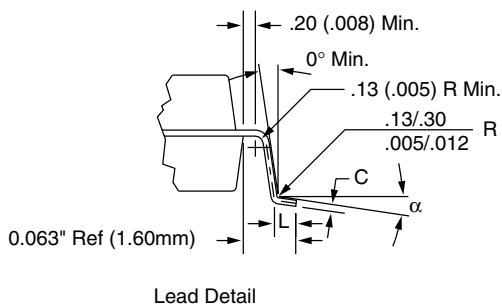
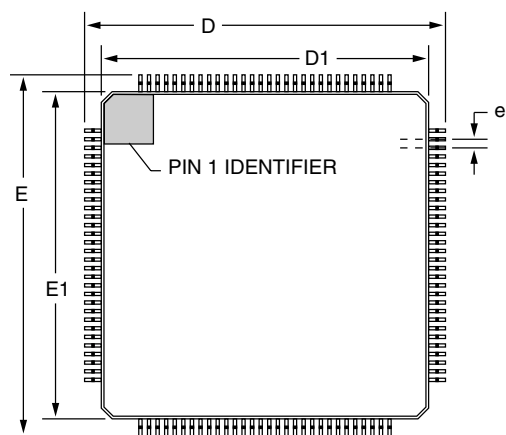
Mechanical Dimensions

120-Lead MQFP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.154	—	3.92	
A1	.010	—	.25	—	
A2	.125	.144	3.17	3.67	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D/E	1.219	1.238	30.95	31.45	
D1/E1	1.098	1.106	27.90	28.10	
e	.0315 BSC		.80 BSC		
L	.026	.037	.65	.95	4
N	120		120		
ND	30		30		
α	0°	7°	0°	7°	
ccc	—	.004	—	.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.



Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2250AG1C	0°C to 70°C	30 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2250AG1C
TMC2250AG1C2	0°C to 70°C	40 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2250AG1C2
TMC2250AG1C3	0°C to 70°C	50 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2250AG1C3
TMC2250AH5C	0°C to 70°C	30 MHz	Commercial	120 Pin Plastic Pin Grid Array	2250AH5C
TMC2250AH5C2	0°C to 70°C	40 MHz	Commercial	120 Pin Plastic Pin Grid Array	2250AH5C2
TMC2250AH5C3	0°C to 70°C	50 MHz	Commercial	120 Pin Plastic Pin Grid Array	2250AH5C3
TMC2250AH6C	0°C to 70°C	30 MHz	Commercial	120 Lead Metric Quad Flatpack to Pin Grid Array	N/A
TMC2250AH6C2	0°C to 70°C	40 MHz	Commercial	120 Lead Metric Quad Flatpack to Pin Grid Array	N/A
TMC2250AH6C3	0°C to 70°C	50 MHz	Commercial	120 Lead Metric Quad Flatpack to Pin Grid Array	N/A
TMC2250AKEC	0°C to 70°C	30 MHz	Commercial	120 Lead Plastic Quad Flatpack	2250AKEC
TMC2250AKEC2	0°C to 70°C	40 MHz	Commercial	120 Lead Plastic Quad Flatpack	2250AKEC2
TMC2250AKEC3	0°C to 70°C	50 MHz	Commercial	120 Lead Plastic Quad Flatpack	2250AKEC3

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.