

**33883**

## H-Bridge Gate Driver IC

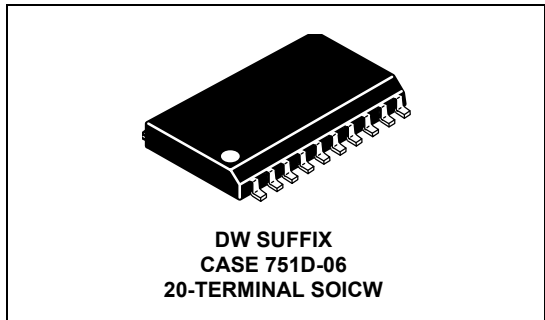
The 33883 is an H-bridge gate driver (also known as a full-bridge predriver) IC with integrated charge pump and independent high- and low-side gate driver channels. The gate driver channels are independently controlled by four separate input terminals, thus allowing the device to be optionally configured as two independent high-side gate drivers and two independent low-side gate drivers. The low-side channels are referenced to ground. The high-side channels are floating.

The gate driver outputs can source and sink up to 1.0 A peak current pulses, permitting large gate-charge MOSFETs to be driven and/or high Pulse Width Modulation (PWM) frequencies to be utilized. A linear regulator is incorporated, providing a 15 V typical gate supply to the low-side gate drivers.

### Features

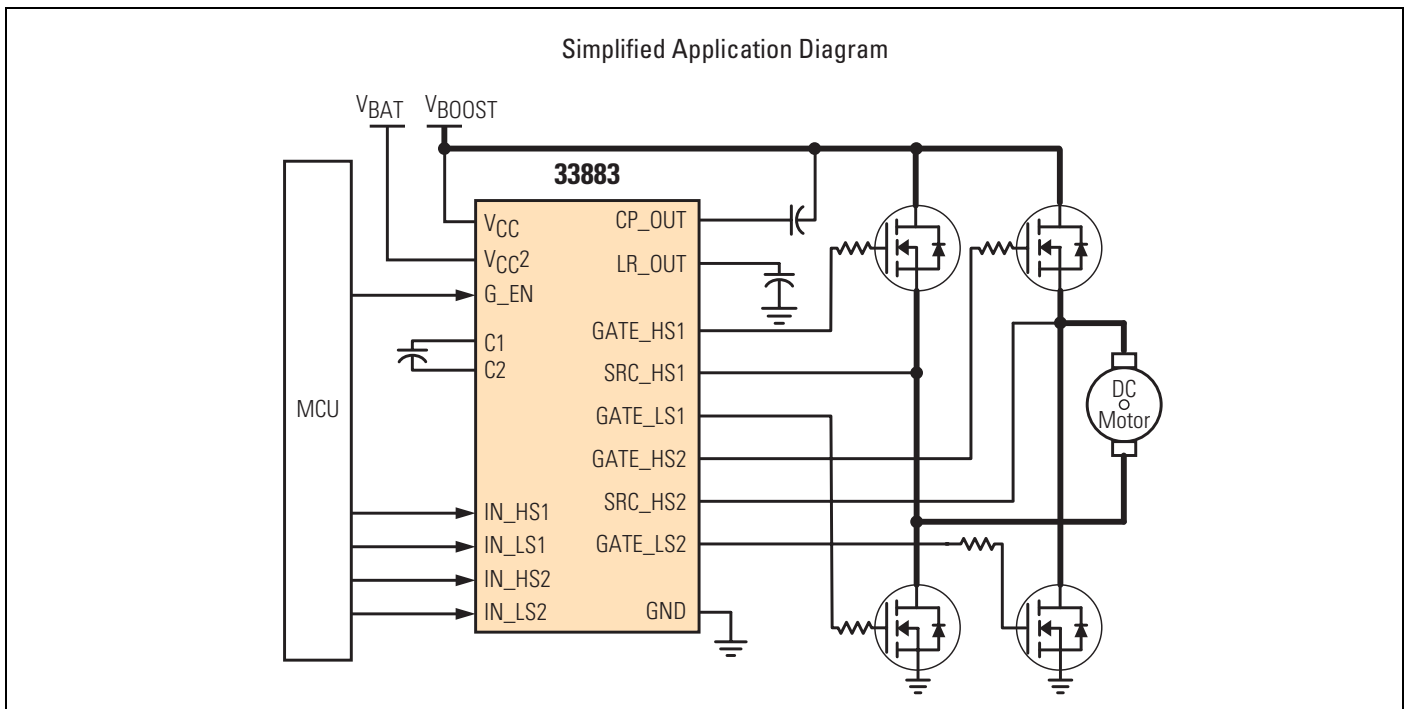
- V<sub>CC</sub> Operating Voltage Range from 5.5 V up to 55 V
- V<sub>CC2</sub> Operating Voltage Range from 5.5 V up to 28 V
- CMOS/LSTTL Compatible I/O
- 1.0 A Peak Gate Driver Current
- Built-In High-Side Charge Pump
- Undervoltage Lockout (UVLO)
- Overvoltage Lockout (OVLO)
- Global Enable with <10 μA Sleep Mode
- Supports PWM up to 100 kHz

**H-BRIDGE GATE DRIVER IC**



### ORDERING INFORMATION

Device	Temperature Range (T <sub>A</sub> )	Package
MC33883DW/R2	-40°C to 125°C	20 SOICW



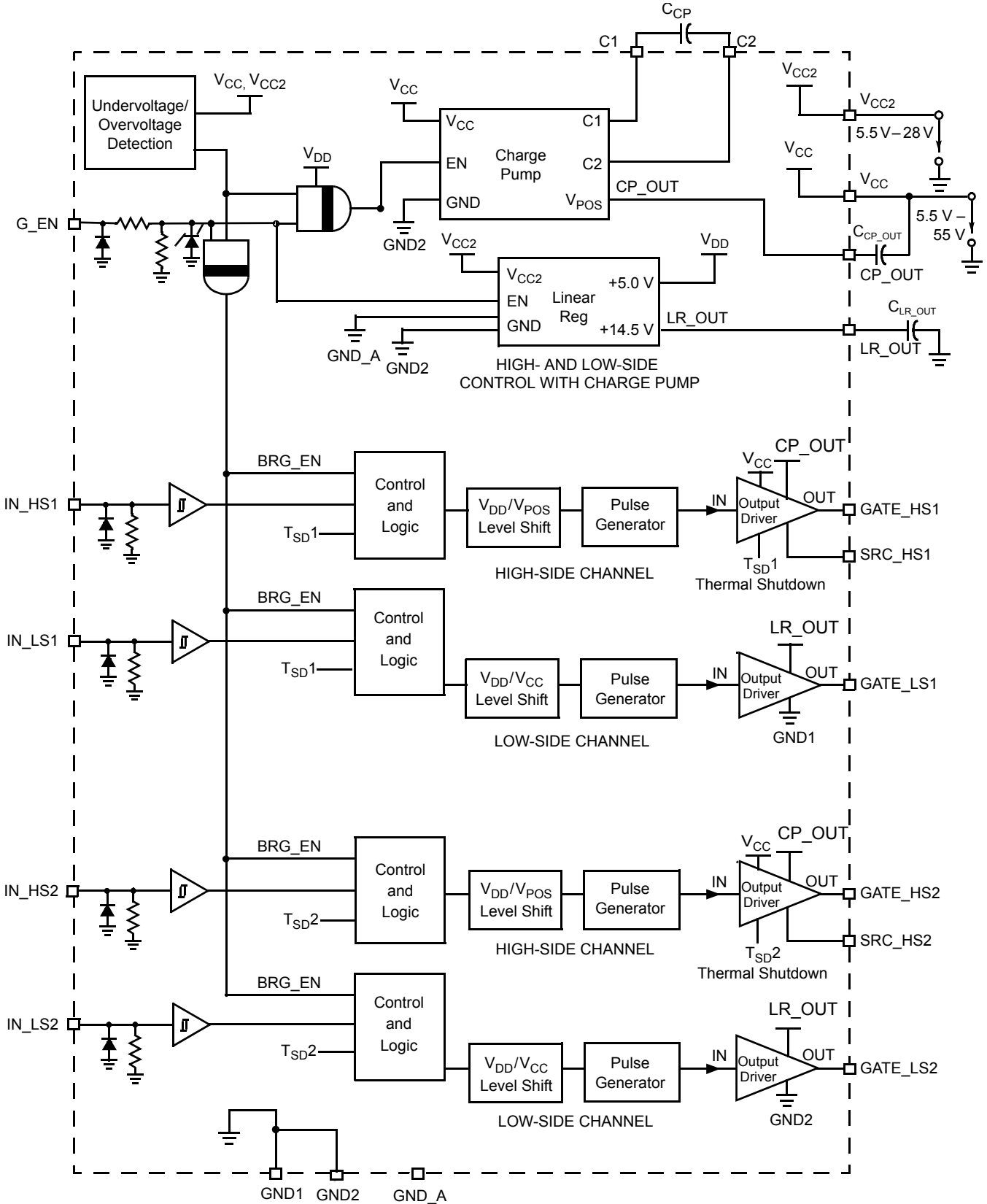
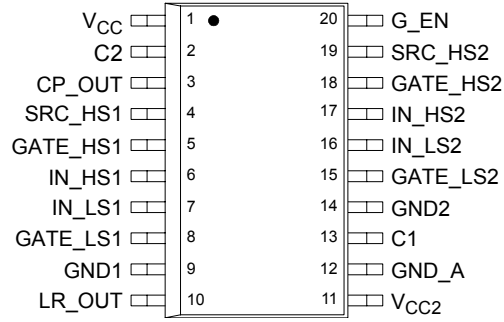


Figure 1. 33883 Simplified Internal Block Diagram



## TERMINAL FUNCTION DESCRIPTION

Terminal	Terminal Name	Formal Name	Definition
1	V <sub>CC</sub>	Supply Voltage 1	Device power supply 1.
2	C2	Charge Pump Capacitor	External capacitor for internal charge pump.
3	CP_OUT	Charge Pump Out	External reservoir capacitor for internal charge pump.
4	SRC_HS1	Source 1 Output High Side	Source of high-side 1 MOSFET
5	GATE_HS1	Gate 1 Output High Side	Gate of high-side 1 MOSFET.
6	IN_HS1	Input High Side 1	Logic input control of high-side 1 gate (i.e., IN_HS1 logic HIGH = GATE_HS1 HIGH).
7	IN_LS1	Input Low Side 1	Logic input control of low-side 1 gate (i.e., IN_LS1 logic HIGH = GATE_LS1 HIGH).
8	GATE_LS1	Gate 1 Output Low Side	Gate of low-side 1 MOSFET.
9	GND1	Ground 1	Device ground 1.
10	LR_OUT	Linear Regulator Output	Output of internal linear regulator.
11	V <sub>CC2</sub>	Supply Voltage 2	Device power supply 2.
12	GND_A	Analog Ground	Device analog ground.
13	C1	Charge Pump Capacitor	External capacitor for internal charge pump.
14	GND2	Ground 2	Device ground 2.
15	GATE_LS2	Gate 2 Output Low Side	Gate of low-side 2 MOSFET.
16	IN_LS2	Input Low Side 2	Logic input control of low-side 2 gate (i.e., IN_LS2 logic HIGH = GATE_LS2 HIGH).
17	IN_HS2	Input High Side 2	Logic input control of high-side 2 gate (i.e., IN_HS2 logic HIGH = GATE_HS2 HIGH).
18	GATE_HS2	Gate 2 Output High Side	Gate of high-side 2 MOSFET.
19	SRC_HS2	Source 2 Output High Side	Source of high-side 2 MOSFET.
20	G_EN	Global Enable	Logic input Enable control of device (i.e., G_EN logic HIGH = Full Operation, G_EN logic LOW = Sleep Mode).

## MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Supply Voltage 1	$V_{CC}$	-0.3 to 65	V
Supply Voltage 2 (Note 1)	$V_{CC2}$	-0.3 to 35	V
Linear Regulator Output Voltage	$V_{LR\_OUT}$	-0.3 to 18	V
High-Side Floating Supply Absolute Voltage	$V_{CP\_OUT}$	-0.3 to 65	V
High-Side Floating Source Voltage	$V_{SRC\_HS}$	-1.0 to 65	V
High-Side Source Current from CP_OUT in Switch ON State	$I_S$	250	mA
High-Side Gate Voltage	$V_{GATE\_HS}$	-0.3 to 65	V
High-Side Gate Source Voltage	$V_{GATE\_HS} - V_{SRC\_HS}$	-0.3 to 20	V
High-Side Floating Supply Gate Voltage	$V_{CP\_OUT} - V_{GATE\_HS}$	-0.3 to 65	V
Low-Side Gate Voltage	$V_{GATE\_LS}$	-0.3 to 17	V
Wake-Up Voltage	$V_{G\_EN}$	-0.3 to 35	V
Logic Input Voltage	$V_{IN}$	-0.3 to 10	V
Charge Pump Capacitor Voltage	$V_{C1}$	-0.3 to $V_{LR\_OUT}$	V
Charge Pump Capacitor Voltage	$V_{C2}$	-0.3 to 65	V
ESD Voltage			V
Human Body Model on All Pins ( $V_{CC}$ and $V_{CC2}$ as Two Power Supplies) (Note 2)	$V_{ESD1}$	±1500	
Machine Model (Note 3)	$V_{ESD2}$	±130	
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation @ 25°C	$P_D$	1.25	W
Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	$T_J$	-40 to 150	°C
Storage Temperature	$T_{STG}$	-65 to 150	°C
Terminal Soldering Temperature (Note 4)	$T_{SOLDER}$	240	°C

### Notes

- $V_{CC2}$  can sustain load dump pulse of 40 V, 400 ms, 2.0  $\Omega$ .
- ESD1 testing is performed in accordance with the Human Body Model ( $C_{ZAP}=100$  pF,  $R_{ZAP}=1500$   $\Omega$ ).
- ESD2 testing is performed in accordance with the Machine Model ( $C_{ZAP}=200$  pF,  $R_{ZAP}=0$   $\Omega$ ).
- Terminal soldering temperature limit is for 10 second maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

## STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions  $V_{CC} = 12\text{ V}$ ,  $V_{CC2} = 12\text{ V}$ ,  $C_{CP} = 33\text{ nF}$ ,  $G_{EN} = 4.5\text{ V}$  unless otherwise noted. Typical values for  $T_A = 25^\circ\text{C}$  and min/max values for  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
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### OPERATING CONDITIONS

Supply Voltage 1 for Output High-Side Driver and Charge Pump	$V_{CC}$	5.5	–	55	V
Supply Voltage 2 for Linear Regulation	$V_{CC2}$	5.5	–	28	V
High-Side Floating Supply Absolute Voltage	$V_{CP\_OUT}$	$V_{CC}+4$	–	$V_{CC}+11$ but < 65	V

### LOGIC

Logic 1 Input Voltage (IN_LS and IN_HS)	$V_{IH}$	2.0	–	10	V
Logic 0 Input Voltage (IN_LS and IN_HS)	$V_{IL}$	–	–	0.8	V
Logic 1 Input Current $V_{IN} = 5.0\text{ V}$	$I_{IN+}$	200	–	1000	$\mu\text{A}$
Wake-Up Input Voltage ( $G_{EN}$ )	$V_{G\_EN}$	4.5	5.0	$V_{CC2}$	V
Wake-Up Input Current ( $G_{EN}$ ) $V_{G\_EN} = 14\text{ V}$	$I_{G\_EN}$	–	200	500	$\mu\text{A}$
Wake-Up Input Current ( $G_{EN}$ ) $V_{G\_EN} = 28\text{ V}$	$I_{G\_EN2}$	–	–	1.5	mA

### LINEAR REGULATOR

Linear Regulator $V_{LR\_OUT}$ @ $V_{CC2}$ from 15 V to 28 V, $I_{LOAD}$ from 0 mA to 20 mA $V_{LR\_OUT}$ @ $I_{LOAD} = 20\text{ mA}$ $V_{LR\_OUT}$ @ $I_{LOAD} = 20\text{ mA}$ , $V_{CC2} = 5.5\text{ V}$ , $V_{CC} = 5.5\text{ V}$	$V_{LR\_OUT}$	12.5 $V_{CC2}-1.5$ 4.0	– – –	16.5 – –	V
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### CHARGE PUMP

Charge Pump Output Voltage, Reference to $V_{CC}$ $V_{CC} = 12\text{ V}$ , $I_{LOAD} = 0\text{ mA}$ , $C_{CP\_OUT} = 1.0\text{ }\mu\text{F}$ $V_{CC} = 12\text{ V}$ , $I_{LOAD} = 7.0\text{ mA}$ , $C_{CP\_OUT} = 1.0\text{ }\mu\text{F}$ $V_{CC2} = V_{CC} = 5.5\text{ V}$ , $I_{LOAD} = 0\text{ mA}$ , $C_{CP\_OUT} = 1.0\text{ }\mu\text{F}$ $V_{CC2} = V_{CC} = 5.5\text{ V}$ , $I_{LOAD} = 7.0\text{ mA}$ , $C_{CP\_OUT} = 1.0\text{ }\mu\text{F}$ $V_{CC} = 55\text{ V}$ , $I_{LOAD} = 0\text{ mA}$ , $C_{CP\_OUT} = 1.0\text{ }\mu\text{F}$ $V_{CC} = 55\text{ V}$ , $I_{LOAD} = 7.0\text{ mA}$ , $C_{CP\_OUT} = 1.0\text{ }\mu\text{F}$	$V_{CP\_OUT}$	7.5 7.0 2.3 1.8 7.5 7.0	– – – – – –	– – – – – –	V
Peak Current Through Pin C1 Under Rapidly Changing $V_{CC}$ Voltages (see <a href="#">Figure 11</a> , page 14)	$I_{C1}$	-2.0	–	2.0	A
Minimum Peak Voltage at Pin C1 Under Rapidly Changing $V_{CC}$ Voltages (see <a href="#">Figure 11</a> , page 14)	$V_{C1min}$	-1.5	–	–	V

## STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions  $V_{CC} = 12\text{ V}$ ,  $V_{CC2} = 12\text{ V}$ ,  $C_{CP} = 33\text{ nF}$ ,  $G_{EN} = 4.5\text{ V}$  unless otherwise noted. Typical values for  $T_A = 25^\circ\text{C}$  and min/max values for  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>SUPPLY VOLTAGE</b>					
Quiescent $V_{CC}$ Supply Current $V_{G\_EN} = 0\text{ V}$ and $V_{CC} = 55\text{ V}$ $V_{G\_EN} = 0\text{ V}$ and $V_{CC} = 12\text{ V}$	$I_{V_{CC}sleep}$	–	–	10 10	$\mu\text{A}$
Operating $V_{CC}$ Supply Current (Note 5) $V_{CC} = 55\text{ V}$ and $V_{CC2} = 28\text{ V}$ $V_{CC} = 12\text{ V}$ and $V_{CC2} = 12\text{ V}$	$I_{V_{CC}op}$	–	2.2 0.7	–	mA
Additional Operating $V_{CC}$ Supply Current for Each Logic Input Terminal Active $V_{CC} = 55\text{ V}$ and $V_{CC2} = 28\text{ V}$ (Note 6)	$I_{V_{CC}log}$	–	–	5.0	mA
Quiescent $V_{CC2}$ Supply Current $V_{G\_EN} = 0\text{ V}$ and $V_{CC} = 12\text{ V}$ $V_{G\_EN} = 0\text{ V}$ and $V_{CC} = 28\text{ V}$	$I_{V_{CC2}sleep}$	–	–	5.0 5.0	$\mu\text{A}$
Operating $V_{CC2}$ Supply Current (Note 5) $V_{CC} = 55\text{ V}$ and $V_{CC2} = 28\text{ V}$ $V_{CC} = 12\text{ V}$ and $V_{CC2} = 12\text{ V}$	$I_{V_{CC2}op}$	–	–	12 9.0	mA
Additional Operating $V_{CC2}$ Supply Current for Each Logic Input Terminal Active $V_{CC} = 55\text{ V}$ and $V_{CC2} = 28\text{ V}$ (Note 6)	$I_{V_{CC2}log}$	–	–	5.0	mA
Undervoltage Shutdown $V_{CC}$	UV	4.0	5.0	5.5	V
Undervoltage Shutdown $V_{CC2}$ (Note 7)	UV2	4.0	5.0	5.5	V
Overvoltage Shutdown $V_{CC}$	OV	57	61	65	V
Overvoltage Shutdown $V_{CC2}$	OV2	29.5	31	35	V

## OUTPUT

Output Sink Resistance (Turned Off) $I_{discharge\ LSS} = 50\text{ mA}$ , $V_{SRC\_HS} = 0\text{ V}$ (Note 8)	$R_{DS}$	–	–	22	$\Omega$
Output Source Resistance (Turned On) $I_{charge\ HSS} = 50\text{ mA}$ , $V_{CP\_OUT} = 20\text{ V}$ (Note 8)	$R_{DS}$	–	–	22	$\Omega$
Charge Current of the External High-Side MOSFET Through GATE_HSn Terminal (Note 8)	$I_{charge\ HSS}$	–	100	200	mA
Maximum Voltage ( $V_{GATE\_HS} - V_{SRC\_HS}$ ) INH = Logic 1, $I_{Smax} = 5.0\text{ mA}$	$V_{max}$	–	–	18	V

### Notes

5. Logic input terminal inactive (high impedance).
6. High-frequency PWM-ing ( $\gg 20\text{ kHz}$ ) of the logic inputs will result in greater power dissipation within the device. Care must be taken to remain within the package power handling rating.
7. The device may exhibit predictable behavior between 4.0 V and 5.5 V.
8. See [Figure 3](#), page 10, for a description of charge current.

## DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions  $V_{CC} = 12\text{ V}$ ,  $V_{CC2} = 12\text{ V}$ ,  $C_{CP} = 33\text{ nF}$ ,  $G\_EN = 4.5\text{ V}$  unless otherwise noted. Typical values for  $T_A = 25^\circ\text{C}$  and min/max values for  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
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### TIMING CHARACTERISTICS

Propagation Delay High Side and Low Side $C_{LOAD} = 5.0\text{ nF}$ , Between 50% Input to 50% Output (Note 9) (see <a href="#">Figure 2</a> )	$t_{pd}$	–	200	300	ns
Turn-On Rise Time $C_{LOAD} = 5.0\text{ nF}$ , 10% to 90% (Note 9), (Note 10) (see <a href="#">Figure 2</a> )	$t_r$	–	80	180	ns
Turn-Off Fall Time $C_{LOAD} = 5.0\text{ nF}$ , 10% to 90% (Note 9), (Note 10) (see <a href="#">Figure 2</a> )	$t_f$	–	80	180	ns

#### Notes

- $C_{LOAD}$  corresponds to a capacitor between GATE\_HS and SRC\_HS for the high side and between GATE\_LS and ground for low side.
- Rise time is given by time needed to change the gate from 1.0 V to 10 V (vice versa for fall time).

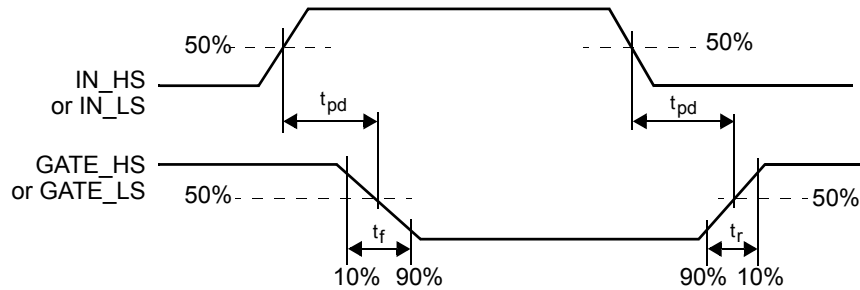


Figure 2. Timing Characteristics

## SYSTEM/APPLICATION INFORMATION

### INTRODUCTION

The 33883 is an H-bridge gate driver (or full-bridge predriver) with integrated charge pump and independent high- and low-side driver channels. It has the capability to drive large gate-

charge MOSFETs and supports high PWM frequency. In sleep mode its supply current is very low.

### FUNCTIONAL TERMINAL DESCRIPTION

#### Supply Voltage Terminals ( $V_{CC}$ and $V_{CC2}$ )

The  $V_{CC}$  and  $V_{CC2}$  terminals are the power supply inputs to the device.  $V_{CC}$  is used for the output high-side drivers and the charge pump.  $V_{CC2}$  is used for the linear regulation. They can be connected together or independent with different voltage values. The device can operate with  $V_{CC}$  up to 55 V and  $V_{CC2}$  up to 28 V.

The  $V_{CC}$  and  $V_{CC2}$  terminals have undervoltage (UV) and overvoltage (OV) shutdown. If one of the supply voltage drops below the undervoltage threshold or rises above the overvoltage threshold, the gate outputs are switched LOW in order to switch off the external MOSFETs. When the supply returns to a level that is above the UV threshold or below the OV threshold, the device resumes normal operation according to the established condition of the input terminals.

#### Input High- and Low-Side Terminals ( $IN_{HSn}$ and $IN_{LSn}$ )

The  $IN_{HSn}$  and  $IN_{LSn}$  terminals are input control terminals used to control the gate outputs. These terminals are 5.0 V CMOS-compatible inputs with hysteresis.  $IN_{HSn}$  and  $IN_{LSn}$  independently control  $GATE_{HSn}$  and  $GATE_{LSn}$ , respectively.

During wake-up, the logic is supplied from the  $G_{EN}$  terminal. There is no internal circuit to prevent the external high-side and low-side MOSFETs from conducting at the same time.

#### Source Output High-Side Terminals ( $SRC_{HSn}$ )

The  $SRC_{HSn}$  terminals are the sources of the external high-side MOSFETs. The external high-side MOSFETs are controlled using the  $IN_{HSn}$  inputs.

#### Gate High- and Low-Side Terminals ( $GATE_{HSn}$ and $GATE_{LSn}$ )

The  $GATE_{HSn}$  and  $GATE_{LSn}$  terminals are the gates of the external high- and low-side MOSFETs. The external high- and low-side MOSFETs are controlled using the  $IN_{HSn}$  and  $IN_{LSn}$  inputs.

#### $G_{EN}$ Terminal

The  $G_{EN}$  terminal is used to place the device in a sleep mode. When the  $G_{EN}$  terminal voltage is a logic LOW state, the device is in sleep mode. The device is enabled and fully operational when the  $G_{EN}$  terminal voltage is logic HIGH, typically 5.0 V.

#### Charge Pump Out Terminal ( $CP_{OUT}$ )

The  $CP_{OUT}$  terminal is used to connect an external reservoir capacitor for the charge pump.

#### Charge Pump Capacitor Terminals ( $C1$ and $C2$ )

The  $C1$  and  $C2$  terminals are used to connect an external capacitor for the charge pump.

#### Linear Regulator Output Terminal ( $LR_{OUT}$ )

The  $LR_{OUT}$  terminal is the output of the internal regulator. It is used to connect an external capacitor.

#### Ground Terminals ( $GNDn$ and $GND_A$ )

These terminals are the ground terminals of the device. They should be connected together with a very low impedance connection.



**Table 1. Functional Truth Table**

Conditions	G_EN	IN_HS <sub>n</sub>	IN_LS <sub>n</sub>	Gate_HS <sub>n</sub>	Gate_LS <sub>n</sub>	Comments
Sleep	0	x	x	0	0	Device is in Sleep mode. The gates are at low state.
Normal	1	1	1	1	1	Normal mode. The gates are controlled independently.
Normal	1	0	0	0	0	Normal mode. The gates are controlled independently.
Undervoltage	1	x	x	0	0	The device is currently in fault mode. The gates are at low state. Once the fault is removed, the 33883 recovers its normal mode.
Overvoltage	1	x	x	0	0	The device is currently in fault mode. The gates are at low state. Once the fault is removed, the 33883 recovers its normal mode.
Overtemperature on High-Side Gate Driver	1	1	x	0	x	The device is currently in fault mode. The high-side gate is at low state. Once the fault is removed, the 33883 recovers its normal mode.
Overtemperature on Low-Side Gate Driver	1	x	1	x	0	The device is currently in fault mode. The low-side gate is at low state. Once the fault is removed, the 33883 recovers its normal mode.

x = Don't care.

## DEVICE DESCRIPTION

### Driver Characteristics

Figure 3 represents the external circuit of the high-side gate driver. In the schematic, HSS represents the switch that is used to charge the external high-side MOSFET through the GATE\_HS terminal. LSS represents the switch that is used to discharge the external high-side MOSFET through the GATE\_HS terminal. The same schematic can be applied to the external low-side MOSFET driver simply by replacing terminal CP\_OUT with terminal LR\_OUT, terminal GATE\_HS with terminal GATE\_LS, and terminal SRC\_HS with GND.

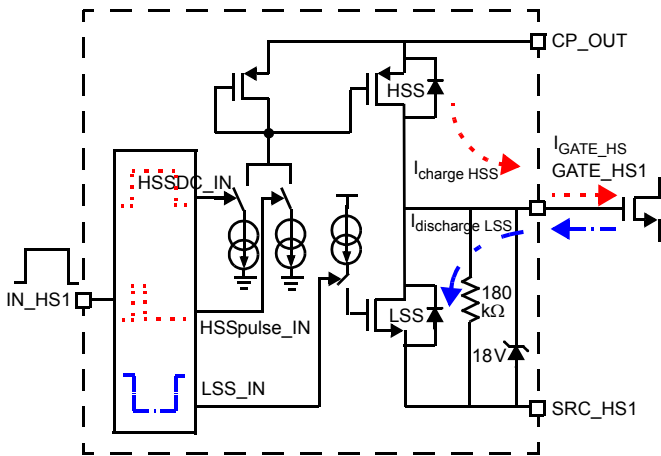
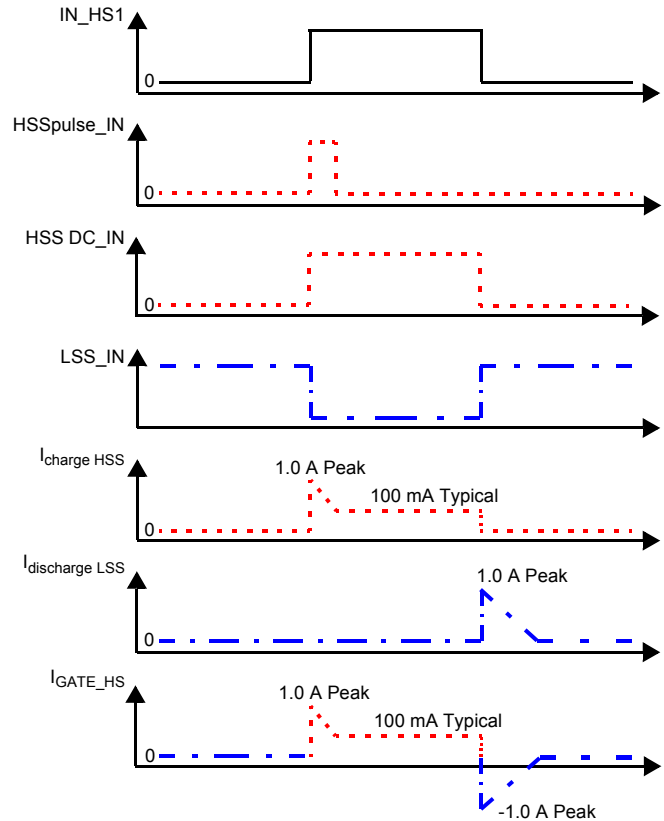


Figure 3. High-Side Gate Driver Functional Schematic

The different voltages and current of the high-side gate driver are illustrated in Figure 4. The output driver sources a peak current of up to 1.0 A for 200 ns to turn on the gate. After 200 ns, 100 mA is continuously provided to maintain the gate charged. The output driver sinks a high current to turn off the gate. This current can be up to 1.0 A peak for a 100 nF load.



**Note** GATE\_HS is loaded with a 100 nF capacitor in the chronograms. A smaller load will give lower peak and DC charge or discharge currents.

Figure 4. High-Side Gate Driver Chronograms

## APPLICATION REQUIREMENTS

### Turn-On

For turn-on, the current required to charge the gate source capacitor  $C_{iss}$  in the specified time can be calculated as follows:

$$I_P = Q_g/t_r = 80 \text{ nC}/80 \text{ ns} \approx 1.0 \text{ A}$$

Where  $Q_g$  is power MOSFET gate charge and  $t_r$  is peak current for rise time.

### Turn-Off

The peak current for turn-off can be obtained in the same way as for turn-on, with the exception that peak current for fall time,  $t_f$ , is substituted for  $t_r$ :

$$I_P = Q_g/t_f = 80 \text{ nC}/80 \text{ ns} \approx 1.0 \text{ A}$$

In addition to the dynamic current required to turn off on the MOSFET, various application-related switching scenarios must be considered. These scenarios are presented in [Figure 5](#). In order to withstand high  $dV/dt$  spikes, a low resistive path between gate and source is implemented during the OFF-state.

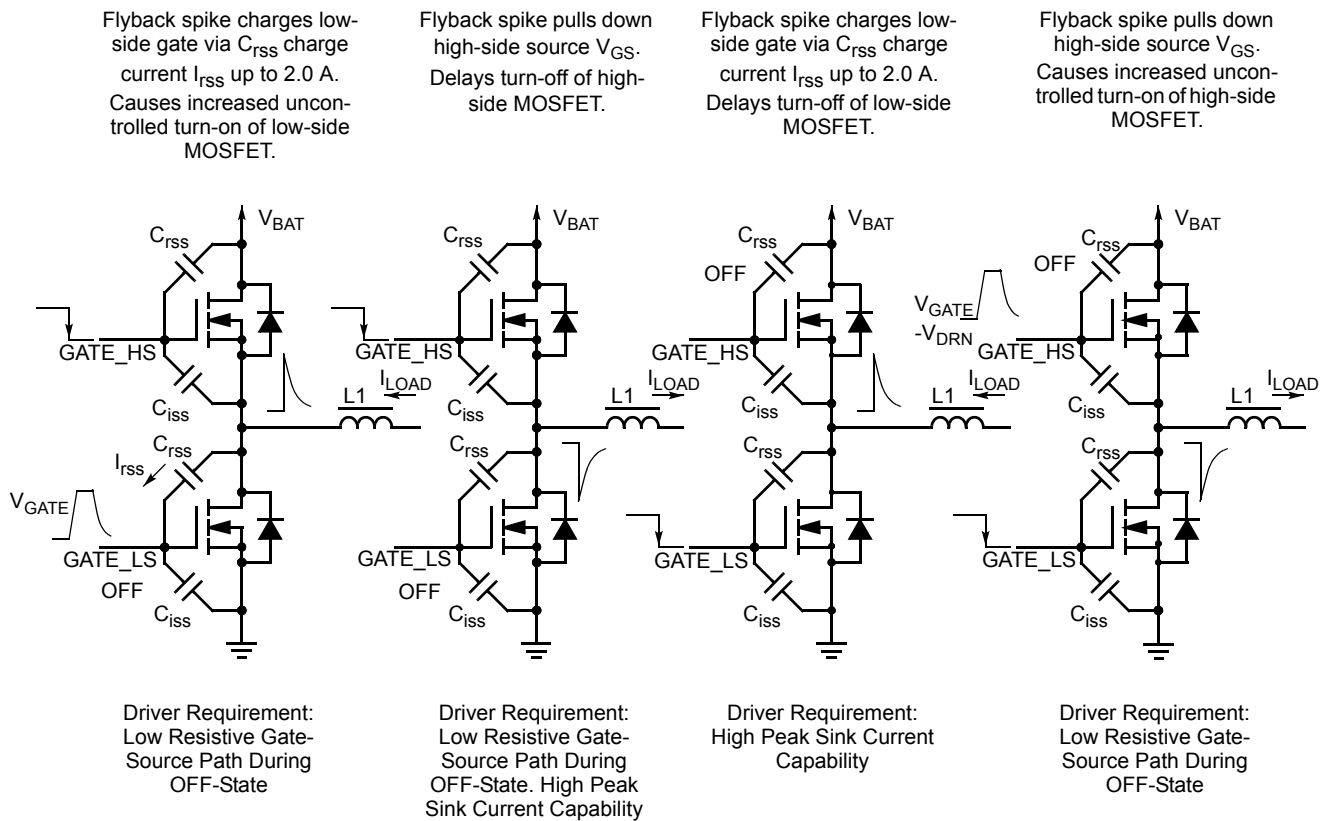


Figure 5. OFF-State Driver Requirement

## Low-Drop Linear Regulator

The low-drop linear regulator is supplied by  $V_{CC2}$ . If  $V_{CC2}$  exceeds 15.0 V, the output is limited to 14.5 V (typical).

The low-drop linear regulator provides the 5.0 V for the logic section of the driver, the  $V_{gs\_ls}$  buffered at LR\_OUT, and the +14.5 V for the charge pump, which generates the CP\_OUT. The low-drop linear regulator provides 4.0 mA average current per driver stage.

In case of the full bridge, that means approximately 16 mA — 8.0 mA for the high side and 8.0 mA for the low side.

**Note:** The average current required to switch a gate with a frequency of 100 kHz is:

$$I_{CP} = Q_g * f_{PWM} = 80 \text{ nC} * 100 \text{ kHz} = 8.0 \text{ mA}$$

In a full-bridge application only one high side and one low side switches on or off at the same time.

## Charge Pump

The charge pump generates the high-side driver supply voltage (CP\_OUT), buffered at  $C_{CP\_OUT}$ . Figure 6 shows the charge pump basic circuit without load.

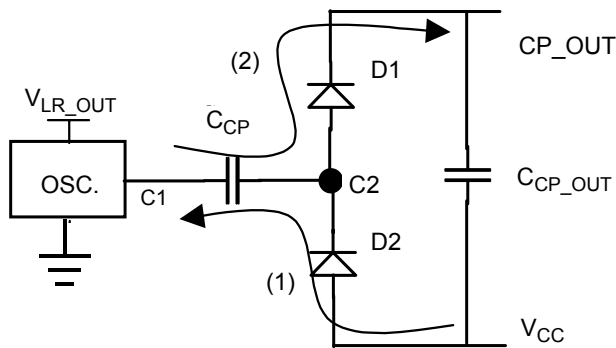


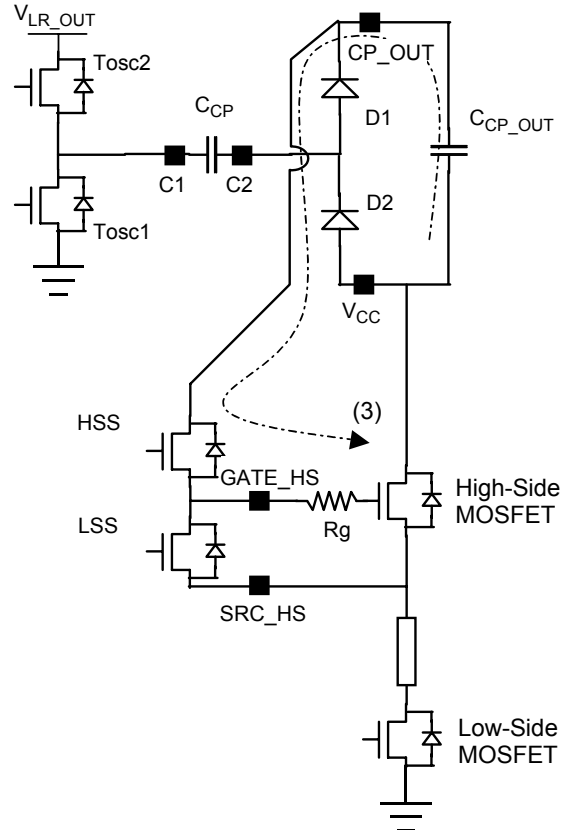
Figure 6. Charge Pump Basic Circuit

When the oscillator is in low state [(1) in Figure 6],  $C_{CP}$  is charged through D2 until its voltage reaches  $V_{CC} - V_{D2}$ . When the oscillator is in high state (2),  $C_{CP}$  is discharged through D1 in  $C_{CP\_OUT}$ , and final voltage of the charge pump,  $V_{CP\_OUT}$ , is  $V_{CC} + V_{LR\_OUT} - 2V_D$ . The frequency of the 33883 oscillator is about 330 kHz.

## External Capacitors Choice

External capacitors on the charge pump and on the linear regulator are necessary to supply high peak current absorbed during switching.

Figure 7 represents a simplified circuitry of the high-side gate driver. Transistors Tosc1 and Tosc2 are the oscillator-switching MOSFETs. When Tosc1 is on, the oscillator is at low level. When Tosc2 is on, the oscillator is at high level. The capacitor  $C_{CP\_OUT}$  provides peak current to the high-side MOSFET through HSS during turn-on (3).

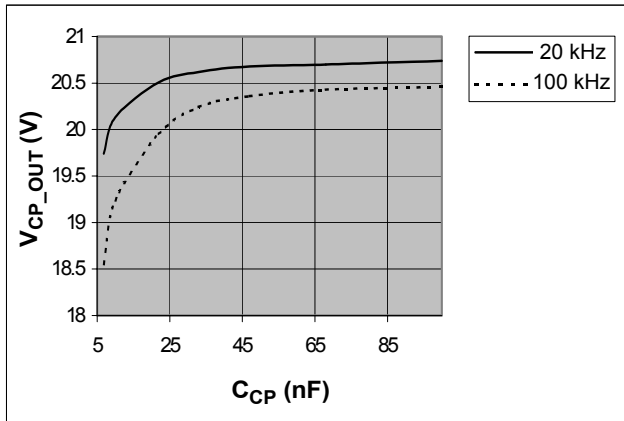


■ Terminals

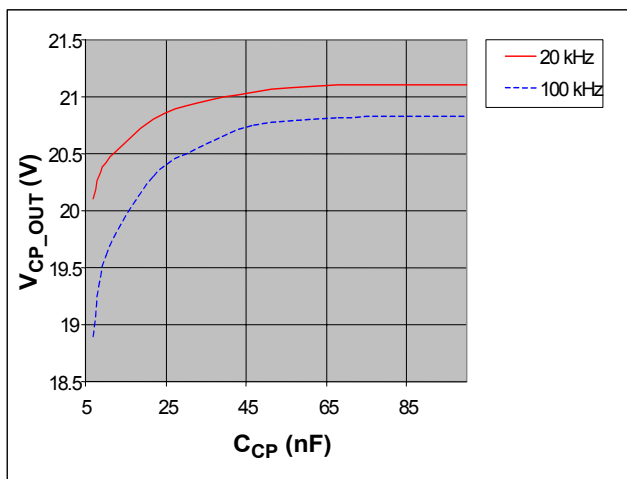
Figure 7. High-Side Gate Driver

## C<sub>CP</sub>

C<sub>CP</sub> choice depends on power MOSFET characteristics and the working switching frequency. Figure 8 contains two diagrams that depict the influence of C<sub>CP</sub> value on V<sub>CP\_OUT</sub> average voltage level. The diagrams represent two different frequencies for two power MOSFETs, MTP60N06HD and MPT36N06V.



MTP60N06HD (Q<sub>g</sub> = 50 nC)



MTP36N06V (Q<sub>g</sub> = 40 nC)

Figure 8. V<sub>CP\_OUT</sub> Versus C<sub>CP</sub>

The smaller the C<sub>CP</sub> value is, the smaller the V<sub>CP\_OUT</sub> value is. Moreover, for the same C<sub>CP</sub> value, when the switching frequency increases, the average V<sub>CP\_OUT</sub> level decreases. For most of the applications, a typical value of 33 nF is recommended.

## C<sub>CP\_OUT</sub>

Figure 9 depicts the simplified C<sub>CP\_OUT</sub> current and voltage waveforms. f<sub>PWM</sub> is the working switching frequency.

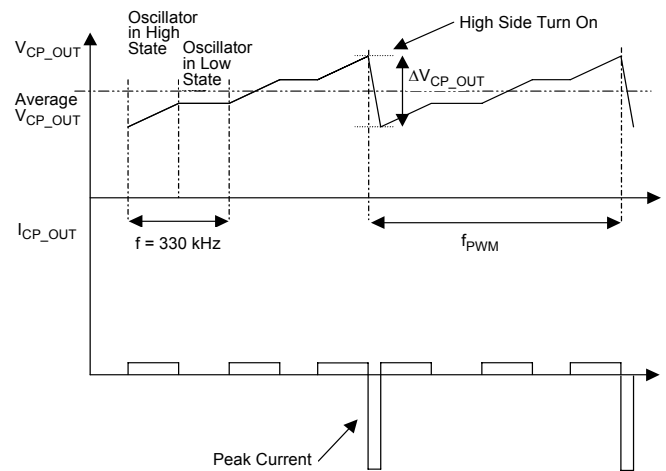


Figure 9. Simplified C<sub>CP\_OUT</sub> Current and Voltage Waveforms

As shown above, at high-side MOSFET turn-on V<sub>CP\_OUT</sub> voltage decreases. This decrease can be calculated according to the C<sub>CP\_OUT</sub> value as follows:

$$\Delta V_{CP\_OUT} = \frac{Q_g}{C_{CP\_OUT}}$$

Where Q<sub>g</sub> is power MOSFET gate charge.

## C<sub>LR\_OUT</sub>

C<sub>LR\_OUT</sub> provides peak current needed by the low-side MOSFET turn-on. V<sub>LR\_OUT</sub> decrease is as follows:

$$\Delta V_{LR\_OUT} = \frac{Q_g}{C_{LR\_OUT}}$$

## Typical Values of Capacitors

In most working cases the following typical values are recommended for a well-performing charge pump:

C<sub>CP</sub> = 33 nF, C<sub>CP\_OUT</sub> = 470 nF, and C<sub>LR\_OUT</sub> = 470 nF

These values give a typical 100 mV voltage ripple on V<sub>CP\_OUT</sub> and V<sub>LR\_OUT</sub> with Q<sub>g</sub> = 50 nC.

## Protection

### Gate Protection

The low-side driver is supplied from the built-in low-drop regulator. The high-side driver is supplied from the internal charge pump buffered at CP\_OUT.

The low-side gate is protected by the internal linear regulator, which ensures that  $V_{GATE\_LS}$  does not exceed the maximum  $V_{GS}$ . Especially when working with the charge pump, the voltage at CP\_OUT can be up to 65 V. The high-side gate is clamped internally in order to avoid a  $V_{GS}$  exceeding 18 V.

Gate protection does not include a flyback voltage clamp that protects the driver and the external MOSFET from a flyback voltage that can occur when driving inductive load. This flyback voltage can reach high negative voltage values and needs to be clamped externally, as shown in [Figure 10](#).

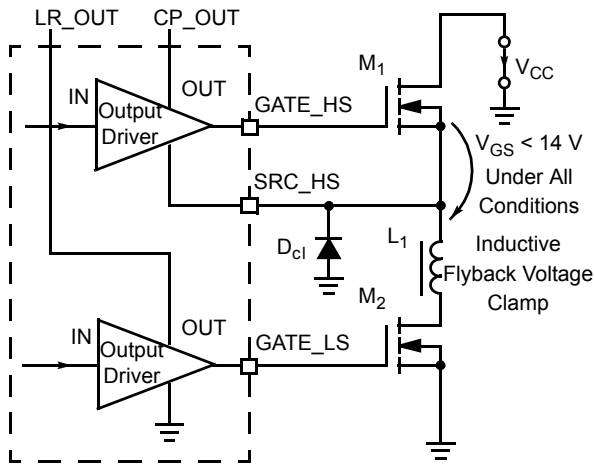


Figure 10. Gate Protection and Flyback Voltage Clamp

### Load Dump and Reverse Battery

$V_{CC}$  and  $V_{CC2}$  can sustain a load dump pulse of 40 V and double battery of 24 V. Protection against reverse polarity is ensured by the external power MOSFET with the free-wheeling diodes forming a conducting pass from ground to  $V_{CC}$ . Additional protection is not provided within the circuit. To protect the circuit an external diode can be put on the battery line. It is not recommended putting the diode on the ground line.

### Temperature Protection

There is temperature shutdown protection per each half-bridge. Temperature shutdown protects the circuitry against temperature damage by switching off the output drivers. Its typical value is 175°C with an hysteresis of 15°C.

### dV/dt at $V_{CC}$

$V_{CC}$  voltage must be higher than (SRC\_HS voltage minus a diode drop voltage) to avoid perturbation of the high-side driver.

In some applications a large dV/dt at terminal C2 owing to sudden changes at  $V_{CC}$  can cause large peak currents flowing through terminal C1, as shown in [Figure 11](#).

For positive transitions at terminal C2, the absolute value of the minimum peak current,  $I_{C1min}$ , is specified at 2.0 A for a  $t_{C1min}$  duration of 600 ns.

For negative transitions at terminal C2, the maximum peak current,  $I_{C1max}$ , is specified at 2.0 A for a  $t_{C1max}$  duration of 600 ns. Current sourced by terminal C1 during a large dV/dt will result in a negative voltage at terminal C1 ([Figure 11](#)). The minimum peak voltage  $V_{C1min}$  is specified at -1.5 V for a duration of  $t_{C1max} = 600$  ns. A series resistor with the charge pump capacitor (Ccp) capacitor can be added in order to limit the surge current.

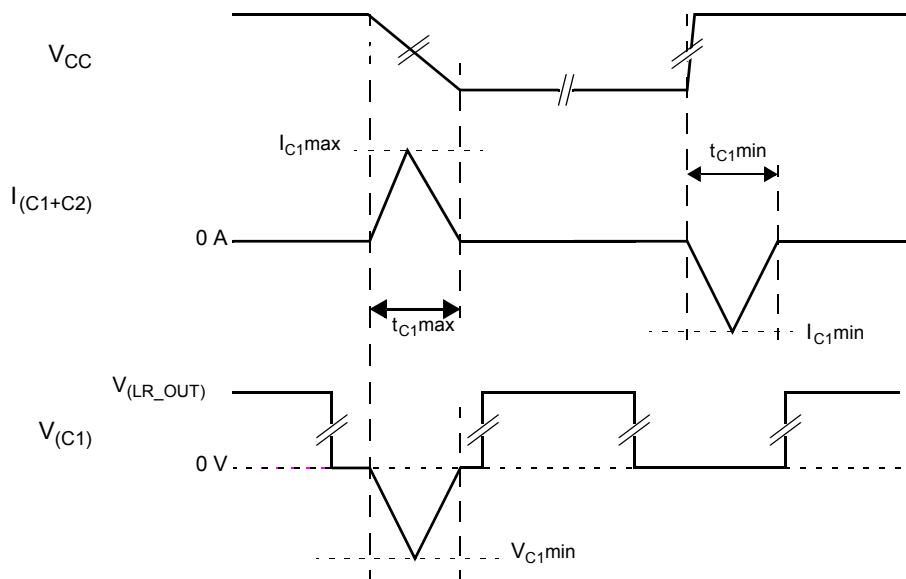


Figure 11. Limits of C1 Current and Voltage with Large Values of dV/dt

In the case of rapidly changing  $V_{CC}$  voltages, the large  $dV/dt$  may result in perturbations of the high-side driver, thereby forcing the driver into an OFF state. The addition of capacitors C3 and C4, as shown in Figure 12, reduces the  $dV/dt$  of the source line, consequently reducing driver perturbation. Typical values for R3/R4 and C3/C4 are 10  $\Omega$  and 10 nF, respectively.

## $dV/dt$ at $V_{CC2}$

When the external high-side MOSFET is on, in case of rapid negative change of  $V_{CC2}$  the voltage ( $V_{GATE\_HS} - V_{SRC\_HS}$ ) can be higher than the specified 18 V. In this case a resistance in the SRC line is necessary to limit the current to 5.0 mA max. It will protect the internal zener placed between GATE\_HS and SRC terminals.

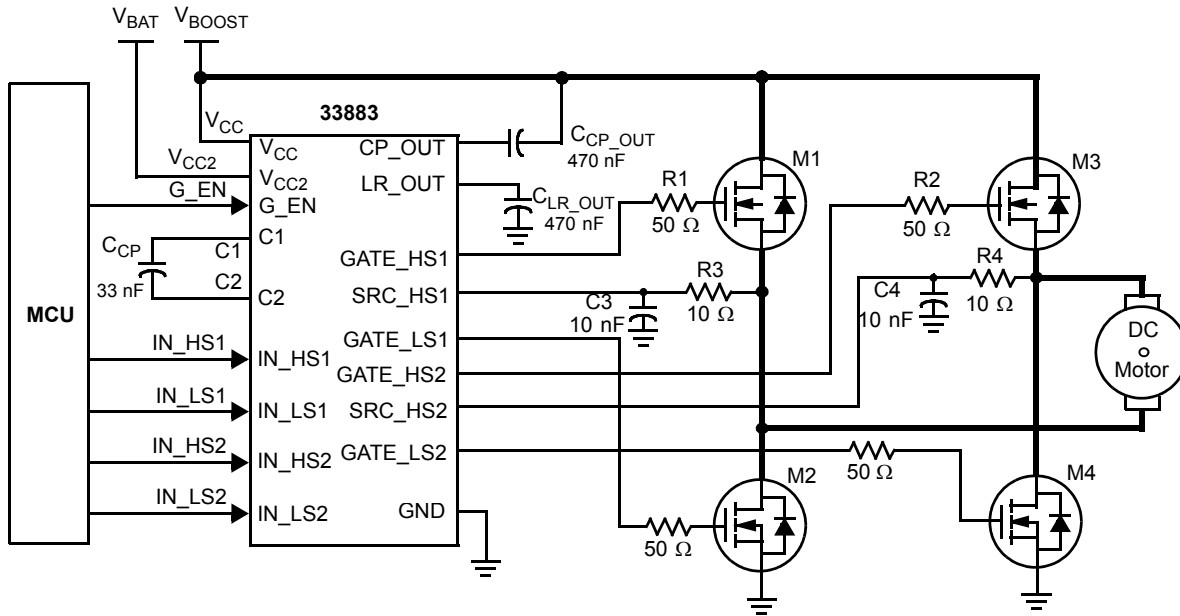
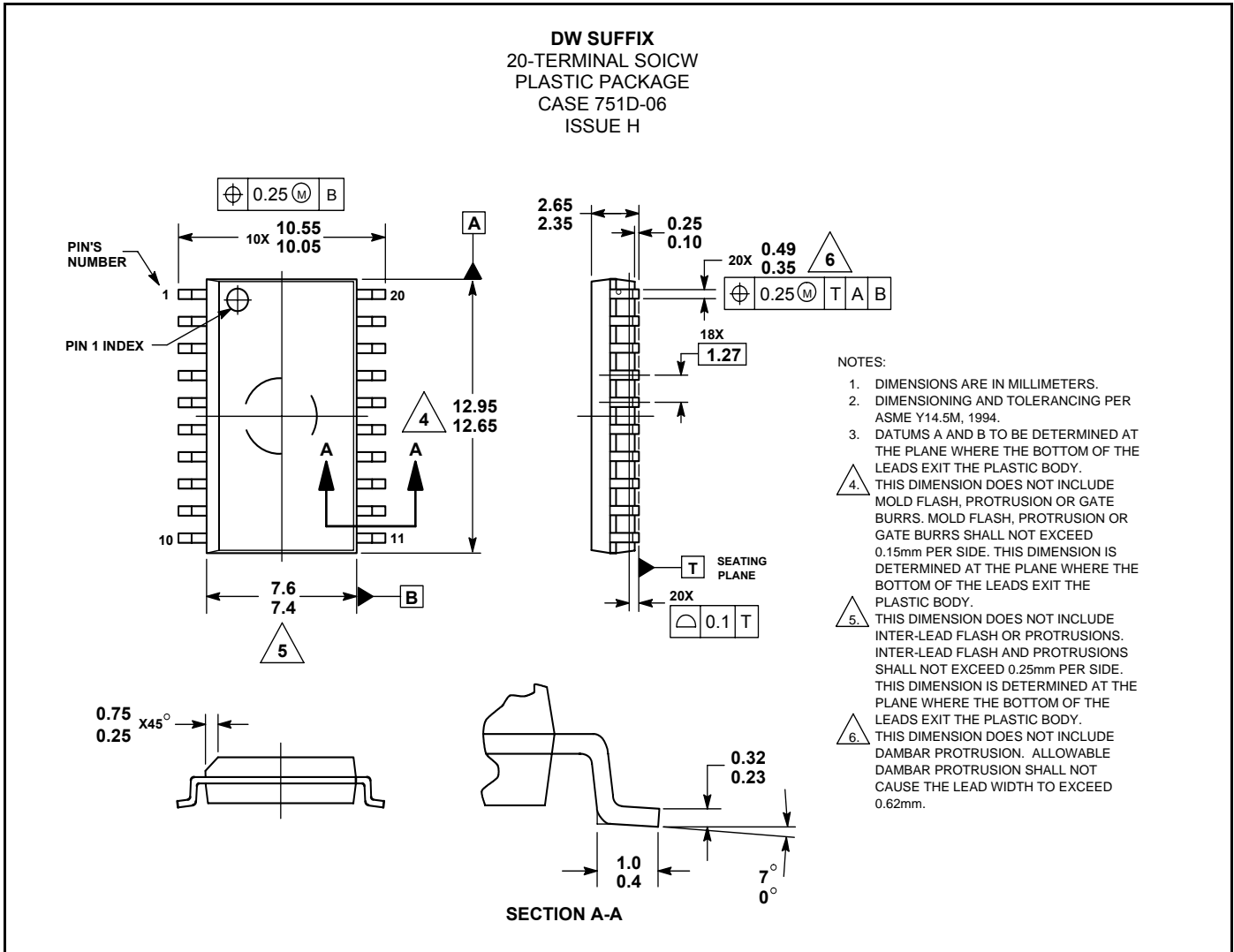


Figure 12. Application Schematic with External Protection Circuit

PACKAGE DIMENSIONS



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**NOTES**

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