

## Peripheral Board Controller (PBC)

## PEB 2050

Preliminary Data

MOS IC

| Type       | Ordering Code | Package        |
|------------|---------------|----------------|
| PEB 2050-C | Q67100-Z157   | C-DIP-40       |
| PEB 2050-N | Q67100-HB392  | PL-CC-44 (SMD) |
| PEB 2050-P | Q67100-H3022  | P-DIP-40       |

The peripheral board controller PEB 2050 is a device for the control of voice, data, and signaling paths of up to 16 subscribers on peripheral component boards in digital telephone systems. In combination with the highly flexible Signal Processing Codec Filter (SICOFI® PEB 2060) it forms an optimized analog subscriber-line board architecture. Its flexibility allows operation as general-purpose controller for data switching and MUX/De MUX applications.

The PBC controls space and time switching functions between subscriber-line devices and time-division multiplex highways. Further, it controls the flow of information between the subscriber interface ports and a processor which can be an optional line card local processor or the central processor directly. Last, it performs all protocol control functions, using the HDLC protocol format for all information passing between the line card and the central processor via a dedicated HDLC line or via interleaved time slots on the PCM lines.

To meet the different requirements the PBC PEB 2050 provides the following interfaces:

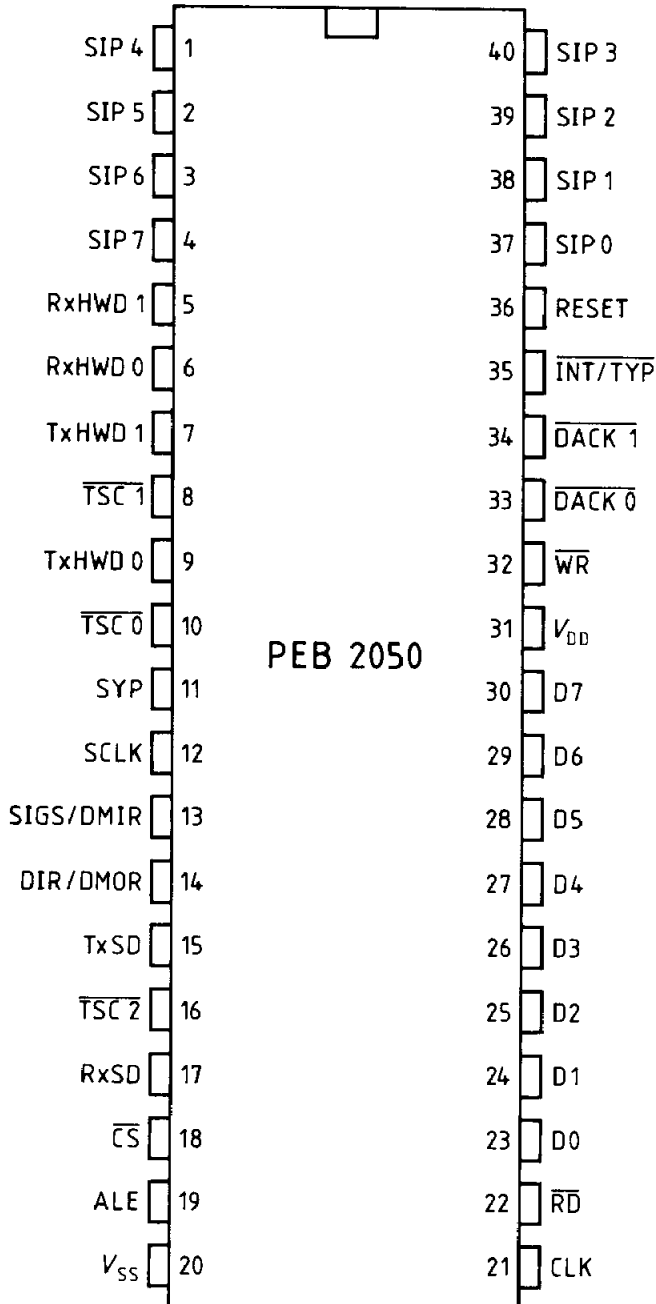
- 8 serial, bidirectional I/O ports for the transfer of voice, data, control, and signaling information between the PBC and codec filters (e.g. SICOFI PEB 2060), digital interface circuits or signal processors
- Double-constructed PCM interface
- Fast serial communication link to the central processor
- Bit-parallel interface for the connection of 8-bit standard microcomputers such as the SAB 8051. The interface is characterized by an interrupt control and two independent DMA channels, one for the transmit and one for the receive direction.

### Features

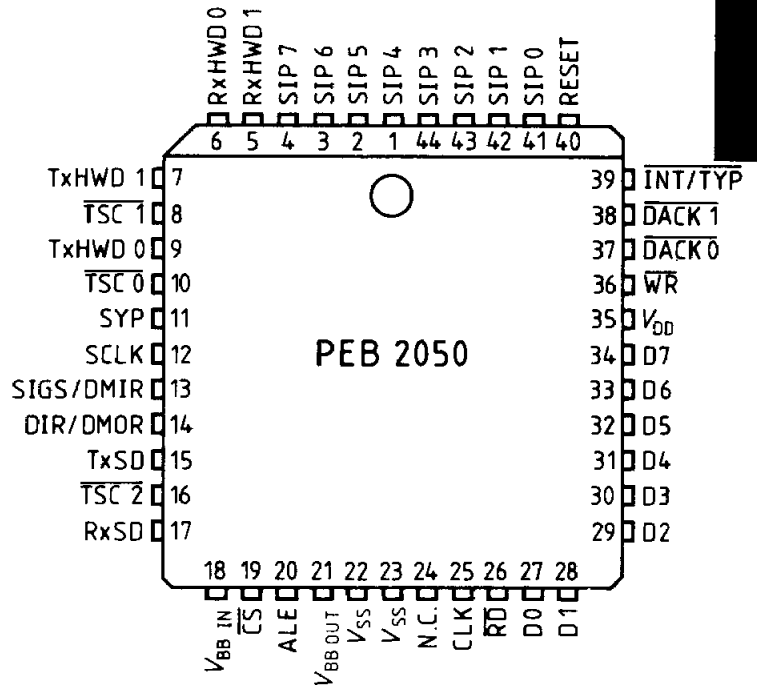
- Board controller for up to 16 subscribers of a digital switching system
- Designed for different PCM systems
- Time-slot assignment freely programmable for all subscribers connected
- Control of voice, data, signaling and line board parameters to minimize hardware requirements and to simplify software
- Provides two full duplex PCM highways for the system interface
- System control uses the HDLC protocol with X.25 level 2 functions performed by the PBC
- Standard  $\mu$ P interface
- Two DMA channels for expansion of internal buffer capability of 16 bytes per direction
- $\mu$ P access to all internal data streams including time-slot oriented data streams
- Support of subscriber circuits by generating timing signals
- Single +5 V power supply
- Low power consumption

**Pin Configuration**  
(top view)

**P-DIP-40  
C-DIP-40**



**PL-CC-44**



V<sub>BB IN</sub> and V<sub>BB OUT</sub> Have to be Short Circuited.

## Pin Definitions and Functions

| Pin No.<br>PL-CC      | Pin No.<br>P-DIP      | Symbol                        | Name   | Function   |
|-----------------------|-----------------------|-------------------------------|--|--|
| 1<br>.<br>.<br>.<br>4 | 1<br>.<br>.<br>.<br>4 | SIP 4<br>.<br>.<br>.<br>SIP 7 | Subscriber interface port (input/output)   | These interface ports are used for bi-directional, bit-serial transfer of speech, data and control words to and from the signal processing codec Filter (SICOFI) or standard codec. Corresponding with the direction signal, the PBC PEB 2050 is transmitting during the high level of DIR within the first half of a 125 $\mu$ s frame. |
| 5                     | 5                     | RxHWD 1                       | Receive highway data (input)   | Receive PCM highway 1 interface.   |
| 6                     | 6                     | RxHWD 0                       | Receive highway data (input)   | Receive PCM highway 0 interface. The PBC serially receives a PCM word (8 bits) through one of these leads at the programmed time slot.   |
| 7                     | 7                     | TxHWD 1                       | Transmit highway data (output)   | Output of the transmit side onto the send PCM highway 1 (serial bus). The 8-bit PCM word is serially sent out on this pin at the programmed time slot. Tristate output.  |
| 8                     | 8                     | $\overline{\text{TSC 1}}$     | Tristate control (output, active low)  | Normally high, this signal goes low while the PBC is transmitting an 8-bit PCM word on the PCM highway 1.  |
| 9                     | 9                     | TxHWD 0                       | Transmit highway data (output)   | Output of the transmit side onto the send PCM highway 0.   |
| 10                    | 10                    | $\overline{\text{TSC 0}}$     | Tristate control (output, active low)  | Tristate control of highway 0.   |
| 11                    | 11                    | SYP                           | Synchronization  | SYP is a frame synchronization pulse which resets the on-chip time-slot counters.  |
| 12                    | 12                    | SCLK                          | Slave clock (output)   | Clock output for the peripheral devices. The signals between the codec filter and the PBC are latched and transmitted with the rising edge of SCLK.  |
| 13                    | 13                    | SIGS/DMIR                     | Signal strobe (output, active high)/ direct memory input request (output, active high) | The SIGS output supplies a programmable strobe signal. In the DMA mode, this pin is used as DMA input request.   |

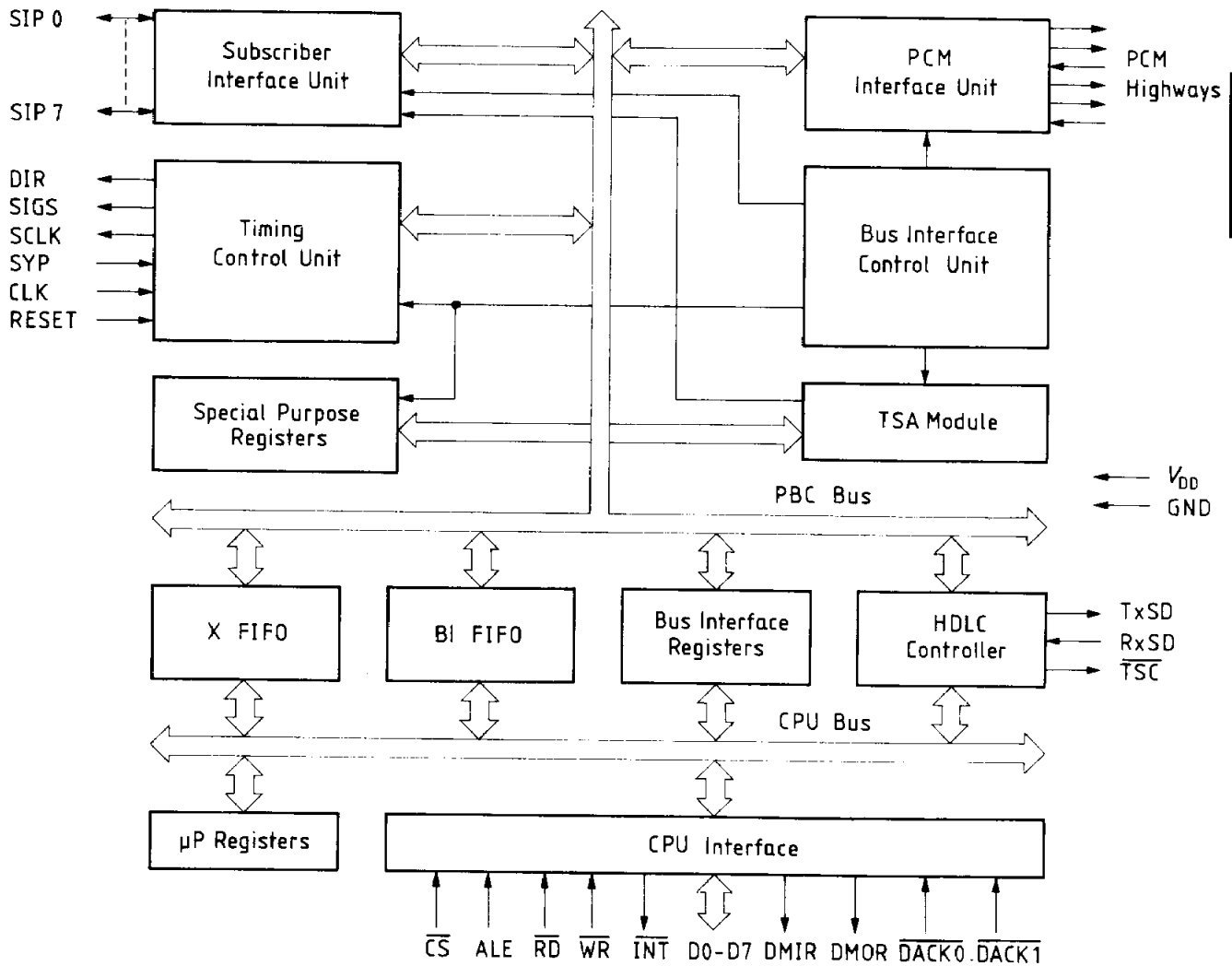
## Pin Definitions and Functions (cont'd)

| Pin No.<br>PL-CC | Pin No.<br>P-DIP | Symbol          | Name   | Function   |
|------------------|------------------|-----------------|--|--|
| 14               | 14               | DIR/DMOR        | Direction (output, active high)/direct memory output request (output, active high) | DIR is an 8-kHz symmetric frame signal which controls the direction of data transfer from and to the peripheral devices. The PBC is able to receive data during the low state of DIR. In the DMA mode this pin is used as DMA output request. DMIR and DMOR are generated by the PBC-internal HDLC receiver or transmitter and are used for handshaking during the DMA transfer. |
| 15               | 15               | TxSD            | Transmit signaling data (output)   | This line transmits the serial data to the dedicated HDLC channel.   |
| 16               | 16               | TSC 2           | Tristate control to 2 (output, active low)   | Normally high, this signal goes low while the PBC is transmitting an HDLC message.   |
| 17               | 17               | RxSD            | Receive signaling data (input)   | This line receives the serial data from the HDLC channel.  |
| 19               | 18               | $\overline{CS}$ | Chip select (input, active low)  | $\overline{CS}$ is used to address the PBC. A low level at this input enables the PBC to accept commands or data from a $\mu P$ within a write cycle, or to transmit data during a read cycle.   |
| 20               | 19               | ALE             | Address latch enable (input, active high)  | A high level at this input indicates that the data on the external bus is an address selecting one of the PBC-internal sources or destinations. Latching into the address latch occurs during the high-low transition.   |
| 22               | 20               | $V_{SS}$        |  | Ground (0 V)   |
| 25               | 21               | CLK             | Clock (input)  | A standard TTL clock provides the basic timing of the controller. The clock is synchronous to the PCM clock.   |
| 26               | 22               | $\overline{RD}$ | Read strobe (input, active low)  | $\overline{RD}$ is used together with $\overline{CS}$ to transfer data from the PBC to a $\mu P$ or memory.  |

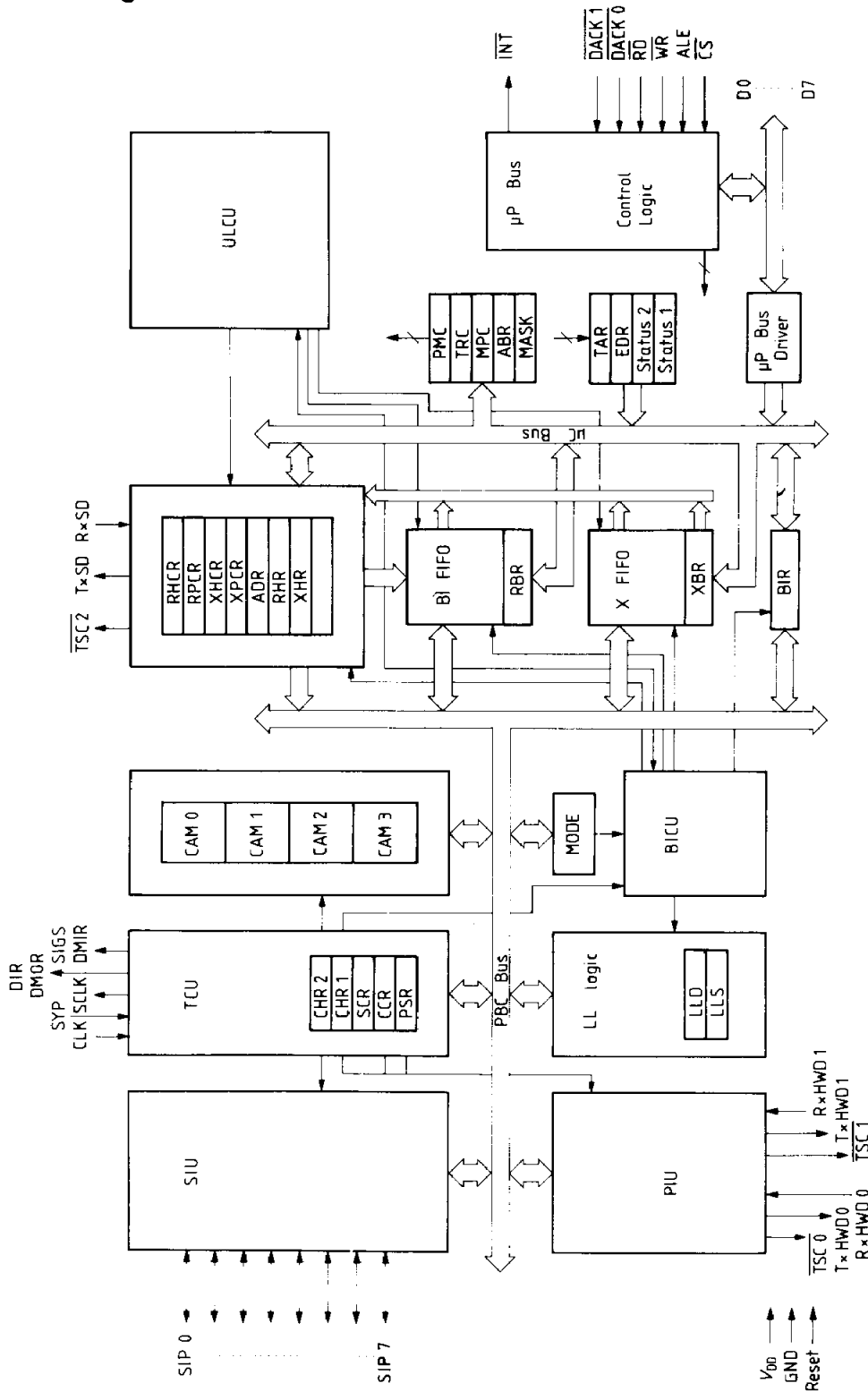
## Pin Definitions and Functions (cont'd)

| Pin No.<br>PL-CC | Pin No.<br>P-DIP | Symbol               | Name                                   | Function   |
|------------------|------------------|----------------------|--|--|
| 27               | 23               | D0                   | System data bus                        | The data bus transfers data and commands between the $\mu$ P or memory and the PBC.  |
| .                | .                | .                    |  |  |
| .                | .                | .                    |  |  |
| .                | .                | .                    |  |  |
| .                | .                | .                    |  |  |
| .                | .                | .                    |  |  |
| 34               | 30               | D7                   |  |  |
| 35               | 31               | $V_{DD}$             |  |  |
| 36               | 32               | $\overline{WR}$      | Write strobe (input, active low)       | During the low state of $\overline{WR}$ data can be transferred from the $\mu$ P or memory to the PBC.   |
| 37               | 33               | $\overline{DACK 0}$  | DMA acknowledge (inputs, active low)   | $\overline{DACK 0}$ and $\overline{DACK 1}$ are used to acknowledge the DMA output and DMA input request, respectively.  |
| 38               | 34               | $\overline{DACK 1}$  |  |  |
| 39               | 35               | $\overline{INT/TYP}$ | Interrupt request (output, active low) | The signal is pulled down, when the PBC is requesting an interrupt. In that case, the $\mu$ P should enter an interrupt routine for reading status register 1.   |
| 40               | 36               | RESET                | Reset (input, active high)             | A high on this input forces the PBC into reset state. The minimum reset pulse is 16 complete clock cycles.   |
| 41               | 37               | SIP 0                |  | These interface ports are used for bi-directional, bit-serial transfer of speech, data and control words to and from the signal processing codec filter (SICOFI) or standard codec. Corresponding with the direction signal, the PBC PEB 2050 is transmitting during the high level of DIR within the first half of a 125 $\mu$ s frame. |
| .                | .                | .                    |  |  |
| .                | .                | .                    |  |  |
| .                | .                | .                    |  |  |
| .                | .                | .                    |  |  |
| .                | .                | .                    |  |  |
| 33               | 40               | SIP 3                |  |  |

**Block Diagram**



Block Diagram



### Description of the Functional Blocks

The PBC has been designed especially for use in peripheral subscriber boards, but its functional flexibility also permits its application in various parts of a digital exchange telecommunications system.

Used in peripheral subscriber boards it performs two essential functions:

- 1) Exchange of control data between a central processing unit, an on-board processing unit and individual subscriber connections. The PBC supports the ISO/CCITT's HDLC communication-line protocol. An application-specific, PBC-internal controller controls the distribution of data on the board.
- 2) The time-slot controlled transfer of PCM data (64 Kbaud channels) between the PCM highways and the subscriber connections.

Data transfer between both parts, such as signaling through PCM highways (common channel) or the access of the on-board  $\mu$ P to 64 Kbaud channels, are considerably simplified by the IC.

The two central functional blocks are reflected in the circuit structure: The PCM synchronous portion constitutes the interfaces to the subscribers and the PCM highways. It comprises the following functional blocks:

- SIU (Serial Interface Unit) with last look logic
- PIU (PCM Interface Unit)
- CAM (Contents-Addressable Memory)
- TCU (Timing Control Unit)
- MODE register
- PBC bus

The asynchronous portion constitutes the interface to the local microprocessor (8-bit parallel), and to the central control (serial HDLC interface) and comprises the following functional blocks:

- HDLC controller
- $\mu$ P interface
- $\mu$ P control and status register
- ULCU (User Level Control Unit)

The two portions are interconnected by the following functional blocks:

- X FIFO (Transmit FIFO)
- Bidirectional FIFO
- BICU (Bus Interface Control Unit)
- BIR (Bus Interface Register)



**Maximum Ratings**

| Parameter           | Symbol    | Limit Values |      | Unit |
|---------------------|-----------|--------------|------|------|
|                     |           | min.         | max. |      |
| Storage temperature | $T_{stg}$ | -65          | 125  | °C   |

**Range of Operation**

|                                       |           |      |     |    |
|---------------------------------------|-----------|------|-----|----|
| Operating temperature                 | $T_A$     | 0    | 70  | °C |
| Voltage at any pin referred to ground | $V_S$     | -0.5 | 7   | V  |
| Total power consumption               | $P_{tot}$ |      | 625 | mW |

**DC Characteristics**

$T_A = 0$  to  $70^\circ\text{C}$ ;  $V_{CC} = 5\text{ V} \pm 0.25\text{ V}$ ;  $\text{GND} = 0\text{ V}$

| Parameter  | Symbol   | Limit Values |      |      | Unit          |
|--|----------|--------------|------|------|---------------|
|  |          | min.         | typ. | max. |               |
| L-input voltage  | $V_{IL}$ | -0.5         |      | 0.8  | V             |
| H-input voltage  | $V_{IH}$ | 2.0          |      | 5.5  | V             |
| L-output voltage<br>$I_{OL} = +1.6\text{ mA}$                | $V_{OL}$ |              |      | 0.45 | V             |
| H-output voltage<br>$I_{OH} = -400\ \mu\text{A}$             | $V_{OH}$ | 2.4          |      |      | V             |
| Input leakage current<br>$V_{IN} = V_{CC}$ to $0\text{ V}$   | $I_{IL}$ | -10          |      | 10   | $\mu\text{A}$ |
| Output leakage current<br>$V_{OUT} = V_{CC}$ to $0\text{ V}$ | $I_{OL}$ | -10          |      | 10   | $\mu\text{A}$ |
| $V_{CC}$ supply current<br>$V_{CC} = 5\text{ V}$             | $I_{CC}$ |              | 70   | 125  | mA            |

**Capacitance** $T_A = 25\text{ }^\circ\text{C}; V_{CC} = \text{GND} = 0\text{ V}$ 

| Parameter  | Symbol    | Limit Values |      |      | Unit |
|--|-----------|--------------|------|------|------|
|  |           | min.         | typ. | max. |      |
| Input capacitance<br>$f_C = 1\text{ MHz}$                | $C_{IN}$  |              | 5    | 10   | pF   |
| Input/output capacitance                                 | $C_{I/O}$ |              | 10   | 20   | pF   |
| Output capacitance<br>unmeasured pins<br>returned to GND | $C_{OUT}$ |              | 8    | 15   | pF   |

**AC Characteristics** $T_A = 0\text{ to }70\text{ }^\circ\text{C}; V_{CC} = 5\text{ V} \pm 0.25\text{ V}; \text{GND} = 0\text{ V}$ **Microprocessor Interface****Read Cycle**

| Parameter  | Symbol   | Limit Values |        | Unit |
|--|----------|--------------|--------|------|
|  |          | min.         | max.   |      |
| Address hold after ALE                                       | $t_{LA}$ | 20           |        | ns   |
| Address to ALE setup   | $t_{AL}$ | 30           |        | ns   |
| Data delay from $\overline{\text{RD}}$                       | $t_{RD}$ |              | 150    | ns   |
| $\overline{\text{RD}}$ pulse width                           | $t_{RR}$ | 150          | $10^7$ | ns   |
| Output float delay   | $t_{DF}$ |              | 25     | ns   |
| $\overline{\text{RD}}$ control interval case 1 <sup>1)</sup> | $t_{RI}$ | 2 x CP       |        | ns   |
| $\overline{\text{RD}}$ control interval case 2 <sup>2)</sup> | $t_{RI}$ | 100          |        | ns   |
| ALE pulse width  | $t_{AA}$ | 60           |        | ns   |

**Write Cycle**

|  |          |        |  |    |
|--|----------|--------|--|----|
| $\overline{\text{WR}}$ pulse width                           | $t_{WW}$ | 100    |  | ns |
| Data setup to $\overline{\text{WR}}$                         | $t_{DW}$ | 50     |  | ns |
| Data hold after $\overline{\text{WR}}$                       | $t_{WD}$ | 25     |  | ns |
| $\overline{\text{WR}}$ control interval case 1 <sup>1)</sup> | $t_{WI}$ | 2 x CP |  | ns |
| $\overline{\text{WR}}$ control interval case 2 <sup>2)</sup> | $t_{WI}$ | 50     |  | ns |

1) Case 1: read, write of BI FIFO and X FIFO

2) Case 2: all other registers

**DMA Read**

| Parameter                             | Symbol    | Limit Values |        | Unit |
|---------------------------------------|-----------|--------------|--------|------|
|                                       |           | min.         | max.   |      |
| DMA read time*)                       | $t_{DMA}$ |              | 7 x CP | ns   |
| DMOR hold time                        | $t_{DH}$  |              | 75     | ns   |
| Address stable before $\overline{RD}$ | $t_{AR}$  | 0            |        | ns   |
| Data delay from $\overline{RD}$       | $t_{RD}$  |              | 150    | ns   |
| Output floating delay                 | $t_{DF}$  |              | 25     | ns   |
| Address hold after $\overline{RD}$    | $t_{RA}$  | 0            |        | ns   |
| $\overline{RD}$ pulse width           | $t_{RR}$  | 150          | $10^4$ | ns   |

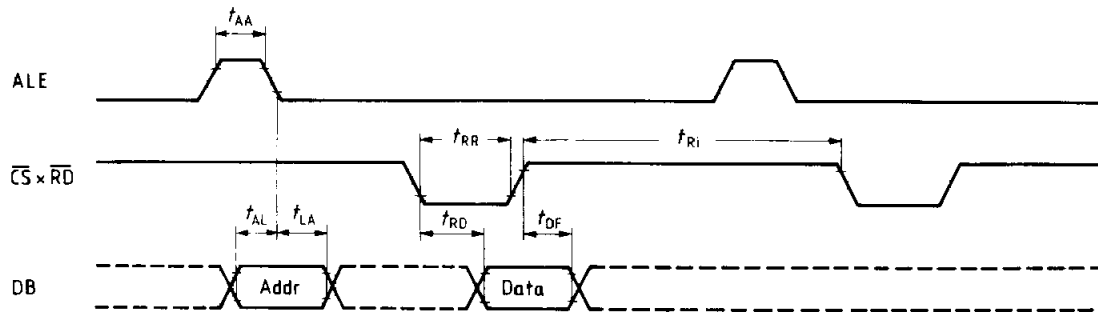
**DMA Write**

|                                       |           |     |        |    |
|---------------------------------------|-----------|-----|--------|----|
| DMA write time*)                      | $t_{DMA}$ |     | 7 x CP | ns |
| DMSIR hold time                       | $t_{IH}$  |     | 90     | ns |
| Address stable before $\overline{WR}$ | $t_{AW}$  | 0   |        | ns |
| Address hold after $\overline{WR}$    | $t_{WA}$  | 0   |        | ns |
| Data setup to $\overline{WR}$         | $t_{DW}$  | 50  |        | ns |
| Data hold after $\overline{WR}$       | $t_{WD}$  | 25  |        | ns |
| $\overline{WR}$ pulse width           | $t_{WW}$  | 100 |        | ns |

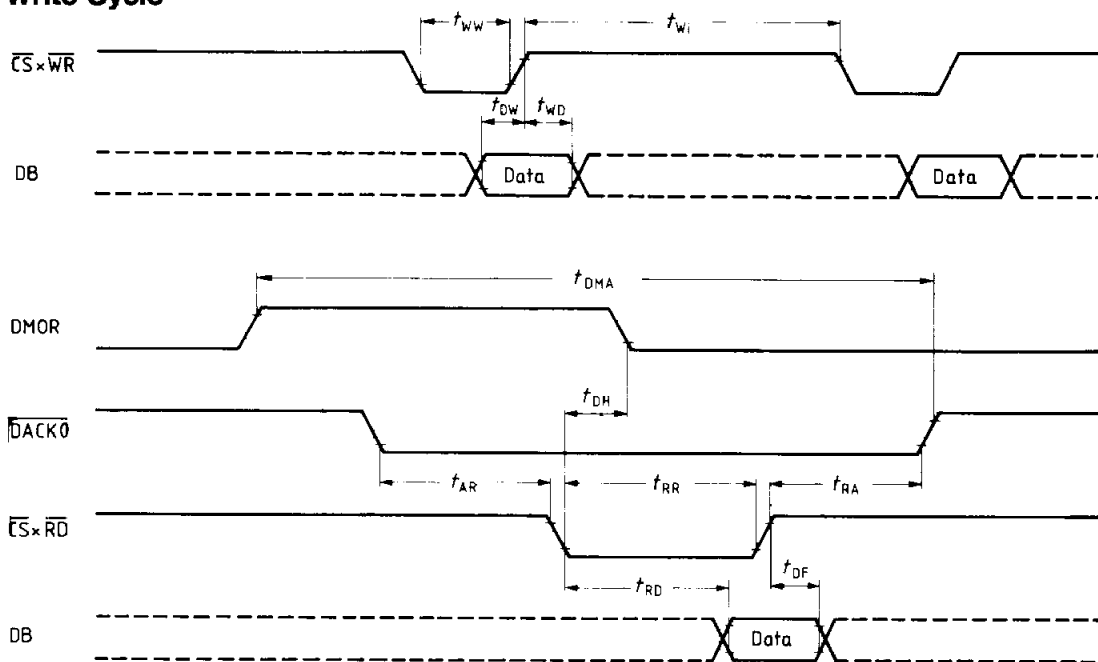
\*)

|                 |       |       |       |       |
|-----------------|-------|-------|-------|-------|
| PBC clock/MHz   | 2.048 | 4.096 | 1.536 | 3.072 |
| 2 x CP/ns       | 980   | 490   | 1300  | 650   |
| 7 x CP/ $\mu$ s | 3.4   | 1.7   | 4.56  | 2.3   |

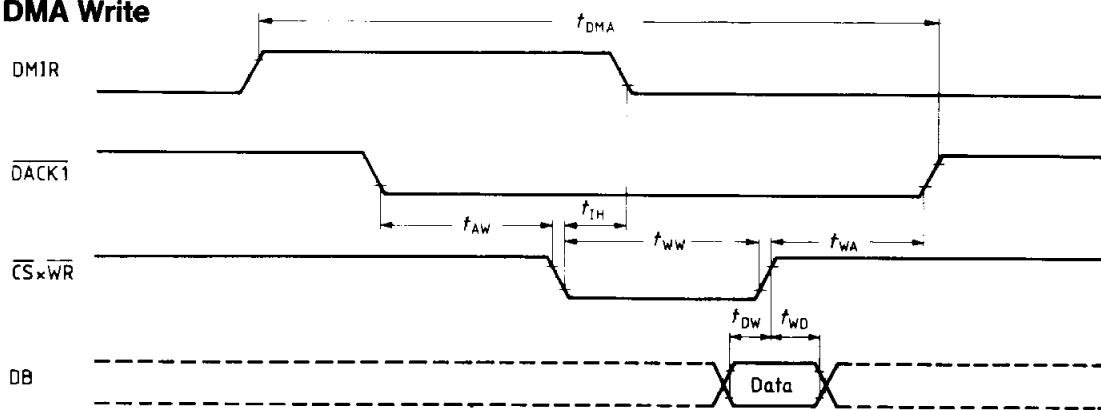
**Read Cycle**



**Write Cycle**



**DMA Write**



**Clock Timing**

| Parameter | Symbol | Limit Values |      | Unit |
|-----------|--------|--------------|------|------|
|           |        | min.         | max. |      |

**System Clock**

|                        |                             |     |                |         |
|------------------------|-----------------------------|-----|----------------|---------|
| System clock frequency | $f_{CLK}$                   | 1   | 4.2            | MHz     |
| Duty cycle             |                             | 45  | 55             | %       |
| Sync pulse period      | $t_{SPP}$                   | 125 | $N \times 125$ | $\mu s$ |
| Sync pulse width       | $t_{SYP}$                   | 60  | $t_{CLK}$      | ns      |
| Pulse delay to CLK     | $t_{dSYP}$                  | 10  |                | ns      |
| Setup time to CLK      | $t_{sSYP}$                  | 50  |                | ns      |
| Clock rise/fall time   | $t_{r CLK}/$<br>$t_{f CLK}$ |     | 10             | ns      |

**Slave Clock**

|                         |             |     |     |     |
|-------------------------|-------------|-----|-----|-----|
| Clock frequency         | $f_{SCLK}$  | 512 | 512 | kHz |
| Clock delay time        | $t_{dSCLK}$ | 100 | 165 | ns  |
| Delay time SCLK to data | $t_{dSD}$   | 20  |     | ns  |

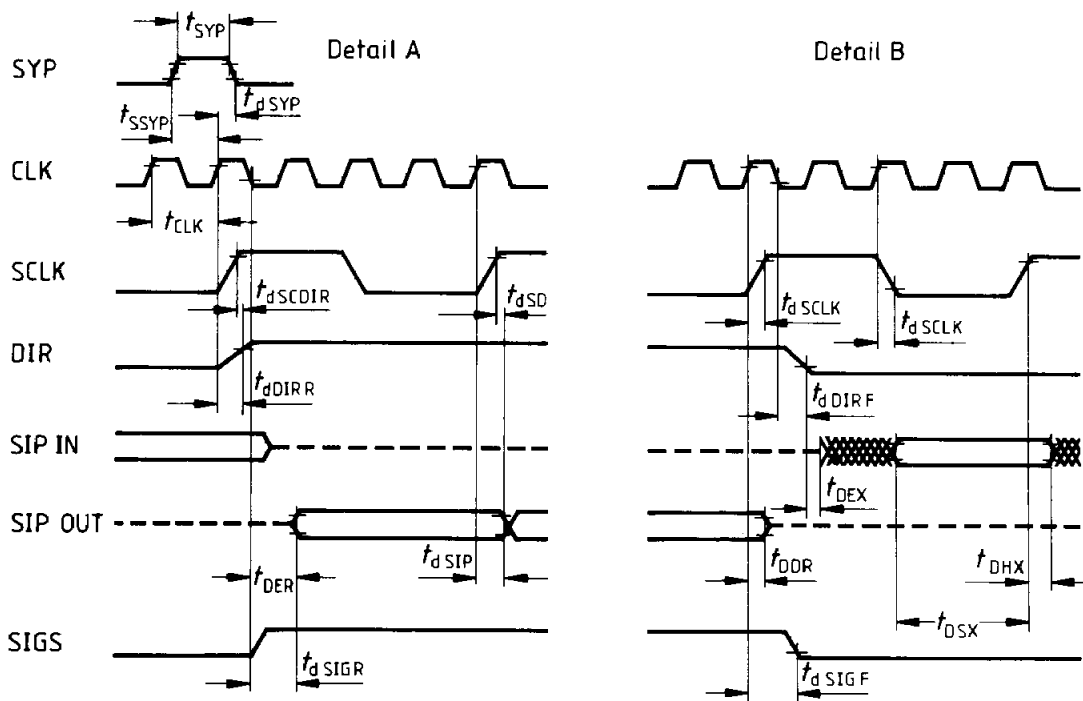
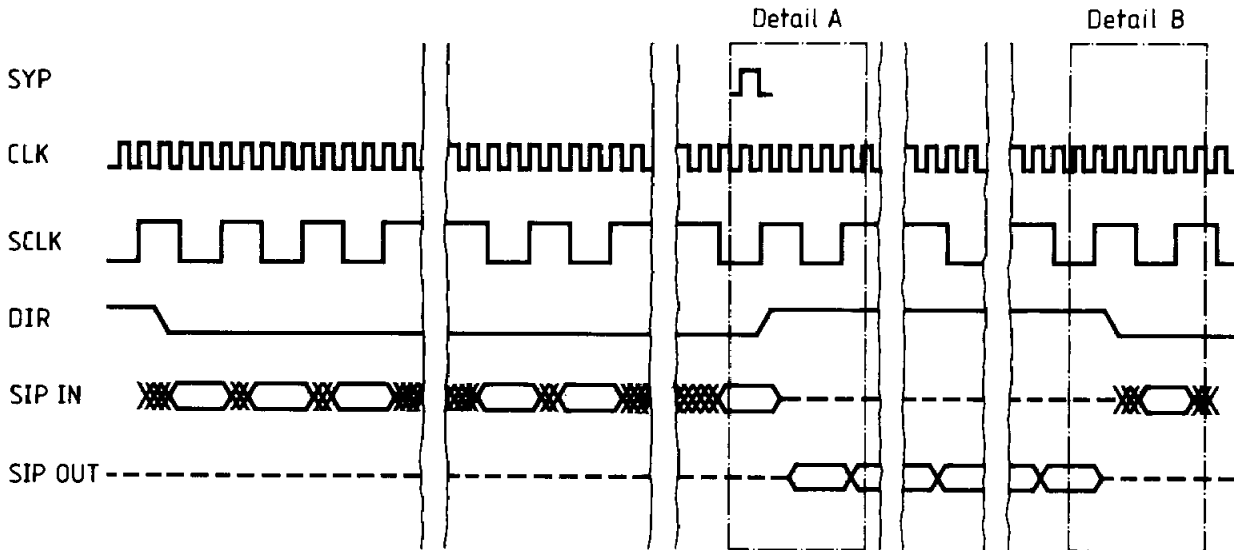
**DIR Clock**

|                                  |              |     |     |    |
|----------------------------------|--------------|-----|-----|----|
| Delay time to CLK (rising edge)  | $t_{dDIR R}$ | 120 | 190 | ns |
| Delay time to CLK (falling edge) | $t_{dDIR F}$ | 30  | 110 | ns |
| Delay time SCLK to DIR           | $t_{dSCDIR}$ | -10 | 70  | ns |

**SIU Interface**

|                                       |              |         |     |    |
|---------------------------------------|--------------|---------|-----|----|
| SIP data delay                        | $t_{dSIP}$   | 160     | 300 | ns |
| Data enable receive                   | $t_{DER}$    | 100     | 180 | ns |
| Data disable receive                  | $t_{DDR}$    | 100     | 180 | ns |
| Data enable transmit                  | $t_{DEX}$    | 0       |     | ns |
| Data hold transmit                    | $t_{DHX}$    | 0       |     | ns |
| Data setup transmit (control data)    | $t_{DSX}$    | CP/+200 |     | ns |
| Data setup transmit                   | $t_{DSX}$    | 200     |     | ns |
| Signaling strobe delay (falling edge) | $t_{DSIG F}$ | 90      | 200 | ns |
| Signaling strobe delay (rising edge)  | $t_{DSIG R}$ | 140     | 220 | ns |

SIP Interface Timing



**Serial Port Timing**

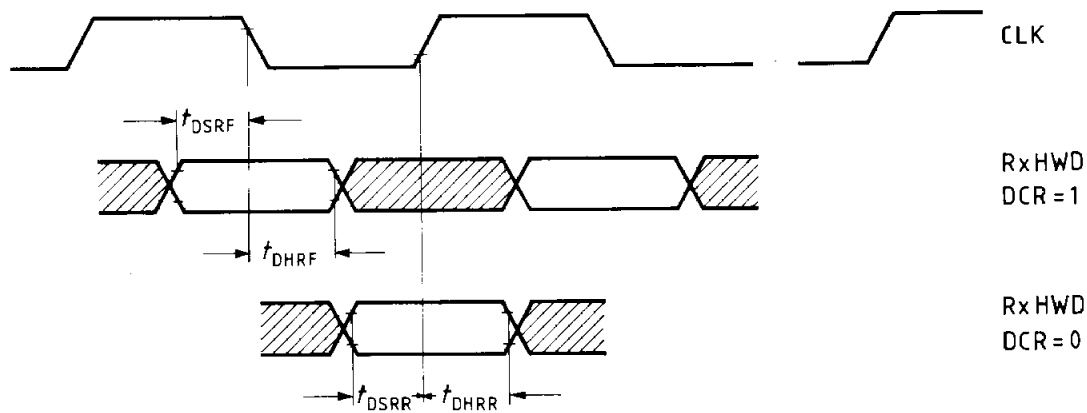
**PCM Interface**

| Parameter | Symbol | Limit Values |      | Unit |
|-----------|--------|--------------|------|------|
|           |        | min.         | max. |      |

**Receive Timing**

|                             |            |    |  |    |
|-----------------------------|------------|----|--|----|
| Receive data setup DCR = 1  | $t_{DSRF}$ | 20 |  | ns |
| Receive data setup DCR = 0* | $t_{DSRR}$ | 40 |  | ns |
| Receive data hold DCR = 1   | $t_{DHRF}$ | 40 |  | ns |
| Receive data hold DCR = 0   | $t_{DHRR}$ | 10 |  | ns |

**Receive Timing**

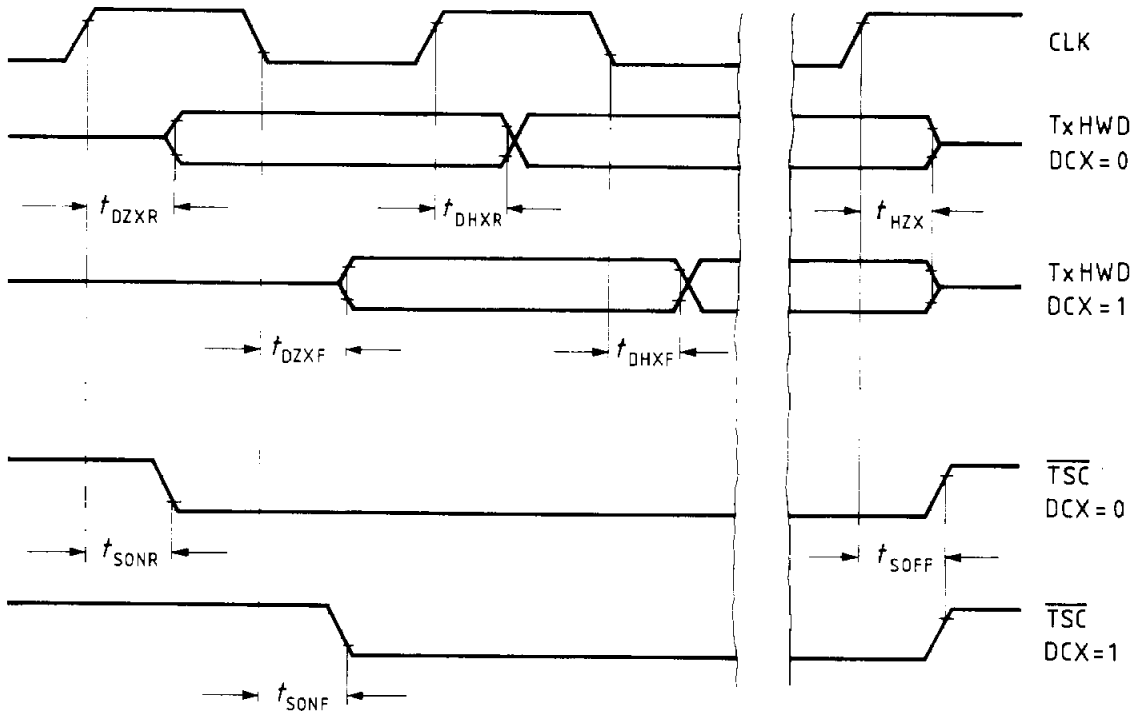


\*) Common channel mode  $t_{DSRR}$  75 ns

PCM Interface (cont'd)

| Parameter                     | Symbol     | Limit Values |      | Unit | Test Conditions        |
|-------------------------------|------------|--------------|------|------|------------------------|
|                               |            | min.         | max. |      |                        |
| <b>Transmit Timing</b>        |            |              |      |      |                        |
| Data enable DCX = 0           | $t_{DZXR}$ | 80           | 160  | ns   | $C_L = 200 \text{ pF}$ |
| Data enable DCX = 1           | $t_{DZXF}$ | 40           | 100  | ns   | $C_L = 200 \text{ pF}$ |
| Data hold time DCX = 0        | $t_{DHXR}$ | 45           | 160  | ns   | $C_L = 200 \text{ pF}$ |
| Data hold time DCX = 1        | $t_{DHXF}$ | 40           | 100  | ns   | $C_L = 200 \text{ pF}$ |
| Data float on TS EXIT         | $t_{HZX}$  | 35           | 80   | ns   | $C_L = 150 \text{ pF}$ |
| Time slot x to enable DCX = 0 | $t_{SONR}$ | 70           | 130  | ns   | $C_L = 150 \text{ pF}$ |
| Time slot x to enable DCX = 1 | $t_{SONF}$ | 40           | 100  | ns   | $C_L = 150 \text{ pF}$ |
| Time slot x to disable        | $t_{SOFF}$ | 40           | 100  | ns   | $C_L = 150 \text{ pF}$ |

Transmit Timing





**HDLC Interface**

| Parameter | Symbol | Limit Values |      | Unit | Test Conditions |
|-----------|--------|--------------|------|------|-----------------|
|           |        | min.         | max. |      |                 |

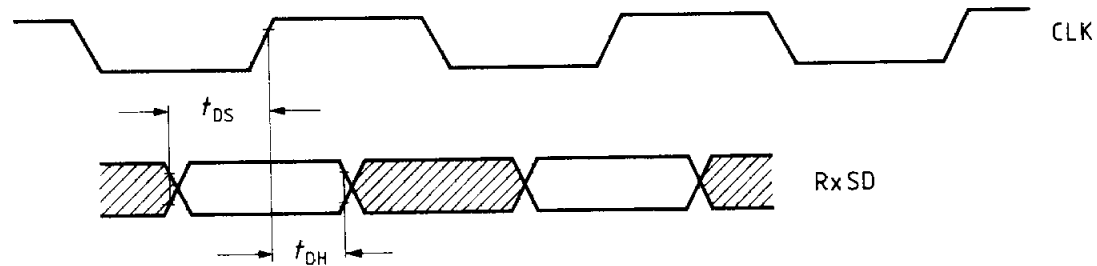
**Receive Timing**

|                    |          |    |  |    |  |
|--------------------|----------|----|--|----|--|
| Receive data setup | $t_{DS}$ | 40 |  | ns |  |
| Receive data hold  | $t_{DH}$ | 10 |  | ns |  |

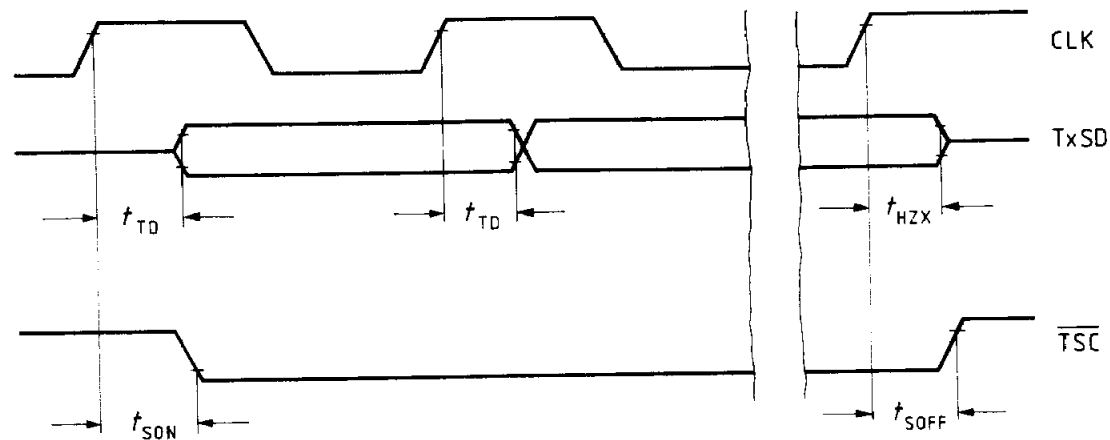
**Transmit Timing**

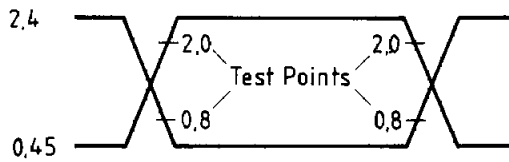
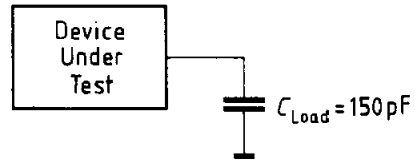
|                        |            |    |     |    |                        |
|------------------------|------------|----|-----|----|------------------------|
| Transmit data delay    | $t_{TD}$   | 40 | 100 | ns | $C_L = 200 \text{ pF}$ |
| Data float on TS EXIT  | $t_{HZX}$  | 35 | 80  | ns | $C_L = 200 \text{ pF}$ |
| Time slot x to enable  | $t_{SON}$  | 40 | 95  | ns | $C_L = 150 \text{ pF}$ |
| Time slot x to disable | $t_{SOFF}$ | 35 | 90  | ns | $C_L = 150 \text{ pF}$ |

**Receive Timing**



**Transmit Timing**



**AC Testing Input, Output Waveform****AC Testing Load Circuit**

AC testing: inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".  
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".