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Migrating from the MC68HC705K1 to the MC68HC705KJ1

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Introduction

Freescale provides two different parts to migrate your current MC68HC705K1 (K1) application easily. Depending on your design, system enhancements, and cost, the MC68HC705KJ1 (KJ1) and the MC68HC805K3 (K3) provide two different migration paths.

The major differences between the KJ1 and the K3 are:

- Price
- Pinout compatibility

The KJ1 is not pin for pin the same as the K1, but it is roughly 70% the cost of the K1. Although the K3 is pin for pin the same as the K1, it is roughly 90% the cost of the K1.

This application note illustrates the differences between the K1 and the KJ1. Using the KJ1's additional features can further enhance your system design. Consult the K1 and KJ1 databooks for detailed design reference. See **References/Additional Reading** in this application note.

For information on migrating your design to the K3, consult the application note titled *Migrating from the MC68HC705K1 to the MC68HC805K3,* Freescale document order number AN1747/D.

MC68HC705KJ1 Features

- 1240 bytes of user EPROM
- 64 bytes of low-power user RAM
- 4-MHz maximum internal bus frequency at 5 volts
- 15-stage multifunction timer
- COP watchdog timer
- 10 bidirectional input/output (I/O) pins, including:
  - 10-mA sink capability on all I/O pins
  - 5.5-mA source capability on six I/O pins
  - Software programmable pulldowns on all I/O pins
  - Keyboard scan with selectable interrupt on four I/O pins
- Selectable sensitivity on external interrupt; edge- and level-sensitive or edge-sensitive only
- On-chip oscillator with options for:
  - Crystal
  - Ceramic resonator
  - Resistor-capacitor (RC) oscillator (MC68HRC705KJ1) with or without external resistor
  - Low-speed (32 kHz) crystal (MC68HLC705KJ1)
  - External clock
- External interrupt mask bit and acknowledge bit
- EPROM security bit[1] to aid in locking out access to programmable EPROM array
- Selectable STOP conversion to HALT and option for fast restart and power-on reset
- Internal steering diode and pullup device on $\overline{\text{RESET}}$ pin to V_{DD}

1. No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

Migrating to the MC68HC705KJ1

Pinouts and Package Types

The KJ1 has a different pinout from the K1, making layout changes necessary. See **Figure 1** and **Figure 2** for pin descriptions.

Both parts are available in either plastic DIP or SOIC packages.

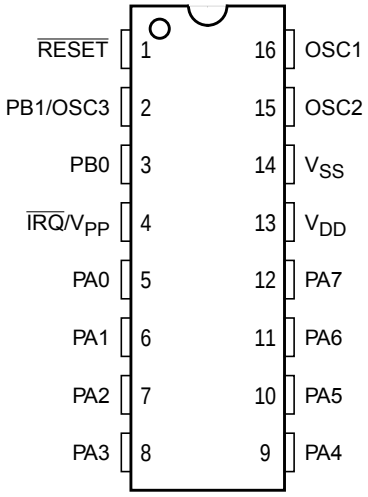

Figure 1. MC68HC705K1 Pinout

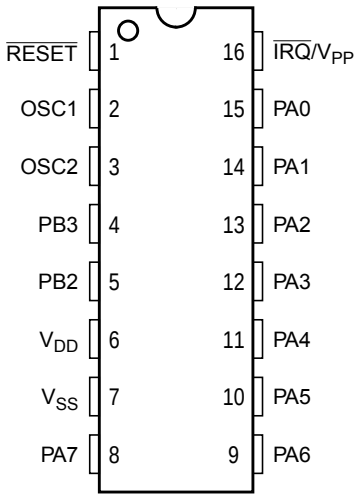

Figure 2. MC68HC705KJ1 Pinout

Block Diagrams

Throughout this application note, refer to the block diagrams for the K1 in **Figure 3** and KJ1 in **Figure 4**.

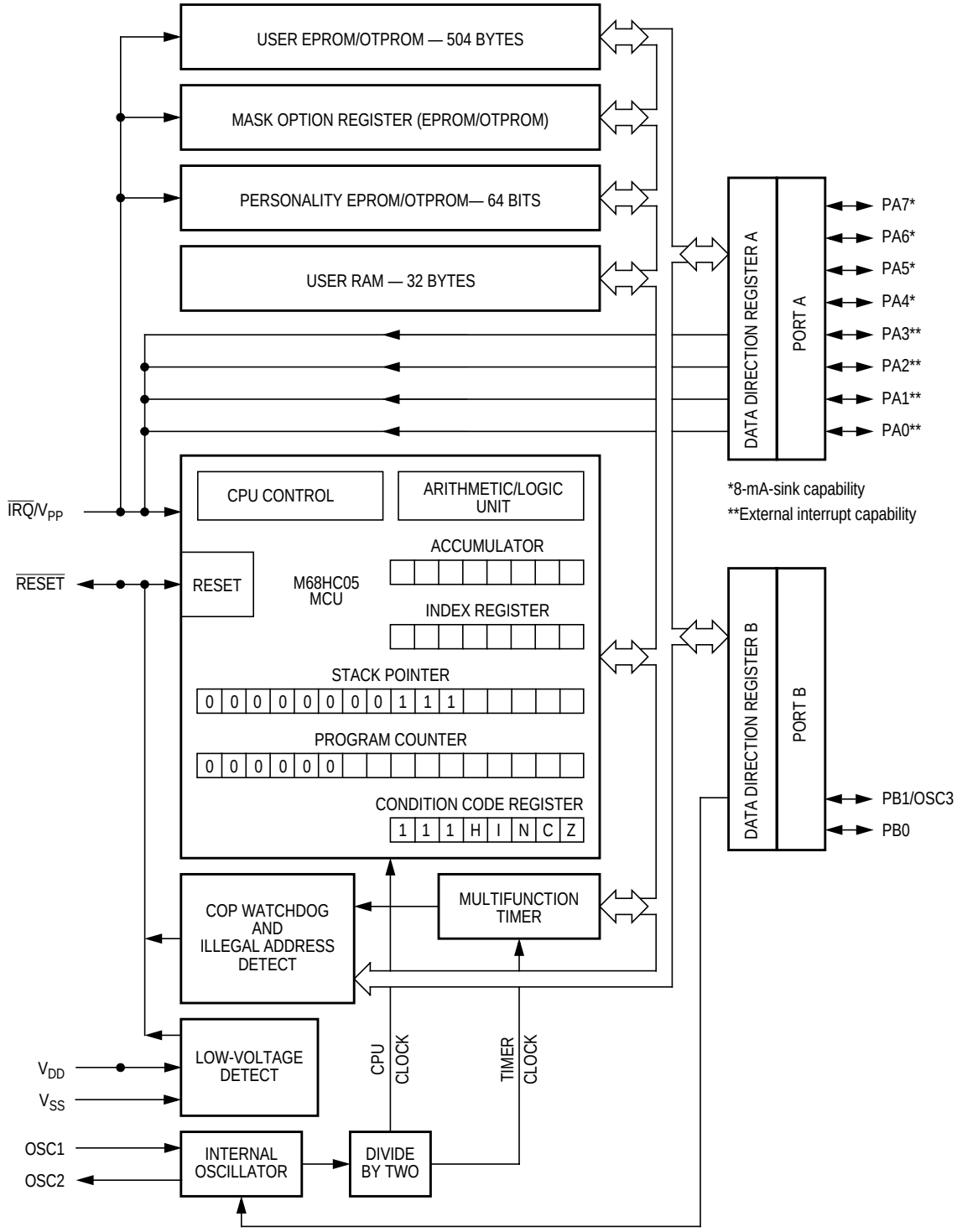

Figure 3. MC68HC705K1 Block Diagram

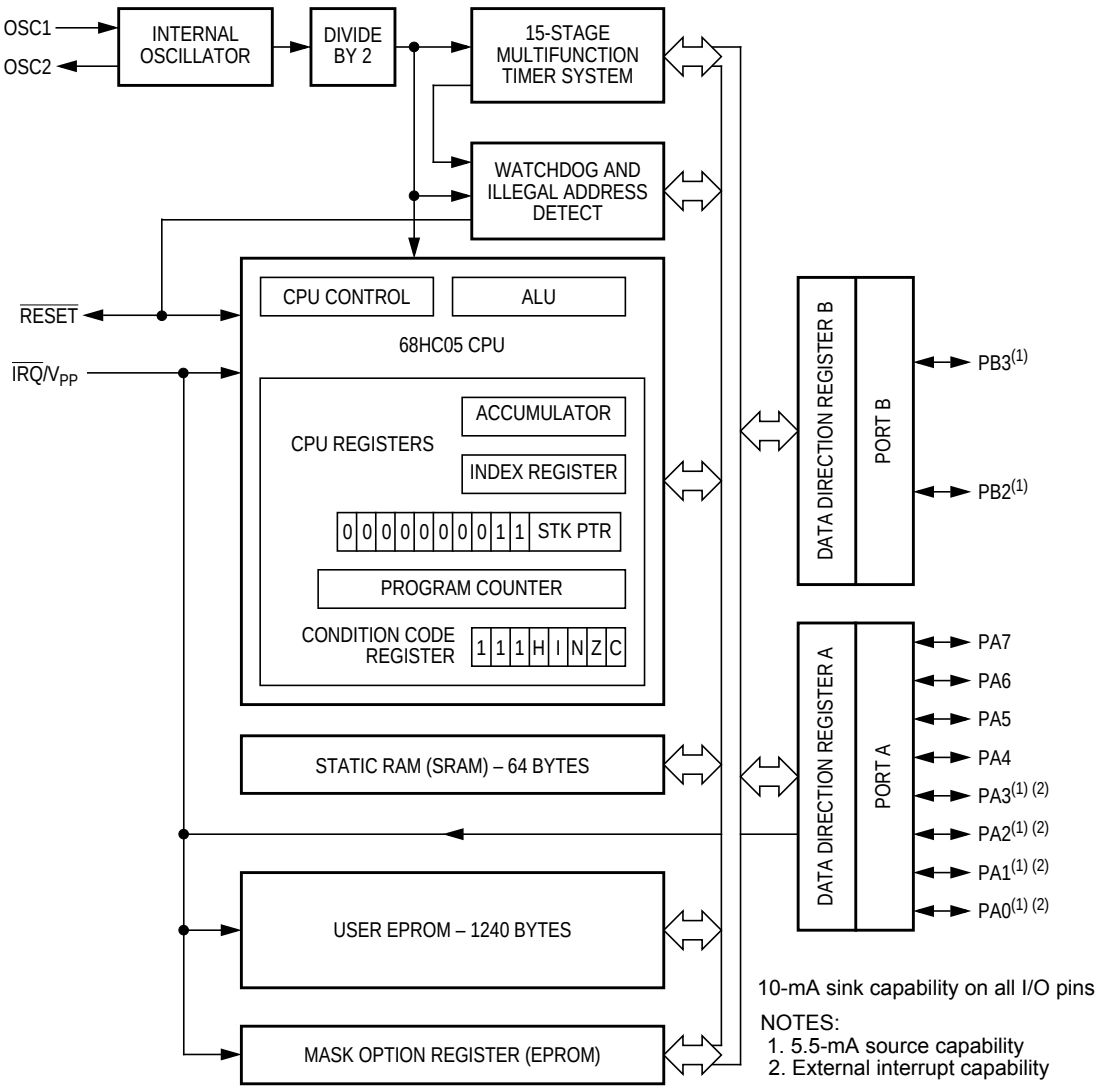

Figure 4. MC68HC705KJ1 Block Diagram

Memory Maps and Registers

Figure 5 and Figure 6 show the memory maps and registers of the K1 and KJ1. Modify your code to reflect these changes:

- The KJ1 has a total of 64 bytes of RAM. If you want to utilize this additional memory of the KJ1, originate RAM memory to start at $C0.
- The KJ1 has a total of 1232 bytes of EPROM for code space. Originate EPROM memory to start at $300.
- Move the MOR register from location $17 on the K1 to location $7F1 on the KJ1.
- Move the location of the COP register from location $3F0 on the K1 to location $7F0 on the KJ1.
- Move the start of the interrupt vectors from location $3F8 on the K1 to location $7F8 on the KJ1.

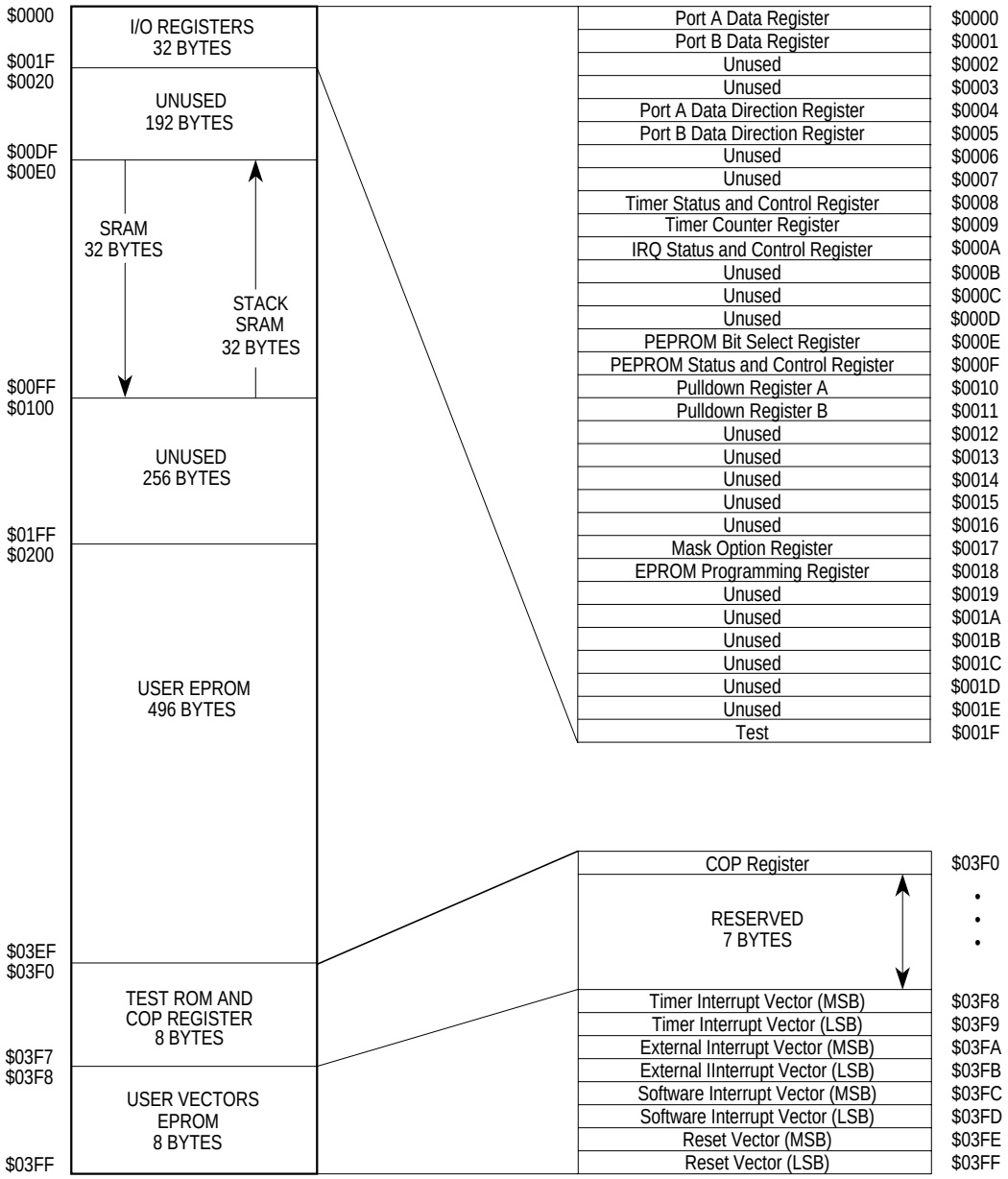

Figure 5. MC68HC705K1 Memory and Register Map

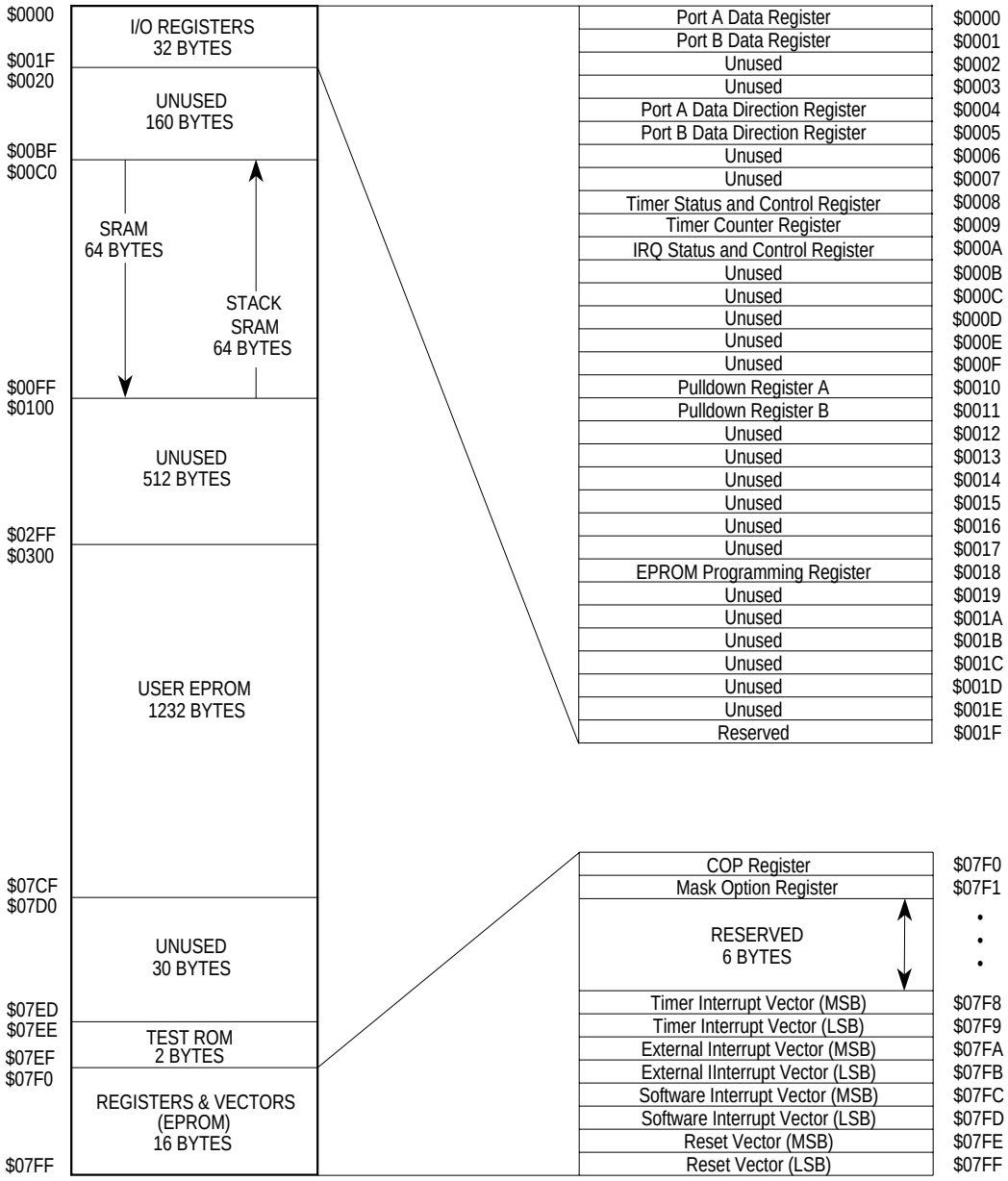

Figure 6. MC68HC705KJ1 Memory and Register Map

Ports

The KJ1 I/O pins have expanded high current capabilities that allow them to source or sink current to a device. Depending on the current requirements, these pins can be used to switch power to other parts of the system, light LEDs, or switch opto-coupled triacs without external transistors. **Table 1** shows the maximum ratings for the I/O pins.

Table 1. KJ1 I/O Maximum Current Ratings

Characteristic	Symbol	Max	Unit
High source current PA7–PA4 pins PA3–PA0 pins PB3–PB2 pins	I_{OH}	 2.5 5.5 5.5	mA
High sink current PA7–PA0 pins PB3–PB2 pins	I_{OL}	 10 10	mA

Consult the KJ1 databook for high-side and low-side driver characteristics and graphs.

Port A

No changes needed on port A.

Port B

The KJ1 has two bits of the port B register bonded out. These are bits 2 and 3. Change your code by mapping the K1's port B pins to the KJ1's port B pins. This mapping also applies to the port B data direction register and the port B pulldown register.

K1 PB0 maps to KJ1 PB2.

K1 PB1 maps to KJ1 PB3.

$0001	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	See Note	See Note	PB3	PB2	See Note	See Note
Write:								
Reset:	Unaffected by reset							

= Unimplemented

PB5, PB4, PB1, and PB0 should be configured as inputs at all times. These bits are available for read/write but are not available externally. Configuring them as inputs will ensure that the pulldown devices are enabled, thus properly terminating them.

Figure 7. Port B Data Register (PORTB)

$0005	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	See Note	See Note	DDRB3	DDRB2	See Note	See Note
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

PB5, PB4, PB1, and PB0 should be configured as inputs at all times. These bits are available for read/write but are not available externally. Configuring them as inputs will ensure that the pulldown devices are enabled, thus properly terminating them.

Figure 8. Port B Data Direction Register (DDRB)

$0011	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	See Note	See Note	PDIB3	PDIB2	See Note	See Note
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

PB5, PB4, PB1, and PB0 should be configured as inputs at all times. These bits are available for read/write but are not available externally. Configuring them as inputs will ensure that the pulldown devices are enabled, thus properly terminating them.

Figure 9. Pulldown Register B (PDRB)

Clock

The KJ1 has different clock circuitry than the K1. The main difference is the RC clock option. The available clocking options on the KJ1 are listed in **Table 2**.

Table 2. KJ1 Clock Options

Clock Option	Comments	Part Number
Crystal oscillator	Internal feedback resistor con gured in MOR	MC68HC705KJ1
Crystal oscillator (32 kHz)	Do not use internal feedback resistor	MC68HLC705KJ1
Ceramic resonator	Internal feedback resistor con gured in MOR	MC68HC705KJ1
RC oscillator	Uses either external or internal resistor	MC68HRC705KJ1
External clock	Direct connection of clock source	MC68HC705KJ1

If you are using a crystal or ceramic resonator and want to use the internal feedback resistor, the OSCRES bit in the mask option register (MOR) must be set to 1. This enables the 2-MΩ feedback resistor. The KJ1 has the option of using a 32-kHz crystal. Consult the KJ1 databook about how to connect a 32-kHz crystal to the KJ1 properly.

The RC option on the KJ1 is quite different from the K1. The RC oscillator has two options:

- For more accurate clocks, use an external resistor between the OSC1 and OSC2 pins. Do not turn on the internal feedback resistor. Make sure the OSCRES bit in the MOR is 0.
- For maximum cost reduction, the RC oscillator can utilize the internal resistor and allow the chip to be driven with no external components. This is also the least accurate way to clock the chip. To use this option, make sure that the OSCRES bit in the MOR is 1.

Like the K1, the KJ1 can be driven by an external clocking source also.

For applications that demand more performance, the KJ1 maximum internal clock frequency is 4 MHz. The K1 maximum internal clock frequency is 2 MHz.

Reset and LVR Circuitry

The reset function on the KJ1 has additional features:

- The $\overline{\text{RESET}}$ pin contains a steering diode to discharge any voltage on the pin to V_{DD} when the power is removed.
- The $\overline{\text{RESET}}$ pin contains an internal pullup resistor to V_{DD} to allow the $\overline{\text{RESET}}$ pin to be left unconnected for low-power applications.
- The KJ1 has all of the K1 reset sources except a low-voltage reset (LVR). These are:
  - Power-on reset
  - Logic 0 on the $\overline{\text{RESET}}$ pin
  - Computer operating properly (COP)
  - Illegal address

The KJ1 does not have an internal LVR. If your K1 design used the LVR, external LVR circuitry must be added to replace this function.

Interrupts

Like the K1, the KJ1 has the same interrupt sources and functionality. These are:

- Software interrupt
- Logic 0 applied to the $\overline{\text{IRQ}}/V_{PP}$ pin
- Logic 1 applied to one of the PA3–PA0 pins
- A timer overflow interrupt
- A real-time interrupt

The port A interrupt option on the K1 is programmed by writing to the PIRQ bit (bit 2) of the MOR at location $17. On the KJ1, write to the PIRQ bit (bit 2) of the MOR at location $7F1.

The external interrupt sensitivity on the K1 is programmed by writing to the LEVEL bit (bit 1) of the MOR at location $17. On the KJ1, write to the LEVEL bit (bit 1) of the MOR at location $7F1.

Timer

The timer on the KJ1 is identical to the K1. No changes are needed in software or hardware.

COP

The COP on the K1 is enabled by programming the COPEN bit (bit 0) of the MOR at location $17 to a 1. On the KJ1, program the COPEN bit (bit 0) of the MOR at location $7F1 to a 1.

The K1 COP timer is cleared by writing a 0 to bit 0 of the COPR (computer operating properly register) at location $3F0. On the KJ1, clear the COP by writing a 0 to bit 0 of the COPR located at $7F0.

Just like the K1, the KJ1 COP timeout is set by the RT1 and RT0 bits of the timer status and control register. No code changes are needed.

Personality EPROM

The K1 provides the user with 64 bits of personality EPROM. The KJ1 does not have a personality EPROM array. Consequently, the personality EPROM bit select register and the personality EPROM status and control register are not found on the KJ1.

To provide this functionality within the KJ1, utilize some of the extra EPROM on the KJ1 to create eight bytes or 64 bits of personality EPROM. This EPROM memory cannot be programmed by the user's code. It can be programmed only at the time the entire EPROM array is being programmed for production.

MOR

The KJ1 gives the designer additional options in the MOR. **Table 3** compares the two MOR registers.

Table 3. MOR Comparison

Part	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
K1	SWPDI	PIN3	RC	SWAIT	LVRE	PIRQ	LEVEL	COPEN
KJ1	SOSCD	EPMSEC	OSCRES	SWAIT	SWPDI	PIRQ	LEVEL	COPEN

SWPDI	The software pulldown inhibit bit has the same functionality on both parts but is found at bit 3 of the KJ1 MOR.
PIN3	Since the KJ1 does not have a 3-pin oscillator option, this option is not found on the KJ1 MOR.
RC	The RC option on the K1 was used to distinguish between using an external RC network or an external crystal, ceramic resonator, or clock source. The KJ1 configures its oscillator with the OSCRES bit.
SWAIT	The STOP conversion to wait bit has the same functionality on both parts.
LVRE	The KJ1 does not have a low-voltage reset function. This option is not found in the KJ1 MOR.
PIRQ	The port A IRQ enable bit has the same functionality on both parts.
LEVEL	The external interrupt sensitivity bit has the same functionality on both parts.
COPEN	The COP enable bit has the same functionality on both parts.
SOSCD	The short oscillator delay bit controls the oscillator stabilization counter. The normal stabilization delay following reset or exit from stop mode is 4064 bus cycles. Setting the SOSCD enables a 128-bus cycle stabilization delay. If your oscillator design has a quick startup time, the SOSCD bit will allow quicker recovery from oscillator startup. Setting the bit to a 1 enables the short oscillator delay.
EPMSEC	To protect your software investment, the KJ1 provides the designer the added functionality of securing the EPROM array. When this bit is set, external access of the EPROM array is denied.

OSCRES The OSCRES bit enables the 2-MΩ internal resistor in the oscillator circuit. When this bit is set to 1, the internal resistor is enabled.

NOTE: *Program the OSCRES bit to logic 0 in devices using low-speed crystal oscillators or RC oscillators with external resistors.*

Ordering Information

Table 4 lists the MC order numbers for the KJ1. All parts are specified to run at –40 to +85 °C temperature.

Table 4. Ordering Information

Package Type	Oscillator Type	Order Number
Plastic DIP	XTAL	MC68HC705KJ1CP
SOIC	XTAL	MC68HC705KJ1CDW
CERDIP	XTAL	MC68HC705KJ1CS
Plastic DIP	RC	MC68HRC705KJ1CP
SOIC	RC	MC68HRC705KJ1CDW
CERDIP	RC	MC68HRC705KJ1CS
Plastic DIP	32-kHz XTAL	MC68HLC705KJ1CP
SOIC	32-kHz XTAL	MC68HLC705KJ1CDW
CERDIP	32-kHz XTAL	MC68HLC705KJ1CS

References/Additional Reading

MC68HC705K1 Technical Data, (MC68HC705K1/D),.

MC68HC705KJ1 Technical Data, (MC68HC705KJ1/D),