TUA6034, TUA6036

3-Band Digital TV / Set-Top-Box Tuner IC

TAIFUN

Version 2.51

Wireless Communication

Never stop thinking.

Edition 2006-01-11

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Revision History: 2006-01-11 V 2.51

Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
Revision History: Target Spec. V1.1, January 2001		
Previous Version: Target Spec. V1.0, November 2000		
div.	div.	in extended mode reference division ratio 80 replaced by 32
5-2	5-2	new definition of thermal properties

Revision History: Preliminary Spec. V1.2, April 2001

Previous Version: Target Spec. V1.1, January 2001		
div.	div.	status: preliminary
div.	div.	bug fixes: TSSOP and VQFN pinning. Changes: application focus to digital applications, tbd's replaced by values
5-10, 5-11	5-10, 5-11	phase noise values added
5-21	5-21	diagrams added

Revision History: Preliminary Spec. V1.3, July 2001

Previous Version: Preliminary Spec. V1.2, April 2001		
div.	div	Stand-by mode added
5-5	5-5	Crystal Oscillator: Input impedances added
5-7	5-7	Output leakage current replaced by port output voltage Symbol for port output saturation voltages changed
5-12	5-12	AGC source current 2 and AGC output voltage changed
5-15	5-15	Definition for MA1= 0 and MA0 = 1 changed

Revision History: Preliminary Spec. V1.4, October 2001

Previous Version: Preliminary Spec. V1.3, July 2001		
3-5, 3-7	3-5, 3-7	PNP ports: Pull-down resistors added
5-5	5-5	MID band: I_{VCC} corrected
5-10, 5-11	5-10, 5-11	Phase Noise: new values
5-12	5-12	AGC output voltage changed

Revision History: Spec. V2.0, May2002

Previous Version: Preliminary Spec. V1.4, October 2001		
all	all	preliminary and confidential deleted

Revision History: 2006-01-11 V 2.51

div	div	tbf's replaced, ISDB-T application deleted

Revision History: Spec. V2.1, August 2002

Previous Version: Spec. V2.0, May 2002		
5-6	5-6	Bus output SDA, Low-level output voltage, I_{OL} = 6 mA at 400 kHz deleted

Revision History: Spec. V2.2, December 2002

Previous Version: Spec. V2.1, August 2002		
3-2	3-2	Pinning of TUA6034-V changed

Revision History: V2.3, February 2003

Previous Version: Spec. V2.2, December 2002		
all	all	Mirrored version TUA6036 added

Revision History: V2.4, March 2003

Previous Version: Spec. V2.3, February 2003		
2-10, 4-29, 4-30	2-10, 4-29, 4-30	Frequencies corrected
5-34	5-34	Ambient temperature extended
5-38, 5-39, 5-40	5-38, 5-39, 5-40	Input IP2,Input IIP3, Output voltage causing 1 dB compression added, test frequencies changed

Revision History: V2.5, April 2004

Previous Version: Spec. V2.4, March 2003		
5-35	33	Crystal oscillation frequency added
div.	div.	TUA6034-V in VQFN-48 package
n.a.	28	ISDB-T application added
all	all	New Infineon template (A5 letter page size, page numbering)

Revision History: V2.51, January 2006

Previous Version: Spec. V2.5, April 2004		
all	all	Infineon Logo and postal address changed
div.	div.	stand-by mode replaced with power down mode
8, 11	15	General description: topics added

Revision History: **2006-01-11** V 2.51

14, 20	15, 21	Package GND added for the VQFN package
n.a.	30 - 32	Application circuits for TUA6034-V added
30	34	Absolute Maximum Ratings definitions updated
60	64	PG-VQFN-48 Outline Drawing updated

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Product Info

General Description

The **TUA6034, TUA6036 'TAIFUN'** device combines a mixer-oscillator block with a digitally programmable phase locked loop (PLL) for use in TV and VCR tuners and in set-top-box applications.

Features

General

- Suitable for PAL, NTSC, DVB and ATSC
- Wideband AGC detector for internal tuner AGC
  – 5 programmable take-over points
  – 2 programmable time constants
- Low phase noise
- Full ESD protection
- Qualified according to JEDEC for consumer applications

Mixer/Oscillator

- High impedance mixer input (common emitter) for LOW band
- Low impedance mixer input (common base) for MID band
- Low impedance mixer input (common base) for HIGH band
- 2 pin oscillator for LOW band
- 2 pin oscillator for MID band
- 4 pin oscillator for HIGH band

IF-Amplifier

- 4 IF pins to connect a 2 pole bandpass
- Symmetrical IF preamplifier with low output impedance able to drive a compensated SAW filter (500Ω//40pF)

PLL

- 4 independent I^2C addresses
- I^2C bus protocol compatible with 3.3 V and 5V micro-controllers up to 400 kHz
- High voltage VCO tuning output
- 4 PNP ports
- 1 NPN port/ADC input
- Internal LOW/MID/HIGH band switch
- Bus controlled power down mode
- Lock-in flag
- 6 programmable reference divider ratios (24, 28, 32, 64, 80, 128)
- 4 programmable charge pump currents

Application

- The IC is suitable for PAL, NTSC, DVB-C, DVB-T, ISDB-T and ATSC tuners. The focus is on digital terrestrial.
- The AGC stage makes the tuner AGC independent of the Video-IF AGC

Ordering Information

Type	Ordering Code	Package
TUA6034-T	Q67034-H0009	PG-TSSOP-38
TUA6036-T	Q67037-A0012	PG-TSSOP-38
TUA6034-V	Q67034-H0008	PG-VQFN-48

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1 Product Description

The **TUA6034, TUA6036 'TAIFUN'** device combines a mixer-oscillator block with a digitally programmable phase locked loop (PLL) for use in TV and VCR tuners and in set-top-box applications.

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, an IF amplifier, a reference voltage, and a band switch.

The PLL block with four independently selectable chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 1024 MHz in increments of 31.25, 50, 62.5, 125, 142.86 or 166.7 kHz. The tuning process is controlled by a microprocessor via an I^2C bus. The device has 5 output ports, one of them (P4) can also be used as ADC input port. A flag is set when the loop is locked. The lock flag can be read by the processor via the I^2C bus.

1.1 Features

1.1.1 General

- Suitable for PAL, NTSC, DVB, ISDB-T and ATSC
- Wideband AGC detector for internal tuner AGC
  – 5 programmable take-over points
  – 2 programmable time constants
- Low phase noise
- Full ESD protection
- Qualified according to JEDEC for consumer applications

1.1.2 Mixer/Oscillator

- High impedance mixer input (common emitter) for LOW band
- Low impedance mixer input (common base) for MID band
- Low impedance mixer input (common base) for HIGH band
- 2 pin oscillator for LOW band
- 2 pin oscillator for MID band
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1.1.3 IF-Amplifier

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- Symmetrical IF preamplifier with low output impedance able to drive a compensated SAW filter (500 Ω//40 pF)

1.1.4 PLL

- 4 independent I^2C addresses
- I^2C bus protocol compatible with 3.3 V and 5V micro-controllers up to 400 kHz
- High voltage VCO tuning output
- 4 PNP ports
- 1 NPN port/ADC input
- Bus controlled power down mode
- Internal LOW/MID/HIGH band switch
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- 6 programmable reference divider ratios (24, 28, 32, 64, 80, 128)
- 4 programmable charge pump currents

1.2 Application

- The IC is suitable for PAL, NTSC, DVB-C, DVB-T, ISDB-T and ATSC tuners. The focus is on digital terrestrial.
- The AGC stage makes the tuner AGC independent of the Video-IF AGC.

Recommended band limits in MHz:

Table 1 ATSC tuners

	RF input		Oscillator	
Band	**min**	**max**	**min**	**max**
LOW	55.25	157.25	101	203
MID	163.25	451.25	201	479
HIGH	457.25	861.25	503	907

Table 2 DVB-T tuners

	RF input		Oscillator	
Band	**min**	**max**	**min**	**max**
LOW	48.25	154.25	87.15	193.15
MID	161.25	439.25	200.15	478.15
HIGH	447.25	863.25	486.15	902.15

Table 3 ISDB-T tuners

	RF input		Oscillator	
Band	**min**	**max**	**min**	**max**
LOW	93	167	150	224
MID	173	467	230	524
HIGH	473	767	530	824

Note: Tuning margin of 3 MHz not included.

2 Functional Description

2.1 Pin Configuration

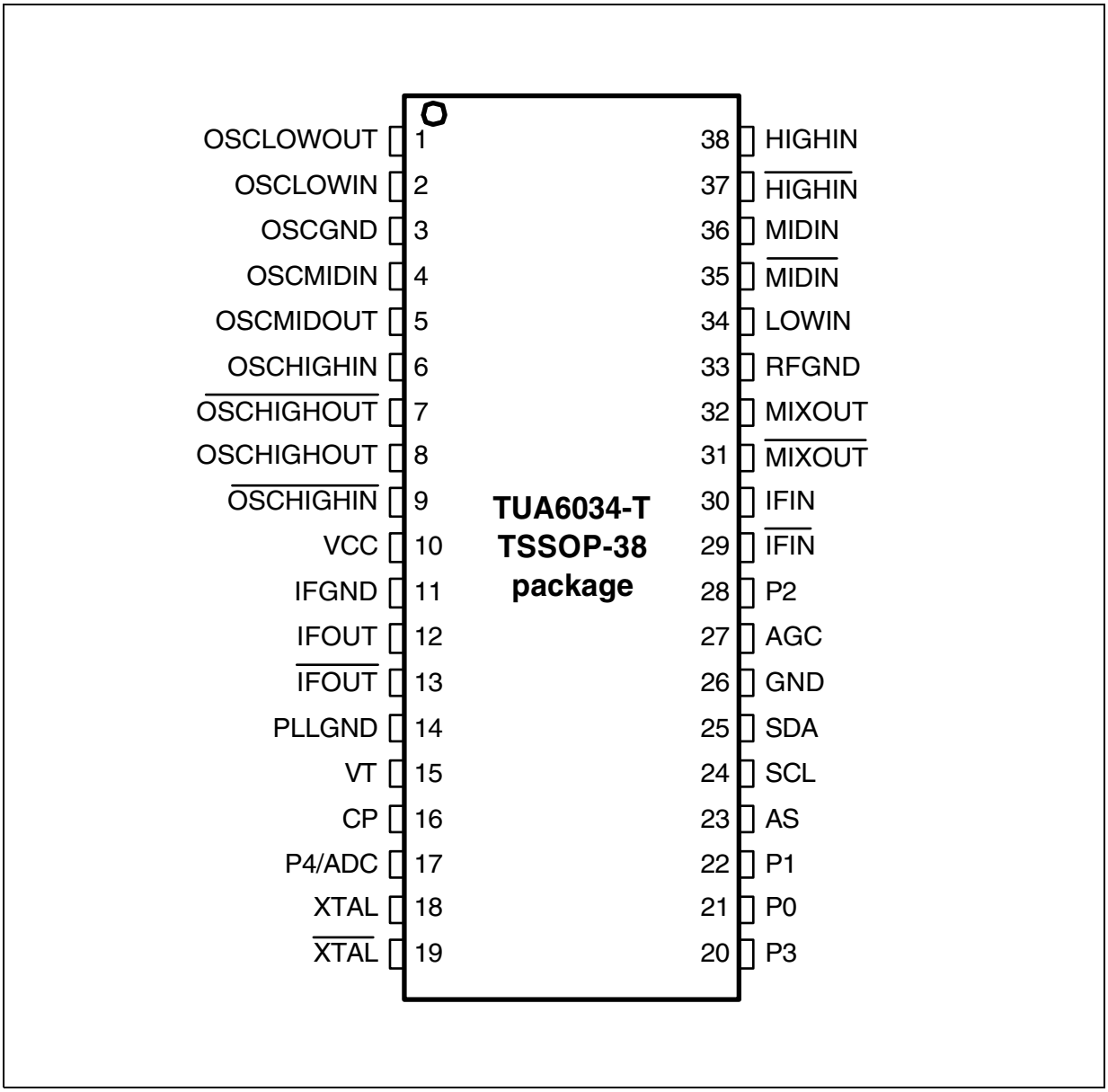


Figure 1 Pin Configuration TUA6034 in PG-TSSOP-38 Package

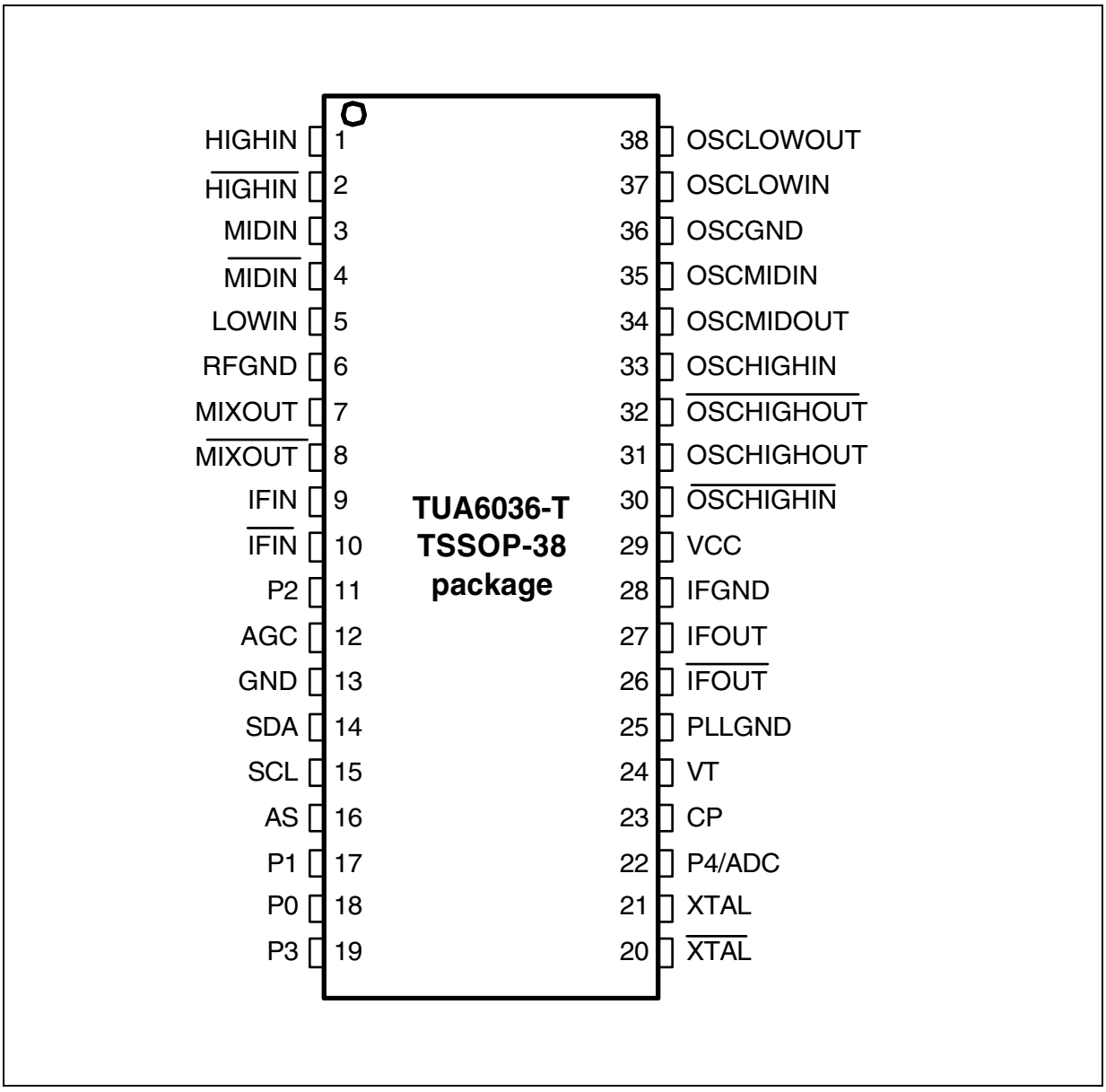


Figure 2 Pin Configuration TUA6036 in PG-TSSOP-38 Package

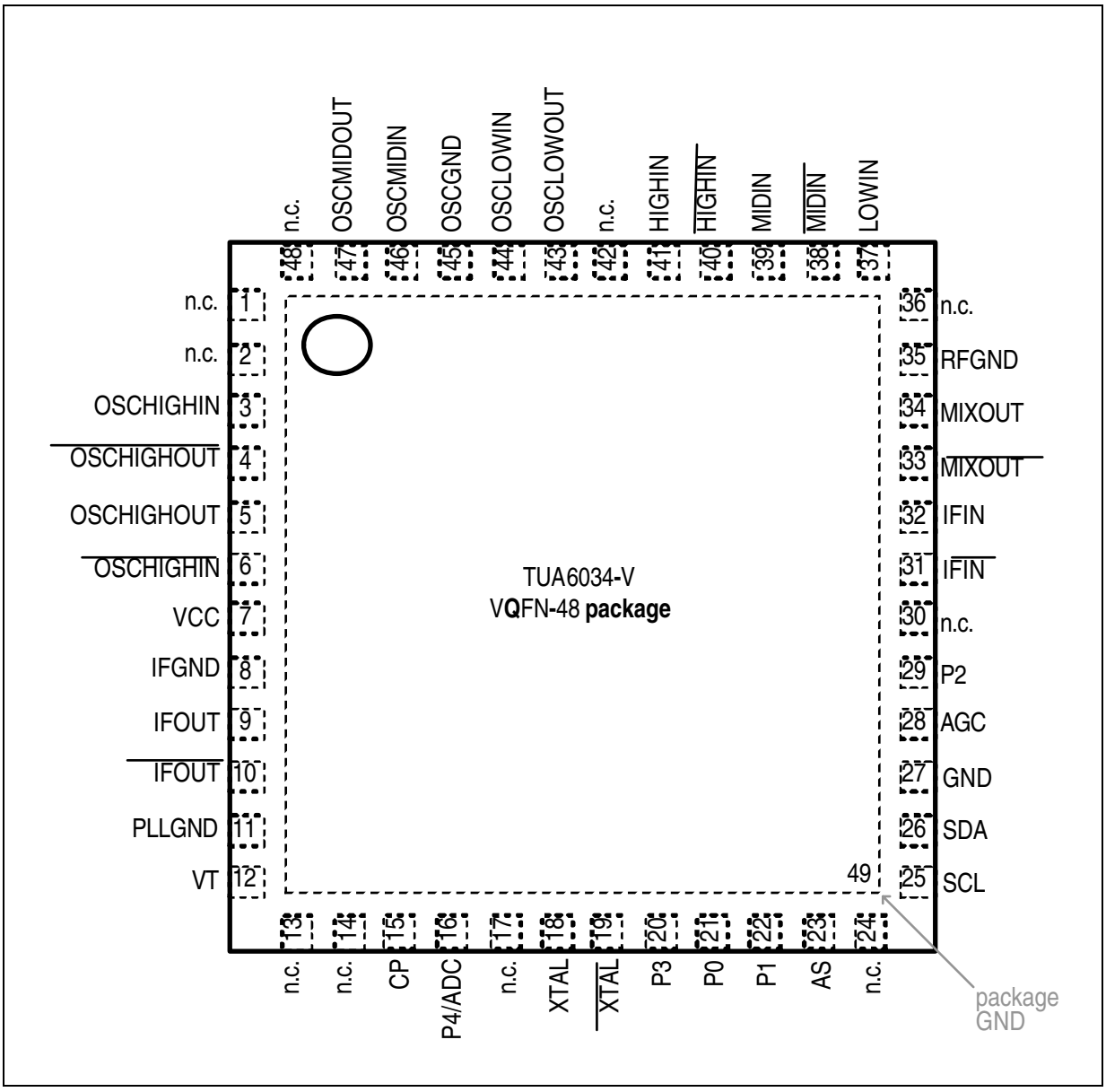
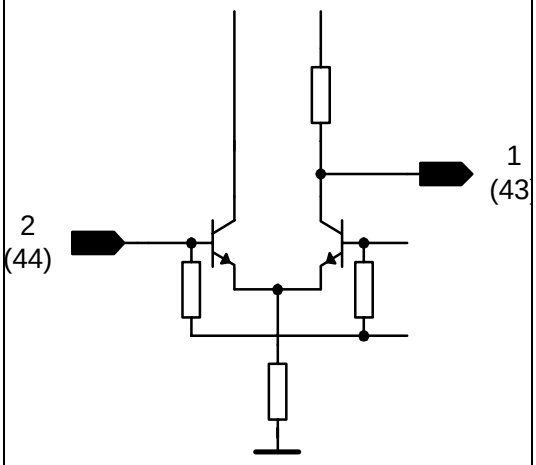
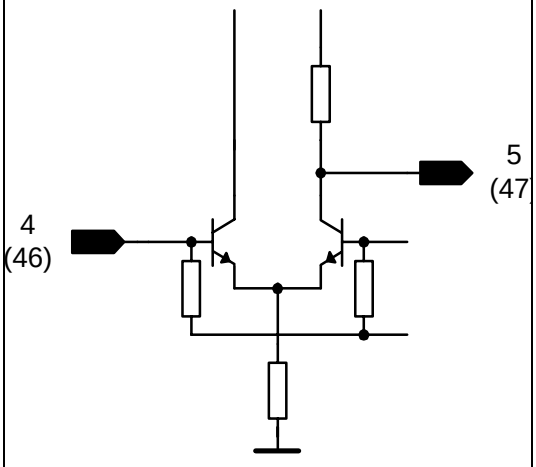
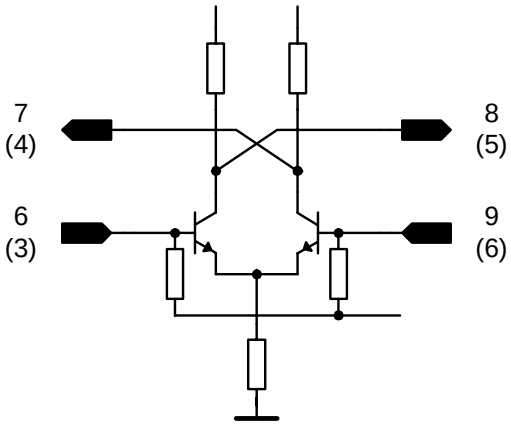
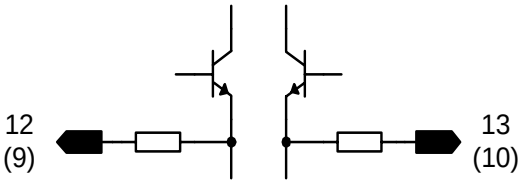


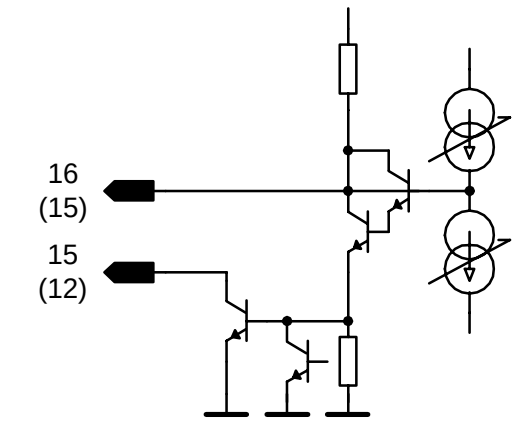
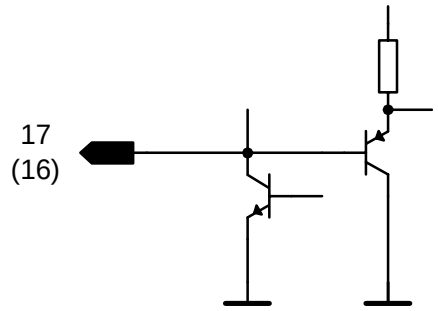
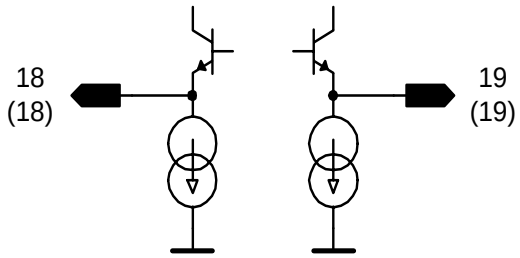
Figure 3 Pin Configuration TUA6034 in PG-VQFN-48 Package

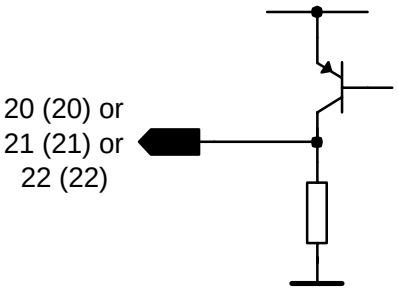
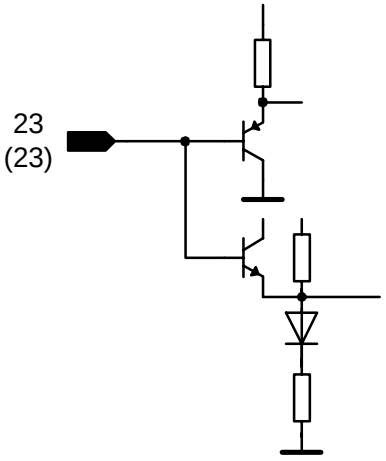
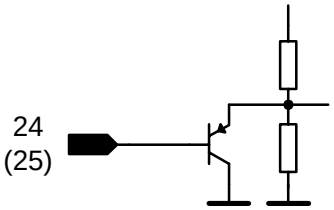
2.2 Pin Definition and Functions

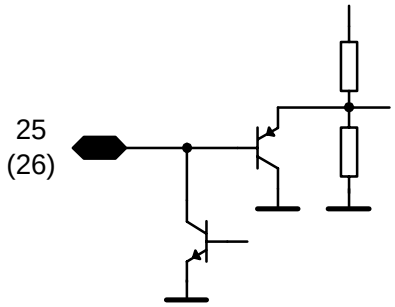
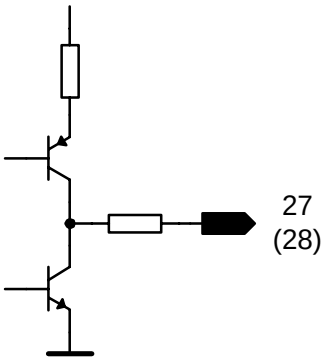
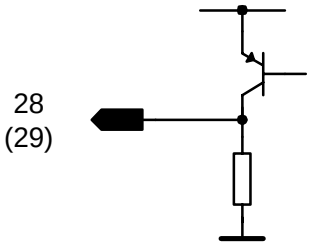
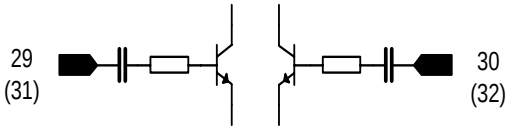
Table 4 Pin Definition and Functions

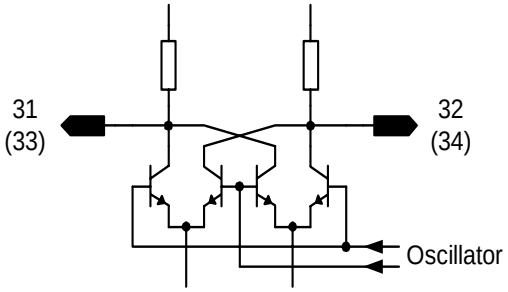
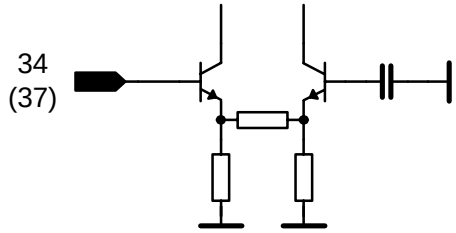
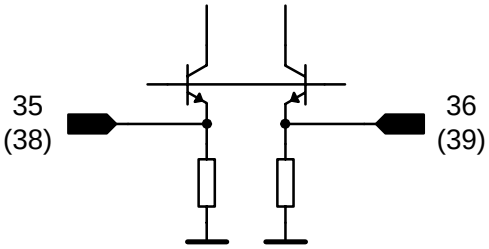
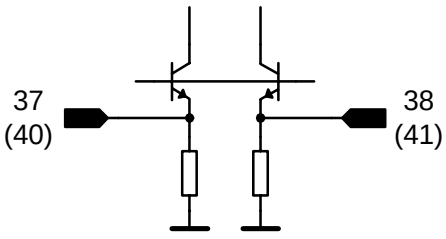
Pin No.		Symbol	Equivalent I/O Schematic pin designation in parenthesis refer to PG-VQFN-48 package	Average DC voltage		
PG-TSSOP-38	PG-VQFN-48			LOW	MID	HIGH
1/38	43	OSCLOWOUT		2.1 V		
2/37	44	OSCLOWIN		1.45 V		
3/36	45	OSCGND	oscillator ground	0.0 V	0.0 V	0.0 V
4/35	46	OSCMIDIN			1.45 V	
5/34	47	OSCMIDOUT			2.1 V	

Pin No.		Symbol	Equivalent I/O Schematic pin designation in parenthesis refer to PG-VQFN-48 package	Average DC voltage		
PG-TSSOP-38	PG-VQFN-48			LOW	MID	HIGH
6/33	3	OSCHIGHIN				1.5 V
7/32	4	OSCHIGHOUT				2.4 V
8/31	5	OSCHIGHOUT				2.4 V
9/30	6	OSCHIGHIN				1.5 V
10/29	7	VCC	supply voltage	5.0 V	5.0 V	5.0 V
11/28	8	IFGND	IF ground	0.0 V	0.0 V	0.0 V
12/27	9	IFOUT		2.2 V	2.2 V	2.2 V
13/26	10	IFOUT		2.2 V	2.2 V	2.2 V
14/25	11	PLLGND	PLL ground	0.0 V	0.0 V	0.0 V

Pin No.		Symbol	Equivalent I/O Schematic pin designation in parenthesis refer to PG-VQFN-48 package	Average DC voltage		
PG-TSSOP-38	PG-VQFN-48			LOW	MID	HIGH
15/24	12	VT		VT	VT	VT
16/23	15	CP		2.0 V	2.0 V	2.0 V
17/22	16	P4/ADC		5 V or V_{CE}	5 V or V_{CE}	5 V or V_{CE}
18/21	18	XTAL		1.7 V	1.7 V	1.7 V
19/20	19	XTAL		1.7 V	1.7 V	1.7 V

Pin No.		Symbol	Equivalent I/O Schematic pin designation in parenthesis refer to PG-VQFN-48 package	Average DC voltage		
PG-TSSOP-38	PG-VQFN-48			LOW	MID	HIGH
20/19	20	P3		0 V or V_{CC} - V_{CE}	0 V or V_{CC} - V_{CE}	0 V or V_{CC} - V_{CE}
21/18	21	P0		V_{CC} - V_{CE}	n.a.	n.a.
22/17	22	P1		n.a.	V_{CC} - V_{CE}	n.a.
23/16	23	AS		n.a.	n.a.	n.a.
24/15	25	SCL		n.a.	n.a.	n.a.

Pin No.		Symbol	Equivalent I/O Schematic pin designation in parenthesis refer to PG-VQFN-48 package	Average DC voltage		
PG-TSSOP-38	PG-VQFN-48			LOW	MID	HIGH
25/14	26	SDA		n.a	n.a	n.a
26/13	27	GND	ground	0.0	0.0	0.0
27/12	28	AGC		3.5 V	3.5 V	3.5 V
28/11	29	P2		n.a.	n.a.	0 V or V_{CC} - V_{CE}
29/10	31	IFIN		n.a.	n.a.	n.a.
30/9	32	IFIN		n.a.	n.a.	n.a.

Pin No.		Symbol	Equivalent I/O Schematic pin designation in parenthesis refer to PG-VQFN-48 package	Average DC voltage		
PG-TSSOP-38	PG-VQFN-48			LOW	MID	HIGH
31/8	33	MIXOUT		4.0 V	4.0 V	4.0 V
32/7	34	MIXOUT		4.0 V	4.0 V	4.0 V
33/6	35	RFGND	RF ground	0.0 V	0.0 V	0.0 V
34/5	37	LOWIN		1.9 V		
35/4	38	MIDIN			0.75 V	
36/3	39	MIDIN			0.75 V	
37/2	40	HIGHIN				0.75 V
38/1	41	HIGHIN				0.75 V
---	49	package GND	Exposed pad ground	0.0 V	0.0 V	0.0 V

2.3 Functional Block Diagram

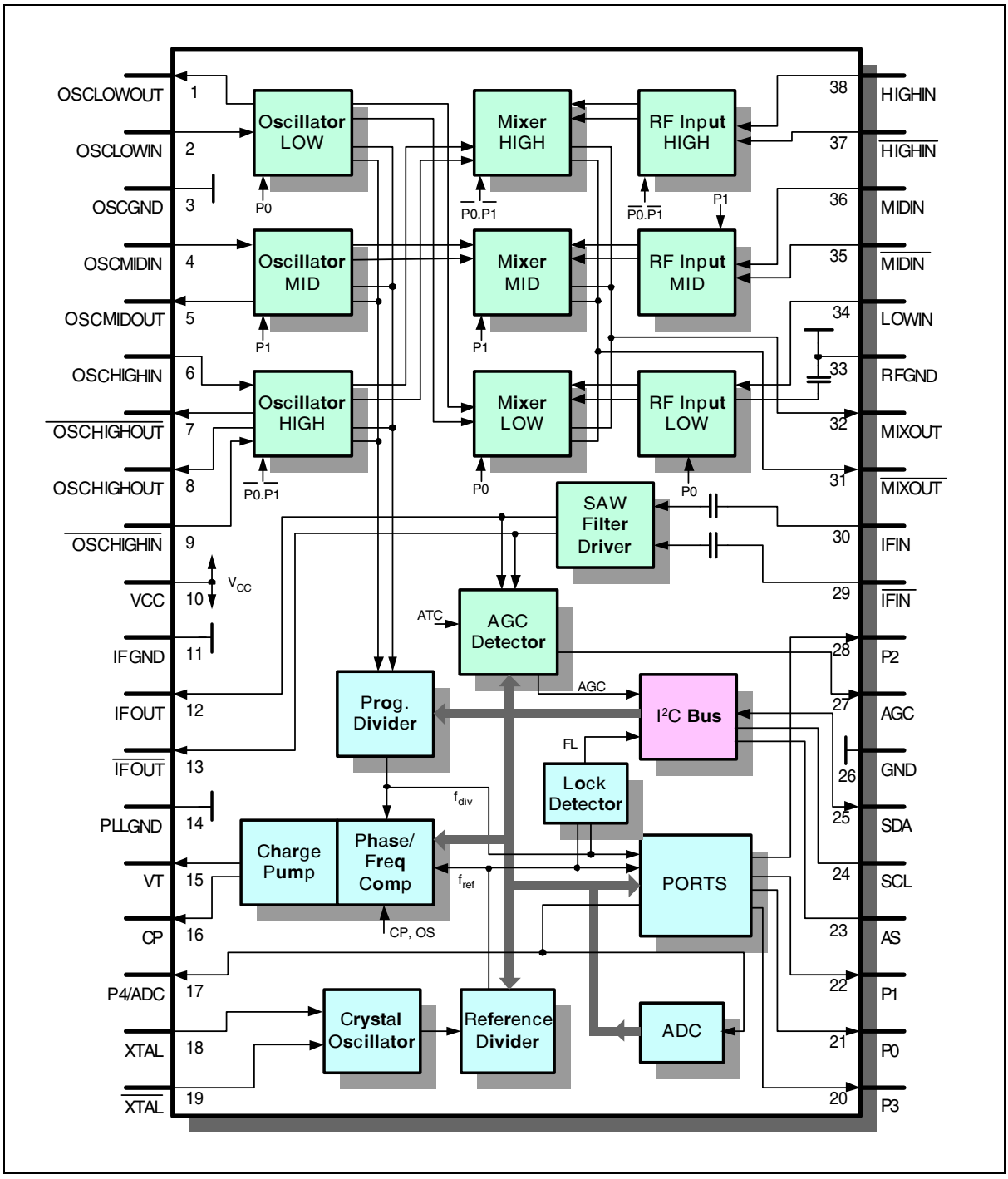


Figure 4 Block Diagram TUA6034 in PG-TSSOP-38 Package

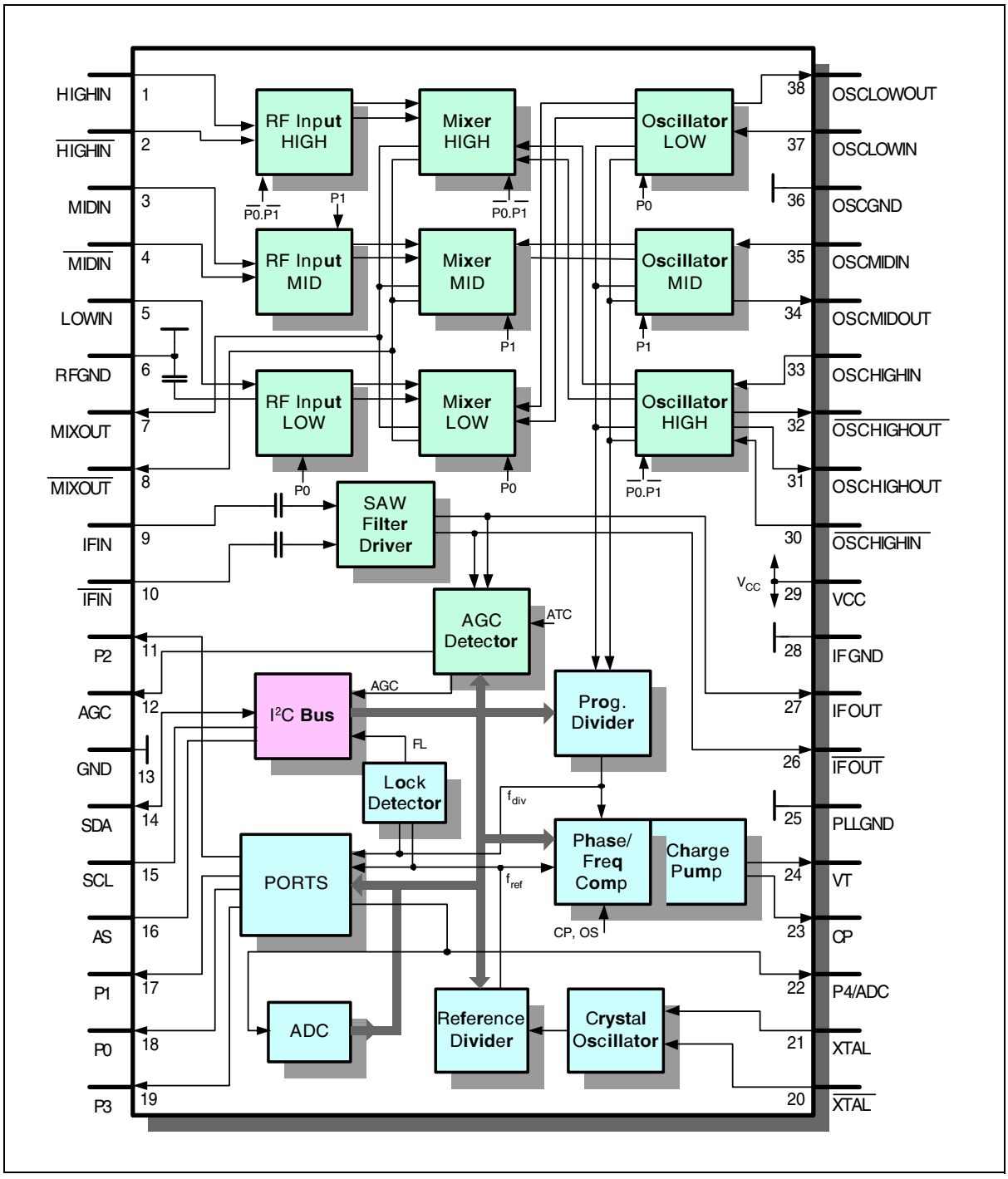


Figure 5 Block Diagram TUA6036 in PG-TSSOP-38 Package

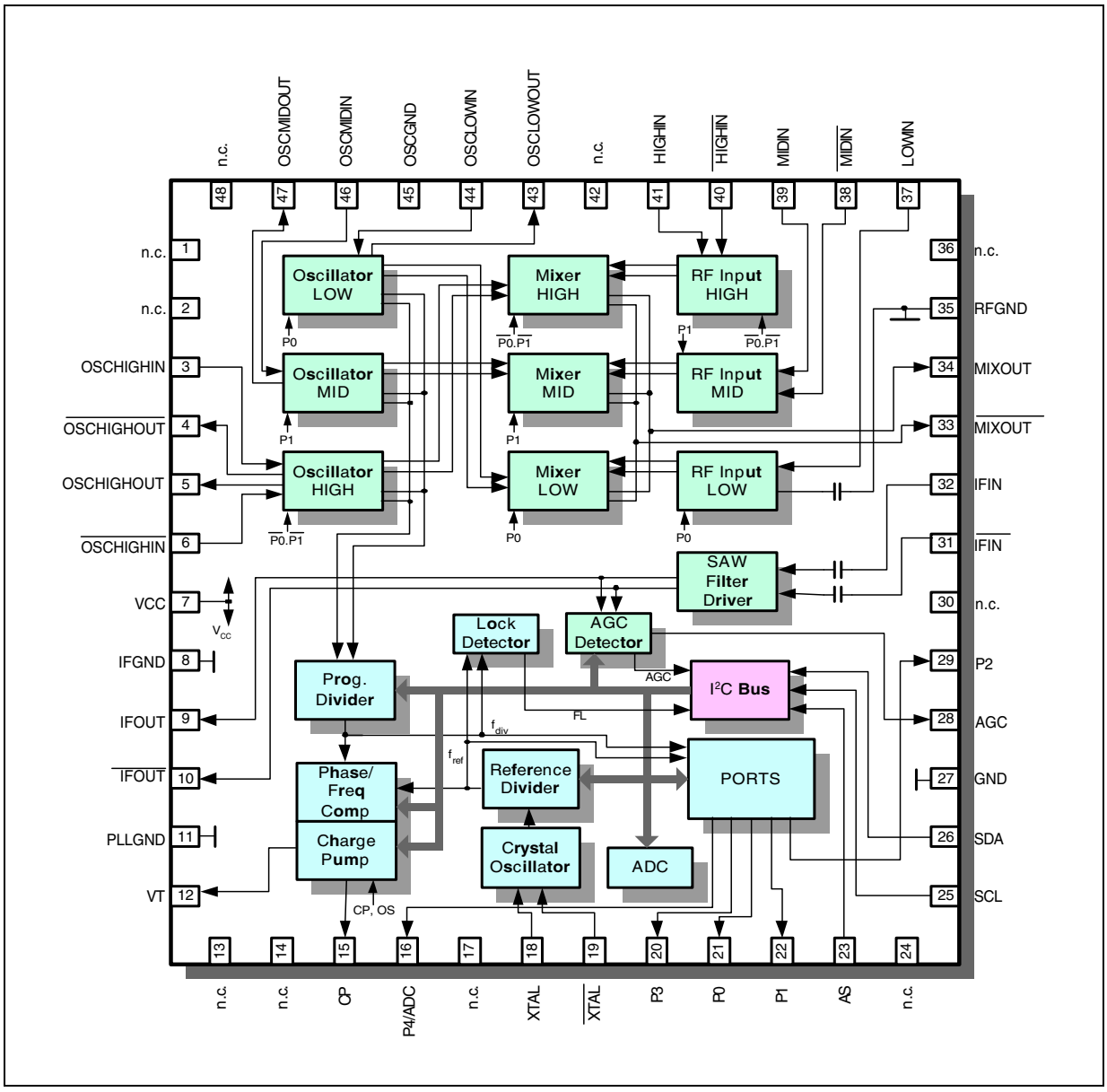


Figure 6 Block Diagram TUA6034 in PG-VQFN-48 package

2.4 Circuit Description

2.4.1 Mixer-Oscillator block

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, an IF amplifier, a reference voltage, and a band switch.

Filters between tuner input and IC separate the TV frequency signals into three bands. The band switching in the tuner front-end is done by using three PNP port outputs. In the selected band the signal passes a tuner input stage with a MOSFET amplifier, a double-tuned bandpass filter and is then fed to the mixer input of the IC which has in case of LOW band a high-impedance input and in case of MID or HIGH band a low-impedance input. The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency. The IF is filtered by means of an IF filter in between the 2 mixer output pins and the 2 input pins of the following IF amplifier. The IF amplifier has a low output impedance to drive the SAW filter directly.

2.4.2 PLL block

The oscillator signal is internally DC-coupled as a differential signal to the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio N = 256 through 32767 and is then compared in a digital frequency/phase detector with a reference frequency f_{ref} = 31.25, 50, 62.5, 125, 142.86 or 166.67 kHz. This frequency is derived from a balanced, low-impedance 4 MHz crystal oscillator (pins XTAL, $\overline{\text{XTAL}}$) divided by 128, 80, 64, 32, 28 or 24. The reference frequencies will be different with a quartz other than 4 MHz.

The phase detector has two outputs which drive four current sources of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the positive current source pulses for the duration of the phase difference. In the reverse case the negative current source pulses. If the two signals are in phase, the charge pump output (CP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pull-up resistor at VT and external RC circuitry). The charge pump output is also switched into the high-impedance state if the control bits T2, T1, T0 = 0, 1, 0. Here it should be noted, however, that the tuning voltage can alter over a long period in the high impedance state as a result of self discharge in the peripheral circuity. VT may be switched off by the control bit OS to allow external adjustments.

If the VCO is not oscillating the PLL locks to a tuning voltage of 33V (V_{TH}).

By means of control bits CP, T0, T1 and T2 the pump current can be switched between four values by software. This programmability permits alteration of the control response of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example.

The software controlled ports P0 to P4 are general purpose open-collector outputs. The test bits T2, T1, T0 =1, 0, 0 switch the test signals f_{div} (divided input signal) and f_{ref} (i.e .4 MHz / 64) to P0 and P1 respectively.

The lock detector resets the lock flag FL if the width of the charge pump current pulses is greater than the period of the crystal oscillator (i.e. 250 ns). Hence, if FL = 1, the maximum deviation of the input frequency from the programmed frequency is given by

$\Delta f = \pm I_P * (K_{VCO} / f_{XTAL}) * (C1+C2) / (C1*C2)$

where I_P is the charge pump current, K_{VCO} the VCO gain, f_{Xtal} the crystal oscillator frequency and C_1, C_2 the capacitances in the loop filter (see Chapter 3 on page 28). As the charge pump pulses at i.e. 62.5 kHz (= f_{ref}), it takes a maximum of 16 µs for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive f_{ref} periods. Therefore it takes between 128 and 144 µs for FL to be set after the loop regains lock.

2.4.3 AGC

The wide band AGC stage detects the level of the IF output signal and generates an AGC voltage for gain control of the tuners input transistors. The AGC take-over and the time constant are selectable by the I^2C bus.

2.4.4 I^2C-Bus Interface

Data is exchanged between the processor and the PLL via the I^2C bus. The clock is generated by the processor (input SCL). Pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have a hysteresis and a low-pass characteristic, which enhance the noise immunity of the I^2C bus.

The data from the processor pass through an I^2C bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are high). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes low, while SCL remains high. Stop condition: SDA goes high while SCL remains high. All further information transfer takes place during SCL = low, and the data is forwarded to the control logic on the positive clock edge.

The table ’Bit Allocation’ (see Table 8 Bit Allocation Read/Write on page 50) should be referred to for the following description. All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to low

(acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (address select). The LSB bit (R/W) determines whether data are written into (R/W = 0) or read from (R/W = 1) the PLL.

In the data portion of the telegram during a WRITE operation, the MSB bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type has to follow the first byte. Appropriate setting of the test bits will decide whether the band-switch byte or the auxiliary byte will be transmitted (see Table 11 Test modes on page 51).

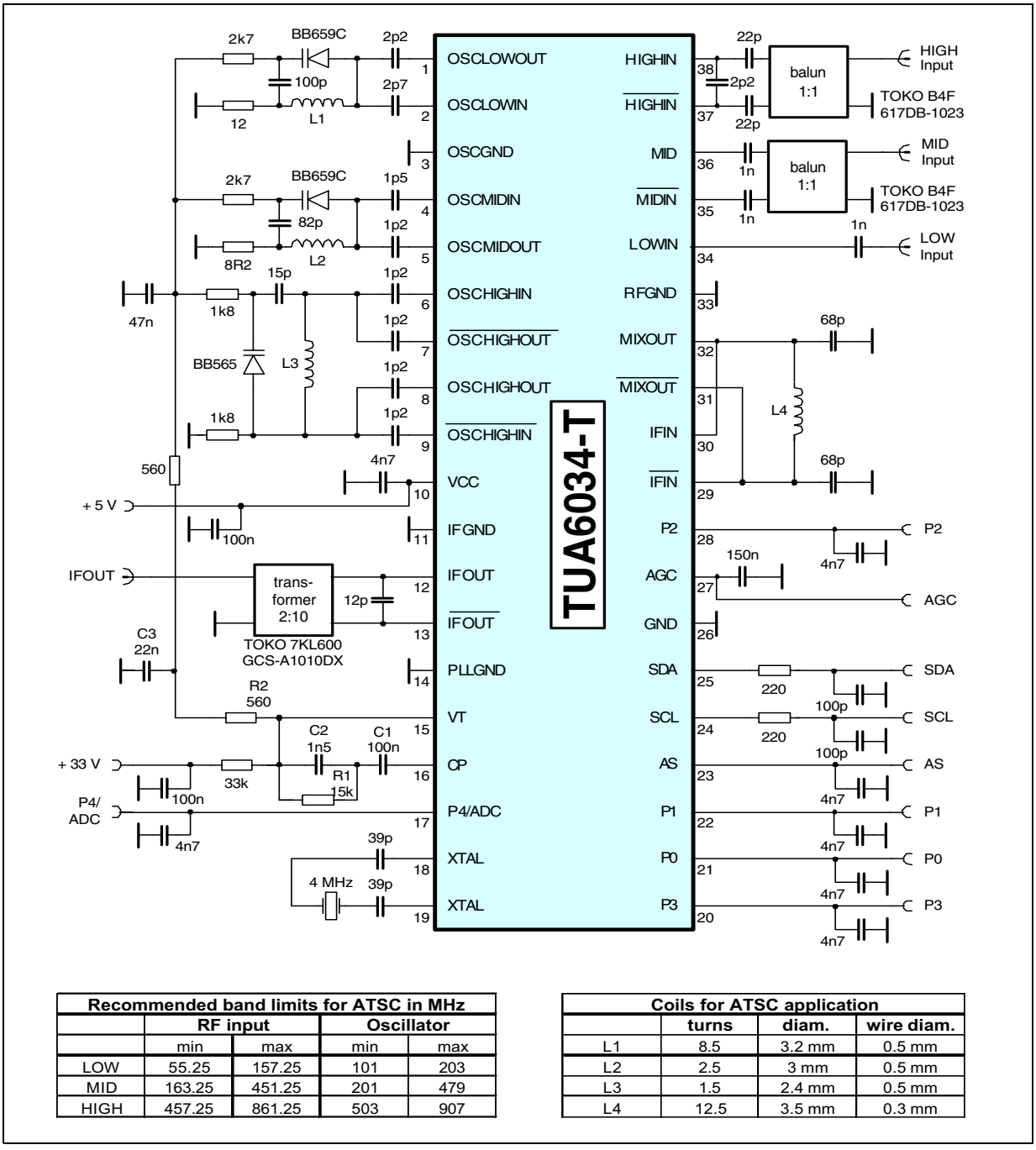
If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line is released to allow the processor to generate a stop condition. The status word consists of three bits from the A/D converter, the lock flag and the power-on flag.

Four different chip addresses can be set by an appropriate DC level at pin AS (see Table 10 Address selection on page 51).

While the supply voltage is applied, a power-on reset circuit prevents the PLL from setting the SDA line to low, which would block the bus. The power-on reset flag POR is set at power-on and if V_{CC} falls below 3.2 V. It will be reset at the end of a READ operation.

3 Applications

3.1 Application Circuit TUA6034-T for ATSC



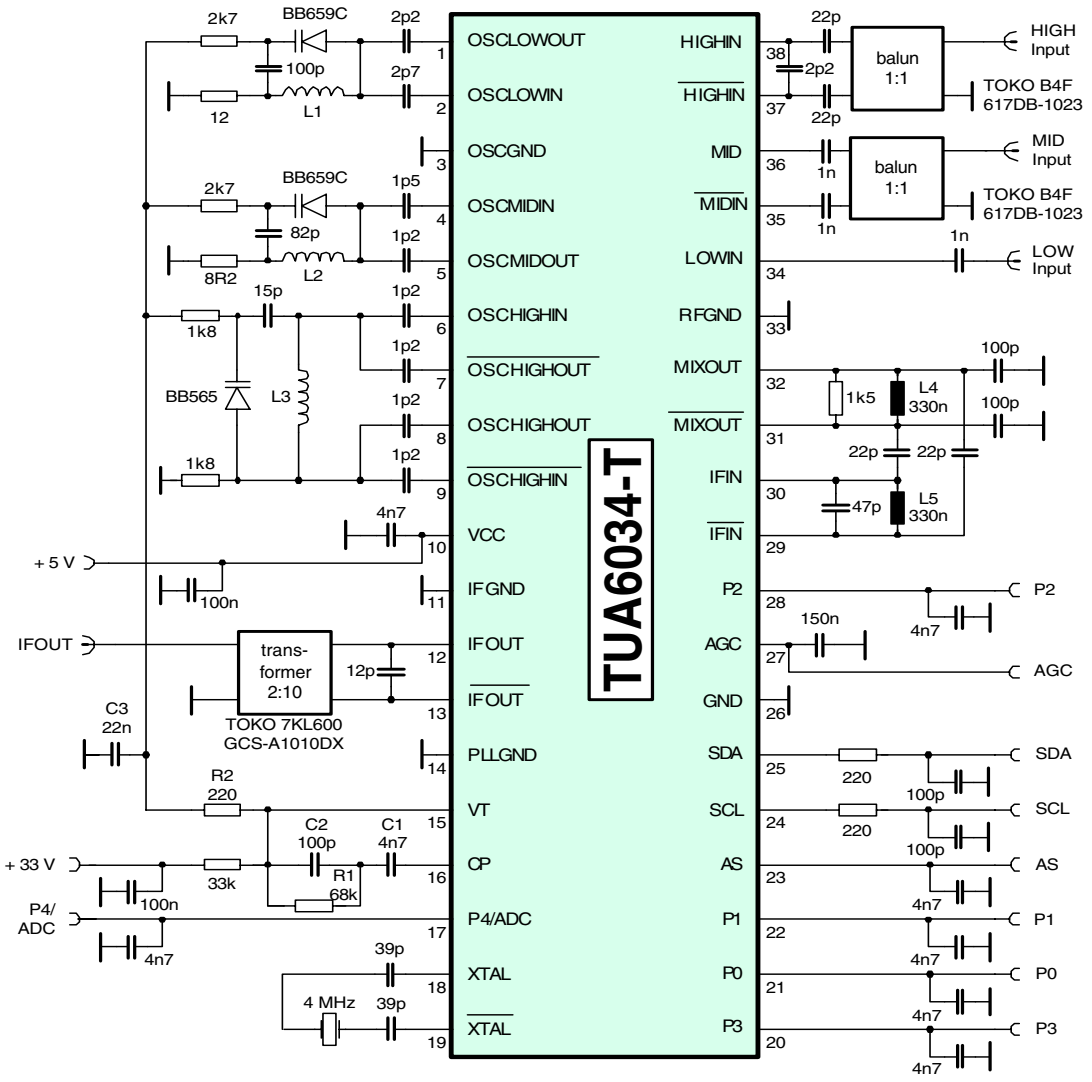
Recommended band limits for ATSC in MHz				
	RF input		Oscillator	
	min	max	min	max
LOW	55.25	157.25	101	203
MID	163.25	451.25	201	479
HIGH	457.25	861.25	503	907

Coils for ATSC application			
	turns	diam.	wire diam.
L1	8.5	3.2 mm	0.5 mm
L2	2.5	3 mm	0.5 mm
L3	1.5	2.4 mm	0.5 mm
L4	12.5	3.5 mm	0.3 mm

Figure 7 Application Circuit TUA6034-T for ATSC

Remark: TUA 6036 has reversed pinning.

3.2 Application Circuit TUA6034-T for DVB-T



Recommended band limits for DVB-T in MHz				
	RF input		Oscillator	
	min	max	min	max
LOW	48.25	154.25	87.15	193.15
MID	161.25	439.25	200.15	478.15
HIGH	447.25	863.25	486.15	902.15

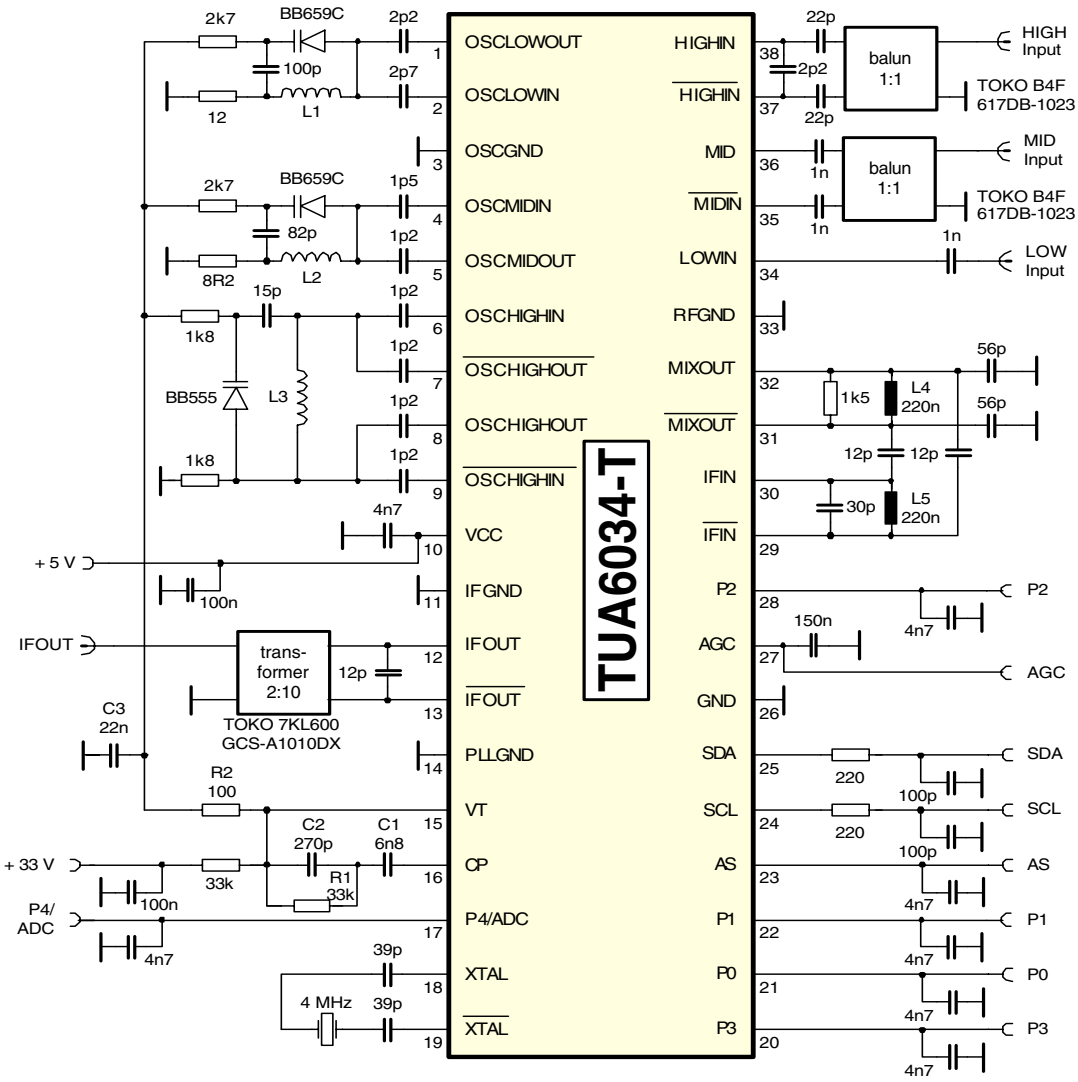
Coils for DVB-T application			
	turns	diam.	wire diam.
L1	8.5	3.2 mm	0.5 mm
L2	2.5	3 mm	0.5 mm
L3	1.5	2.4 mm	0.5 mm
L4, L5	SMD	0805	330n

SMD = Surface Mounted Device

Figure 8 Application Circuit TUA6034-T for DVB-T

Remark: TUA 6036 has reversed pinning.

3.3 Application Circuit TUA6034-T for ISDB-T



Recommended band limits for ISDB-T in MHz				
	RF input		Oscillator	
	min	max	min	max
LOW	93	167	150	224
MID	173	467	230	524
HIGH	473	767	530	824

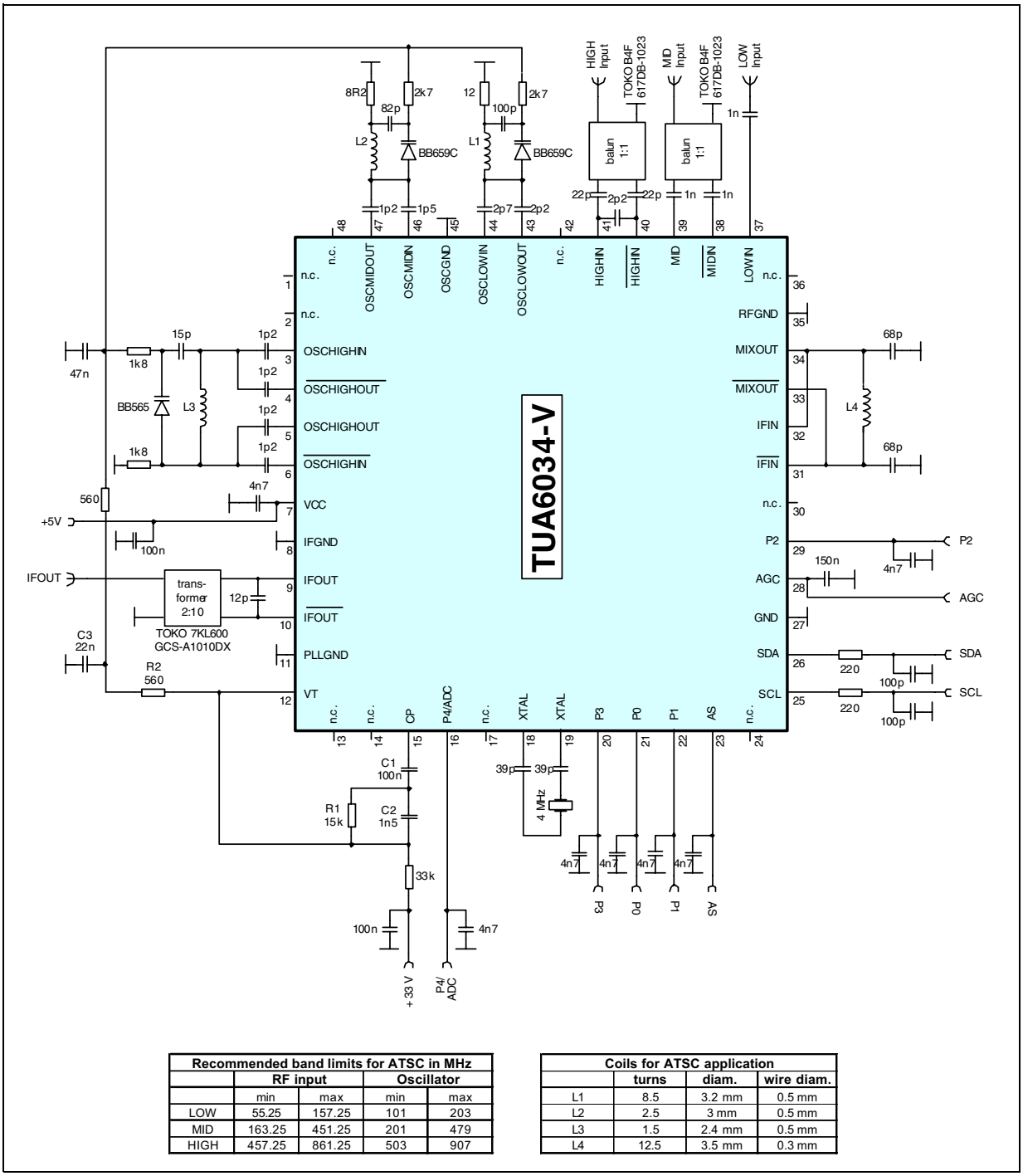
Coils for ISDB-T application			
	turns	diam.	wire diam.
L1	8.5	3.2 mm	0.5 mm
L2	2.5	3 mm	0.5 mm
L3	1.5	2.4 mm	0.5 mm
L4, L5	SMD	0805	220n

SMD = Surface Mounted Device

Figure 9 Application Circuit TUA6034-T for ISDB-T

Remark: TUA 6036 has reversed pinning.

3.4 Application Circuit TUA6034-V for ATSC

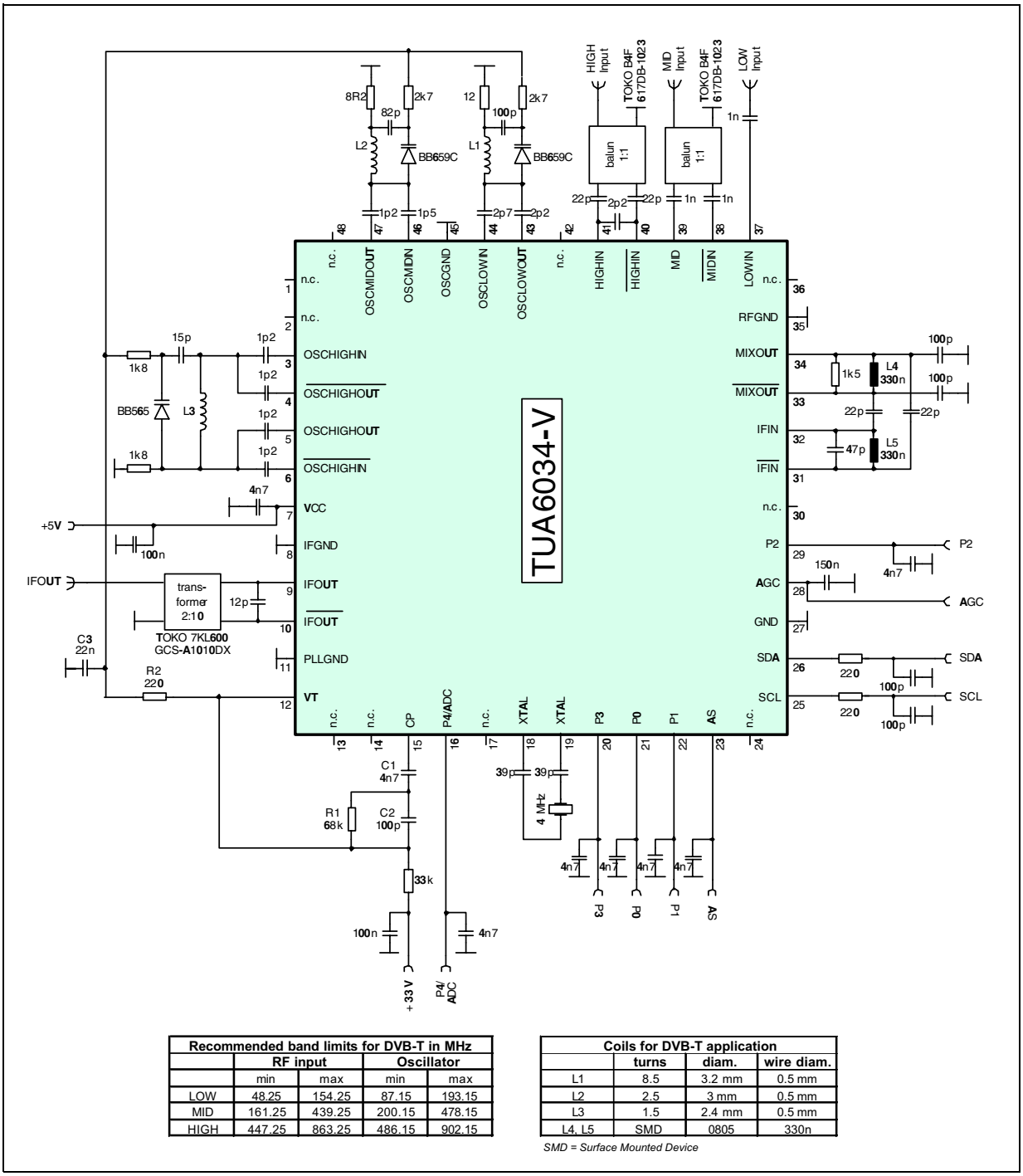


Recommended band limits for ATSC in MHz				
	RF input		Oscillator	
	min	max	min	max
LOW	55.25	157.25	101	203
MID	163.25	451.25	201	479
HIGH	457.25	861.25	503	907

Coils for ATSC application			
	turns	diam.	wire diam.
L1	8.5	3.2 mm	0.5 mm
L2	2.5	3 mm	0.5 mm
L3	1.5	2.4 mm	0.5 mm
L4	12.5	3.5 mm	0.3 mm

Figure 10 Application Circuit TUA6034-V for ATSC

3.5 Application Circuit TUA6034-V for DVB-T



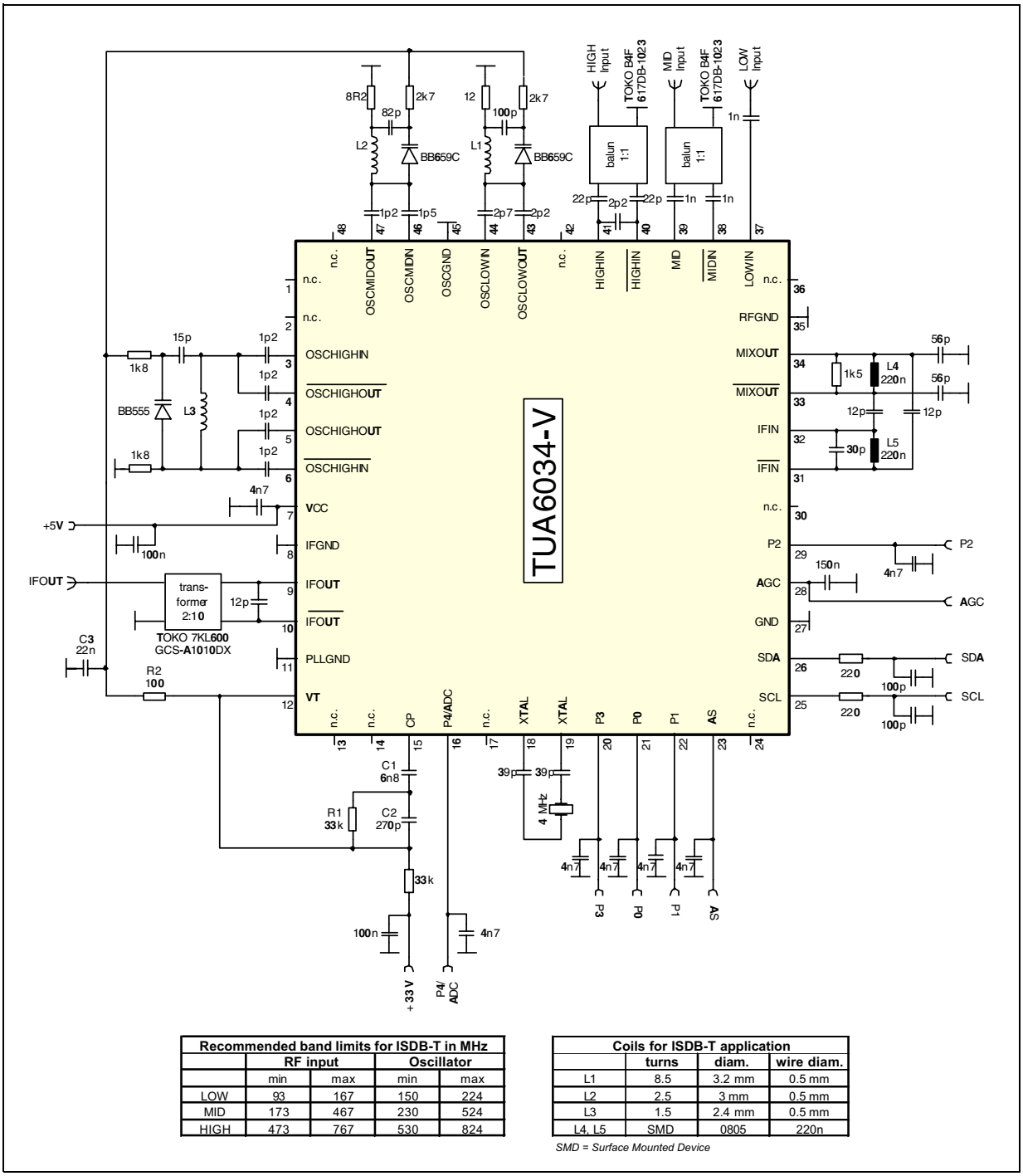
Recommended band limits for DVB-T in MHz				
	RF input		Oscillator	
	min	max	min	max
LOW	48.25	154.25	87.15	193.15
MID	161.25	439.25	200.15	478.15
HIGH	447.25	863.25	486.15	902.15

Coils for DVB-T application			
	turns	diam.	wire diam.
L1	8.5	3.2 mm	0.5 mm
L2	2.5	3 mm	0.5 mm
L3	1.5	2.4 mm	0.5 mm
L4, L5	SMD	0805	330n

SMD = Surface Mounted Device

Figure 11 Application Circuit TUA6034-V for DVB-T

3.6 Application Circuit TUA6034-V for ISDB-T



Recommended band limits for ISDB-T in MHz				
	RF input		Oscillator	
	min	max	min	max
LOW	93	167	150	224
MID	173	467	230	524
HIGH	473	767	530	824

Coils for ISDB-T application			
	turns	diam.	wire diam.
L1	8.5	3.2 mm	0.5 mm
L2	2.5	3 mm	0.5 mm
L3	1.5	2.4 mm	0.5 mm
L4, L5	SMD	0805	220n

SMD = Surface Mounted Device

Application Circuit TUA6034-V for ISDB-T

4 Reference

4.1 Electrical Data

4.1.1 Absolute Maximum Ratings

Attention: The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 5 Absolute Maximum Ratings

#	Parameter[1)]	Symbol	Limit Values		Unit	Remarks
			min.	max.		
1.	Supply voltage	V_{CC}	-0.3	6	V	
2.	Ambient temperature	T_A	-40	T_{Amax} [2)]	°C	
3.	Junction temperature	T_J		+125	°C	
4.	Storage temperature	T_{Stg}	-40	+125	°C	
5.	Temperature difference junction to case[3)]	T_{JC}		2	K	
PLL						
6.	CP	V_{CP}	-0.3	3	V	
7.		I_{CP}		1	mA	
8.	Crystal oscillator pin XTAL	V_Q		6	V	
9.		I_Q	-5		mA	
10.	Bus input/output SDA	V_{SDA}	-0.3	6	V	
11.	Bus output current SDA	$I_{SDA(L)}$		10	mA	open collector
12.	Bus input SCL	V_{SCL}	-0.3	6	V	
13.	Chip address switch AS	V_{AS}	-0.3	6	V	
14.	VCO tuning output (loop filter)	V_{VT}	-0.3	35	V	
15.	NPN port output voltage of P4	V_{P4}	-0.3	6	V	open collector

#	Parameter[1)]	Symbol	Limit Values		Unit	Remarks
			min.	max.		
16.	NPN port output current of P4	$I_{P4(L)}$	-1	10	mA	open collector, t_{max} = 0.1 s at 5.5 V
17.	P4/ADC input/output voltage	$V_{P4/ADC}$	-0.3	6	V	
18.	NPN port output current of P4	$I_{P4/ADC(L)}$	-1	10	mA	open collector, t_{max} = 0.1 s at 5.5 V
19.	PNP port output voltage of P0, P1, P2, P3	$V_{P0, 1, 2, 3}$	-0.3	6	V	open collector
20.	PNP port output current of P1	$I_{P1(L)}$	+1	-25	mA	open collector, t_{max} = 0.1 s at 5.5 V
21.	PNP port output current of P0	$I_{P0(L)}$	+1	-10	mA	open collector, t_{max} = 0.1 s at 5.5 V
22.	PNP port output current of P2, P3	$I_{P2, 3(L)}$	+1	-5	mA	open collector, t_{max} = 0.1 s at 5.5 V
23.	Total port output current of PNP ports	$\Sigma I_{P(L)}$		-40	mA	t_{max} = 0.1 s at 5.5 V
Mixer-Oscillator						
24.	Mix inputs LOW band	V_{LOW}	-0.3	3	V	
25.	Mix inputs MID/HIGH band	$V_{MID/HIGH}$		2	V	
26.		$I_{MID/HIGH}$	-5	6	mA	
27.	VCO base voltage	V_B	-0.3	3	V	LOW, MID and HIGH band oscillators
28.	VCO collector voltage	V_C		6	V	LOW, MID and HIGH band oscillators
29.	AGC output	V_{AGC}	-0.3	4	V	
30.		I_{AGC}		1	mA	
31.	Voltage on all other input and output pins except GNDs	V_{max}	-0.3	V_{CC}	V	

#	Parameter[1)]	Symbol	Limit Values		Unit	Remarks
			min.	max.		
ESD-Protection[4)]						
32.	all pins	V_{ESD}		2	kV	

1) All values are referred to ground (pin), unless stated otherwise.
Currents with a positive sign flow into the pin and currents with a negative sign flow out of pin.

2) The maximum ambient temperature depends on the mounting conditions of the package. Any application mounting must guarantee not to exceed the maximum junction temperature of 125 °C. As reference the temperature difference junction to case is given.

3) Referred to top center of package.

4) According to EIA/JESD22-A114-B (HBM incircuit test), as a single device incircuit contact discharge test.

4.1.2 Operating Range

Table 6 Operating Range

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
1.	Supply voltage	V_{CC}	+4.5	+5.5	V	
2.	Programmable divider factor	N	256	32767		
3.	LOW mixer input frequency range	f_{MIXV}	30	200	MHz	
4.	MID and HIGH band mixer input frequency range	f_{MIXU}	130	900	MHz	
5.	LOW oscillator frequency range	f_{OH}	65	250	MHz	
6.	MID band oscillator frequency range	f_{OU}	165	530	MHz	
7.	HIGH band oscillator frequency range	f_{OU}	400	950	MHz	
8.	Ambient temperature	T_A	-20	T_{Amax}[1)]	°C	

1) see 4.1.1 Absolute Maximum Ratings on page 34.

4.1.3 AC/DC Characteristics

Table 7 AC/DC Characteristics, $T_A = 25°C$, $V_{CC} = 5V$

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
Supply								
1.	Supply voltage	V_{CC}	4.5	5	5.5	V		
2.	Current consumption in active mode	I_{VCC}	59	74	89	mA	LOW band	
3.		I_{VCC}	59	74	89	mA	MID band	
4.		I_{VCC}	57	71	85	mA	HIGH band	
5.	Current consumption in power down mode	I_{stby}		20		mA	P0, P1 = 1	
Digital Part								
PLL								
Crystal oscillator connections XTAL								
6.	Crystal frequency	f_{XTAL}	3.2	4.0	4.8	MHz	series resonance	
7.	Crystal resistance	R_{XTAL}		30	300	Ω	series resonance	
8.	Oscillation frequency	f_{XTAL}	3,99975	4,000	4,00025	MHz	f_{XTAL} = 4 MHz	
9.	Input impedance	Z_{XTAL}		-650	-500	Ω	f_{XTAL} = 4 MHz	
Charge pump output CP								
10.	Output current, see Table 15 Charge pump current on page 53	I_{CPDH}	± 430	± 650	± 860	µA	V_{CP} = 1.8 V	
11.		I_{CPH}	± 180	± 250	± 360	µA	V_{CP} = 1.8 V	
12.		I_{CPDL}	± 90	± 125	± 180	µA	V_{CP} = 1.8 V	
13.		I_{CPL}	± 35	± 50	± 70	µA	V_{CP} = 1.8 V	
14.	Tristate current	I_{CPZ}		± 1		nA	T2, T1, T0 = 0,1,0, V_{CP} = 2 V	
15.	Output voltage	V_{CP}	1.0		2.5	V	loop locked	
Tuning voltage output VT (open collector)								
16.	Leakage current	I_{TH}			10	µA	V_{TH} = 33 V, OS = 1	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
17.	Output voltage when the loop is closed, (test mode in normal operation)	V_{TL}	0.4		32.7	V	OS = 0, R_{Load} = 33 kΩ, tuning supply = 33 V	
I^2C-Bus								
Bus inputs SCL, SDA								
18.	High-level input voltage	V_{IH}	2.3		5.5	V		
19.	Low-level input voltage	V_{IL}	0		1.5	V		
20.	High-level input current	I_{IH}			10	µA	V_{bus} = 5.5 V, V_{CC} = 0 V	
21.		I_{IH}			10	µA	V_{bus} = 5.5 V, V_{CC} = 5.5 V	
22.	Low-level input current	I_{IL}			10	µA	V_{bus} = 1.5 V, V_{CC} = 0 V	
23.		I_{IL}	-10			µA	V_{bus} = 0 V, V_{CC} = 5.5 V	
Bus output SDA (open collector)								
24.	Leakage current	I_{OH}			10	µA	V_{OH} = 5.5 V	
25.	Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 3 mA	
Edge speed SCL,SDA								
26.	Rise time	t_r			300	ns		
27.	Fall time	t_f			300	ns		
Clock timing SCL								
28.	Frequency	f_{SCL}	0	100	400	kHz		
29.	High pulse width	t_H	0.6			µs		
30.	Low pulse width	t_L	1.3			µs		
Start condition								
31.	Set-up time	t_{susta}	0.6			µs		

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
32.	Hold time	t_{hsta}	0.6			µs		
Stop condition								
33.	Set up time	t_{susto}	0.6			µs		
34.	Bus free	t_{buf}	1.3			µs		
Data transfer								
35.	Set-up time	t_{sudat}	0.1			µs		
36.	Hold time	t_{hdat}	0			µs		
37.	Input hysteresis SCL, SDA	V_{hys}		200		mV		
38.	Pulse width of spikes which are suppressed	t_{sp}	0		50	ns		
39.	Capacitive load for each bus line	C_L			400	pF		
PNP port outputs P0, P1, P2, P3 (open collector)								
40.	Port output voltage	$V_{POH0to3}$		0.05	0.4	V	$I_{POLH0to3}$ = 0 mA, port disabled	
41.	Output saturation voltage port 0	$V_{PL0} = V_{CC} - V_{CESat0}$		0.25	0.4	V	I_{POL0} = 10 mA, port enabled	
42.	Output saturation voltage port 1	$V_{PL1} = V_{CC} - V_{CESat1}$		0.25	0.4	V	I_{POL1} = 15 mA port enabled	
43.	Output saturation voltage ports 2, 3	$V_{PL2,3} = V_{CC} - V_{CESat2,3}$		0.25	0.4	V	$I_{POL2,3}$ = 5 mA port enabled	
NPN port output P4 (open collector)								
44.	Output leakage current	I_{POH4}			10	µA	V_{CC} = 5.5, V_{Pn4} = 6 V	
45.	Output saturation voltage	V_{PL04}		0.25	0.4	V	I_{POL4} = 5 mA	
ADC input								
46.	ADC input voltage	V_{ADC}	0		5.5	V		

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
47.	High-level input current	I_{ADCH}			10	µA		
48.	Low-level input current	I_{ADCL}	-10			µA		
Address selection input AS								
49.	High-level input current	I_{ASH}			50	µA	V_{ASH} = 5.5 V	
50.	Low-level input current	I_{ASL}	-50			µA	V_{ASL} = 0 V	
Analog Part								
LOW band mixer mode (P0 = 1, P1 = 0, including IF amplifier)								
51.	RF frequency	f_{RF}	44.25		170.25	MHz	picture carrier [1)]	
52.	Voltage gain	G_V	23.5	26	28.5	dB	f_{RF} = 44.25 MHz, see 4.5.1 on page 59	
53.		G_V	23.5	26	28.5	dB	f_{RF} =170.25 MHz, see 4.5.1 on page 59	
54.	Noise figure	NF		8	10	dB	f_{RF} = 50 MHz, see 4.5.4 on page 60 see 4.5.3 on page 60	
55.		NF		8	10	dB	f_{RF} =150 MHz, see 4.5.4 on page 60 see 4.5.3 on page 60	
56.	Output voltage causing 0.8% of crossmodulation in channel	V_o		113		dBµV	f_{RF} = 48.25 MHz, see 4.5.6 on page 61	
57.		V_o		113		dBµV	f_{RF} = 154.25 MHz, see 4.5.6 on page 61	
58.	Input IP2	IIP2		160		dBµV	f_{RF1} = 48.25 MHz f_{RF2} = 97.50 MHz, $P_{RF1} = P_{RF2}$	
59.		IIP2		145		dBµV	f_{RF1} = 154.25 MHz f_{RF2} = 309.50 MHz, $P_{RF1} = P_{RF2}$	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
60.	Input IP3	IIP3		118		dBµV	f_{RF1} = 48.25 MHz f_{RF2} = 49.25 MHz $P_{RF1} = P_{RF2}$	
61.		IIP3		117		dBµV	f_{RF1} = 154.25 MHz f_{RF2} = 155.25 MHz, $P_{RF1} = P_{RF2}$	
62.	Output voltage causing 1 dB compression	V_o		124		dBµV	f_{RF} = 48.25 MHz	
63.		V_o		124		dBµV	f_{RF} = 154.25 MHz	
64.	Output voltage causing 1.1 kHz incidental FM	V_o	108	111		dBµV	f_{RF} = 48.25 MHz [2)]	
65.		V_o	108	111		dBµV	f_{RF} = 154.25 MHz [2.)]	
66.	Local oscillator FM caused by I^2C communication	FM_{I2C}			2.12	kHz	f_{RF} = 154.25 MHz [3)]	
67.	750 Hz Pulling	V_i	88			dBµV	f_{RF} = 154.25 MHz [4)]	
68.	Channel S02 beat	INT_{S02}	57	60		dBc	P_{RF} = 115 dBµV at IF output [5)]	
69.	Channel A-5 beat	INT_{A-5}	57	60		dBc	P_{RF} = 115 dBµV at IF output [6)]	
70.	Channel CH6 color beat	INT_{CH6}	63	66		dBc	$P_{RF1} = P_{RF2}$ = 80 dBµV[7)]	
71.	RF input level without lock-out	V_i			120	dBµV	[8)]	
72.	Input conductance $Y_i = (g_p + j\omega C_p)$	g_p		0.15		mS	f_{RF} = 48.25 to 154.25 MHz, see 4.4.1 on page 56	
73.	Input capacitance	C_p		1		pF	f_{RF} = 48.25 to 154.25 MHz, see 4.4.1 on page 56	
Mid band mixer mode (P0 = 0, P1 =1, including IF amplifier)								
74.	RF frequency	f_{RF}	154.25		454.25	MHz	picture carrier [1.)]	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
75.	Voltage gain	G_V	33	36	39	dB	f_{RF} = 161.25 MHz, see 4.5.2 on page 59	
76.		G_V	33	36	39	dB	f_{RF} = 439.25 MHz, see 4.5.2 on page 59	
77.	Noise figure (not corrected for image)	NF		6	8	dB	f_{RF} = 161.25 MHz, see 4.5.5 on page 61	
78.		NF		6	8	dB	f_{RF} = 300 MHz, see 4.5.5 on page 61	
79.	Output voltage causing 0.8% of crossmodulation in channel	V_o		112		dBµV	f_{RF} = 161.25 MHz, see 4.5.7 on page 62	
80.		V_o		112		dBµV	f_{RF} = 439.25 MHz, see 4.5.7 on page 62	
81.	Input IP2	IIP2		146		dBµV	f_{RF1} = 161.25 MHz f_{RF2} = 323.50 MHz, $P_{RF1} = P_{RF2}$	
82.		IIP2		140		dBµV	f_{RF1} = 440.25 MHz f_{RF2} = 818.50 MHz, $P_{RF1} = P_{RF2}$	
83.	Input IP3	IIP3		105		dBµV	f_{RF1} = 161.25 MHz f_{RF2} = 162.25 MHz $P_{RF1} = P_{RF2}$	
84.		IIP3		106		dBµV	f_{RF1} = 439.25 MHz f_{RF2} = 440.25 MHz $P_{RF1} = P_{RF2}$	
85.	Output voltage causing 1 dB compression	V_o		124		dBµV	f_{RF} = 161.25 MHz	
86.		V_o		124		dBµV	f_{RF} = 439.25 MHz	
87.	Output voltage causing 1.1 kHz incidental FM	V_o	108	111		dBµV	f_{RF} = 161.25 MHz 2.)	
88.		V_o	108	111		dBµV	f_{RF} = 439.25 MHz 2.)	
89.	Local oscillator FM caused by I^2C communication	FM_{I2C}			2.12	kHz	f_{RF} = 439.25 MHz 3.)	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
90.	N+5 - 1 MHz pulling	N+5 - 1 MHz	77	80		dBµV	f_{RFw} = 359.25 MHz, f_{OSC} = 398.15 MHz, f_{RFu} = 399.25 MHz 9)	
91.	750 Hz Pulling	V_i	78			dBµV	f_{RF} = 439.25 MHz 4.)	
92.	RF input level without lock-out	V_i			120	dBµV	8.)	
93.	Input impedance $Z_i = (R_s + j\omega L_s)$	R_s		35		Ω	f_{RF} = 161.25 MHz, see 4.4.2 on page 56	
94.		R_s		35		Ω	f_{RF} = 439.25 MHz, see 4.4.2 on page 56	
95.		L_s		8		nH	f_{RF} = 161.25 MHz, see 4.4.2 on page 56	
96.		L_s		8		nH	f_{RF} = 439.25 MHz, see 4.4.2 on page 56	
HIGH band mixer mode (P0 = 0, P1 = 0, including IF amplifier)								
97.	RF frequency	f_{RF}	399.25		863.25	MHz	picture carrier 1.)	
98.	Voltage gain	G_V	33	36	39	dB	f_{RF} = 447.25 MHz, see 4.5.2 on page 59	
99.		G_V	33	36	39	dB	f_{RF} = 863.25 MHz, see 4.5.2 on page 59	
100.	Noise figure (not corrected for image)	NF		6	8	dB	f_{RF} = 447.25 MHz, see 4.5.5 on page 61	
101.		NF		7	9	dB	f_{RF} = 863.25 MHz, see 4.5.5 on page 61	
102.	Output voltage causing 0.8% of crossmodulation in channel	V_o		112		dBµV	f_{RF} = 447.25 MHz, see 4.5.7 on page 62	
103.		V_o		112		dBµV	f_{RF} = 863.25 MHz, see 4.5.7 on page 62	
104.	Input IP2	IIP2		136		dBµV	f_{RF1} = 447.25 MHz f_{RF2} = 895.50 MHz $P_{RF1} = P_{RF2}$	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
105.	Input IP3	IIP3		106		dBµV	f_{RF1} = 447.25 MHz f_{RF2} = 448.25 MHz $P_{RF1} = P_{RF2}$	
106.		IIP3		106		dBµV	f_{RF1} = 863.25 MHz f_{RF2} = 864.25 MHz $P_{RF1} = P_{RF2}$	
107.	Output voltage causing 1 dB compression	V_o		124		dBµV	f_{RF} = 447.25 MHz	
108.		V_o		124		dBµV	f_{RF} = 863.25 MHz	
109.	Output voltage causing 1.1 kHz incidental FM	V_o	108	111		dBµV	f_{RF} = 447.25 MHz 2.)	
110.		V_o	108	111		dBµV	f_{RF} = 454.25 MHz 2.)	
111.	Local oscillator FM caused by I^2C communication	FM_{I2C}			2.12	kHz	f_{RF} = 863.25 MHz 3.)	
112.	N+5 - 1 MHz pulling	N+5 - 1 MHz	77	80		dBµV	f_{RFw} = 823.25 MHz, f_{OSC} = 862.15 MHz, f_{RFu} = 862.25 MHz 9.)	
113.	750 Hz Pulling	V_i	78			dBµV	f_{RF} = 855.25 MHz 4.)	
114.	RF input level without lock-out	V_i			120	dBµV	8.)	
115.	Input impedance $Z_i = (R_s + j\omega L_s)$	R_s		35		Ω	f_{RF} = 447.25 MHz, see 4.4.3 on page 57	
116.		R_s		35		Ω	f_{RF} = 863.25 MHz, see 4.4.3 on page 57	
117.		L_s		8		nH	f_{RF} = 447.25 MHz, see 4.4.3 on page 57	
118.		L_s		8		nH	f_{RF} = 863.25 MHz, see 4.4.3 on page 57	
LOW band oscillator, (see Chapter 3 on page 28)								
119.	Oscillator frequency	f_{OSC}	80		210	MHz	10)	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
120.	Oscillator frequency shift	$\Delta f_{OSC(V)}$		20	70	kHz	ΔV_{CC} = 5% 11)	
121.		$\Delta f_{OSC(V)}$		110		kHz	ΔV_{CC} = 10% 11.)	
122.	Oscillator frequency drift	$\Delta f_{OSC(T)}$		300	500	kHz	ΔT = 25 °C, with compensation 12)	
123.	Oscillator frequency drift	$\Delta f_{OSC(t)}$		150	250	kHz	5 s to 15 min. after switch on 13)	
124.	Phase noise, carrier to noise sideband	Φ_{OSC}	77 14)	85		dBc/ Hz	±1 kHz frequency offset, worst case in frequency range	
125.			88 15)	92		dBc/ Hz	±10 kHz frequency offset, worst case in frequency range	
126.			108 14), 15)	112		dBc/ Hz	±100 kHz frequency offset, worst case in frequency range	
127.	Ripple susceptibility of V_P	RSC	15	20		mV	4.75 < V_P < 5.25 V, worst case in frequency range, ripple frequency 500 kHz 16)	
MID band oscillator, (see Chapter 3 on page 28)								
128.	Oscillator frequency	f_{OSC}	201		493	MHz	10.)	
129.	Oscillator frequency shift	$\Delta f_{OSC(V)}$		20	70	kHz	ΔV_{CC} = 5% 11.)	
130.		$\Delta f_{OSC(V)}$		110		kHz	ΔV_{CC} = 10% 11.)	
131.	Oscillator frequency drift	$\Delta f_{OSC(T)}$		500	750	kHz	ΔT = 25 °C; with compensation 12.)	
132.	Oscillator frequency drift	$\Delta f_{OSC(t)}$		250	500	kHz	5 s to 15 min. after switch on 13.)	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
133.	Phase noise, carrier to noise sideband	Φ_{OSC}	73 [14)]	80		dBc/ Hz	±1 kHz frequency offset, worst case in frequency range	
134.			88 [15)]	92		dBc/ Hz	±10 kHz frequency offset, worst case in frequency range	
135.			106 [14), 15)]	112		dBc/ Hz	±100 kHz frequency offset, worst case in frequency range	
136.	Ripple susceptibility of V_P	RSC	15	20		mV	$4.75 < V_P < 5.25$ V, worst case in frequency range, ripple frequency 500 kHz [14.)]	
HIGH band oscillator, (see Chapter 3 on page 28)								
137.	Oscillator frequency	f_{OSC}	435		905	MHz	[10.)]	
138.	Oscillator frequency shift	$\Delta f_{OSC(V)}$		20	70	kHz	ΔV_{CC} = 5% [11.)]	
139.		$\Delta f_{OSC(V)}$		300		kHz	ΔV_{CC} = 10% [11.)]	
140.	Oscillator frequency drift	$\Delta f_{OSC(T)}$		600	1000	kHz	ΔT = 25 °C; with compensation [12.)]	
141.	Oscillator frequency drift	$\Delta f_{OSC(t)}$		250	500	kHz	5 s to 15 min. after switch on [13).]	
142.	Phase noise, carrier to noise sideband	Φ_{OSC}	70 [14)]	77		dBc/ Hz	±1 kHz frequency offset, worst case in frequency range	
143.			86 [15)]	90		dBc/ Hz	±10 kHz frequency offset, worst case in frequency range	
144.			106 [14), 15)]	109		dBc/ Hz	±100 kHz frequency offset, worst case in frequency range	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
145.	Ripple susceptibility of V_P	RSC	15	20		mV	$4.75 < V_P < 5.25$ V, worst case in frequency range, ripple frequency 500 kHz [14.)]	
IF amplifier								
146.	Input impedance $Z_i = (R_s + j\omega L_s)$	R_S		460		Ω	at 36 MHz, see 4.4.4 on page 57	
147.		L_S		10		nH	at 36 MHz, see 4.4.4 on page 57	
148.	Output reflection coefficient	S_{22}		10		dB	magnitude, see 4.4.4 on page 57	
149.		S_{22}		0.85		°	phase, see 4.4.4 on page 57	
150.	Output impedance $Z_o = (R_s + j\omega L_s)$	R_S		65		Ω	at 36 MHz, see 4.4.6 on page 58	
151.		L_S		20		nH	at 36 MHz, see 4.4.6 on page 58	
Rejection at the IF outputs								
152.	Level of divider interferences in the IF signal	INT_{DIV}			20	dBµV	[17)], worst case	
153.	Crystal oscillator interferences rejection	INT_{XTAL}	60	66		dBc	V_{IF} = 100 dBµV, worst case in frequency range[18)]	
154.	Reference frequency rejection	INT_{REF}	60	66		dBc	V_{IF} = 100 dBµV, worst case in frequency range [19)]	
AGC output								
155.	AGC take-over point	AGC_{TOP}		112		dBµV	AL2, AL1, AL0 = 0, 1, 0	
156.	Source current 1	$I_{AGCfast}$	7.2	9.0	10.8	µA		
157.	Source current 2	$I_{AGCslow}$	210	300	390	nA		
158.	Peak sink to ground	$I_{AGCpeak}$	80	100	120	µA		

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
159.	AGC output voltage	V_{AGCmax}	3.6	3.8	4.0	V	maximum level, I_{AGC} = 9 µA	
160.	AGC output voltage	V_{AGCmin}	0		0.25	V	minimum level	
161.	RF voltage range to switch the AGC from active to inactive mode	AGC_{SLIP}			0.5	dB		
162.	AGC output voltage	AGC_{RML}	0		2.9	V	AGC bit high or AGC active	
163.	AGC output voltage	AGC_{RMH}	3.3	3.8	VCC-0.5 or 4	V	AGC bit low or AGC inactive	
164.	AGC leakage current	AGC_{LEAK}	-50		50	nA	AL2, AL1, AL0 = 1,1,0 $0 < V_{AGC} < V_{CC}$	
165.	AGC output voltage	AGC_{OFF}	3.3	3.8	VCC-0.5 or 4	V	AL2, AL1, AL0 = 1,1,1 AGC is disabled	

■ This value is only guaranteed in lab.

1) The RF frequency range is defined by the oscillator frequency range and the intermediate frequency (IF).

2) This is the level of the RF unwanted signal (50% amplitude modulated with 1kHz) that causes a 1.1 kHz FM modulation of the local oscillator and thus of the wanted signal; V_{wanted} = 100 dBµV; $f_{unwanted} = f_{wanted}$ + 5.5 MHz.

3) Local oscillator FM modulation resulting from I^2C communication is measured at the IF output using a modulation analyzer with a peak to peak detector $((P_+ + P_-)/2)$ and a post detection filter 30 Hz - 200 kHz. The I^2C messages are sent to the tuner in such a way that the tuner is addressed but the content of the PLL registers are not altered. The refresh interval between each data set shall be 20 ms to 1s.

4) This is the level of the RF signal (100% amplitude modulated with 11.89 kHz) that causes a 750 Hz frequency deviation on the oscillator signal producing sidebands 30 dB below the level of the oscillator signal.

5) Channel S02 beat is the interfering product of f_{RFpix}, f_{IF} and f_{OSC} of channel S02, f_{BEAT} = 37.35 MHz. The possible mechanisms are f_{OSC} - 2 x f_{IF} or 2 x f_{RFpix} - f_{OSC}.

6) Channel A-5 beat is the interfering product of $f_{RFpix,}$ f_{IF} and f_{OSC} of channel A-5; f_{BEAT}= 45.5 MHz. The possible mechanisms are: f_{OSC} - 2 x f_{IF} or 2 x f_{RFpix} - f_{OSC}.

7) Channel 6 beat is the interfering product of f_{RFpix} + f_{RFsnd} - f_{OSC} of channel 6 at 42 MHz.

8) The IF output signal stays stable within the range of the f_{ref} step for a low level RF input up to 120 dBµV.

9) N+5 -1 MHz is defined as the input level of channel N+5, at frequency 1 MHz lower, causing FM sidebands 30 dB below the wanted carrier.

10) Limits are related to the tank circuit used in the application board (see Chapter 3 on page 28). Frequency bands may be adjusted by the choice of external components.

11) The frequency shift is defined as a change in oscillator frequency when the supply voltage varies from V_{CC} = 5 to 4.75 V (4.5 V) or from V_{CC} = 5 to 5.25 V (5.5 V). The oscillator is free running during this measurement.

12) The frequency drift is defined as a change in oscillator frequency if the ambient temperature varies from T_A = 25 to 50 °C or from T_A = 25 to 0 °C. The oscillator is free running during this measurement.

13) The switch-on drift is defined as a change in oscillator frequency between 5 s and 15 min. after switch-on. The oscillator is free running during this measurement.

14) see Figure 8 Application Circuit TUA6034-T for DVB-T on page 29.

15) see Figure 7 Application Circuit TUA6034-T for ATSC on page 28.

16) The supply ripple susceptibility is measured in the application board (see Chapter 3 on page 28), using a spectrum analyzer connected to the IF output. An unmodulated RF signal is applied to the test board RF input. A sinewave signal with a frequency of 500 kHz is superposed onto the supply voltage (see 4.5.8 on page 62). The amplitude of this ripple is adjusted to bring the 500 kHz sidebands around the IF carrier to a level of 53.5 dBc referred to the carrier.

17) This is the level of divider interferences close to the IF frequency. For example channel S3: f_{OSC} = 158.15 MHz, 1/4 f_{OSC} = 39.5375 MHz. Divider interference is measured with the application board (see Chapter 3 on page 28). All ground pins are connected to a single ground plane under the IC. The LOWIN input must be left open (i.e. not connected to any load or cable). The MIDIN and HIGHIN inputs are connected to a hybrid. The measured level of divider interference are influenced by layout, grounding and port decoupling. The measurement results between various applications and the reference board could vary as much as 10 dB.

18) Crystal oscillator interference means the 4 MHz sidebands caused by the crystal oscillator. The rejection has to be greater than 60 dB for an IF output of 100 dBµV.

19) The reference frequency rejection is the level of reference frequency sidebands (e.g. 62.5 kHz) related to the carrier. The rejection has to be greater than 60 dB for an IF output of 100 dBµV.

4.2 Programming

Table 8 Bit Allocation Read/Write

Name	Byte	Bits								Ack
		MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB	
Write Data										
Address Byte	ADB	1	1	0	0	0	MA1	MA0	R/W=0	A
Divider Byte 1	DB1	0	N14	N13	N12	N11	N10	N9	N8	A
Divider Byte 2	DB2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte	CB	1	CP	T2	T1	T0	RSA	RSB	OS	A
Bandswitch byte	BB				P4	P3	P2	P1	P0	A
Auxiliary byte [1)]	AB	ATC	AL2	AL1	AL0	0	0	0	0	A
Read data										
Address byte	ADB	1	1	0	0	0	MA1	MA0	R/W=1	A
Status byte	SB	POR	FL	1	1	AGC	A2	A1	A0	A

1) AB replaces BB when T2, T1, T0 = 0, 1, 1, see Table 11 Test modes on page 51.

Table 9 Description of Symbols

Symbol	Description
A	Acknowledge
MA0, MA1	Address selection bits, see Table 10 Address selection on page 51
N14 to N0	programmable divider bits: $N = 2^{14} \times N14 + 2^{13} \times N13 + ... + 2^3 \times N3 + 2^2 \times N2 + 2^1 \times N1 + N0$
CP	charge pump current bit: bit = 0: charge pump current = 50 µA or 125 µA bit = 1: charge pump current = 250 µA (default) or 650 µA, see Table 15 Charge pump current on page 53
T0, T1, T2	test bits, see Table 11 Test modes on page 51
RSA, RSB	reference divider bits, see Table 12 Reference divider ratios on page 52
OS	tuning amplifier control bit: bit = 0: enable V_T; bit = 1: disable V_T (default)
P0, P1, P2, P3	PNP ports control bits bit = 0: Port is inactive, high impedance state (default) bit = 1: Port is active, $V_{OUT} = V_{CC}-V_{CESAT}$

P4	NPN port control bit bit = 0: Port is inactive, high impedance state (default) bit = 1: Port is active, V_{OUT}= V_{CESAT}
ATC	AGC time constant bit bit = 0: I_{AGC}=300 nA; Δt=2s with C=160 nF (default) bit = 1: I_{AGC}=9 µA; Δt=50ms with C=160 nF
AL0, AL1, AL2	AGC take-over point bits, see Table 13 AGC take-over point on page 52
POR	Power-on reset flag; POR =1 at power-on
FL	PLL lock flag; bit = 1: loop is locked
AGC	internal AGC flag. AGC=1 when internal AGC is active (level below 3V)
A0, A1, A2	digital output of the 5-level ADC

Table 10 Address selection

Voltage at AS	MA1	MA0
(0 to 0.1) x V_{CC}	0	0
open circuit or (0.2 to 0.3) x V_{CC}	0	1
(0.4 to 0.6) x V_{CC}	1	0
(0.9 to 1) x V_{CC}	1	1

Table 11 Test modes

Mode	T2	T1	T0
Normal mode, charge pump currents 50 and 250 µA selectable	0	0	0
Normal mode, charge pump currents 50 and 250 µA selectable (default)	0	0	1
CP is in high-impedance state	0	1	0
byte AB will follow (otherwise byte BB will follow)	0	1	1
P0 = f_{div} output, P1 = f_{ref} output	1	0	0
not in use	1	0	1
Extended mode, charge pump currents 50 and 250 µA selectable	1	1	0
Extended mode, charge pump currents 125 and 650 µA selectable	1	1	1

Table 12 Reference divider ratios

Reference divider ratio	f_{ref} [1)]	Mode	T2	T1	RSA	RSB
80	50 kHz	normal	0	0	0	0
128	31.25 kHz	normal	0	0	0	1
24	166.67 kHz	x	x	x	1	0
64	62.5 kHz	x	x	x	1	1
32	125 kHz	extended	1	1	0	0
28	142.86 kHz	extended	1	1	0	1

1) With a 4 MHz quartz.

Table 13 AGC take-over point

IF output level, symmetrical mode	Remark	AL2	AL1	AL0
115 dBµV		0	0	0
115 dBµV		0	0	1
112 dBµV	default mode at POR	0	1	0
109 dBµV		0	1	1
106 dBµV		1	0	0
103 dBµV		1	0	1
I_{AGC} = 0	External AGC [1)]	1	1	0
3.8 V	Disabled [2)]	1	1	1

1) The AGC detector is disabled. Both the sinking and sourcing current from the IC is disabled. The AGC output goes into a high impedance state and an external AGC source can be connected in parallel and will not be influenced.

2) The AGC detector is disabled.

Table 14 A to D converter levels

Voltage at ADC	A2	A1	A0
(0 to 0.15) * V_{CC}	0	0	0
(0.15 to 0.3) * V_{CC}	0	0	1
(0.3 to 0.45) * V_{CC}	0	1	0
(0.45 to 0.6) * V_{CC}	0	1	1
(0.6 to 1) * V_{CC}	1	0	0

1) No erratic codes in the transition.

Table 15 Charge pump current

Charge pump current	Mode	CP	T2	T1	T0
50 µA	normal	0	0	0	x[1)]
250 µA (default)		1			x
50 µA	extended	0	1	1	0
125 µA		0			1
250 µA		1			0
650 µA		1			1

1) x = don‘t care.

Table 16 Internal band selection

Band	Mixer	Oscillator
LOW	P0.$\overline{P1}$ [1)]	P0.$\overline{P1}$
MID	P1.$\overline{P0}$	P1.$\overline{P0}$
HIGH (default)	$\overline{P0}$.$\overline{P1}$	$\overline{P0}$.$\overline{P1}$
Power down mode	P0, P1	P0, P1

1) Means: (P0 *AND NOT* P1); that is: LOW mixer is switched on if (P0=1 and P1=0).

Table 17 Defaults at power-on reset

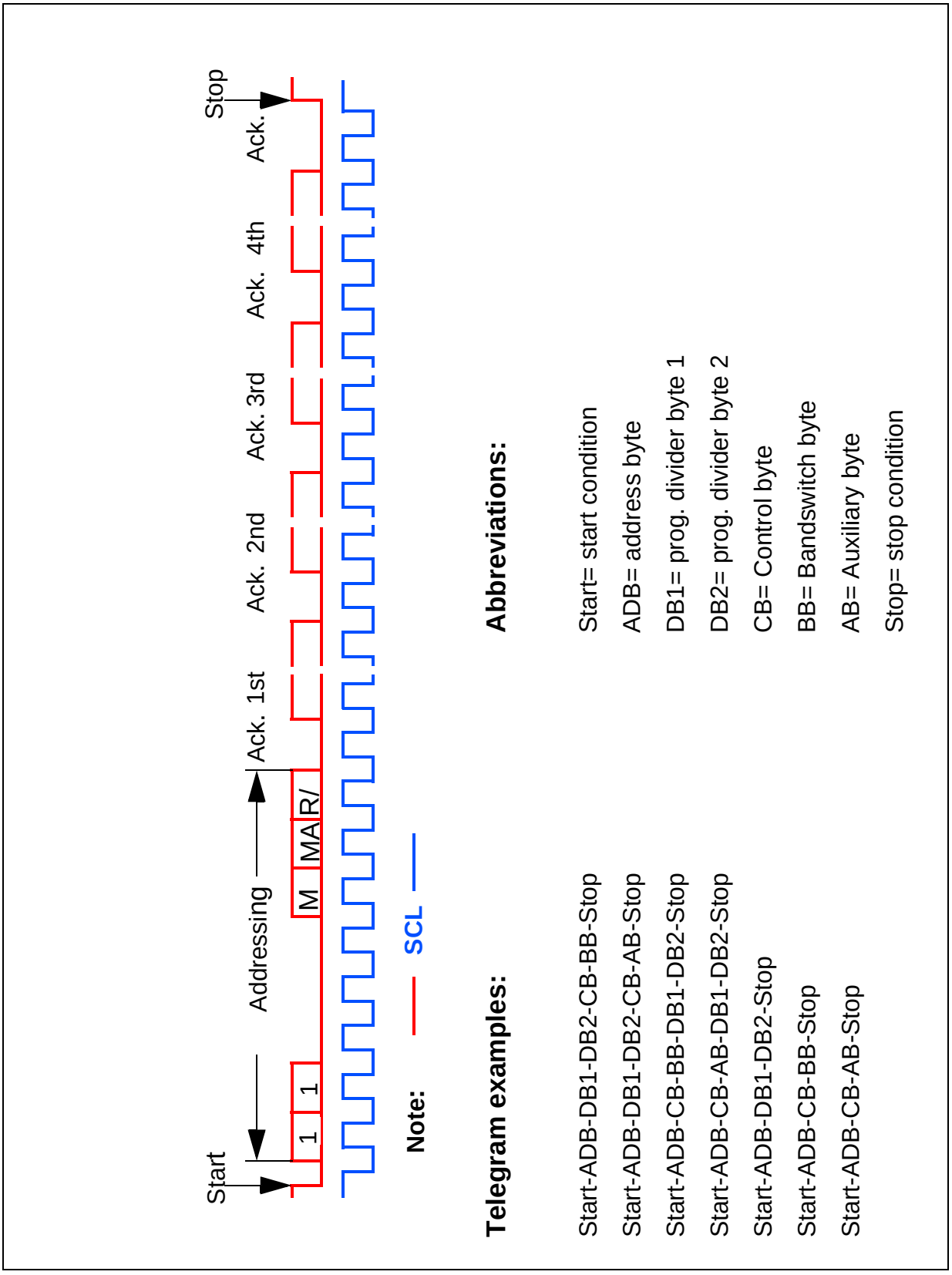
Name	Byte	Bits							
		MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB
Write Data									
Address Byte	ADB	1	1	0	0	0	MA1	MA0	R/W=0
Divider byte 1	DB1	0	x[1)]	x	x	x	x	x	x
Divider byte 2	DB2	x	x	x	x	x	x	x	x
Control byte	CB	1	1	0	0	1	x	x	1
Bandswitch byte	BB	0	0	0	0	0	0	0	0
Auxiliary byte	AB	0	0	1	0				

1) x = don‘t care.

Table 18 Description of modes

Mode	Description
normal	Reference divider ratios 24, 64, **80**, **128** selectable. Charge pump currents 50, 250 µA selectable. Auxiliary byte to follow Control byte (T2=0, T1=1, T0=1), otherwise Bandswitch byte to follow Control byte.
extended	Reference divider ratios 24, **28**, **32**, 64 selectable. Charge pump currents 50, **125**, 250, **650** µA selectable. Auxiliary byte to follow Control byte (T2=0, T1=1, T0=1), otherwise Bandswitch byte to follow Control byte.

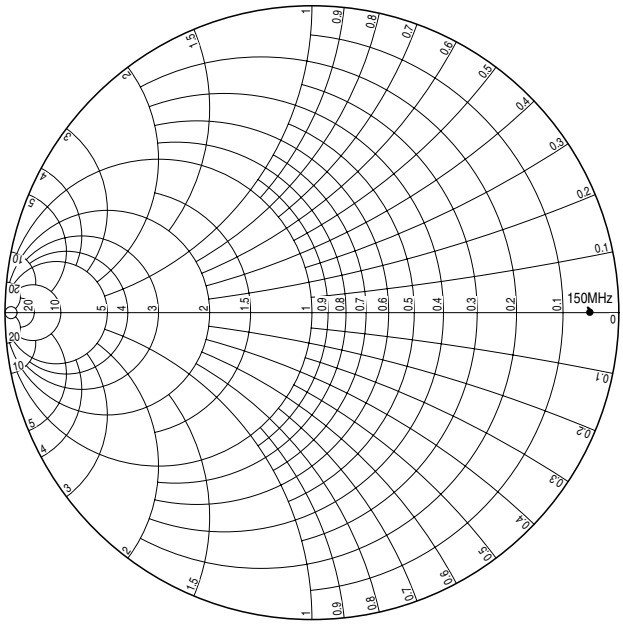
4.3 I²C Bus Timing Diagram



4.4 Electrical Diagrams

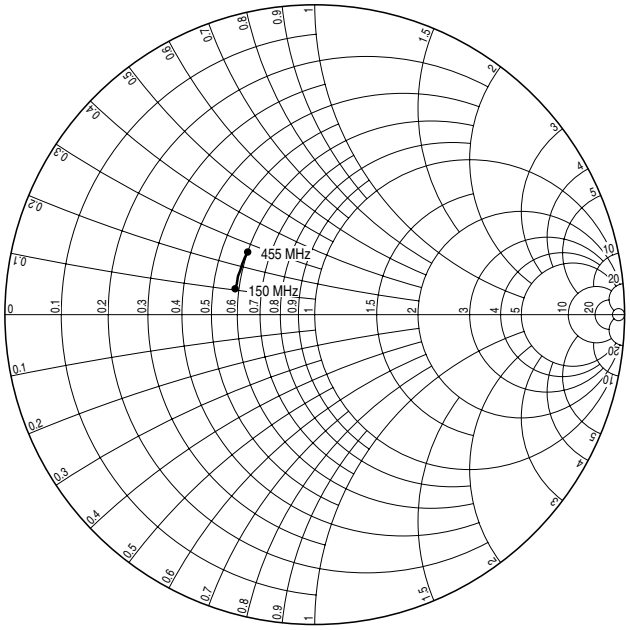
4.4.1 Input admittance (S11) of the LOW band mixer (40 to 150 MHz)

Y_0 = 20mS



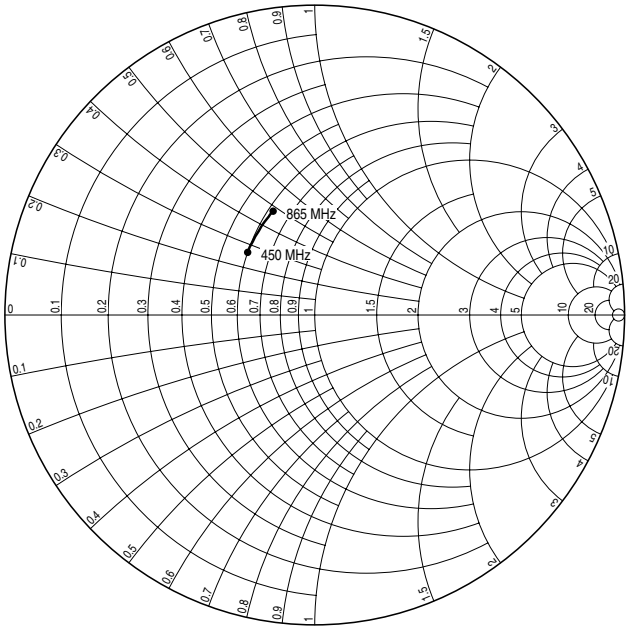
4.4.2 Input impedance (S11) of the MID band mixer (150 to 455 MHz)

Z_0 = 50 Ω



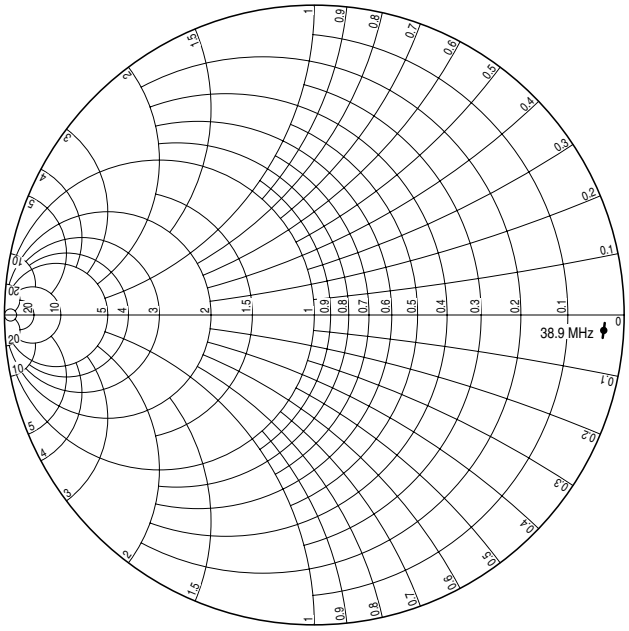
4.4.3 Input impedance (S11) of the HIGH band mixer (450 to 865 MHz)

$Z_0 = 50\ \Omega$



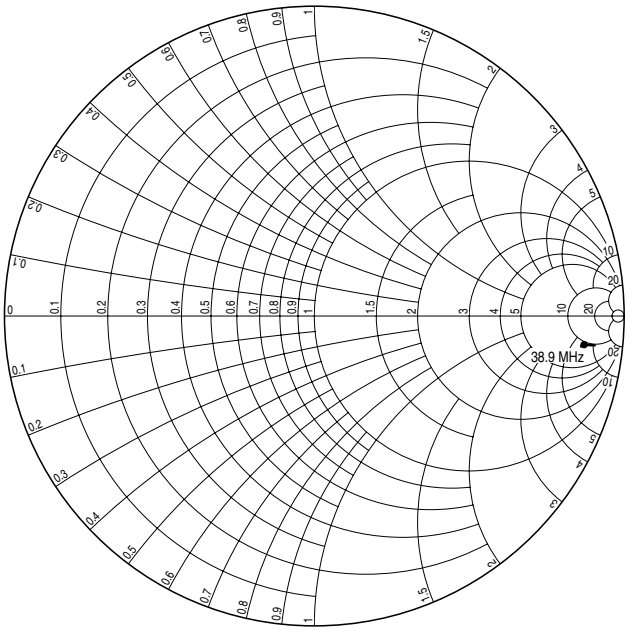
4.4.4 Output admittance (S22) of the of the mixers (30 to 50 MHz)

$Y_0 = 20ms$



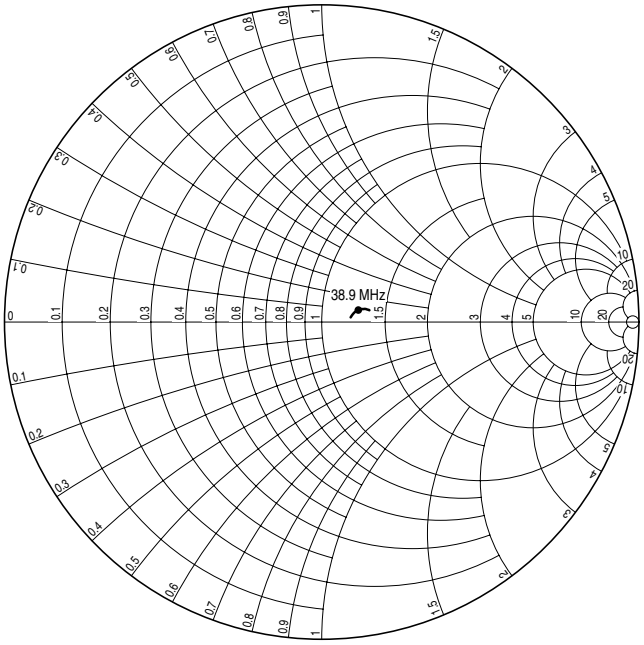
4.4.5 Input impedance (S11) of the IF amplifier (30 to 50 MHz)

$Z_0 = 50\ \Omega$



4.4.6 Output impedance (S22) of the IF amplifier (30 to 50 MHz)

$Z_0 = 50\ \Omega$



4.5 Measurement Circuits

4.5.1 Gain (G_V) measurement in LOW band

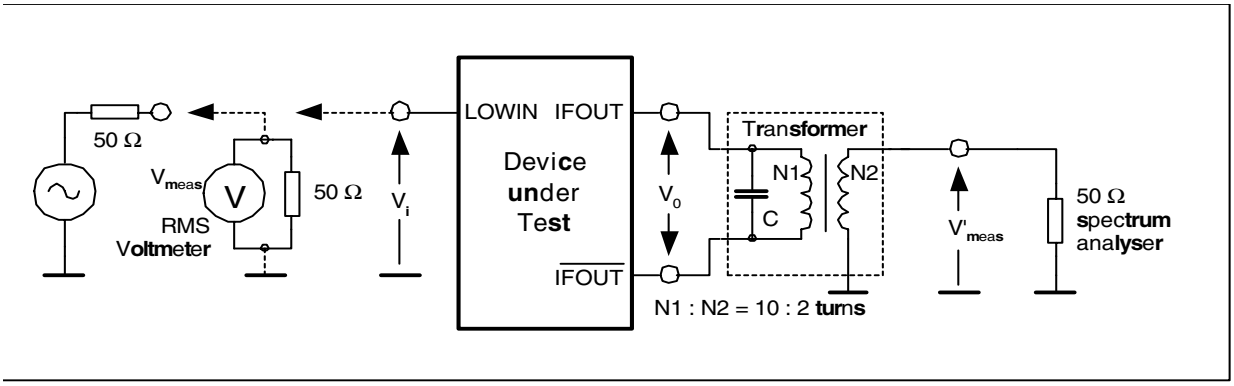


Figure 12 Gain (G_V) measurement in LOW band

- Z_i >> 50 Ω => V_i = 2 x V_{meas} = 80 dBµV
- V_i = V_{meas} + 6dB = 80 dBµV
- V_0 = V'_{meas} + 16 dB (transformer ratio N1:N2 and transformer loss)
- G_v = 20 log(V_0 / V_i)

4.5.2 Gain (G_V) measurement in MID and HIGH bands

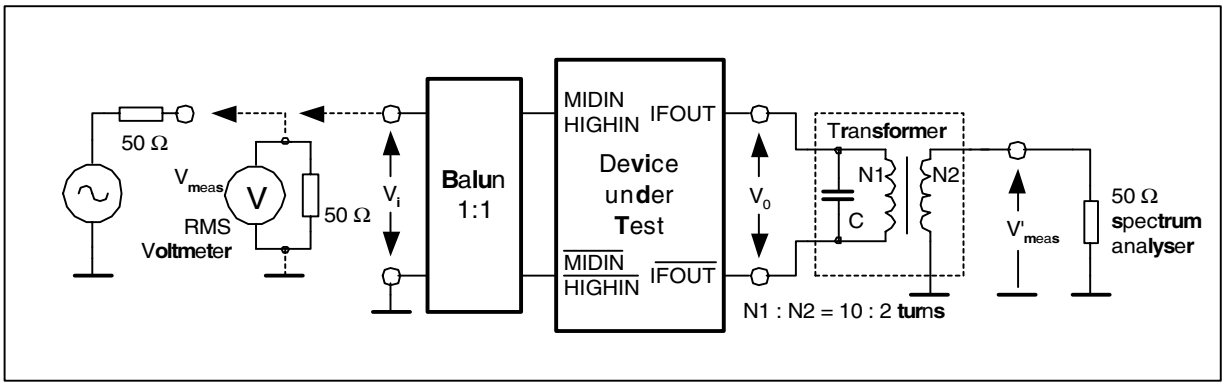


Figure 13 Gain (G_V) measurement in MID and HIGH bands

- V_i = V_{meas} = 70 dBµV
- V_0 = V'_{meas} + 16 dB (transformer ratio N1:N2 and transformer loss
- G_v = 20 log(V_0 / V_i) + 1 dB (1 dB = insertion loss of balun)

4.5.3 Matching circuit for optimum noise figure in LOW band

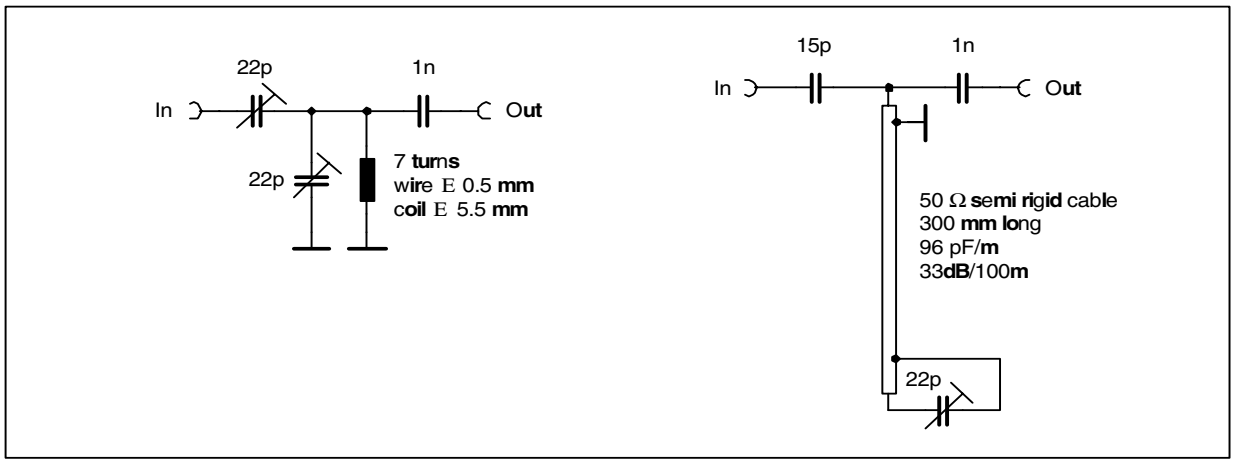


Figure 14 Matching circuit for optimum noise figure in LOW band

For f_{RF} = 50 MHz
loss = 0 dB
image suppression = 16 dB

For f_{RF} = 150 MHz
loss = 1.3 dB
image suppression = 13 dB

4.5.4 Noise figure (NF) measurement in LOW band

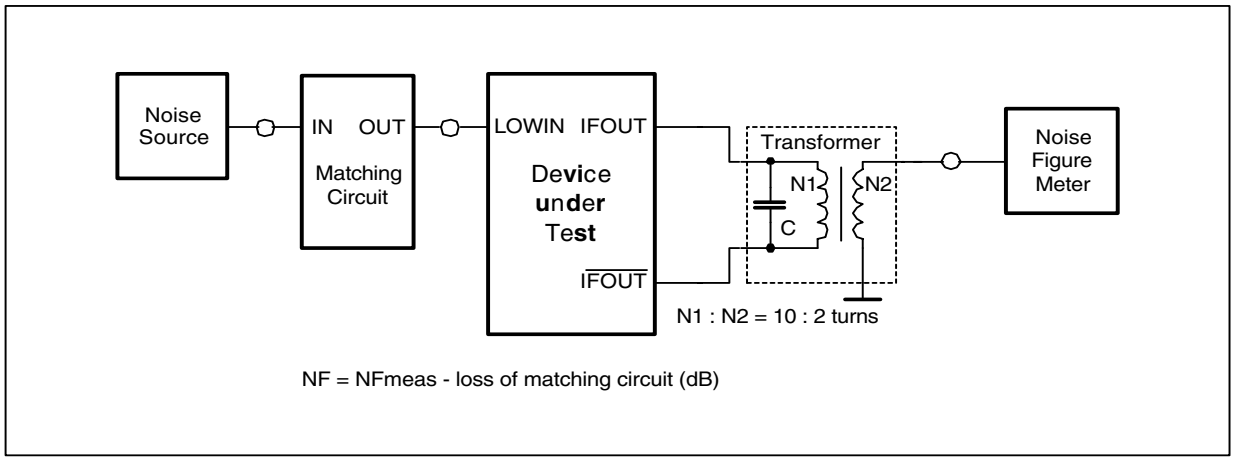


Figure 15 Noise figure (NF) measurement in LOW band

4.5.5 Noise figure (NF) measurement in MID and HIGH bands

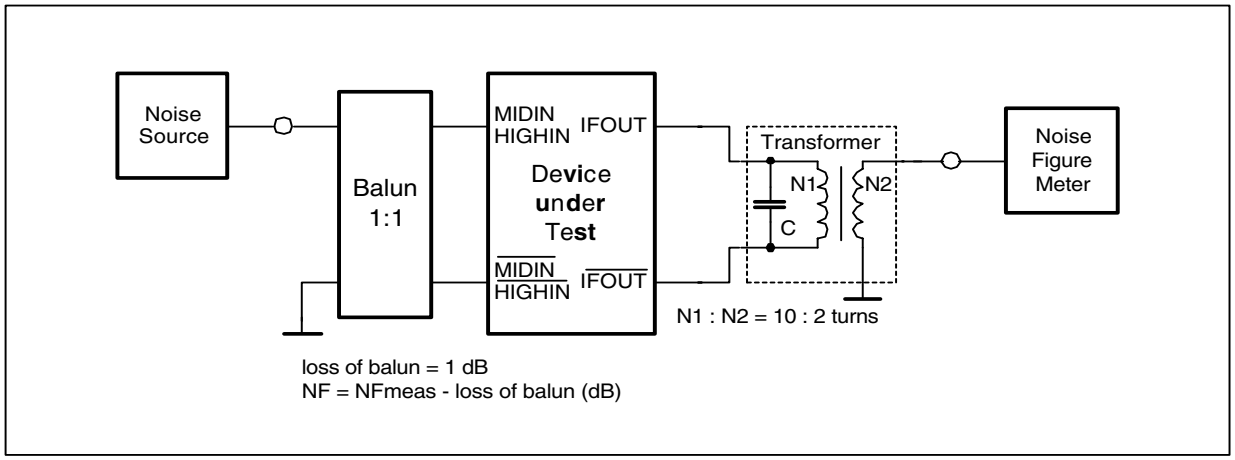


Figure 16 Noise figure (NF) measurement in MID and HIGH bands

4.5.6 Cross modulation measurement in LOW band

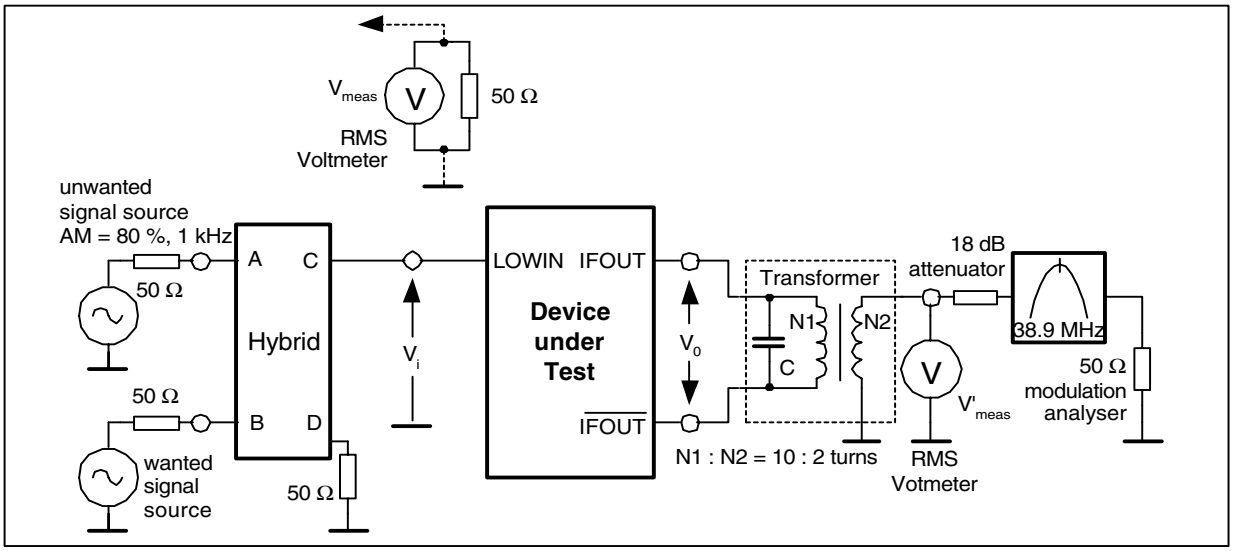


Figure 17 Cross modulation measurement in LOW band

- $Z_i >> 50\ \Omega \Rightarrow V_i = 2 \times V_{meas}$
- $V'_{meas} = V_0$ - 16 dB (transformer ratio N1:N2 and transformer loss)
- wanted output signal at f_{pix}, V_o = 100 dBµV
- unwanted output signal at f_{snd}

4.5.7 Cross modulation measurement in MID and HIGH bands

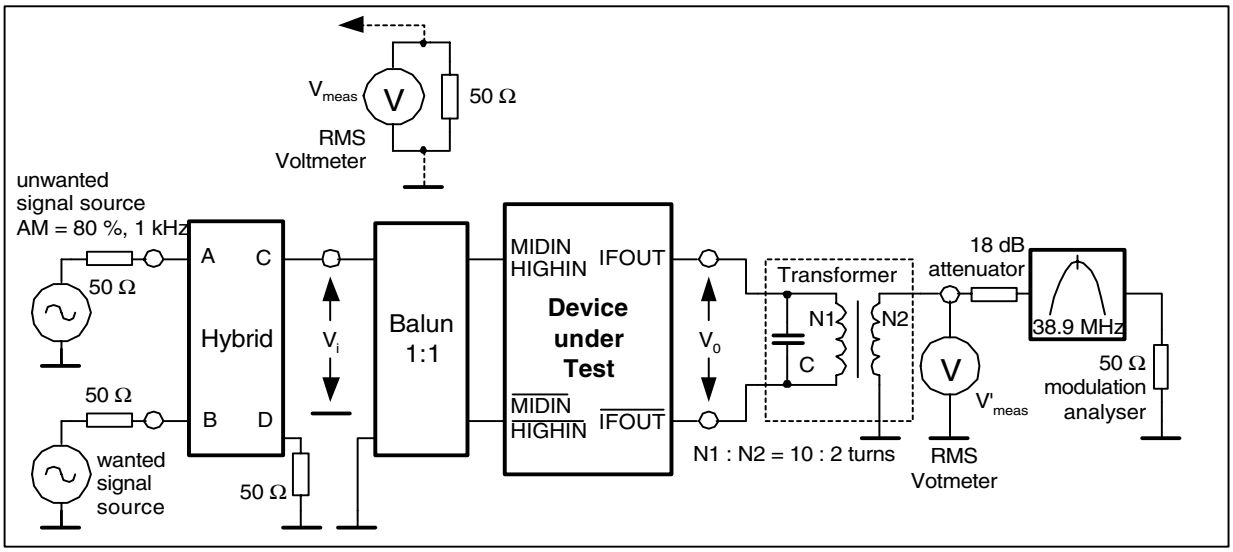


Figure 18 Cross modulation measurement in MID and HIGH bands

- $V'_{meas} = V_0$ - 16 dB (transformer ratio N1:N2 and transformer loss)
- wanted output signal at f_{pix}, V_o = 100 dBµV
- unwanted output signal at f_{snd}

4.5.8 Ripple susceptibility measurement

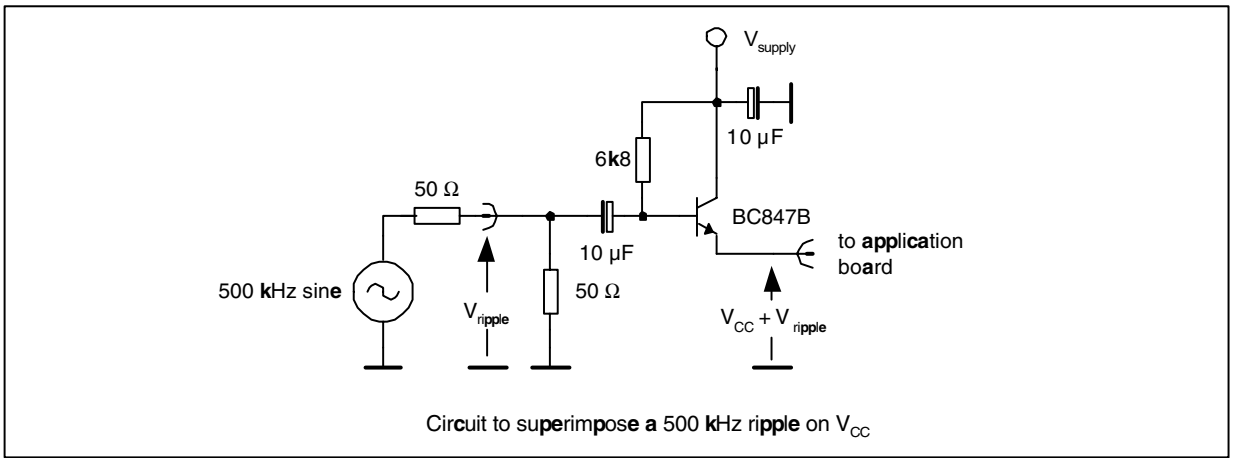


Figure 19 Ripple susceptibility measurement

5 Package Outlines

5.1 Package TSSOP-38

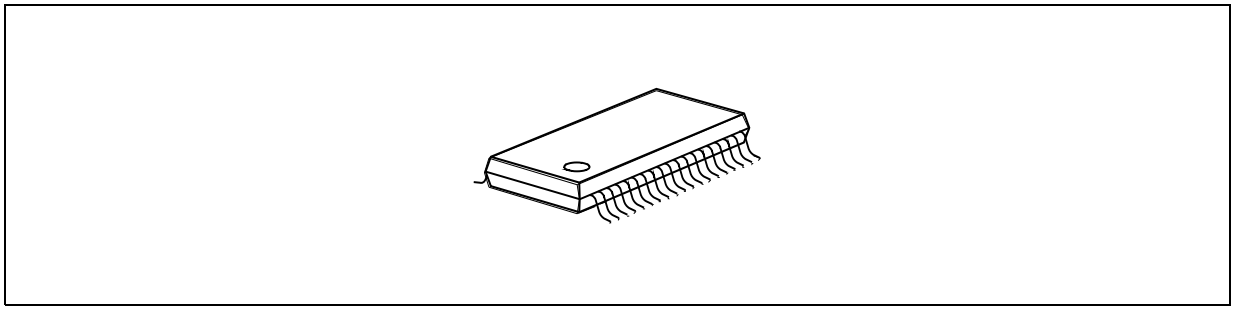


Figure 20 PG-TSSOP-38 Vignette

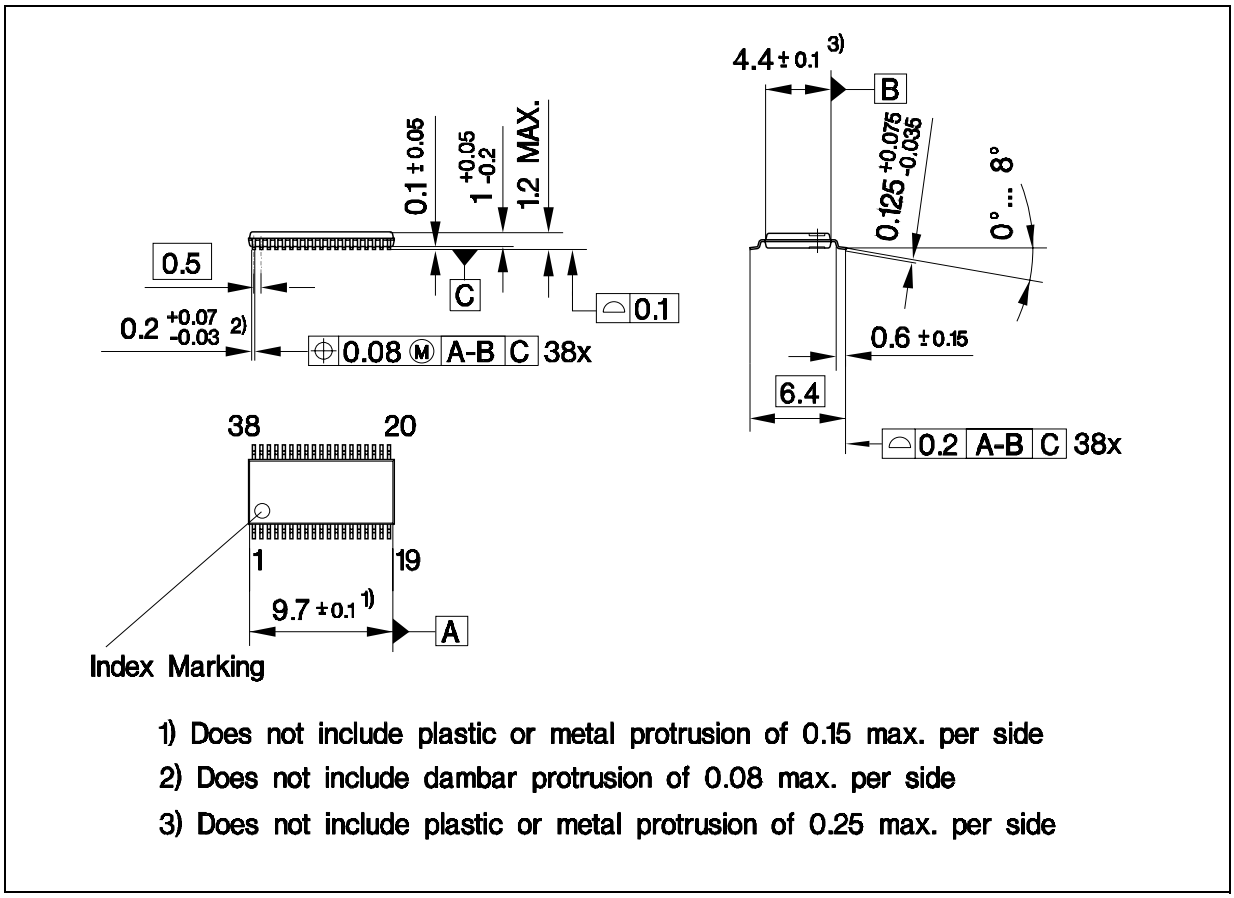


Figure 21 PG-TSSOP-38 Outline Drawing

5.2 Package VQFN-48

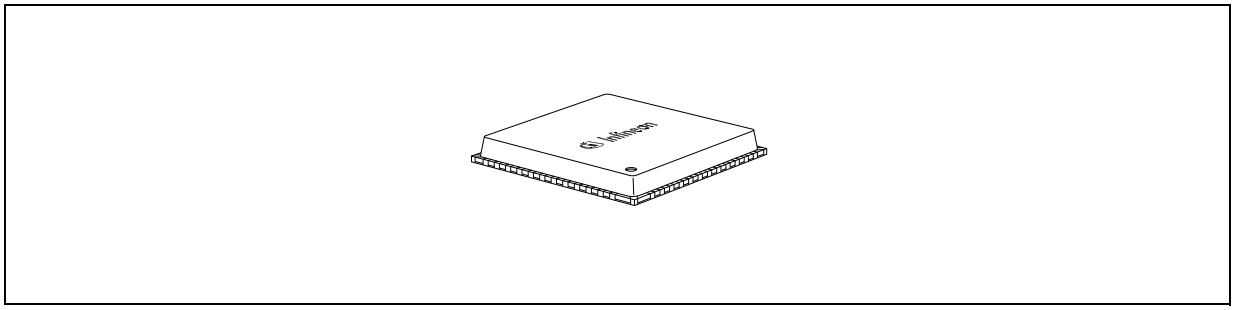


Figure 22 PG-VQFN-48 Vignette

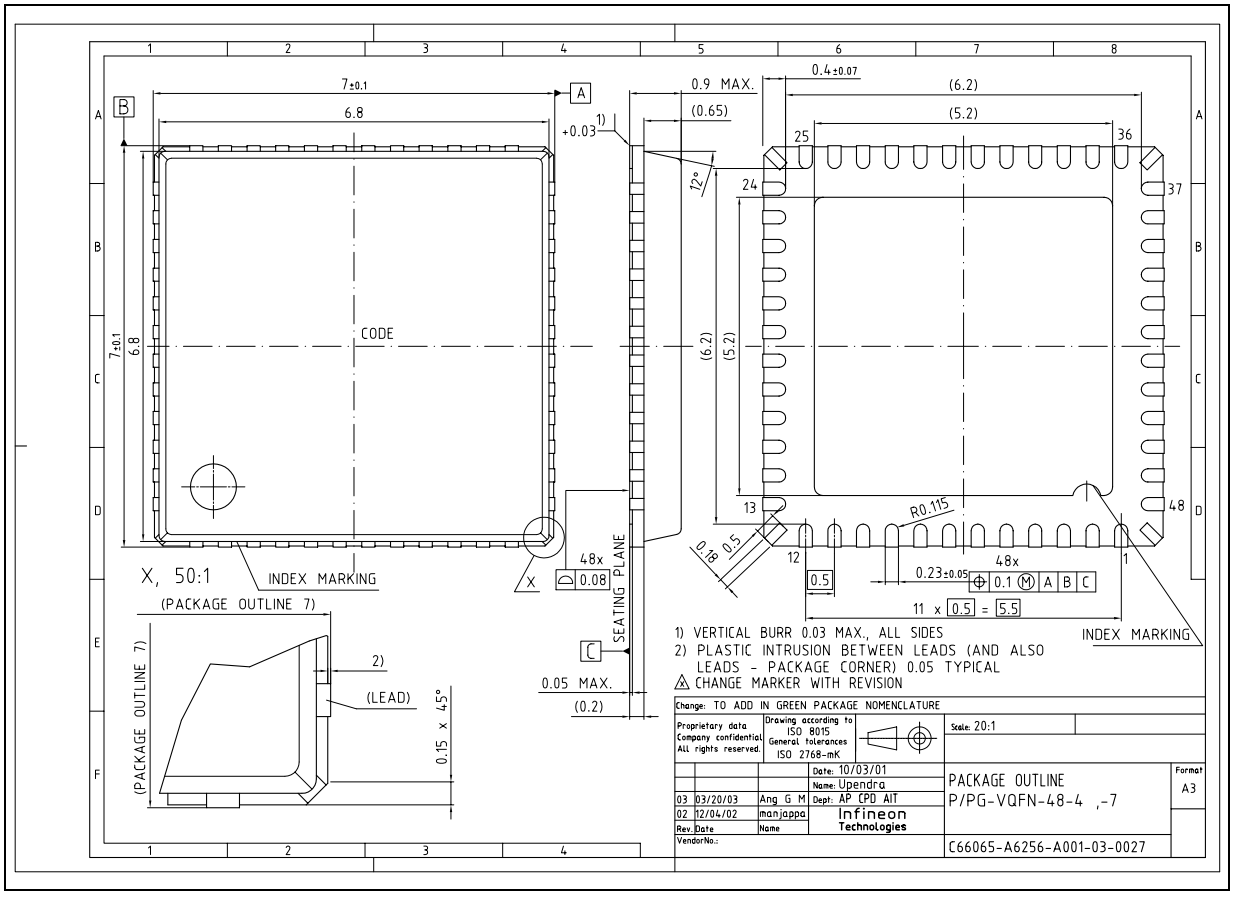


Figure 23 PG-VQFN-48 Outline Drawing

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

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