

# DUAL FREQUENCY CRYSTAL OSCILLATOR (XO) (10 MHz TO 1.4 GHz)

## Features

- Available with any-rate output frequencies from 10 MHz to 945 MHz and select frequencies to 1.4 GHz
- 2 selectable output frequencies
- 3rd generation DSPLL<sup>®</sup> with superior jitter performance
- 3x better frequency stability than SAW-based oscillators
- Pin 1 output enable (OE)
- Internal fixed crystal frequency ensures high reliability and low aging
- Available CMOS, LVPECL, LVDS, and CML outputs
- 3.3, 2.5, and 1.8 V supply options
- Industry-standard 5 x 7 mm package and pinout
- Pb-free/RoHS-compliant

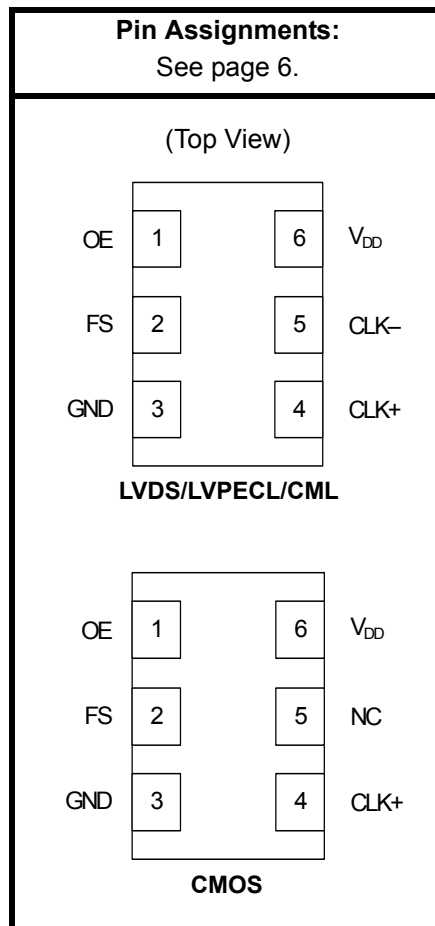
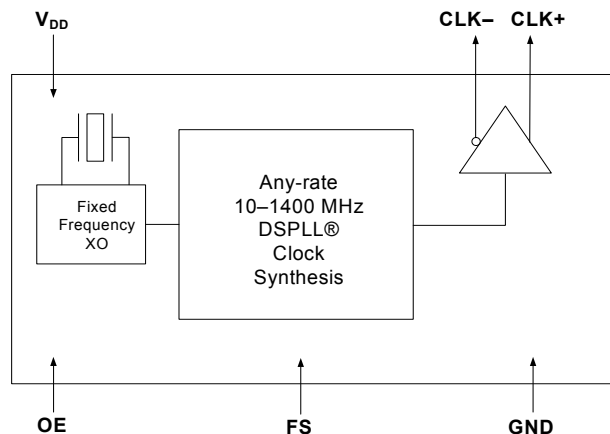
## Applications

- SONET/SDH
- Networking
- SD/HD video
- Clock and data recovery
- FPGA/ASIC clock generation

## Description

The Si533 dual frequency XO utilizes Silicon Laboratories' advanced DSPLL<sup>®</sup> circuitry to provide a low jitter clock at high frequencies. The Si533 is available with any-rate output frequency from 10 to 945 MHz and select frequencies to 1400 MHz. Unlike a traditional XO, where a different crystal is required for each output frequency, the Si533 uses one fixed crystal to provide a wide range of output frequencies. This IC based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments typically found in communication systems. The Si533 IC based XO is factory configurable for a wide variety of user specifications including frequency, supply voltage, output format, and temperature stability. Specific configurations are factory programmed at time of shipment, thereby eliminating long lead times associated with custom oscillators.

## Functional Block Diagram



## 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage <sup>1</sup>	$V_{DD}$	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	
		1.8 V option	1.71	1.8	1.89	
Supply Current	$I_{DD}$	Output enabled				mA
		LVPECL	—	111	121	
		CML	—	99	108	
		LVDS	—	90	98	
		CMOS	—	81	88	
Tristate mode	—	60	75			
Output Enable (OE) and Frequency Select (FS) <sup>2</sup>		$V_{IH}$	$0.75 \times V_{DD}$	—	—	V
		$V_{IL}$	—	—	0.5	
Operating Temperature Range	$T_A$		−40	—	85	°C

**Notes:**

- Selectable parameter specified by part number. See Section 3. "Ordering Information" on page 7 for further details.
- OE and FS pins include a 17 k $\Omega$  pullup resistor to  $V_{DD}$ .

**Table 2. CLK $\pm$  Output Frequency Characteristics**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Nominal Frequency <sup>1,2</sup>	$f_O$	LVPECL/LVDS/CML	10	—	945	MHz
		CMOS	10	—	160	
Initial Accuracy	$f_i$	Measured at +25 °C at time of shipping	—	$\pm 1.5$	—	ppm
Temperature Stability <sup>1,3</sup>			−7	—	+7	ppm
			−20	—	+20	
			−50	—	+50	
Aging	$f_a$	Frequency drift over first year	—	—	$\pm 3$	ppm
		Frequency drift over 15 year life	—	—	$\pm 10$	ppm

**Notes:**

- See Section 3. "Ordering Information" on page 7 for further details.
- Specified at time of order by part number. Also available in frequencies from 970 to 1134 MHz and 1213 to 1417 MHz.
- Selectable parameter specified by part number.
- Time from powerup or tristate mode to  $f_O$ .

Table 2. CLK± Output Frequency Characteristics (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Total Stability		Temp stability = ±7 ppm	—	—	±20	ppm
		Temp stability = ±20 ppm	—	—	±31.5	ppm
		Temp stability = ±50 ppm	—	—	±61.5	ppm
Powerup Time <sup>4</sup>	t <sub>OSC</sub>		—	—	10	ms
Settling Time After FS Change	t <sub>FRQ</sub>		—	—	10	ms
<b>Notes:</b>						
1. See Section 3. "Ordering Information" on page 7 for further details.						
2. Specified at time of order by part number. Also available in frequencies from 970 to 1134 MHz and 1213 to 1417 MHz.						
3. Selectable parameter specified by part number.						
4. Time from powerup or tristate mode to f <sub>O</sub> .						

Table 3. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option <sup>1</sup>	V <sub>O</sub>	mid-level	V <sub>DD</sub> - 1.42	—	V <sub>DD</sub> - 1.25	V
	V <sub>OD</sub>	swing (diff)	1.1	—	1.9	V <sub>PP</sub>
	V <sub>SE</sub>	swing (single-ended)	0.55	—	0.95	V <sub>PP</sub>
LVDS Output Option <sup>2</sup>	V <sub>O</sub>	mid-level	1.125	1.20	1.275	V
	V <sub>OD</sub>	swing (diff)	0.5	0.7	0.9	V <sub>PP</sub>
CML Output Option <sup>2</sup>	V <sub>O</sub>	mid-level	—	V <sub>DD</sub> - 0.75	—	V
	V <sub>OD</sub>	swing (diff)	0.70	0.95	1.20	V <sub>PP</sub>
CMOS Output Option <sup>3</sup>	V <sub>OH</sub>	I <sub>OH</sub> = 32 mA	0.8 x V <sub>DD</sub>	—	V <sub>DD</sub>	V
	V <sub>OL</sub>	I <sub>OL</sub> = 32 mA	—	—	0.4	
Rise/Fall time (20/80%)	t <sub>R</sub> , t <sub>F</sub>	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with C <sub>L</sub> = 15 pF	—	1	—	ns
Symmetry (duty cycle)	SYM	LVPECL: V <sub>DD</sub> - 1.3 V (diff) LVDS: 1.25 V (diff) CMOS: V <sub>DD</sub> /2	45	—	55	%
<b>Notes:</b>						
1. 50 Ω to V <sub>DD</sub> - 2.0 V.						
2. R <sub>term</sub> = 100 Ω (differential).						
3. C <sub>L</sub> = 15 pF						

**Table 4. CLK± Output Phase Jitter**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)* for F <sub>OUT</sub> ≥ 500 MHz	ϕ <sub>J</sub>	12 kHz to 20 MHz (OC-48)	—	0.25	0.40	ps
		50 kHz to 80 MHz (OC-192)	—	0.26	0.37	
Phase Jitter (RMS)* for F <sub>OUT</sub> of 125 to 500 MHz	ϕ <sub>J</sub>	12 kHz to 20 MHz (OC-48)	—	0.36	0.50	ps
		50 kHz to 20 MHz (OC-192)	—	0.34	0.42	

**\*Note:** Differential Modes: LVPECL/LVDS/CML. Refer to AN256 for further information.

**Table 5. CLK± Output Period Jitter**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter*	J <sub>PER</sub>	RMS	—	2	—	ps
		Peak-to-Peak	—	14	—	

**\*Note:** Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information.

**Table 6. CLK± Output Phase Noise (Typical)**

Offset Frequency (f)	120.00 MHz	156.25 MHz	622.08 MHz	Units
	LVDS	LVPECL	LVPECL	
100 Hz	-112	-105	-97	dBc/Hz
1 kHz	-122	-122	-107	
10 kHz	-132	-128	-116	
100 kHz	-137	-135	-121	
1 MHz	-144	-144	-134	
10 MHz	-150	-147	-146	
100 MHz	n/a	n/a	-148	

**Table 7. Absolute Maximum Ratings<sup>1</sup>**

Parameter	Symbol	Rating	Units
Maximum Operating Temperature	$T_{AMAX}$	85	°C
Supply Voltage	$V_{DD}$	-0.5 to +3.8	Volts
Input Voltage (any input pin)	$V_I$	-0.5 to $V_{DD} + 0.3$	Volts
Storage Temperature	$T_S$	-55 to +125	°C
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2500	Volts
Soldering Temperature (Pb-free profile) <sup>2</sup>	$T_{PEAK}$	260	°C
Soldering Temperature Time @ $T_{PEAK}$ (Pb-free profile) <sup>2</sup>	$t_p$	20–40	seconds

**Notes:**

- Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
- The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download at [www.silabs.com/VCXO](http://www.silabs.com/VCXO) for further information, including soldering profiles.

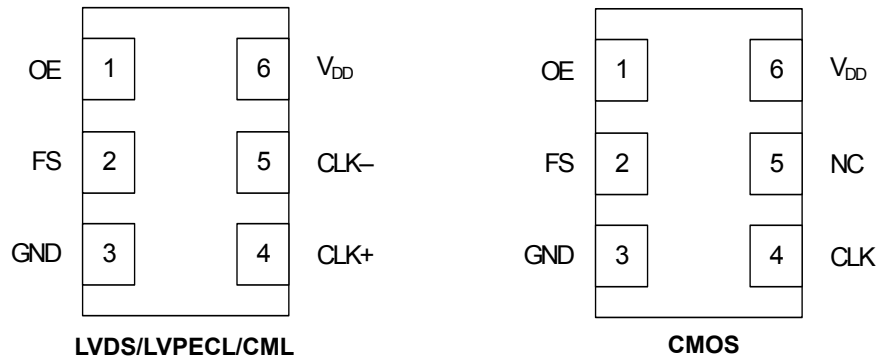
**Table 8. Environmental Compliance**

The Si533 meets the following qualification test requirements.

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002.3 B
Mechanical Vibration	MIL-STD-883F, Method 2007.3 A
Solderability	MIL-STD-883F, Method 203.8
Gross & Fine Leak	MIL-STD-883F, Method 1014.7
Resistance to Solvents	MIL-STD-883F, Method 2016

## 2. Pin Descriptions

(Top View)



Pin #	Symbol	LVDS/LVPECL/CML Function	CMOS Function
1	OE*	Output Enable* 0 = clock output disabled (outputs tristated) 1 = clock output enabled	Output Enable* 0 = clock output disabled (outputs tristated) 1 = clock output enabled
2	FS*	Frequency Select* 0 = First frequency selected 1 = Second frequency selected	Frequency Select* 0 = First frequency selected 1 = Second frequency selected
3	GND	Electrical and Case Ground	Electrical and Case Ground
4	CLK+	Oscillator Output	Oscillator Output
5	CLK-	Complementary Output	No Connection
6	V <sub>DD</sub>	Power Supply Voltage	Power Supply Voltage

**\*Note:** FS and OE include a 17 kΩ pullup resistor to V<sub>DD</sub>. See Section 3. "Ordering Information" on page 7 for details on frequency value ordering.

### 3. Ordering Information

The Si533 XO supports a variety of options including frequency, temperature stability, output format, and  $V_{DD}$ . Specific device configurations are programmed into the Si533 at time of shipment. Configurations can be specified using the Part Number Configuration chart below. Silicon Laboratories provides a web browser-based part number configuration utility to simplify this process. Refer to [www.silabs.com/VCXOPartNumber](http://www.silabs.com/VCXOPartNumber) to access this tool and for further ordering instructions. The Si533 is supplied in an industry-standard, RoHS compliant, 6-pad, 5 x 7 mm package. The Si533 supports output enable (OE) on pin 1.

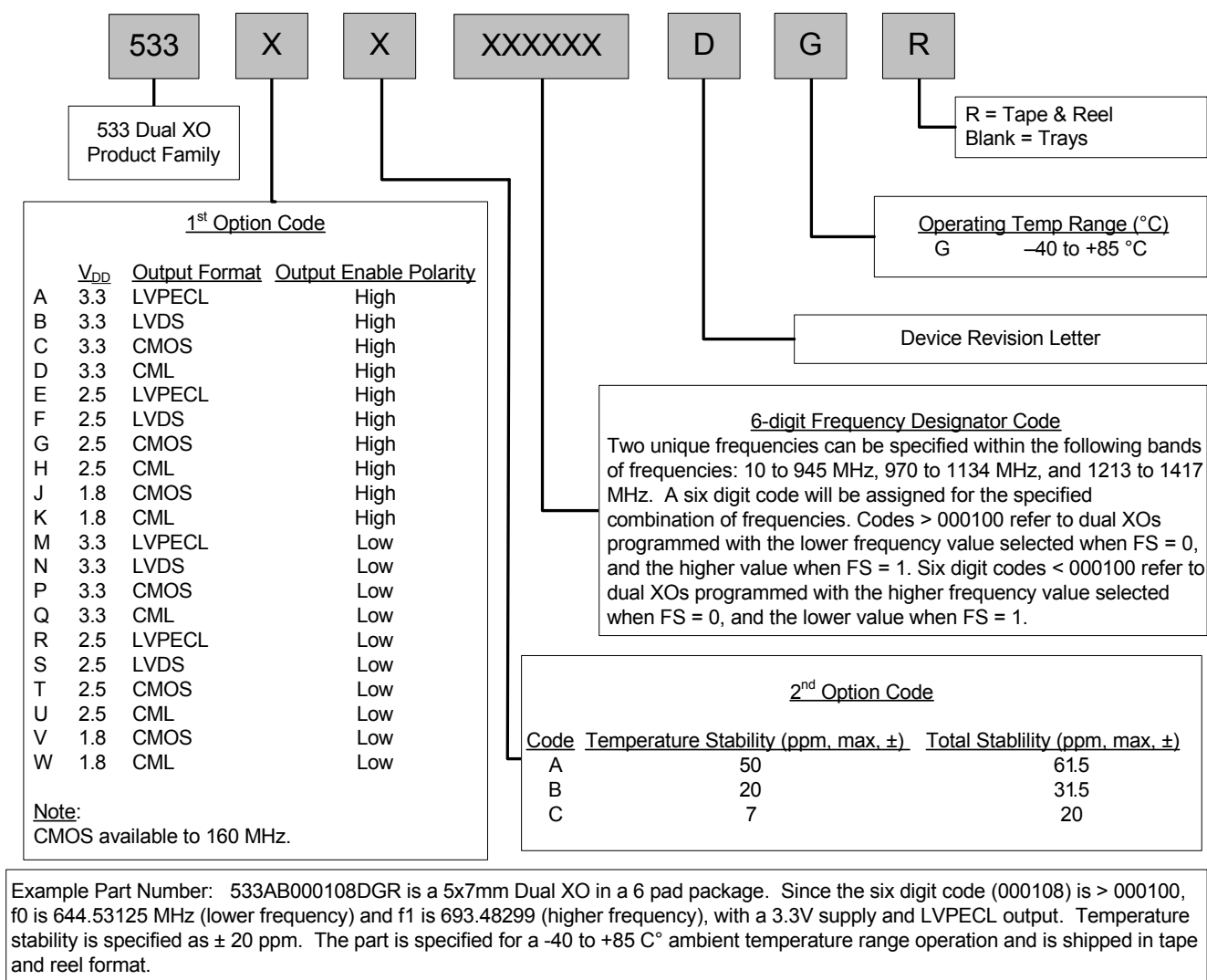


Figure 1. Part Number Convention

## 4. Outline Diagram and Suggested Pad Layout

Figure 2 illustrates the package details for the Si533. Table 9 lists the values for the dimensions shown in the illustration.

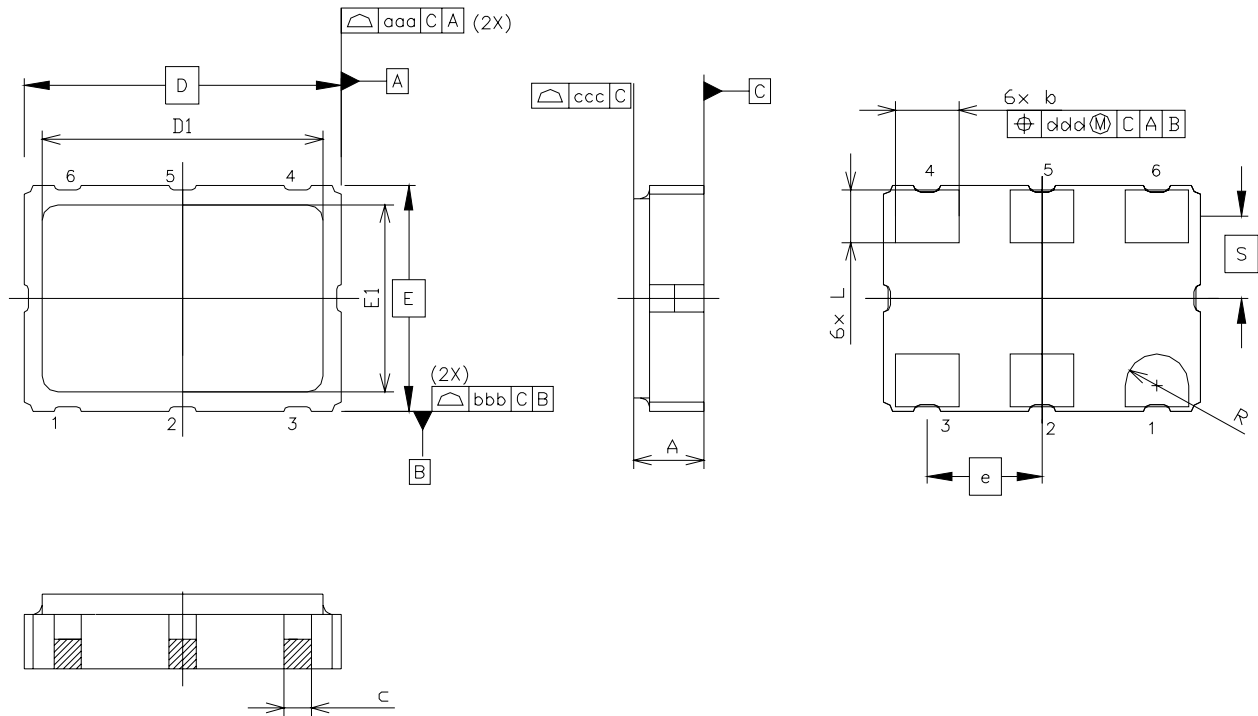


Figure 2. Si533 Outline Diagram

Table 9. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.45	1.65	1.85
b	1.2	1.4	1.6
c	0.60 TYP.		
D	7.00 BSC.		
D1	6.10	6.2	6.30
e	2.54 BSC.		
E	5.00 BSC.		
E1	4.30	4.40	4.50
L	1.07	1.27	1.47
S	1.815 BSC.		
R	0.7 REF.		
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10



## 5. Si533 Mark Specification

Figure 3 illustrates the mark specification for the Si533. Table 10 lists the line information.



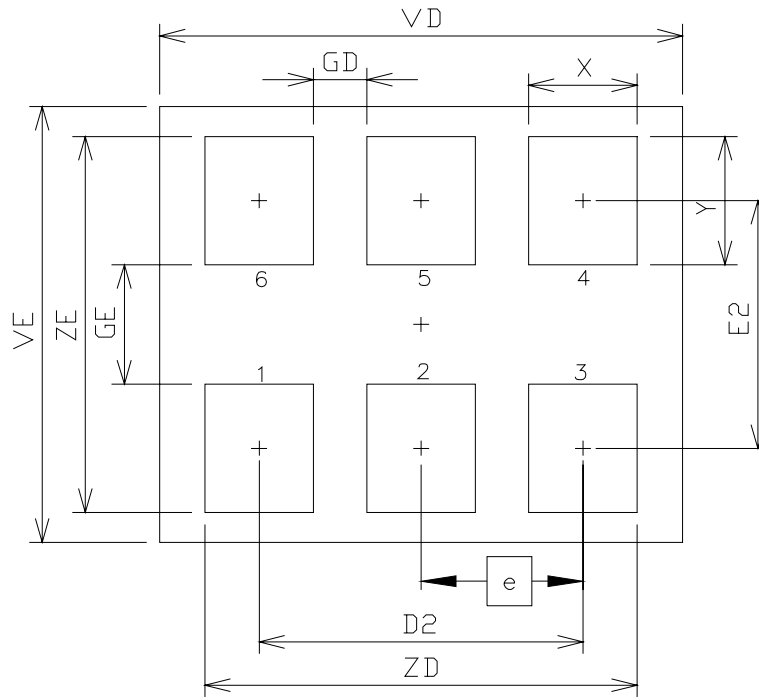
**Figure 3. Mark Specification**

**Table 10. Si53x Top Mark Description**

Line	Position	Description
1	1–10	“SiLabs”+ Part Family Number, 5xx (First 3 characters in part number)
2	1–10	Si530, Si531: Option1 + Option2 + Freq(7) + Temp Si532, Si533, Si534, Si530/Si531 w/ 8-digit resolution: Option1 + Option2 + ConfigNum(6) + Temp
3	<b>Trace Code</b>	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2007 = 7)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	“+” to indicate Pb-Free and RoHS-compliant

## 6. 6-Pin PCB Land Pattern

Figure 4 illustrates the 6-pin PCB land pattern for the Si533. Table 11 lists the values for the dimensions shown in the illustration.



**Figure 4. Si533 PCB Land Pattern**

**Table 11. PCB Land Pattern Dimensions (mm)**

Dimension	Min	Max
D2		5.08 REF
e		2.54 BSC
E2		4.15 REF
GD	0.84	—
GE	2.00	—
VD		8.20 REF
VE		7.30 REF
X		1.70 TYP
Y		2.15 REF
ZD	—	6.78
ZE	—	6.30

**Notes:**

1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design based on IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

## DOCUMENT CHANGE LIST

### Revision 1.0 to Revision 1.1

- Updated Table 1, “Recommended Operating Conditions,” on page 2.
  - Device maintains stable operation over  $-40$  to  $+85$  °C operating temperature range.
  - Supply current specifications updated for revision D.
- Updated Table 2, “CLK± Output Frequency Characteristics,” on page 2.
  - Added specification for  $\pm 20$  ppm lifetime stability ( $\pm 7$  ppm temperature stability) XO.
- Updated Table 3, “CLK± Output Levels and Symmetry,” on page 3.
  - Updated LVDS differential peak-peak swing specifications.
- Updated Table 4, “CLK± Output Phase Jitter,” on page 4.
- Updated Table 5, “CLK± Output Period Jitter,” on page 4.
  - Revised period jitter specifications.
- Updated Table 7, “Absolute Maximum Ratings<sup>1</sup>,” on page 5 to reflect the soldering temperature time at  $260$  °C is 20–40 sec per JEDEC J-STD-020C.
- Updated 3. “Ordering Information” on page 7.
  - Changed ordering instructions to revision D.
- Added 5. “Si533 Mark Specification” on page 9.

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