National Semiconductor

October 2007

LM4510
Synchronous Step-Up DC/DC Converter with True Shutdown Isolation

General Description

The LM4510 is a current mode step-up DC/DC converter with a 1.2A internal NMOS switch designed to deliver up to 120 mA at 16V from a Li-Ion battery.

The device's synchronous switching operation (no external Schottky diode) at heavy-load, and non-synchronous switching operation at light-load, maximizes power efficiency.

True shutdown function by synchronous FET and related circuitry ensures input and output isolation.

A programmable soft-start circuit allows the user to limit the amount of inrush current during startup. The output voltage can be adjusted by external resistors.

The LM4510 features advanced short-circuit protection to maximize safety during output to ground short condition. During shutdown the feedback resistors and the load are disconnected from the input to prevent leakage current paths to ground.

The LM4510 is available in a 10-pin thermally enhanced Leadless Leadframe Package: LLP-10.

Features

- 18V@80 mA from 3.2V input
- 5V@280 mA from 3.2V input
- No external Schottky diode required
- 85% peak efficiency
- Soft start
- True shutdown isolation
- Stable with small ceramic or tantalum output capacitors
- Output short-circuit protection
- Feedback fault protection
- Input under-voltage lock out
- Thermal shutdown
- 0.002 µA shutdown current
- Wide input voltage range: 2.7V to 5.5V
- 1.0 MHz fixed frequency operation
- Low-profile 10–pin LLP package (3mm x 3mm x 0.8mm)

Applications

- Organic LED Panel Power Supply
- Charging Holster
- White LED Backlight
- USB Power Supply
- Class D Audio Amplifier
- Camera Flash LED Driver

Typical Application Circuit

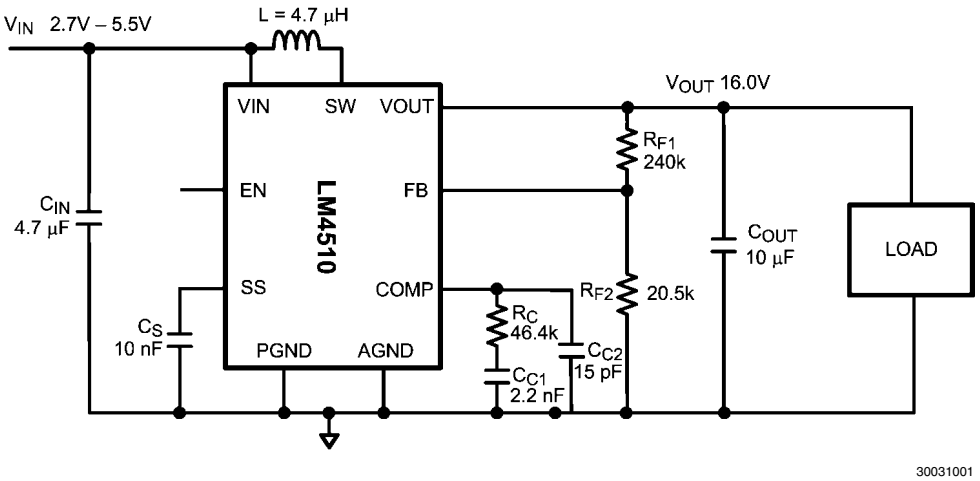
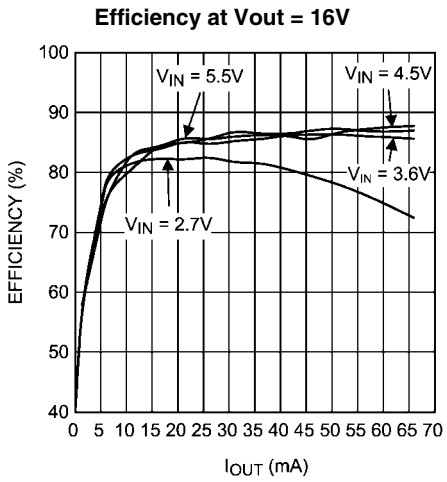


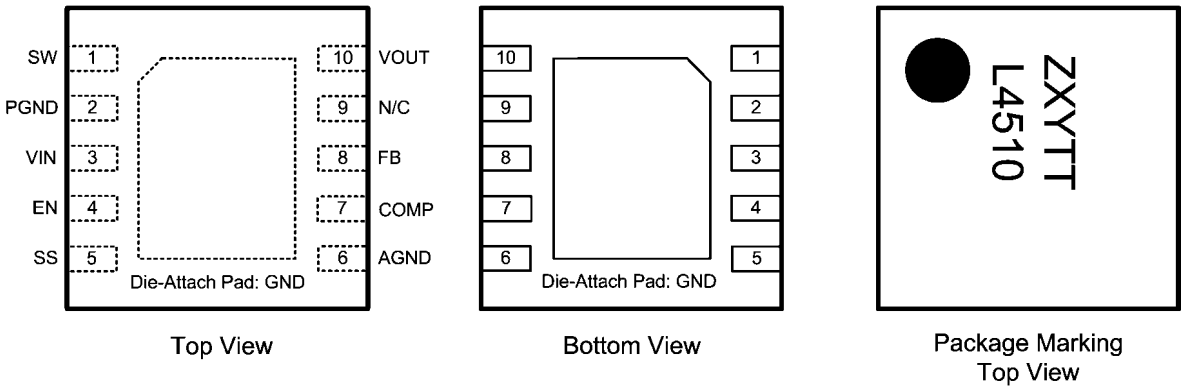
FIGURE 1. Typical Application Circuit



30031030

Connection Diagram

LLP-10 No Pullback Package, 3mm x 3mm x 0.8mm
NS Package Number SDA10A



Note: The actual physical placement of the package marking will vary from part to part. The package marking "ZXYTT" is a code for die traceability. "L4510" identifies the device (part number, voltage option, etc.). See the Order Information table below for the device ID codes.

30031002

Ordering Information

Order Number	SPEC	Package Type	NSC Package Drawing	Package Marking	Supplied As
LM4510SD	NOPB	LLP-10	SDA10A	L4510	1000 Units, Tape and Reel
LM4510SDX	NOPB	LLP-10	SDA10A	L4510	4500 Units, Tape and Reel

Pin Descriptions/Functions

Pin	Name	Function
1	SW	Switch pin. Drain connections of both internal NMOS and PMOS devices.
2	PGND	Power ground
3	VIN	Analog and Power supply input. Input range: 2.7V to 5.5V.
4	EN	Enable logic input. HIGH= Enabled, LOW=Shutdown.
5	SS	Soft-start pin
6	AGND	Analog ground
7	COMP	Compensation network connection.

Pin	Name	Function
8	FB	Output voltage feedback connection.
9	N/C	No internal connection.
10	VOUT	Internal PMOS source connection for synchronous rectification.
DAP	DAP	Die Attach Pad thermal connection

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN	−0.3V to 6.5V
VOUT	−0.3V to 21V
SW (Note 3)	−0.3V to V_{OUT}+0.3V
EN, SS, COMP FB	−0.3V to 6.5V
PGND to AGND	−0.2V to 0.2V
Continuous Power Dissipation (Note 4)	Internally Limited
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temperature (Soldering, 10 sec) (Note 5)	260°C
ESD Ratings (Note 12)	
Human Body Model	2.0kV
Machine Model	200V

Operating Conditions

Supply Voltage Range (V_{IN})	2.7V to 5.5V
Junction Temperature Range (T_J) (Note 6)	−40°C to +125°C
Ambient Temperature Range (T_A)	−40°C to +85°C
Output Voltage Range (V_{OUT})	Up to 18V

Thermal Properties

Junction to Ambient Thermal Resistance (θ_{JA}) LLP-10 Package (Note 7)	36°C/W

Electrical Characteristics (Notes 8, 9)

Limits in standard type face are for T_J = 25°C only. Limits in **boldface type** apply over the full operating junction temperature range (−40°C ≤ T_J ≤+125°C). Unless otherwise stated the following conditions apply: VIN = 3.6V, EN = 3.6V.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 9)	Max (Note 8)	Units
V_{FB}	FB Pin Voltage	2.7V ≤ VIN ≤ 5.5V	**1.24**	1.265	**1.29**	V
I_{FB}	FB Pin Bias Current (Note 11)			0.050	**1.5**	µA
$R_{DS(on)}$	NMOS Switch $R_{DS(on)}$	I_{SW} = 0.3A		0.45	1.1	Ω
	PMOS Switch $R_{DS(on)}$	I_{SW} = 0.3A, VOUT = 10V		0.9	1.1	
I_{CL}	NMOS Switch Current Limit		1.0	1.2	1.8	A
I_Q	Device Switching	EN = 3.6V, FB = COMP		1.7	**2.5**	mA
	Non-switching Current	EN = 3.6V, FB > 1.29V		0.8	**2.0**	mA
	Shutdown Current	EN = 0V		0.002	0.050	µA
I_L	SW Leakage Current (Note 11)	SW = 20V		0.01	0.150	µA
I_{VOUT}	VOUT Bias Current (Note 11)	VOUT = 20V	**50**	90	**150**	µA
I_{VL}	PMOS Switch Leakage Current	SW = 0V, VOUT = 20V		0.001	0.100	µA
f_{SW}	Switching Frequency		**0.85**	1.0	**1.2**	MHz
D_{MAX}	Maximum Duty Cycle	FB = 0V	**88**	94		%
D_{MIN}	Minimum Duty Cycle			15	20	%
Gm	Error Amplifier Transconductance		**70**	130	**200**	µmho
EN Threshold	Device Enable	HIGH	**1.2**	0.81		V
	Device Shutdown	LOW		0.78	**0.4**	
I_{EN}	EN Pin Bias Current	0 < EN < 3.6V		3.2	**8.0**	µA
FB Fault Protection	Feedback Fault Protection	ON Threshold	**18.0**	19.7	**20.7**	V
		OFF Threshold	**17.0**	18.7	**20.0**	
UVLO	Input Undervoltage Lockout	ON Threshold		2.5	**2.65**	V
		OFF Threshold	**2.1**	2.35		
I_{SS}	Soft-Start Pin Current (Note 10)		**9**	11.3	**15**	µA

Note 1: Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: This condition applies if $V_{IN} < V_{OUT}$. If $V_{IN} > V_{OUT}$, a voltage greater than V_{IN} + 0.3V should not be applied to the VOUT or VSW pins. The absolute maximum specification applies to DC voltage. An extended negative voltage limit of -1V applies for a pulse of up to 1 µs, and -2V for a pulse of up to 40 ns. An extended positive voltage limit of 22V applies for a pulse of up to 20 ns.

Note 4: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=150°C (Typ.) and disengages at T_J=140°C (Typ.).

Note 5: For detailed soldering information and specifications, please refer to National Semiconductor Application Note 1187: Leadless Leadframe Package (LLP) , available at www.national.com.

Note 6: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$

Note 7: Junction-to-ambient thermal resistance (θ_{JA}) is taken by a numerical analysis conforming to JEDEC standards. In applications where high maximum power dissipation exists (high V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues when designing the board layout. For more information on these topics, please refer to Application Note 1187: Leadless Leadframe Package (LLP).

Note 8: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are production tested, guaranteed through statistical analysis or guaranteed by design. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 9: Typical numbers are at 25°C and represent the most likely norm.

Note 10: Current flows out of the pin.

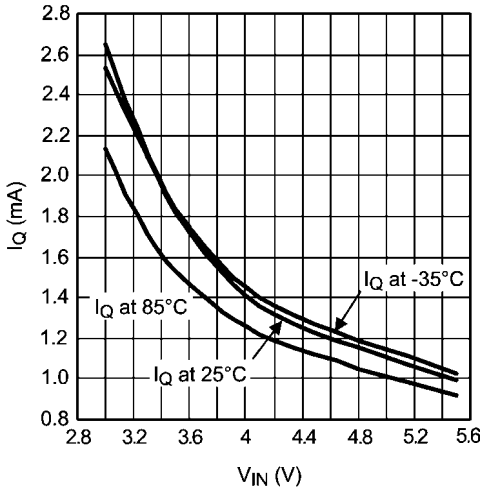
Note 11: Current flows into the pin.

Note 12: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin (MIL-STD-883 3015.7). The machine model is a 200 pF capacitor discharged directly into each pin.

Typical Performance Characteristics

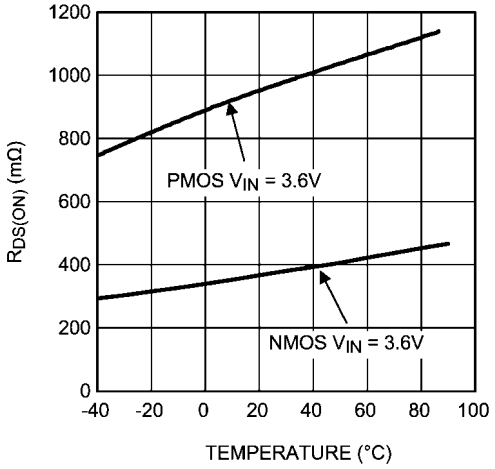
LM4510SD, Circuit of Figure 1, (L=4.7 µH, COILCRAFT, DO3316-472ML; C_{IN}=4.7 µF, TDK, C2012X5R0J475K; C_{OUT}=10 µF, AVX, 12103D106KAT2A; C_S=10 nF, TDK, C1608C0G1E103J; C_{C1}=2.2 nF, Taiyo Yuden, TMK107SD222JA-T; R_C=46.4 KΩ, Yageo, 9t06031A4642FBHFT), V_{IN}=3.6V, V_{OUT}=16V, T_A=25°C, unless otherwise noted.

Switching Quiescent Current vs V_{IN}



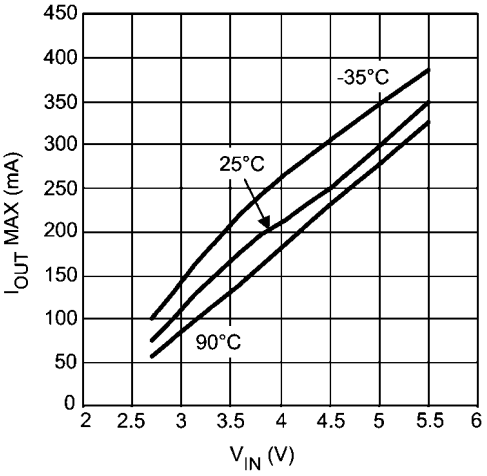
30031005

$R_{DS(on)}$ vs Temperature at V_{IN}= 3.6V



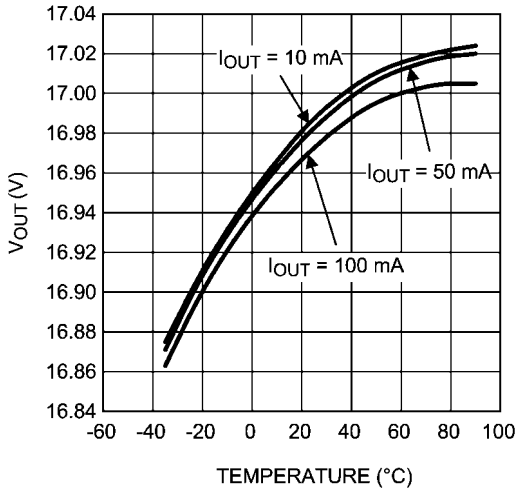
30031035

Load Capabilty vs V_{IN} (V_{OUT} = 16 V)



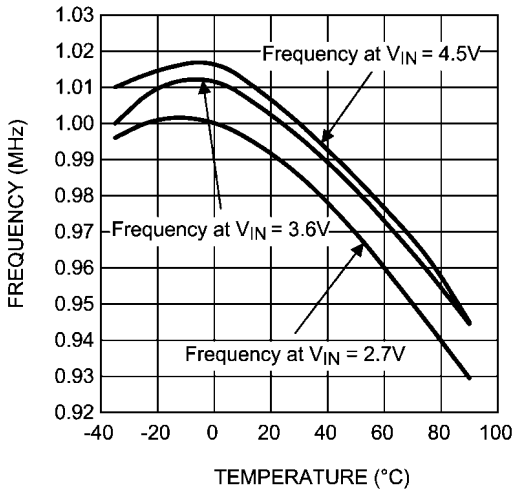
30031006

Output Voltage vs Temperature (V_{OUT} = 17 V)



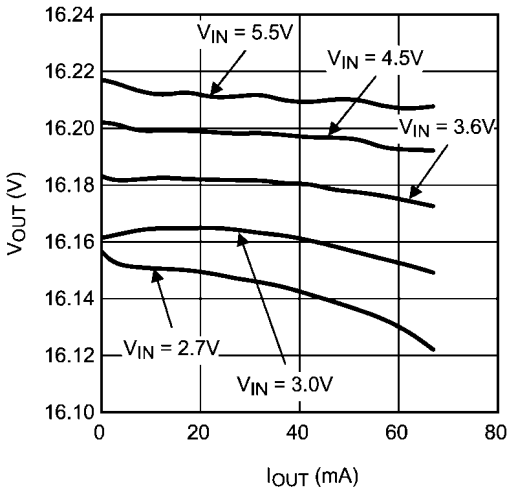
30031010

Switching Frequency vs Temperature



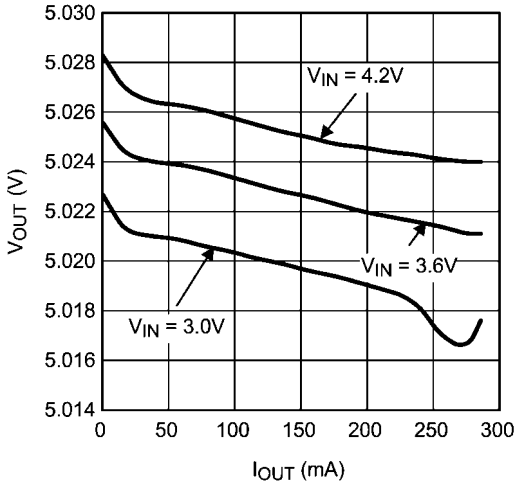
30031011

Load Regulation (V_{OUT} = 16 V)



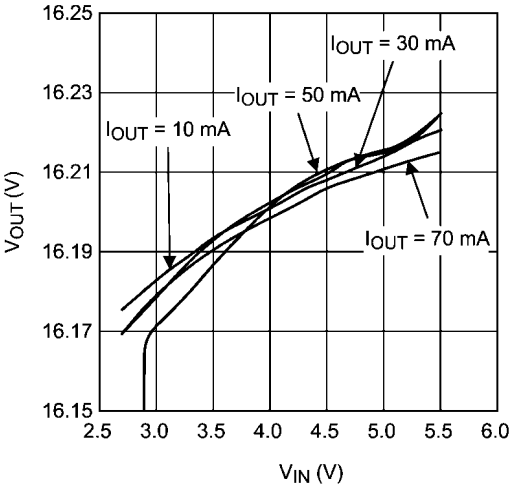
30031012

Load Regulation (V_{OUT} = 5 V)



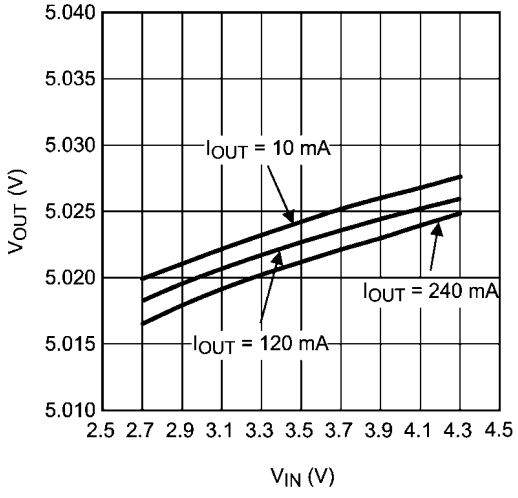
30031034

Line Regulation (V_{OUT} = 16 V)



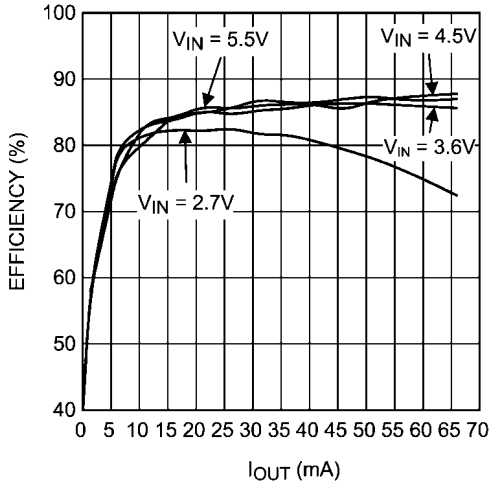
30031029

Line Regulation (V_{OUT} = 5 V)



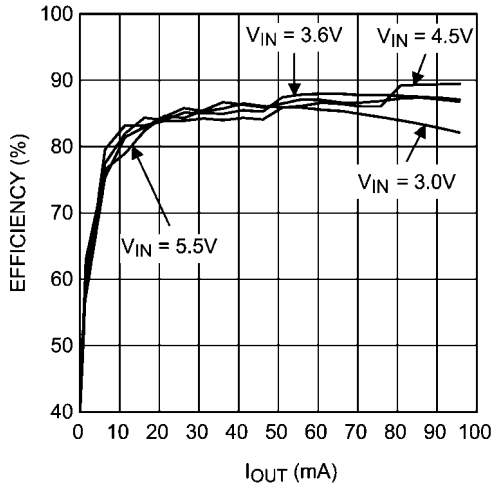
30031033

Efficiency vs Output Current (V_{OUT} = 16 V)



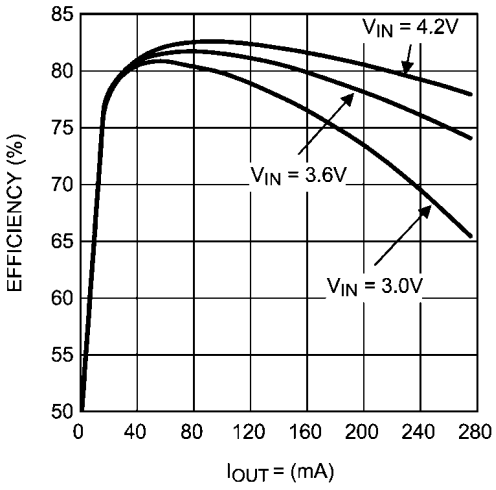
30031030

Efficiency vs Output Current
(V_{OUT} = 12 V)



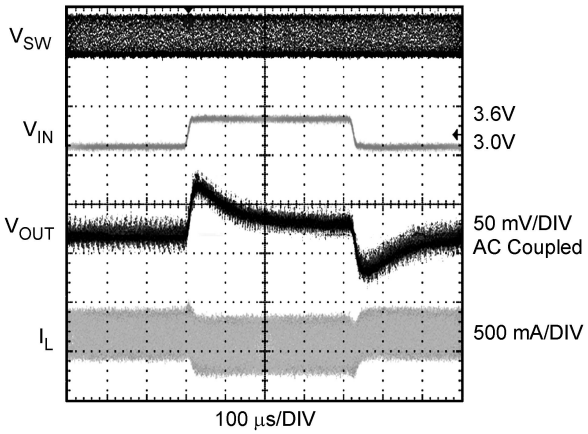
30031031

Efficiency vs Output Current
(V_{OUT} = 5 V, L= DO3314-472ML)



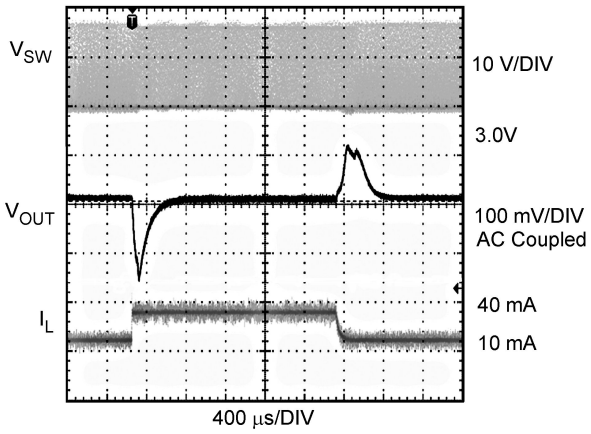
30031032

Line Transient Response
(V_{OUT} = 16 V)



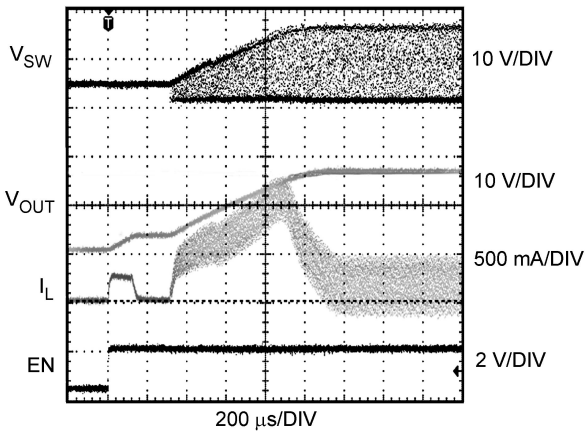
30031003

Load Transient Response
(V_{OUT} = 16 V)



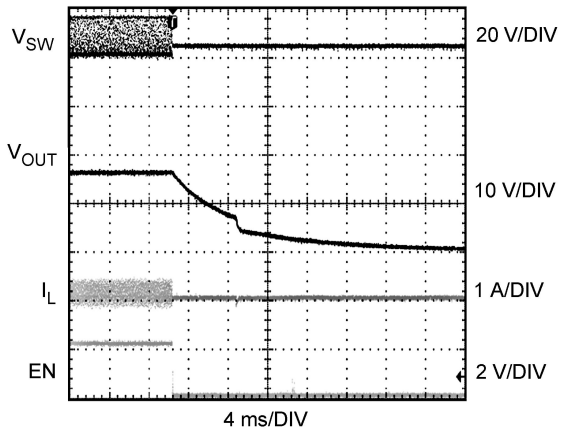
30031004

Start Up
(V_{OUT} = 16 V, R_{LOAD} = 530 Ω)



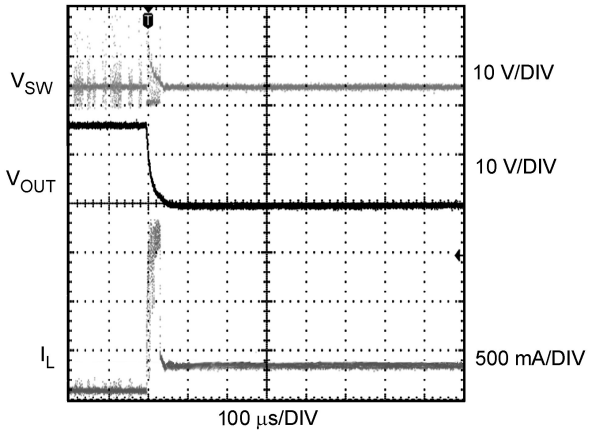
30031007

Shut Down
(V_{OUT} = 16 V, R_{LOAD} = 940 Ω)



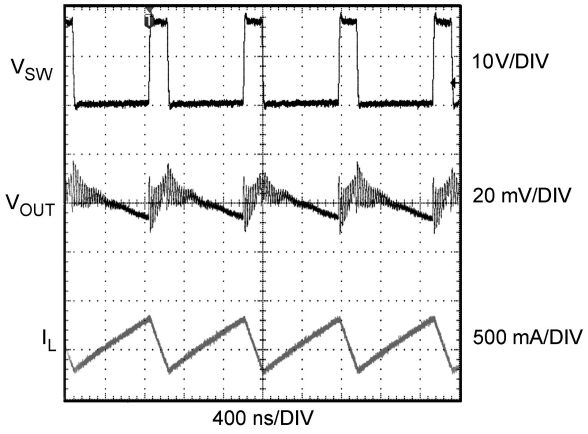
30031009

Short Circuit Response
(V_{OUT} = 16 V)



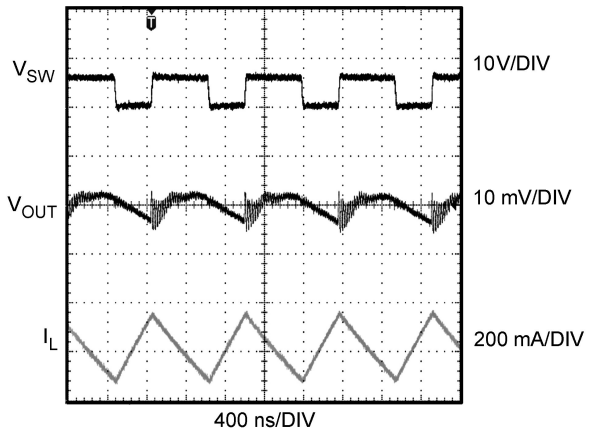
30031008

Output Voltage Ripple
(V_{OUT} = 16 V, I_{OUT} = 90 mA)



30031098

Output Voltage Ripple
(V_{OUT} = 5 V, I_{OUT} = 100 mA)



30031099

Block Diagram

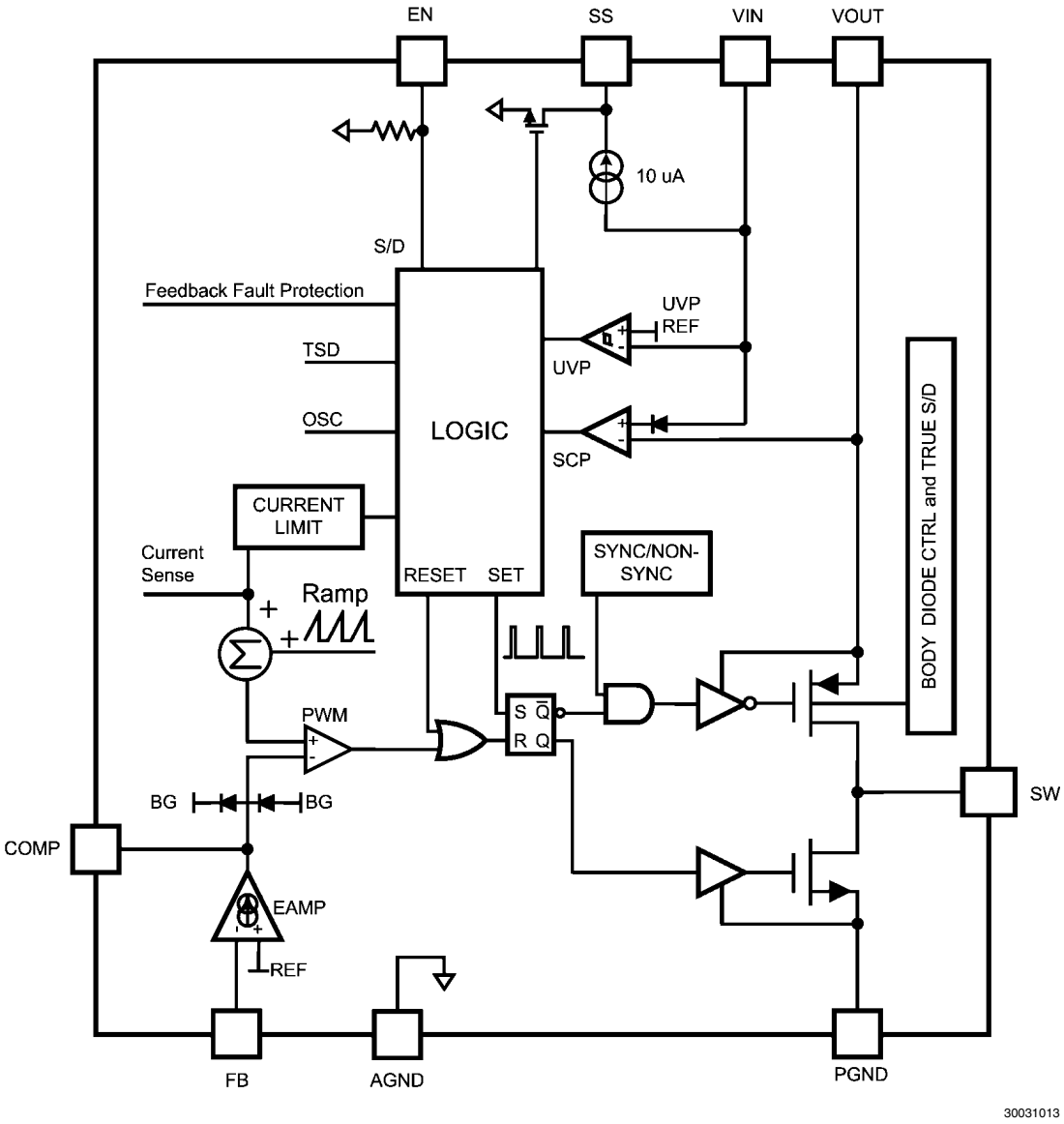


FIGURE 2. LM4510 Block Diagram

Operation Description

LM4510 is a peak current-mode, fixed-frequency PWM boost regulator that employs both Synchronous and Non-Synchronous Switching.

The DC/DC regulator regulates the feedback output voltage providing excellent line and load transient response. The operation of the LM4510 can best be understood by referring to the Block Diagram.

NON-SYNCHRONOUS OPERATION

The device operates in Non-synchronous Mode at light load (I_{OUT} < 10 mA) or when output voltage is lower than 10V (typ.). At light load, LM4510 automatically changes its switching operation from 'Synchronous' to 'Non-Synchronous' depending on V_{IN} and L. Non-Synchronous operation at light load maximizes power efficiency by reducing PMOS driving loss.

OPERATION IN SYNCHRONOUS CONTINUOUS CONDUCTION MODE (CYCLE 1, CYCLE 2)

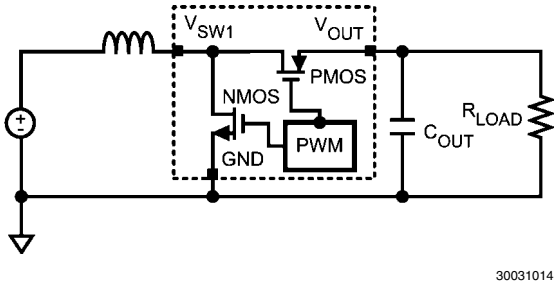


FIGURE 3. Schematic of Synchronous Boost Converter

Synchronous boost converter is shown in Figure 3. At the start of each cycle, the oscillator sets the driver logic and turns on the NMOS power device and turns off the PMOS power device.

Cycle 1 Description

Refer to Figure 4. NMOS switch turn-on → Inductor current increases and flows to GND.

PMOS switch turn-off → Isolate VOUT from SW → Output capacitor supplies load current.

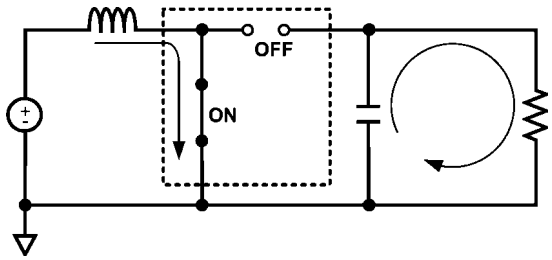


FIGURE 4. Equivalent Circuit During Cycle 1

During operation, EAMP output voltage (V_{COMP}) increases for larger loads and decreases for smaller loads. When the sum of the ramp compensation and the sensed NMOS current reaches a level determined by the EAMP output voltage, the PWM COMP resets the logic, turning off the NMOS power device and turning on the PMOS power device.

Cycle 2 Description

Refer to Figure 5. NMOS Switch turn-off → PMOS Switch turn-on→ Inductor current decreases and flows through PMOS → Inductor current recharges output capacitor and supplies load current.

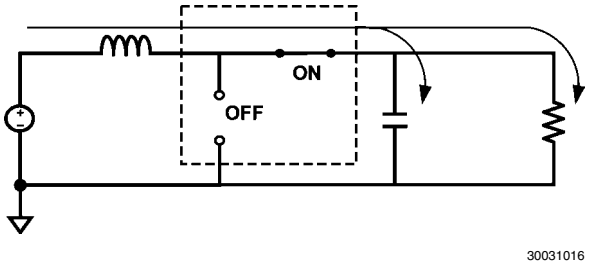


FIGURE 5. Equivalent Circuit During Cycle 2

After the switching period the oscillator then sets the driver logic again repeating the process.

ON/OFF CONTROL

The LM4510 shuts down when the EN pin is low. In this mode the feedback resistors and the load are disconnected from the input in order to avoid leakage current flow and to allow the output voltage to drop to 0V.

The LM4510 turns on when EN is high. There is an internal pull-down resistor on the EN pin so the device is in a normally off state.

SHORT CIRCUIT PROTECTION

When V_{OUT} goes down to V_{IN}–0.7V (typ.), the device stops switching due to the short-circuit protection circuitry and the short-circuit output current is limited to I_{INIT_CHARGE}.

FEEDBACK FAULT PROTECTION

The LM4510 features unique Feedback Fault Protection to maximize safety when the feedback resistor is not properly connected to a circuit or the feedback node is shorted directly to ground.

Feedback fault triggers V_{OUT} monitoring. During monitoring, if V_{OUT} reaches a protection level, the device shuts down. When the feedback network is reconnected and V_{OUT} is lower than the OFF threshold level of Feedback Fault Protection, V_{OUT} monitoring stops. V_{OUT} is then regulated by the control loop.

INPUT UNDER-VOLTAGE LOCK-OUT

The LM4510 has dedicated circuitry to protect the IC and the external components when the battery voltage is lower than the preset threshold. This under-voltage lock-out with hysteresis prevents malfunctions during startup or abnormal power off.

THERMAL SHUTDOWN

If the die temperature exceeds 150°C (typ.), the thermal protection circuitry shuts down the device. The switches remain off until the die temperature is reduced to approximately 140°C (typ.).

Application Information

ADJUSTING OUTPUT VOLTAGE

The output voltage is set using the feedback pin and a resistor voltage divider (R_{F1}, R_{F2}) connected to the output as shown in the Typical Application Circuit.

The ratio of the feedback resistors sets the output voltage.

R_{F2} Selection

First of all choose a value for R_{F2} generally between 10 kΩ and 25 kΩ.

R_{F1} Selection

Calculate R_{F1} using the following equation:

$$R_{F1} = \left(\frac{V_O}{V_{FB}} - 1\right) \times R_{F2}\,[\Omega]$$

Table 1 gives suggested component values for several typical output voltages.

TABLE 1. Suggested Component Values for Different Output Voltages

Output Voltage (V)	R_{F2} (kΩ)	R_{F1} (kΩ)	R_C (kΩ)	C_{C1} (nF)
16	20.5	240	46.4	2.2
12	20.5	174	46.4	2.2
5	20.5	60.4	46.4	2.2
3.3	20.5	33	46.4	2.2

MAXIMUM OUTPUT CURRENT

When the output voltage is set at different level, it is important to know the maximum load capability. By first order estimation, $I_{OUT(MAX)}$ can be estimated by the following equation:

$$I_{OUT\_Max} = \frac{1.32 \times V_{IN} - 2.79}{V_{OUT}} [A]$$

INDUCTOR SELECTION

The larger value inductor makes lower peak inductor current and reduces stress on internal power NMOS.

On the other hand, the smaller value inductor has smaller outline, lower DCR and a higher current capacity. Generally a 4.7 µH to 15 µH inductor is recommended.

I_{L_AVE} CHECK

The average inductor current is given by the following equation:

$$I_{L\_AVE} = \frac{I_{OUT}}{\eta \times D'} [A], D' = \frac{V_{IN}}{V_{OUT}}$$

Where I_{OUT} is output current, η is the converter efficiency of the total driven load and D' is the off duty cycle of the switching regulator.

Inductor DC current rating (40°C temperature rise) should be more than the average inductor current at worst case.

ΔI Define

The inductor ripple current is given by the following equations:

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} [A], D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

Where D is the on-duty cycle of the switching regulator. A common choice is to set ΔI_L to about 30% of I_{L_AVE}.

$I_{L\_PK} \leq I_{CL}$ Check & I_{MIN} Define

The peak inductor current is given by the following equation:

$$I_{L\_pk} = I_{L\_AVE} + \frac{\Delta I_L}{2} [A]$$

$$I_{L\_pk} = \frac{I_{OUT}}{\eta \times D'} + \frac{V_{IN} \times D}{2L \times f_{SW}} [A]$$

To prevent loss of regulation, ensure that the NMOS power switch current limit is greater than the worst-case peak inductor current in the target application.

Also make sure that the inductor saturation current is greater than the peak inductor current under the worst-case load transient, high ambient temperature and startup conditions. Refer to Table 2 for suggested inductors.

TABLE 2. Suggested Inductors and Their Suppliers

Model	Vendor	Dimensions LxWxH (mm)	D.C.R (max)
DO3314-472ML	COILCRAFT	3.3mm x 3.3mm x 1.4mm	320 mΩ
DO3316P-472ML	COILCRAFT	12.95mm x 9.4mm x 5.4mm	18 mΩ

INPUT CAPACITOR SELECTION

Due to the presence of an inductor, the input current waveform is continuous and triangular. So the input capacitor is less critical than output capacitor in boost applications. Typically, a 4.7 µF to 10 µF ceramic input capacitor is recommended on the VIN pin of the IC.

I_{CIN_RMS} Check

The RMS current in the input capacitor is given by the following equation:

$$I_{CIN\_RMS} = \frac{\Delta I_L}{\sqrt{12}} [A]$$

The input capacitor should be capable of handling the RMS current.

OUTPUT CAPACITOR SELECTION

The output capacitor in a boost converter provides all the output current when the switch is closed and the inductor is charging. As a result, it sees very large ripple currents.

A ceramic capacitor of value 4.7 µF to 10 µF is recommended at the output. If larger amounts of capacitance are desired for improved line support and transient response, tantalum capacitors can be used.

I_{COUT_RMS} Check

The RMS current in the output capacitor is given by the following equation:

$$I_{COUT\_RMS} = \sqrt{(1-D)\left[I_{OUT}^2 \frac{D}{(1-D)^2} + \frac{\Delta I_L^2}{12}\right]} [A]$$

The output capacitor should be capable of handling the RMS current.

The ESR and ESL of the output capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. The output capacitor also affects the soft-start time. See Soft-Start Function and Soft-Start Capacitor Selection. Table 3 shows suggested input and output capacitors.

TABLE 3. Suggested C_{IN} and C_{OUT} Capacitors and Their Suppliers

Model	Type	Vendor	Voltage Rating	Case Size Inch (mm)
4.7 µF for C_{IN}				
C2012X5R0J475	Ceramic, X5R	TDK	6.3V	0805 (2012)
GRM21BR60J475	Ceramic, X5R	muRata	6.3V	0805 (2012)
JMK212BJ475	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)
C2012X5R0J475K	Ceramic, X5R	TDK	6.3V	0603 (1608)
10 µF for C_{OUT}				
TMK316BJ106KL	Ceramic, X5R	Taiyo-Yuden	25V	1206 (3216)
12103D106KAT2A	Ceramic, X5R	AVX	25V	1210 (3225)

SOFT-START FUNCTION AND SOFT-START CAPACITOR SELECTION

The LM4510 has a soft-start pin that can be used to limit the input inrush current. Connect a capacitor from SS pin to GND to set the soft-start period. Figure 6 describes the soft start process.

- Initial charging period: When the device is turned on, the control circuitry linearly regulating initial charge current charges V_{OUT} by limiting the inrush current.
- Soft-start period: After V_{OUT} reaches V_{IN} -0.7V (typ.), the device starts switching and the C_S is charged at a constant current of 11 µA, ramping up to V_{IN}. This period ends when V_{SS} reaches V_{FB}. C_S should be large enough to ensure soft-start period ends after C_O is fully charged.

During the initial charging period, the required load current must be smaller than the initial charge current to ensure V_{OUT} reaches V_{IN} -0.7V (typ.).

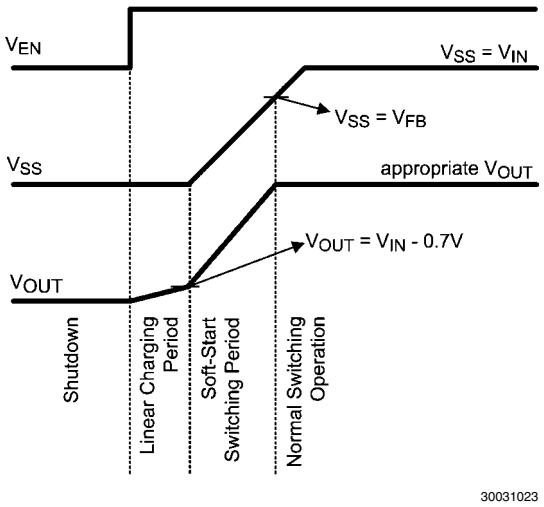


FIGURE 6. Soft Start Timing Diagram

C_S Selection

The soft-start time without load can be estimated as:

$$t_{SS} = \frac{C_{OUT} \times (V_{IN} - 0.7)}{I_{INIT\_CHARGE}} + \frac{C_S \times V_{FB}}{I_{SS\_CHARGE}} \text{ [sec]}$$

Where the I_{INIT_CHARGE} is Initial Charging Current depending on V_{IN} and I_{SS_CHARGE} (11 µA (typ.)). Also, when selecting the fuse current rating, make sure the value is higher than the initial charging current.

COMPENSATION COMPONENT SELECTION

The LM4510 provides a compensation pin COMP to customize the voltage loop feedback. It is recommended that a series combination of R_C and C_{C1} be used for the compensation network, as shown in the typical application circuit. In addition, C_{C2} is used for compensating high frequency zeros.

The series combination of R_C and C_{C1} introduces a pole-zero pair according to the following equations:

$$f_{PC} = \frac{1}{2\pi(R_C + R_O)C_{C1}} \text{ [Hz]}$$

$$f_{ZC} = \frac{1}{2\pi R_C C_{C1}} \text{ [Hz]}$$

In addition, C_{C2} introduces a pole according to the following equation:

$$f_{PC2} = \frac{1}{2\pi(R_C // R_O)C_{C2}} \text{ [Hz]}$$

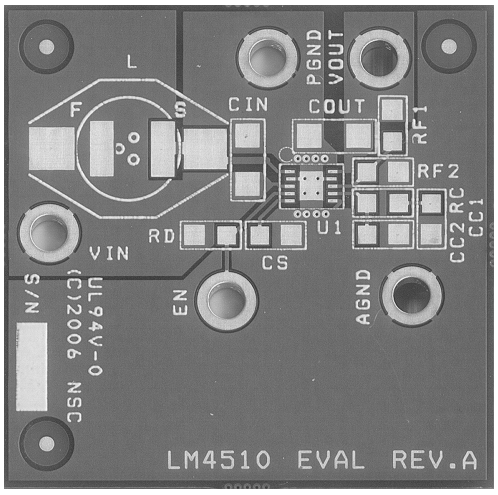
Where R_O is the output impedance of the error amplifier, approximately 1 MΩ, and amplifier voltage gain is typically 200 V/V depending on temperature and V_{IN}.

Refer to Table 4 for suggested soft start capacitor and compensation components.

TABLE 4. Suggested C_S and Compensation Components

Model	Type	Vendor	Voltage Rating	Case Size Inch (mm)
(C_S) C1608C0G1E103J	Ceramic, X5R	TDK	6.3V	603 (1608)
(C_1)TMK107SD222JA-T	Ceramic, X5R	Taiyo Yuden	25V	603 (1608)
(R_C) 9t06031A4642FBHFT	Resistor	Yageo Corporation	1/10W	603 (1608)

LAYOUT CONSIDERATIONS AND THERMAL MANAGEMENT



30031096

FIGURE 7. Evaluation Board Layout

High frequency switching regulators require very careful layout of components in order to get stable operation and low noise. All components must be as close as possible to the LM4510 device. Refer to Figure 7 as an example. Some additional guidelines to be observed:

1. C_{IN} must be placed close to the device and connected directly from VIN to PGND pins. This reduces copper trace resistance, which affects the input voltage ripple of the device. For additional input voltage filtering, typically a 0.1 uF bypass capacitor can be placed between VIN and AGND. This bypass capacitor should be placed near the device closer than C_{IN}.

2. C_{OUT} must also be placed close to the device and connected directly from VOUT to PGND pins. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly affects output voltage ripple and makes noise during output voltage sensing.

3. All voltage-sensing resistors (R_{F1}, R_{F2}) should be kept close to the FB pin to minimize copper trace connections that can inject noise into the system. The ground connection for the voltage-sensing resistor should be connected directly to the AGND pin.

4. Trace connections made to the inductor should be minimized to reduce power dissipation, EMI radiation and increase overall efficiency. Also poor trace connection increases the ripple of SW.

5. C_S, C_{C1}, C_{C2}, R_C must be placed close to the device and connected to AGND.

6. The AGND pin should connect directly to the ground. Not connecting the AGND pin directly, as close to the chip as possible, may affect the performance of the LM4510 and limit its current driving capability. AGND and PGND should be separate planes and should be connected at a single point.

7. For better thermal performance, DAP should be connected to ground, but cannot be used as the primary ground connection. The PC board land may be modified to a "dog bone" shape to reduce LLP thermal impedance. For detail information, refer to Application Note AN-1187.

FLASH/TORCH APPLICATION

LM4510 can be configured to drive white LEDs for the flash and torch functions. The flash/torch can be set up with the circuit shown in Figure 8 by using the resistor R_T to determine the current in Torch Mode and R_F to determine the current in Flash Mode. The amount of current can be estimated using the following equations:

$$I_{Torch} = \frac{V_{FB}}{R_T} [A]$$

$$I_{Flash} = \frac{V_{FB}}{R_T // R_F} [A]$$

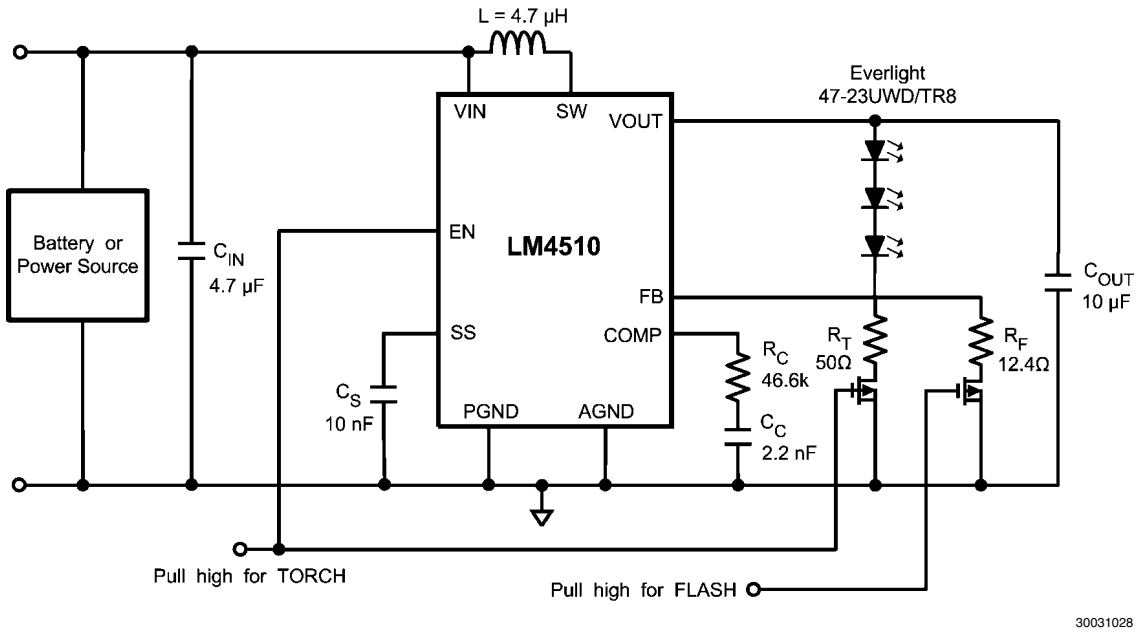
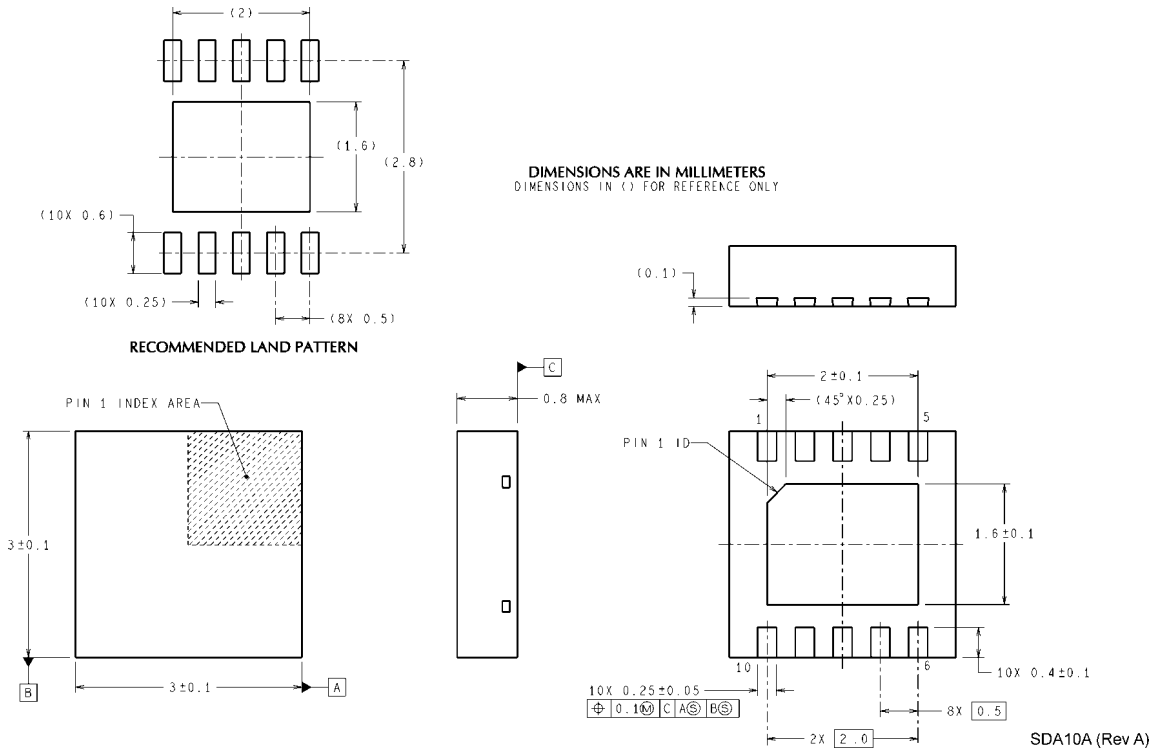


FIGURE 8. Flash/Torch Circuit Using LM4510

Physical Dimensions inches (millimeters) unless otherwise noted



10-pin LLP Package
For Ordering, Refer to Ordering Information Table
NS Package Number SDA10A
3mm x 3mm x 0.8mm

Notes

Notes

National Semiconductor Americas Customer Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Customer Support Center
Fax: +49 (0) 180-530-85-86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +49 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560