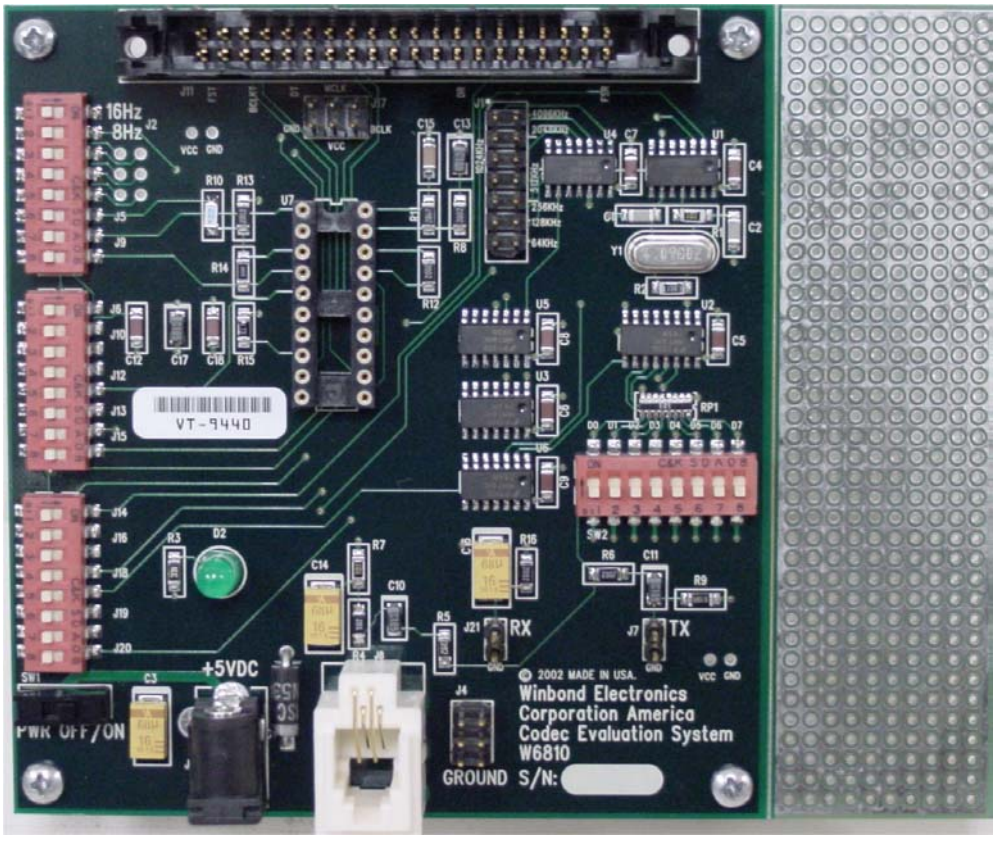
Winbond W6810 Codec Evaluation System User's Guide

W6810DK Evaluation Board Rev 1.06



Chapter - 1

General Description

Winbond's W6810DK Evaluation/Development System is a Stand-Alone unit that serves as a simple, easy-to-use demonstration board as well as a powerful evaluation system. All the functions of the W6810 PCM Codec may be selected in real time to allow complete evaluation of this IC for an end application. The hardware includes many useful connectors that will allow easy connection to external hardware for use as an evaluation tool.

Introduction:

The W6810 is a member of the W68XX family of PCM Codecs. This CMOS product includes a single voice band CODEC. The CODEC complies with the specifications of the ITU-T G.712 recommendation. The W6810 also includes a complete μ-Law and A-Law compander. The μ-Law and A-Law companders are designed to comply with the specifications of the ITU-T G.711 recommendation. The system can work at 256 kHz, 512 kHz, 1536 kHz, 1544 kHz, 2048 kHz, 2560 kHz & 4096 kHz clock rates. The system clock is supplied through the master clock input and can be derived from the bit-clock if desired.

User I/O to the W6810DK Evaluation board is provided via a number of connectors. These connectors are:

- A 40-pin header provides access to W6810 analog and digital signals (J11)
- RJ11 handset jack (J8)
- Analog transmit(J8) and receive path headers.(J7,J21)

W6810DK Features:

- Easy to use (a stand-alone evaluation system)
- Single 5 V power supply
- Single 3v Power Supply for W6811 or W68310
- Prototype area for application development
- Useful connectors that can be used to connect to standard test equipment
- RJ11 jack for standard handset

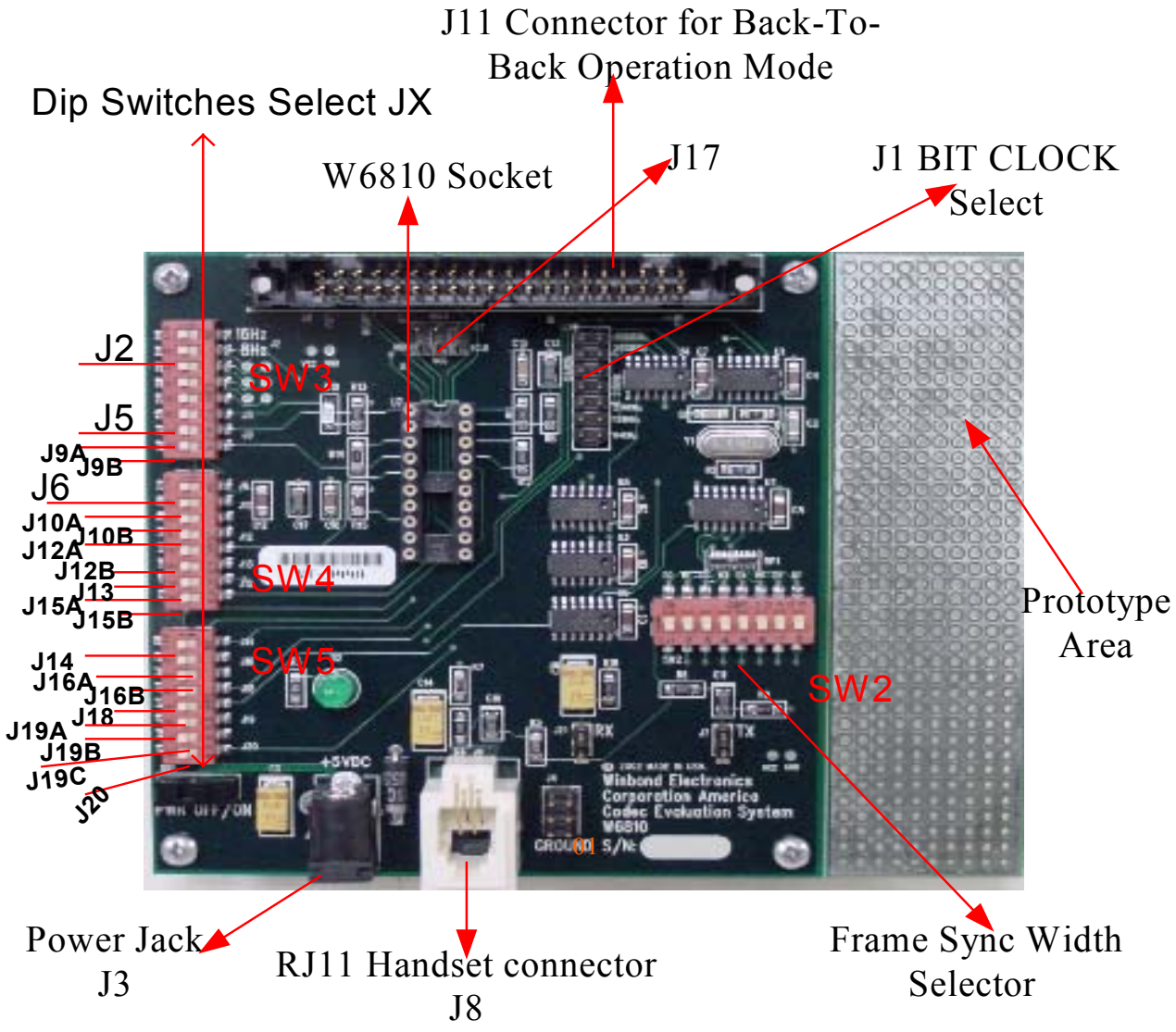


Figure 1: W6810DK Evaluation System Component Placement

Chapter - 2

Hardware Description

Clock Generator:

All the necessary clock rates such as Frame Sync, Bit Clock and the 256KHz for the W6810DK evaluation system are driven from a single 4.096MHz crystal oscillator.

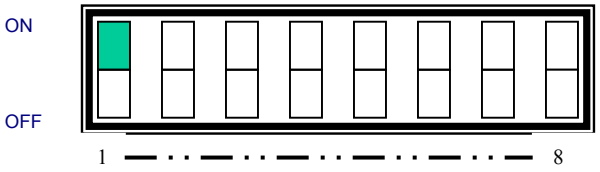
Frame Sync:

The Frame Sync is generated on the W6810DK evaluation board. J19 and J20(SW5) control the FSR (Frame Sync Receive) and FSX (Frame Sync Transmit) routing. Populating these jumpers also routes the signal to the 40-pin header (J11).
Setting Dip Switches:
Switch SW2 selects the width of the Frame Sync. The pulse width is set as a number of BCLKs. The following number of BCLKs for Frame Sync can be set with SW2.

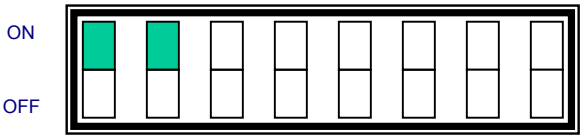
- 1-2-3-4-5-6-7-8

The Dip-Switch SW2 configurations are:

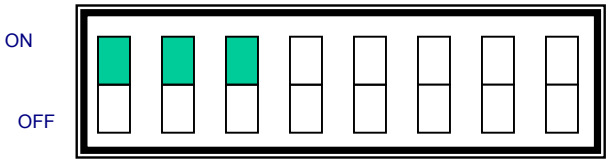
Frame Sync = 8 BCLK



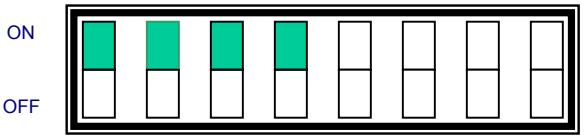
Frame Sync = 7 BCLK



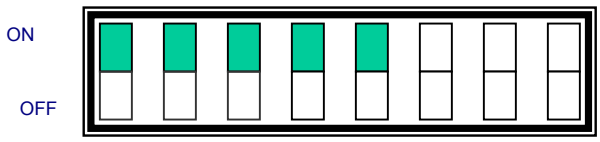
Frame Sync = 6 BCLK



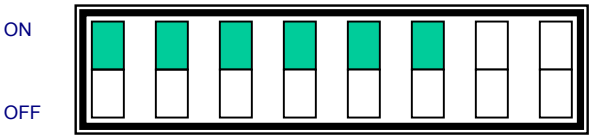
Frame Sync = 5 BCLK



Frame Sync = 4 BCLK



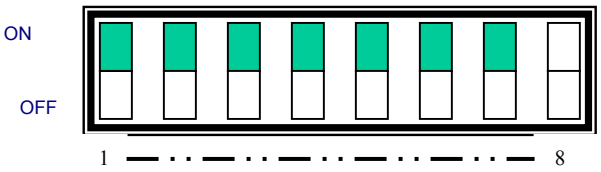
Frame Sync = 3 BCLK



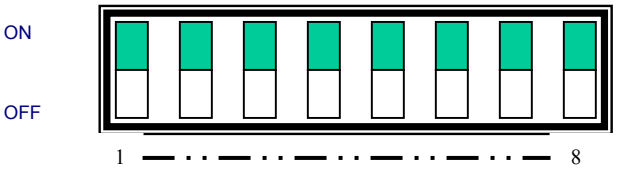
Long Frame Sync

Short Frame Sync

Frame Sync = 2



Frame Sync = 1



BIT CLOCK:

Bit clock is routed to the 2x20 (J11) header connector pins 5 (BCLKT) and 36 (BCLKR) through J17A and J14. J1 is used to select the frequency at which Bit Clock operates. The selected frequencies are 4.096 MHz, 2.048 MHz, 1.024 MHz, 512KHz, 128KHz and 64KHz.

256 KHZ:

The 256 KHz is a possible frequency setting for the master clock (MCLK) J15A(SW4) input on the chosen PCM Codec-filter. J15B will configure the MCLK input to have a frequency equal to Bit Clock.

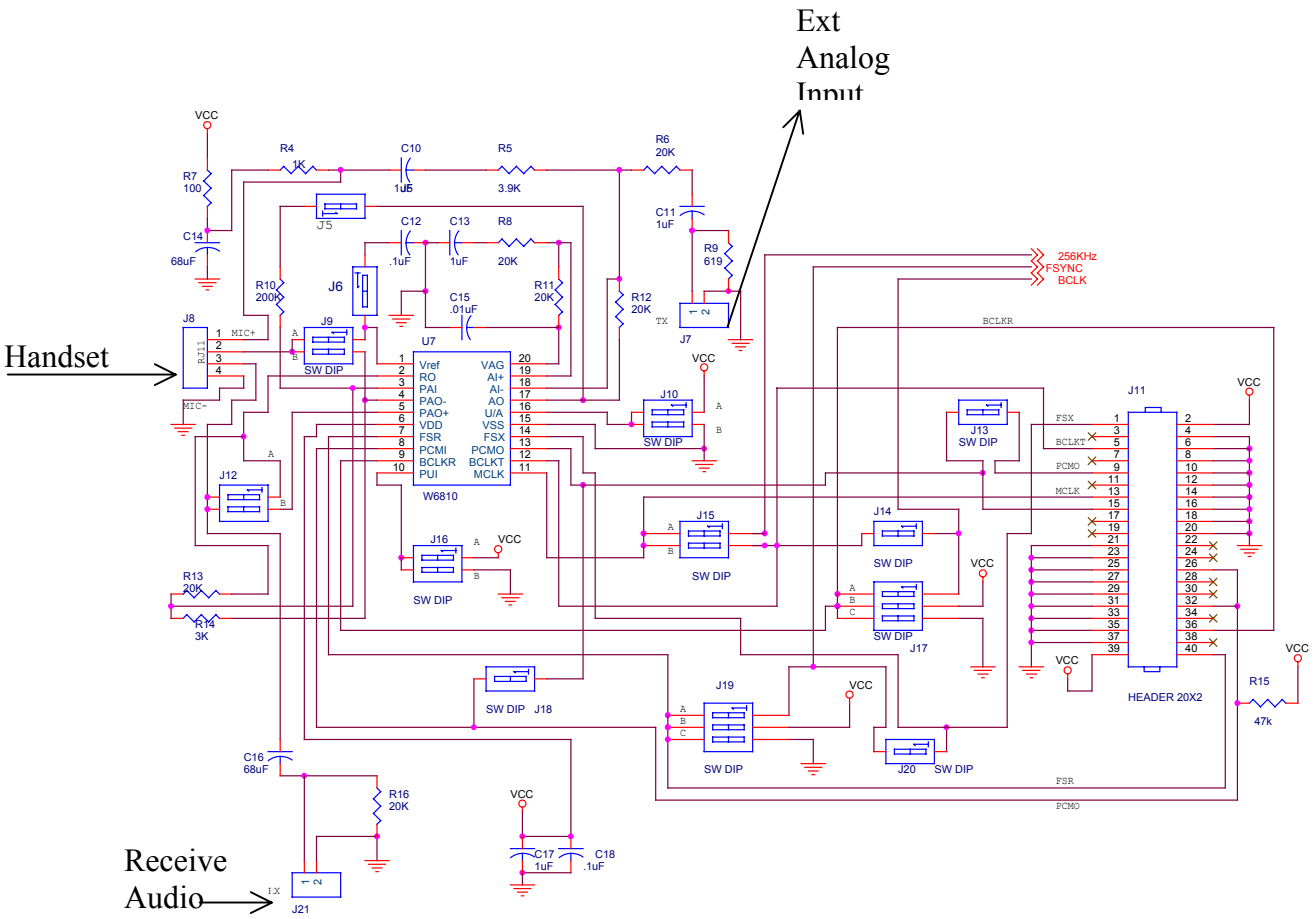


Figure 2: W6810DK Evaluation System Schematic Diagram

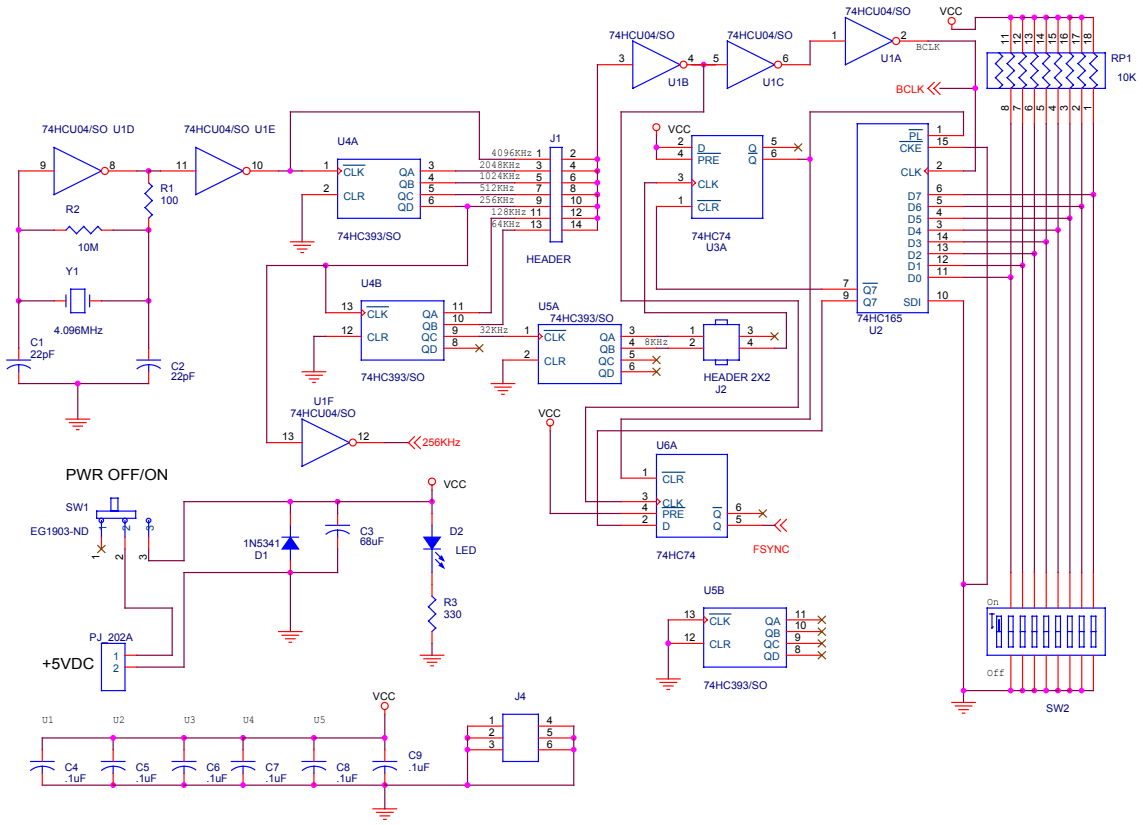


Figure 3: W6810DK Evaluation System Schematic Diagram:

Chapter - 3

Jumper Descriptions

Dips switches on the left hand corner of the evaluation system are used to select a particular jumper. When a Jumper is populated (switch is closed), it enables the function; an unpopulated Jumper(Open Switches) disables the function. A Jumper, when referenced as a letter for example J7A, J7B. Only one Jumper is populated for a selected function not both.

Please see page 4.Figure 1: W6810DK Evaluation System Component Placement

J1: Bit Clock Select:

J1 selects the Bit Clock frequencies from 4.096MHz to 64KHz.

J2A: Frame Sync:

J2A sets the Frame Sync (FSR) to 8KHz (SW3-2)

J3: Power Supply 5VDC

J4: GND TST points

J5: Side Tone (SW3-6)
J5 enables the side tone path on the PCM Codec filter

J6: VAG CAP ENABLE: (SW4-1)
J6 enables VAG filter cap

J7: Transmitter
Transmit output level at 1000Hz: -46dBV ± 4dB
Output Impedance at 100 Hz: 1000 ± 300 Ω

J8: RJ11 Handset connector.

J9A: 2.5V Reference Voltage (SW3-7)
J9A is not used.

J9B: SPKR+ = PAO (SW3-8)
J9B connects pin 4 W6810 to the RJ11 handset

J10: A-Law and μ-Law Selection: (SW4-2)

J10A Selects μ _Law and J10B Selects A-Law.

J11: 2x20 pin Header:

This 40-pin header provides access to W6810 analog and digital signals for a user defined system, or a second W6810DK evaluation system for back-to-back operation.

J12A: SPKR- = R0- (SW4-4)

J12A connects RO- (Pin2) to the RJ11 and the RX output connector.

J12B: SPKR-=PA0+ (SW4-5)

J12B connects PA0+ (Pin 5) to the RJ11 and the RX output connector.

J13: PCMT: (SW4-6)

J13 Connects the PCMT (PCM output W6810) to J11 (Pin 9).

J14: BCLKT=BCLK (SW5-1)

J14 connects BCLK to BCLKT (Pin 12) of the W6810 Codec-Filter.

J15A: MCLK = 256KHz (SW4-7)

J15A sets the MCLK Pin 11 to 256KHz.

J15B: MCLK=BCLK (SW4-8)

J15B sets the MCLK Pin 11 to be equal to BCLK.

J16A: POWER-UP (SW5-2)

J16A connects the PUI Pin10 of the W6810 Codec to VCC to power up the device.

J16B: POWER-Down (SW5-3)

J16B connects the PUI Pin10 of the W6810 Codec to GND to power down the device.

J17A: BCLKR = BCLK

J17A connects BCLKR (Pin 9) of the PCM W6810 Codec to BCLK.

J17B: BCLKR = BCLK

J17B connects BCLKR (Pin 9) of the PCM W6810 Codec to VCC.

J17C: BCLKR = BCLK

J17Cconnects BCLKR (Pin 9) of the PCM W6810 Codec to Ground

J18: PCMT = PCMR (SW5-4)

J18 Connects PCM output data transmit Pin (13) to PCM input data receive Pin (8) of the W6810 Codec.

J19A: FSR = FSYNC (SW5-5)

J19 A connects FSR (Pin 7) of the W6810 Codec to Frame Sync.

J19B: FSR = VCC (SW5-6)

J19 B connects FSR (Pin 7) of the W6810 Codec to VCC.

J19C: FSR = GND (SW5-7)

J19 C connects FSR (Pin 7) of the W6810 Codec to Ground.

J20: FSX= FSYNC (SW5-8)

J20 connects the on board generated Frame Sync to W6810 FSX (Pin 14) as well as to Pin 1 of the J11.

J21: Receiver Path

J21 can be connected to test equipment for measurements.

Receive output level at 1000Hz: 79dBSPL ± 4dB
Receive input Impedance at 100 Hz: 150Ω ± 20%

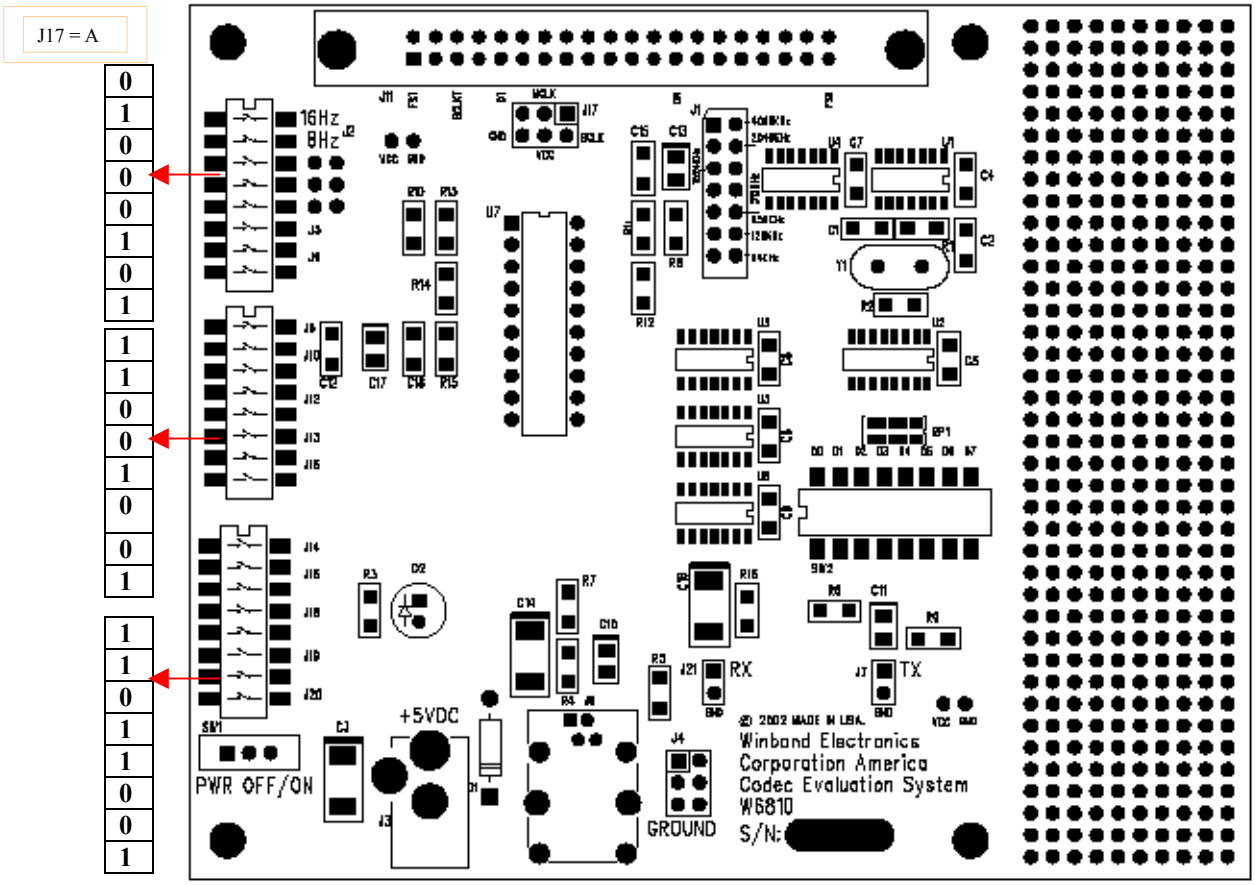
Chapter - 4

Operation Modes

The W6810DK operates in two modes, Standalone and Back- To- Back mode.

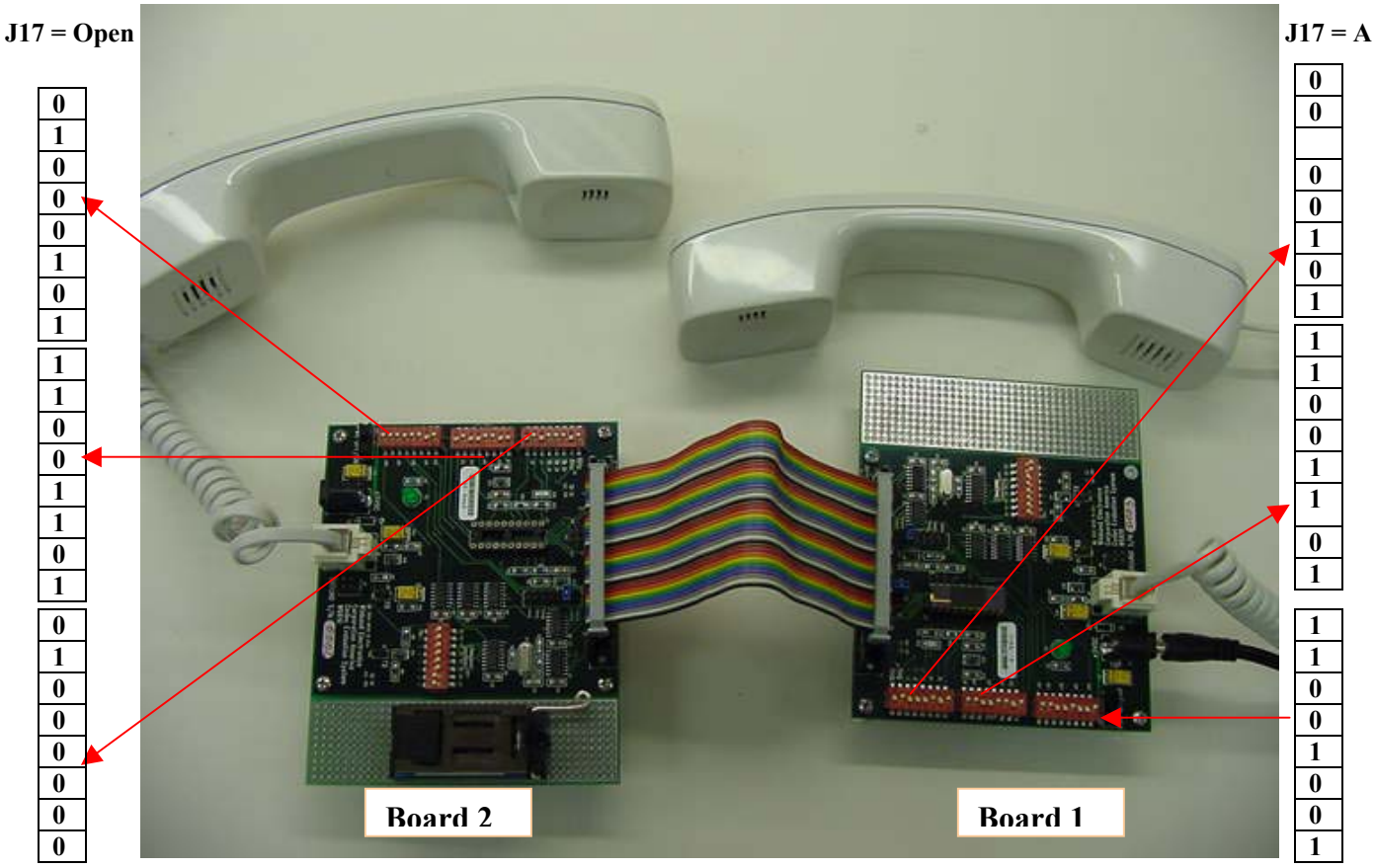
Standalone Operation:

In this mode of operation the W6810DK the signal input at Transmit input (J7), is presented to the encoder of the W6810, where it is digitized and output on the PCM input data transmit pin (J6). This provides a local loop back. Of the PCM, data to the PCM data input receive pin (PCMR) of the W6810, where it is reconstructed and output at J12 (RX). The following Jumpers are populated in this mode J1 (2.048MHz), J17A and J20 the Dipswitches are set as follows.



Back-To-Back Operation:

The W6810DK evaluation system can be connected back to back using the 20x2 header (J11) .The cable should be maximum 2-3 inches in length. It makes all necessary electrical connections, allowing a full "analog-to-analog, "handset-to-handset" path to be established.
For Back to Back operation the jumper setting are set to ON position as follows for (W6810DK #1 Master board) unit. J1 (2.048MHz), J2B, J5 (side tone), J9B, J6, J10, J7A J12B, J13, J15B, J14, J16, J19Aand J20B W6810DK #1 acts as the system master, providing BCLK and FSYNC to W6810DK #2. The jumper setting for board #2 is as follows. J1 (2.048MHz), J2, J5, J9B, J6, J10A J12B, J13, J15B and J16.
The following Dip-switches are set as for back-to-back -mode
Note: Do not connect the power supply to the second board. It will be bussed to the second board through the 2x20 cable. Make sure the cable is connected as shown below.

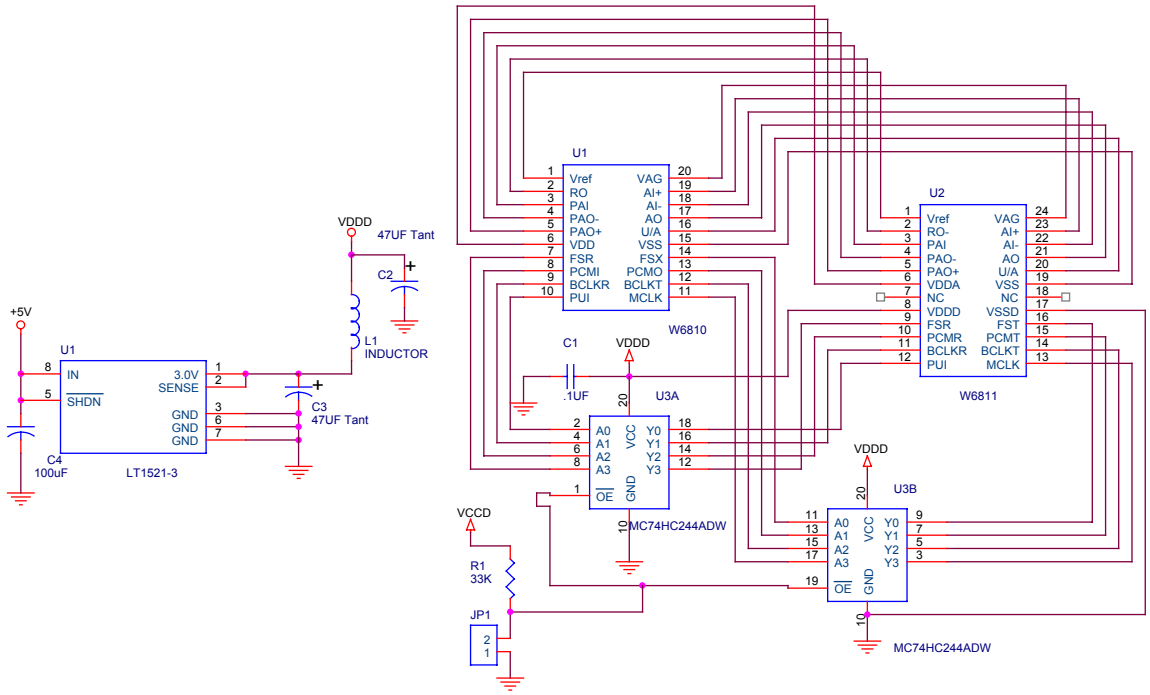


W6810 Conversion to W6811.

The W6811 is a general-purpose single channel PCM CODEC with pin-selectable μ-Law or A-Law companding. The device is compliant with the ITU G.712 specification. It operates off a separated analog (5V) and digital (3V) power supplies. Functions performed include digitization and reconstruction of voice signals, and band limiting and smoothing filters required for PCM systems. The filters are compliant with ITU G.712 specification. W6811 performance is specified over the industrial temperature range of –40°C to+85°C.

The W6811 includes an on-chip precision voltage reference and an additional power amplifier, Capable of driving 300 ohm loads differentially up to a level of 6.3V peak-to-peak. The analog section is fully differential, reducing noise and improving the power supply rejection ratio.

For evaluation of the W6811, use W6810DK prototype area to connect the W6811 to W6810 socket as shown below (only if it is desired to connect a separate 3V power supply for digital I/O otherwise use the direct connection below)



For performance evaluation of the W6811 with 5v Digital I/O (the device works similar to W6810) you can connect the W6810 Socket on the W6810DK to a prototype board which has the W6811 foot print as below.