National Semiconductor

October 1995

DP83950B RIC™ Repeater Interface Controller

General Description

The DP83950B Repeater Interface Controller "RIC" may be used to implement an IEEE 802.3 multiport repeater unit. It fully satisfies the IEEE 802.3 repeater specification including the functions defined by the repeater, segment partition and jabber lockup protection state machines.

The RIC has an on-chip phase-locked-loop (PLL) for Manchester data decoding, a Manchester encoder and an Elasticity Buffer for preamble regeneration.

Each RIC can connect to 13 cable segments via its network interface ports. One port is fully AUI compatible and is able to connect to an external MAU using the maximum length of AUI cable. The other 12 ports have integrated 10BASE-T transceivers. These transceiver functions may be bypassed so that the RIC may be used with external transceivers, for example DP8392 coaxial transceivers. In addition, large repeater units, containing several hundred ports may be constructed by cascading RICs together over an Inter-RIC bus.

The RIC is configurable for specific applications. It provides port status information for LED array displays and a simple interface for system processors. The RIC posseses multifunction counter and status flag arrays to facilitate network statistics gathering. A serial interface, known as the Management Interface is available for the collection of data in Managed Hub applications.

Features

- Compliant with the IEEE 802.3 Repeater Specification
- 13 network connections (ports) per chip
- Selectable on-chip twisted-pair transceivers
- Cascadable for large hub applications
- Compatible with AUI compliant transceivers
- On-chip Elasticity Buffer, Manchester encoder and decoder
- Separate partition state machines for each port
- Provides port status information for LED displays including: receive, collision, partition and link status
- Power-up configuration options:
  Repeater and Partition Specifications, Transceiver Interface, Status Display, Processor Operations
- Simple processor interface for repeater management and port disable
- On-chip Event Counters and Event Flag Arrays
- Serial Management Interface to combine packet and repeater status information together
- CMOS process for low power dissipation
- Single 5V supply

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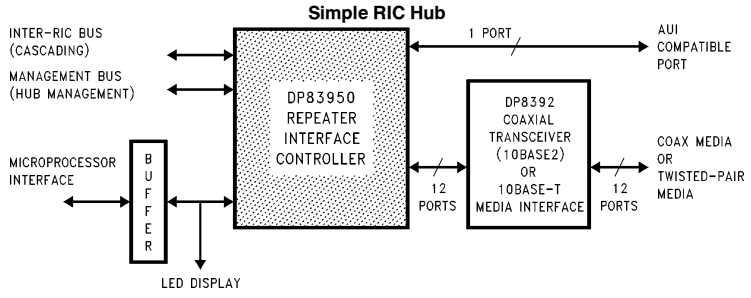
1.0 System Diagram



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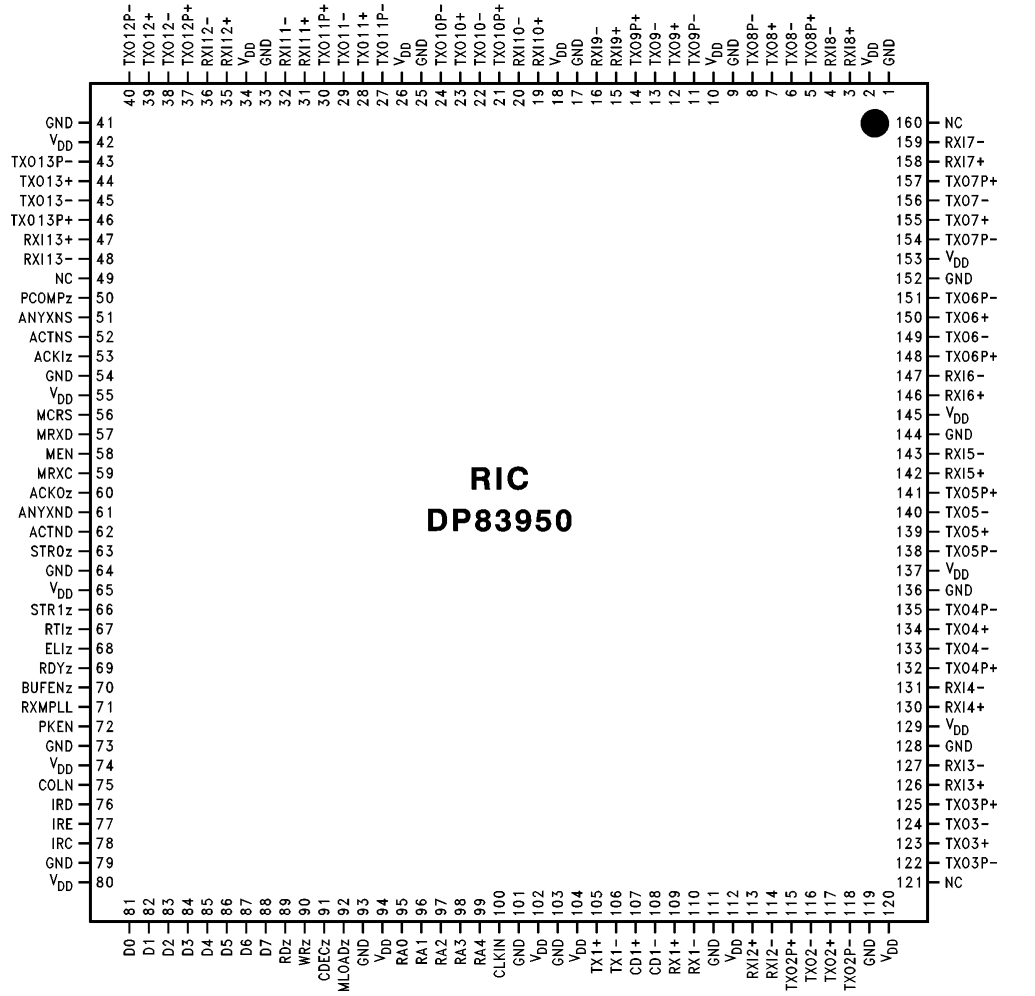
2.0 Connection Diagram—160 Pin PQFP Package

Pin Table (12 T.P. Ports + 1 AUI Bottom View)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TXO12P−	40	NC	160	V_{CC}	120	V_{CC}	80
TXO12+	39	RXI7−	159	GND	119	GND	79
TXO12−	38	RXI7+	158	TXO2P−	118	IRC	78
TXO12P+	37	TXO7P+	157	TXO2+	117	IRE	77
RXI12−	36	TXO7−	156	TXO2−	116	IRD	76
RXI12+	35	TXO7+	155	TXO2P+	115	COLN	75
V_{CC}	34	TXO7P−	154	RXI2−	114	V_{CC}	74
GND	33	V_{CC}	153	RXI2+	113	GND	73
RXI11−	32	GND	152	V_{CC}	112	PKEN	72
RXI11+	31	TXO6P−	151	GND	111	RXMPLL	71
TXO11P+	30	TXO6+	150	RX1−	110	$\overline{BUFEN}$	70
TXO11−	29	TXO6−	149	RX1+	109	$\overline{RDY}$	69
TXO11+	28	TXO6P+	148	CD1−	108	$\overline{ELI}$	68
TXO11P−	27	RXI6−	147	CD1+	107	$\overline{RTI}$	67
V_{CC}	26	RXI6+	146	TX1−	106	$\overline{STR1}$	66
GND	25	V_{CC}	145	TX1+	105	V_{CC}	65
TXO10P−	24	GND	144	V_{CC}	104	GND	64
TXO10+	23	RXI5−	143	GND	103	$\overline{STR0}$	63
TXO10−	22	RXI5+	142	V_{CC}	102	ACTND	62
TXO10P+	21	TXO5P+	141	GND	101	ANYXND	61
RXI10−	20	TXO5−	140	CLKIN	100	$\overline{ACKO}$	60
RXI10+	19	TXO5+	139	RA4	99	MRXC	59
V_{CC}	18	TXO5P−	138	RA3	98	MEN	58
GND	17	V_{CC}	137	RA2	97	MRXD	57
RXI9−	16	GND	136	RA1	96	MCRS	56
RXI9+	15	TXO4P−	135	RA0	95	V_{CC}	55
TXO9P+	14	TXO4+	134	V_{CC}	94	GND	54
TXO9−	13	TXO4−	133	GND	93	$\overline{ACKI}$	53
TXO9+	12	TXO4P+	132	$\overline{MLOAD}$	92	ACTNS	52
TXO9P−	11	RXI4−	131	$\overline{CDEC}$	91	ANYXNS	51
V_{CC}	10	RXI4+	130	$\overline{WR}$	90	$\overline{PCOMP}$	50
GND	9	V_{CC}	129	$\overline{RD}$	89	NC	49
TXO8P−	8	GND	128	D7	88	RXI13−	48
TXO8+	7	RXI3−	127	D6	87	RXI13+	47
TXO8−	6	RXI3+	126	D5	86	TXO13P+	46
TXO8P+	5	TXO3P+	125	D4	85	TXO13−	45
RXI8−	4	TXO3−	124	D3	84	TXO13+	44
RXI8+	3	TXO3+	123	D2	83	TXO13P−	43
V_{CC}	2	TXO3P−	122	D1	82	V_{CC}	42
GND	1	NC	121	D0	81	GND	41

Note: NC = No Connect

2.0 Connection Diagram—160 Pin PQFP Package (Continued)



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Ports 2–13 TP
Port 1 AUI

Order Number DP83950BVQB
See NS Package Number VUL160A

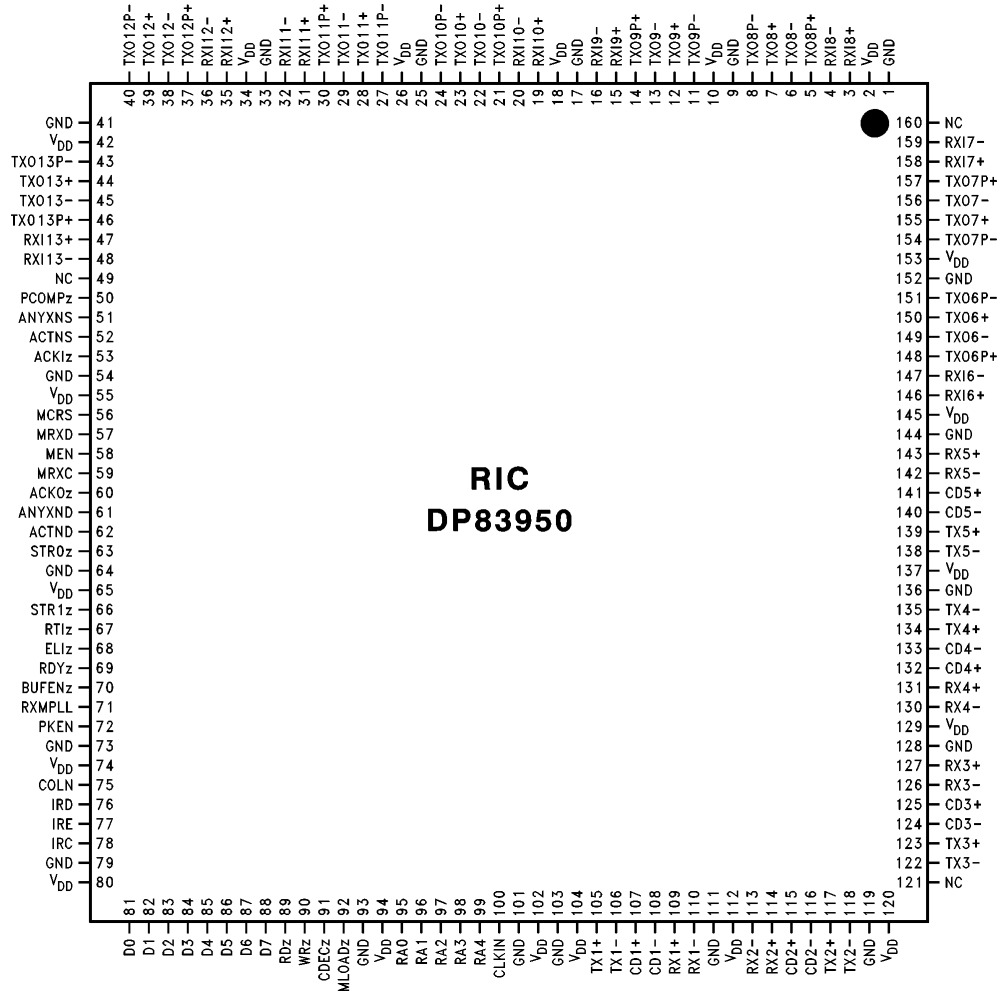
2.0 Connection Diagram—160 Pin PQFP Package (Continued)

Pin Table (1–5 AUI + 6–13 T.P. Ports)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TXO12P−	40	NC	160	V_{CC}	120	V_{CC}	80
TXO12+	39	RXI7−	159	GND	119	GND	79
TXO12−	38	RXI7+	158	TX2−	118	IRC	78
TXO12P+	37	TXO7P+	157	TX2+	117	IRE	77
RXI12−	36	TXO7−	156	CD2−	116	IRD	76
RXI12+	35	TXO7+	155	CD2+	115	COLN	75
V_{CC}	34	TXO7P−	154	RX2+	114	V_{CC}	74
GND	33	V_{CC}	153	RX2−	113	GND	73
RXI11−	32	GND	152	V_{CC}	112	PKEN	72
RXI11+	31	TXO6P−	151	GND	111	RXMPLL	71
TXO11P+	30	TXO6+	150	RX1−	110	$\overline{BUFEN}$	70
TXO11−	29	TXO6−	149	RX1+	109	$\overline{RDY}$	69
TXO11+	28	TXO6P+	148	CD1−	108	$\overline{ELI}$	68
TXO11P−	27	RXI6−	147	CD1+	107	$\overline{RTI}$	67
V_{CC}	26	RXI6+	146	TX1−	106	$\overline{STR1}$	66
GND	25	V_{CC}	145	TX1+	105	V_{CC}	65
TXO10P−	24	GND	144	V_{CC}	104	GND	64
TXO10+	23	RX5+	143	GND	103	$\overline{STR0}$	63
TXO10−	22	RX5−	142	V_{CC}	102	ACTND	62
TXO10P+	21	CD5+	141	GND	101	ANYXND	61
RXI10−	20	CD5−	140	CLKIN	100	$\overline{ACKO}$	60
RXI10+	19	TX5+	139	RA4	99	MRXC	59
V_{CC}	18	TX5−	138	RA3	98	MEN	58
GND	17	V_{CC}	137	RA2	97	MRXD	57
RXI9−	16	GND	136	RA1	96	MCRS	56
RXI9+	15	TX4−	135	RA0	95	V_{CC}	55
TXO9P+	14	TX4+	134	V_{CC}	94	GND	54
TXO9−	13	CD4−	133	GND	93	$\overline{ACKI}$	53
TXO9+	12	CD4+	132	$\overline{MLOAD}$	92	ACTNS	52
TXO9P−	11	RX4+	131	$\overline{CDEC}$	91	ANYXNS	51
V_{CC}	10	RX4−	130	$\overline{WR}$	90	$\overline{PCOMP}$	50
GND	9	V_{CC}	129	$\overline{RD}$	89	NC	49
TXO8P−	8	GND	128	D7	88	RXI13−	48
TXO8+	7	RX3+	127	D6	87	RXI13+	47
TXO8−	6	RX3−	126	D5	86	TXO13P+	46
TXO8P+	5	CD3+	125	D4	85	TXO13−	45
RXI8−	4	CD3−	124	D3	84	TXO13+	44
RXI8+	3	TX3+	123	D2	83	TXO13P−	43
V_{CC}	2	TX3−	122	D1	82	V_{CC}	42
GND	1	NC	121	D0	81	GND	41

Note: NC = No Connect

2.0 Connection Diagram—160 Pin PQFP Package (Continued)



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Ports 6–13 TP
Ports 1–5 AUI

Order Number DP83950BVQB
See NS Package Number VUL160A

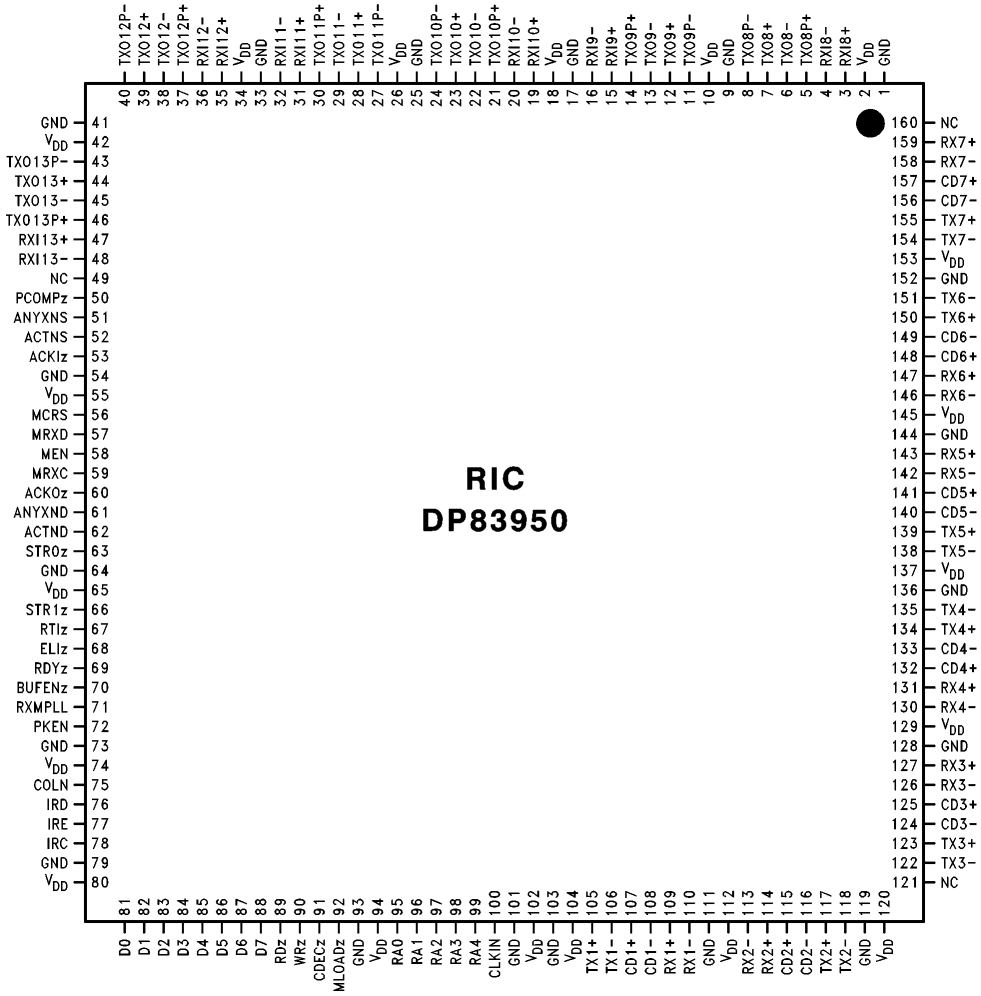
2.0 Connection Diagram—160 Pin PQFP Package (Continued)

Pin Table (1–7 AUI + 8–13 T.P. Ports)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TXO12P−	40	NC	160	V_{CC}	120	V_{CC}	80
TXO12+	39	RX7+	159	GND	119	GND	79
TXO12−	38	RX7−	158	TX2−	118	IRC	78
TXO12P+	37	CD7+	157	TX2+	117	IRE	77
RXI12−	36	CD7−	156	CD2−	116	IRD	76
RXI12+	35	TX7+	155	CD2+	115	COLN	75
V_{CC}	34	TX7−	154	RX2+	114	V_{CC}	74
GND	33	V_{CC}	153	RX2−	113	GND	73
RXI11−	32	GND	152	V_{CC}	112	PKEN	72
RXI11+	31	TX6−	151	GND	111	RXMPLL	71
TXO11P+	30	TX6+	150	RX1−	110	$\overline{BUFEN}$	70
TXO11−	29	CD6−	149	RX1+	109	$\overline{RDY}$	69
TXO11+	28	CD6+	148	CD1−	108	$\overline{ELI}$	68
TXO11P−	27	RX6+	147	CD1+	107	$\overline{RTI}$	67
V_{CC}	26	RX6−	146	TX1−	106	$\overline{STR1}$	66
GND	25	V_{CC}	145	TX1+	105	V_{CC}	65
TXO10P−	24	GND	144	V_{CC}	104	GND	64
TXO10+	23	RX5+	143	GND	103	$\overline{STR0}$	63
TXO10−	22	RX5−	142	V_{CC}	102	ACTND	62
TXO10P+	21	CD5+	141	GND	101	ANYXND	61
RXI10−	20	CD5−	140	CLKIN	100	$\overline{ACKO}$	60
RXI10+	19	TX5+	139	RA4	99	MRXC	59
V_{CC}	18	TX5−	138	RA3	98	MEN	58
GND	17	V_{CC}	137	RA2	97	MRXD	57
RXI9−	16	GND	136	RA1	96	MCRS	56
RXI9+	15	TX4−	135	RA0	95	V_{CC}	55
TXO9P+	14	TX4+	134	V_{CC}	94	GND	54
TXO9−	13	CD4−	133	GND	93	$\overline{ACKI}$	53
TXO9+	12	CD4+	132	$\overline{MLOAD}$	92	ACTNS	52
TXO9P−	11	RX4+	131	$\overline{CDEC}$	91	ANYXNS	51
V_{CC}	10	RX4−	130	$\overline{WR}$	90	$\overline{PCOMP}$	50
GND	9	V_{CC}	129	$\overline{RD}$	89	NC	49
TXO8P−	8	GND	128	D7	88	RXI13−	48
TXO8+	7	RX3+	127	D6	87	RXI13+	47
TXO8−	6	RX3−	126	D5	86	TXO13P+	46
TXO8P+	5	CD3+	125	D4	85	TXO13−	45
RXI8−	4	CD3−	124	D3	84	TXO13+	44
RXI8+	3	TX3+	123	D2	83	TXO13P−	43
V_{CC}	2	TX3−	122	D1	82	V_{CC}	42
GND	1	NC	121	D0	81	GND	41

Note: NC = No Connect

2.0 Connection Diagram—160 Pin PQFP Package (Continued)



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Ports 8–13 TP
Ports 1–7 AUI

Order Number DP83950BVQB
See NS Package Number VUL160A

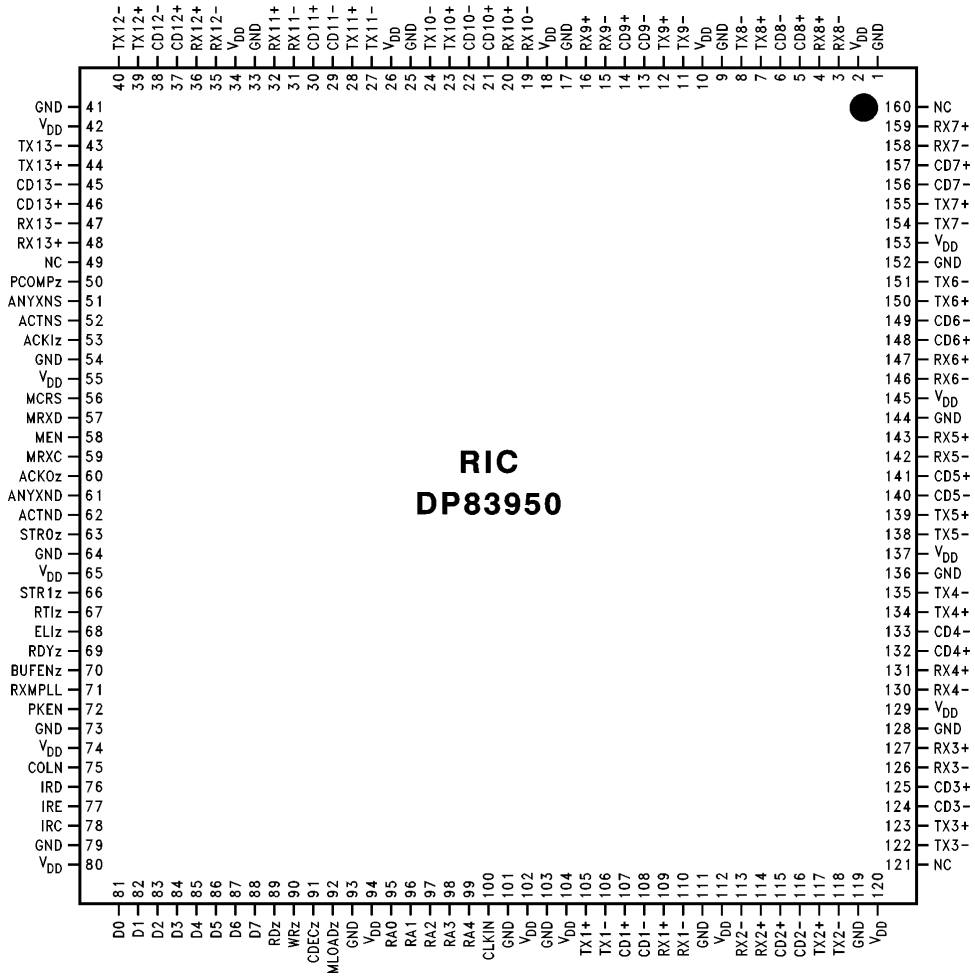
2.0 Connection Diagram—160 Pin PQFP Package (Continued)

Pin Table (All AUI Ports)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TX12−	40	NC	160	V_{CC}	120	V_{CC}	80
TX12+	39	RX7+	159	GND	119	GND	79
CD12−	38	RX7−	158	TX2−	118	IRC	78
CD12+	37	CD7+	157	TX2+	117	IRE	77
RX12+	36	CD7−	156	CD2−	116	IRD	76
RX12−	35	TX7+	155	CD2+	115	COLN	75
V_{CC}	34	TX7−	154	RX2+	114	V_{CC}	74
GND	33	V_{CC}	153	RX2−	113	GND	73
RX11+	32	GND	152	V_{CC}	112	PKEN	72
RX11−	31	TX6−	151	GND	111	RXMPLL	71
CD11+	30	TX6+	150	RX1−	110	$\overline{BUFEN}$	70
CD11−	29	CD6−	149	RX1+	109	$\overline{RDY}$	69
TX11+	28	CD6+	148	CD1−	108	$\overline{ELI}$	68
TX11−	27	RX6+	147	CD1+	107	$\overline{RTI}$	67
V_{CC}	26	RX6−	146	TX1−	106	$\overline{STR1}$	66
GND	25	V_{CC}	145	TX1+	105	V_{CC}	65
TX10−	24	GND	144	V_{CC}	104	GND	64
TX10+	23	RX5+	143	GND	103	$\overline{STR0}$	63
CD10−	22	RX5−	142	V_{CC}	102	ACTND	62
CD10+	21	CD5+	141	GND	101	ANYXND	61
RX10+	20	CD5−	140	CLKIN	100	$\overline{ACKO}$	60
RX10−	19	TX5+	139	RA4	99	MRXC	59
V_{CC}	18	TX5−	138	RA3	98	MEN	58
GND	17	V_{CC}	137	RA2	97	MRXD	57
RX9+	16	GND	136	RA1	96	MCRS	56
RX9−	15	TX4−	135	RA0	95	V_{CC}	55
CD9+	14	TX4+	134	V_{CC}	94	GND	54
CD9−	13	CD4−	133	GND	93	$\overline{ACKI}$	53
TX9+	12	CD4+	132	$\overline{MLOAD}$	92	ACTNS	52
TX9−	11	RX4+	131	$\overline{CDEC}$	91	ANYXNS	51
V_{CC}	10	RX4−	130	$\overline{WR}$	90	$\overline{PCOMP}$	50
GND	9	V_{CC}	129	$\overline{RD}$	89	NC	49
TX8−	8	GND	128	D7	88	RX13+	48
TX8+	7	RX3+	127	D6	87	RX13−	47
CD8−	6	RX3−	126	D5	86	CD13+	46
CD8+	5	CD3+	125	D4	85	CD13−	45
RX8+	4	CD3−	124	D3	84	TX13+	44
RX8−	3	TX3+	123	D2	83	TX13−	43
V_{CC}	2	TX3−	122	D1	82	V_{CC}	42
GND	1	NC	121	D0	81	GND	41

Note: NC = No Connect

2.0 Connection Diagram—160 Pin PQFP Package (Continued)



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All AUI Ports

Order Number DP83950BVQB
See NS Package Number VUL160A

2.0 Connection Diagram—160 Pin PGA Package (Continued)

Pin Table (12 T.P. Ports + 1 AUI Bottom View)

Pin Name	Pin No.
TXO12P−	A15
TXO12+	A14
TXO12−	B14
TXO12P+	C13
RXI12−	B13
RXI12+	A13
V_{CC}	C12
GND	C11
RXI11−	B12
RXI11+	B11
TXO11P+	A12
TXO11−	A11
TXO11+	C10
TXO11P−	A10
V_{CC}	B10
GND	B9
TXO10P−	C9
TXO10+	C8
TXO10−	A9
TXO10P+	A8
RXI10−	B8
RXI10+	B7
V_{CC}	C7
GND	A7
RXI9−	A6
RXI9+	B6
TXO9P+	C6
TXO9−	C5
TXO9+	B5
TXO9P−	A5
V_{CC}	A4
GND	B4
TXO8P−	C4
TXO8+	A3
TXO8−	C3
TXO8P+	D4
RXI8−	B3
RXI8+	B2
V_{CC}	A2
GND	D3

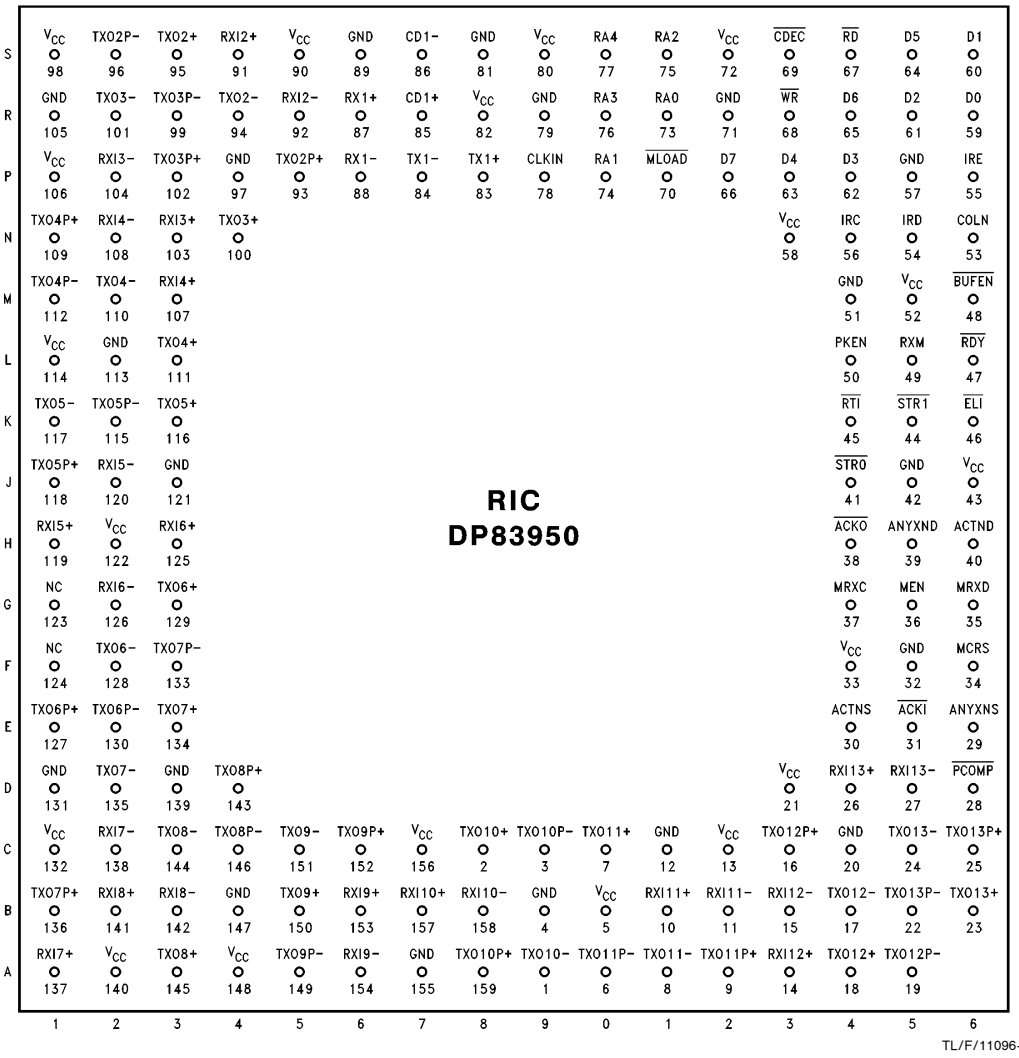
Pin Name	Pin No.
RXI7−	C2
RXI7+	A1
TXO7P+	B1
TXO7−	D2
TXO7+	E3
TXO7P−	F3
V_{CC}	C1
GND	D1
TXO6P−	E2
TXO6+	G3
TXO6−	F2
TXO6P+	E1
RXI6−	G2
RXI6+	H3
NC	F1
NC	G1
V_{CC}	H2
GND	J3
RXI5−	J2
RXI5+	H1
TXO5P+	J1
TXO5−	K1
TXO5+	K3
TXO5P−	K2
V_{CC}	L1
GND	L2
TXO4P−	M1
TXO4+	L3
TXO4−	M2
TXO4P+	N1
RXI4−	N2
RXI4+	M3
V_{CC}	P1
GND	R1
RXI3−	P2
RXI3+	N3
TXO3P+	P3
TXO3−	R2
TXO3+	N4
TXO3P−	R3

Pin Name	Pin No.
V_{CC}	S1
GND	P4
TXO2P−	S2
TXO2+	S3
TXO2−	R4
TXO2P+	P5
RXI2−	R5
RXI2+	S4
V_{CC}	S5
GND	S6
RX1−	P6
RX1+	R6
CD1−	S7
CD1+	R7
TX1−	P7
TX1+	P8
V_{CC}	R8
GND	S8
V_{CC}	S9
GND	R9
CLKIN	P9
RA4	S10
RA3	R10
RA2	S11
RA1	P10
RA0	R11
V_{CC}	S12
GND	R12
$\overline{MLOAD}$	P11
$\overline{CDEC}$	S13
$\overline{WR}$	R13
$\overline{RD}$	S14
D7	P12
D6	R14
D5	S15
D4	P13
D3	P14
D2	R15
D1	S16
D0	R16

Pin Name	Pin No.
V_{CC}	N13
GND	P15
IRC	N14
IRE	P16
IRD	N15
COLN	N16
V_{CC}	M15
GND	M14
PKEN	L14
RXM	L15
$\overline{BUFEN}$	M16
$\overline{RDY}$	L16
$\overline{ELI}$	K16
$\overline{RTI}$	K14
$\overline{STR1}$	K15
V_{CC}	J16
GND	J15
$\overline{STR0}$	J14
ACTND	H16
ANYXND	H15
$\overline{ACKO}$	H14
MRXC	G14
MEN	G15
MRXD	G16
MCRS	F16
V_{CC}	F14
GND	F15
$\overline{ACKI}$	E15
ACTNS	E14
ANYXNS	E16
$\overline{PCOMP}$	D16
RXI13−	D15
RXI13+	D14
TXO13P+	C16
TXO13−	C15
TXO13+	B16
TXO13P−	B15
V_{CC}	D13
GND	C14

Note: NC = No Connect

2.0 Connection Diagram—160 Pin PGA Package (Continued)



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Bottom View
1 AUI + 2–13 T.P. Ports

Order Number DP83950BNU
See NS Package Number UP159A

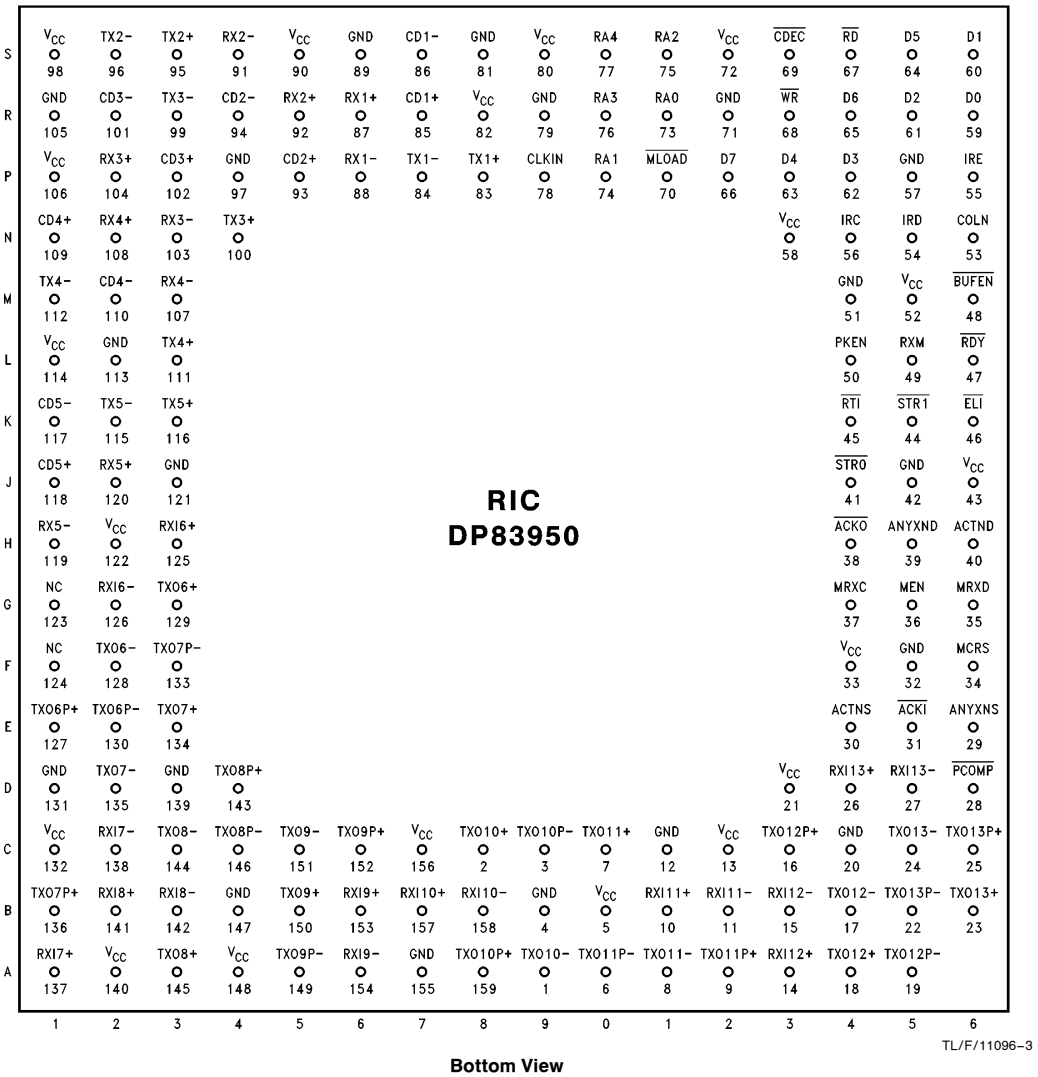
2.0 Connection Diagram—160 Pin PGA Package (Continued)

Pin Table (1–5 AUI + 6–13 T.P. Ports)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TXO12P−	A15	RXI7−	C2	V_{CC}	S1	V_{CC}	N13
TXO12+	A14	RXI7+	A1	GND	P4	GND	P15
TXO12−	B14	TXO7P+	B1	TX2−	S2	IRC	N14
TXO12P+	C13	TXO7−	D2	TX2+	S3	IRE	P16
RXI12−	B13	TXO7+	E3	CD2−	R4	IRD	N15
RXI12+	A13	TXO7P−	F3	CD2+	P5	COLN	N16
V_{CC}	C12	V_{CC}	C1	RX2+	R5	V_{CC}	M15
GND	C11	GND	D1	RX2−	S4	GND	M14
RXI11−	B12	TXO6P−	E2	V_{CC}	S5	PKEN	L14
RXI11+	B11	TXO6+	G3	GND	S6	RXM	L15
TXO11P+	A12	TXO6−	F2	RX1−	P6	$\overline{BUFEN}$	M16
TXO11−	A11	TXO6P+	E1	RX1+	R6	$\overline{RDY}$	L16
TXO11+	C10	RXI6−	G2	CD1−	S7	$\overline{ELI}$	K16
TXO11P−	A10	RXI6+	H3	CD1+	R7	$\overline{RTI}$	K14
V_{CC}	B10	NC	F1	TX1−	P7	$\overline{STR1}$	K15
GND	B9	NC	G1	TX1+	P8	V_{CC}	J16
TXO10P−	C9	V_{CC}	H2	V_{CC}	R8	GND	J15
TXO10+	C8	GND	J3	GND	S8	$\overline{STR0}$	J14
TXO10−	A9	RX5+	J2	V_{CC}	S9	ACTND	H16
TXO10P+	A8	RX5−	H1	GND	R9	ANYXND	H15
RXI10−	B8	CD5+	J1	CLKIN	P9	$\overline{ACKO}$	H14
RXI10+	B7	CD5−	K1	RA4	S10	MRXC	G14
V_{CC}	C7	TX5+	K3	RA3	R10	MEN	G15
GND	A7	TX5−	K2	RA2	S11	MRXD	G16
RXI9−	A6	V_{CC}	L1	RA1	P10	MCRS	F16
RXI9+	B6	GND	L2	RA0	R11	V_{CC}	F14
TXO9P+	C6	TX4−	M1	V_{CC}	S12	GND	F15
TXO9−	C5	TX4+	L3	GND	R12	$\overline{ACKI}$	E15
TXO9+	B5	CD4−	M2	$\overline{MLOAD}$	P11	ACTNS	E14
TXO9P−	A5	CD4+	N1	$\overline{CDEC}$	S13	ANYXNS	E16
V_{CC}	A4	RX4+	N2	$\overline{WR}$	R13	$\overline{PCOMP}$	D16
GND	B4	RX4−	M3	$\overline{RD}$	S14	RXI13−	D15
TXO8P−	C4	V_{CC}	P1	D7	P12	RXI13+	D14
TXO8+	A3	GND	R1	D6	R14	TXO13P+	C16
TXO8−	C3	RX3+	P2	D5	S15	TXO13−	C15
TXO8P+	D4	RX3−	N3	D4	P13	TXO13+	B16
RXI8−	B3	CD3+	P3	D3	P14	TXO13P−	B15
RXI8+	B2	CD3−	R2	D2	R15	V_{CC}	D13
V_{CC}	A2	TX3+	N4	D1	R16	GND	C14
GND	D3	TX3−	R3	D0	R16		

Note: NC = No Connect

2.0 Connection Diagram—160 Pin PGA Package (Continued)



TL/F/11096–3

Bottom View
1–5 AUI + 6–13 T.P. Ports

Order Number DP83950BNU
See NS Package Number UP159A

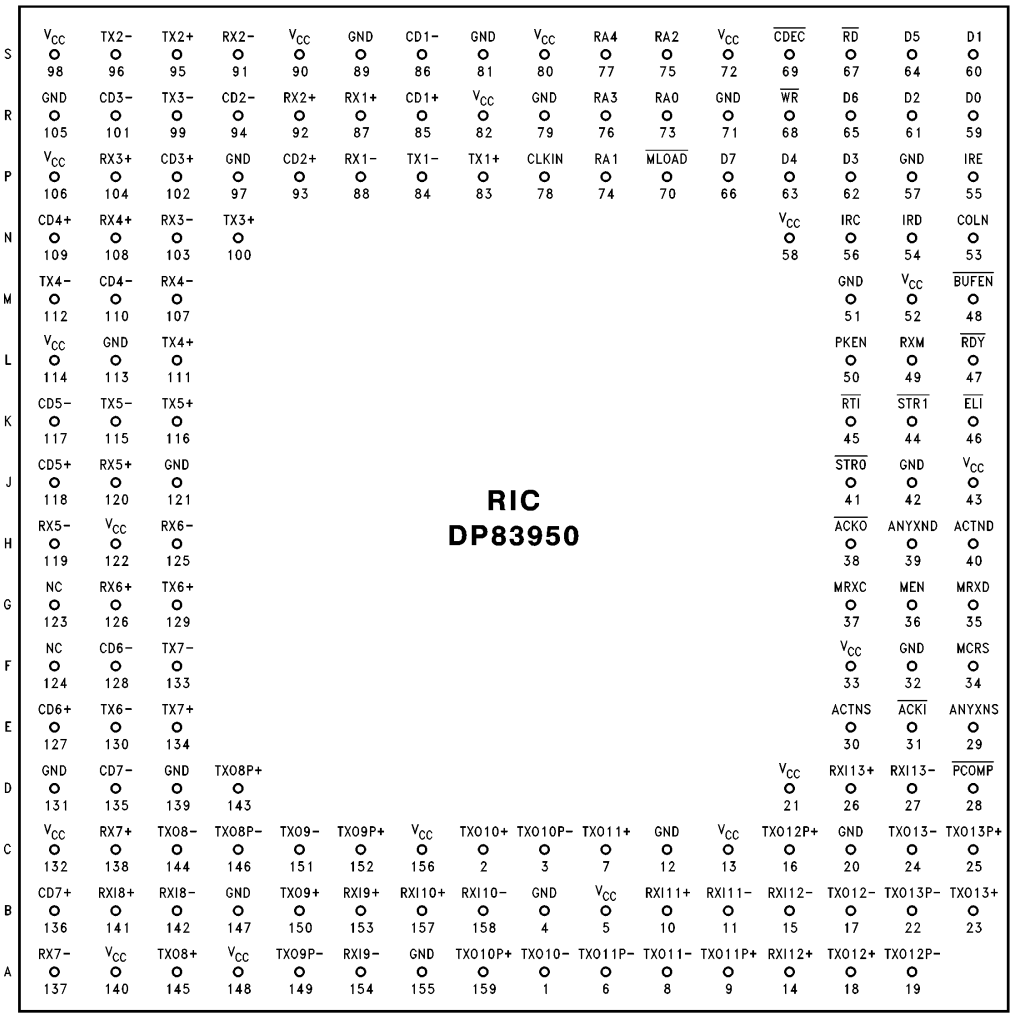
2.0 Connection Diagram—160 Pin PGA Package (Continued)

Pin Table (1–7 AUI + 8–13 T.P. Ports)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TXO12P−	A15	RX7+	C2	V_{CC}	S1	V_{CC}	N13
TXO12+	A14	RX7−	A1	GND	P4	GND	P15
TXO12−	B14	CD7+	B1	TX2−	S2	IRC	N14
TXO12P+	C13	CD7−	D2	TX2+	S3	IRE	P16
RXI12−	B13	TX7+	E3	CD2−	R4	IRD	N15
RXI12+	A13	TX7−	F3	CD2+	P5	COLN	N16
V_{CC}	C12	V_{CC}	C1	RX2+	R5	V_{CC}	M15
GND	C11	GND	D1	RX2−	S4	GND	M14
RXI11−	B12	TX6−	E2	V_{CC}	S5	PKEN	L14
RXI11+	B11	TX6+	G3	GND	S6	RXM	L15
TXO11P+	A12	CD6−	F2	RX1−	P6	$\overline{BUFEN}$	M16
TXO11−	A11	CD6+	E1	RX1+	R6	$\overline{RDY}$	L16
TXO11+	C10	RX6+	G2	CD1−	S7	$\overline{ELI}$	K16
TXO11P−	A10	RX6−	H3	CD1+	R7	$\overline{RTI}$	K14
V_{CC}	B10	NC	F1	TX1−	P7	$\overline{STR1}$	K15
GND	B9	NC	G1	TX1+	P8	V_{CC}	J16
TXO10P−	C9	V_{CC}	H2	V_{CC}	R8	GND	J15
TXO10+	C8	GND	J3	GND	S8	$\overline{STR0}$	J14
TXO10−	A9	RX5+	J2	V_{CC}	S9	ACTND	H16
TXO10P+	A8	RX5−	H1	GND	R9	ANYXND	H15
RXI10−	B8	CD5+	J1	CLKIN	P9	$\overline{ACKO}$	H14
RXI10+	B7	CD5−	K1	RA4	S10	MRXC	G14
V_{CC}	C7	TX5+	K3	RA3	R10	MEN	G15
GND	A7	TX5−	K2	RA2	S11	MRXD	G16
RXI9−	A6	V_{CC}	L1	RA1	P10	MCRS	F16
RXI9+	B6	GND	L2	RA0	R11	V_{CC}	F14
TXO9P+	C6	TX4−	M1	V_{CC}	S12	GND	F15
TXO9−	C5	TX4+	L3	GND	R12	$\overline{ACKI}$	E15
TXO9+	B5	CD4−	M2	$\overline{MLOAD}$	P11	ACTNS	E14
TXO9P−	A5	CD4+	N1	$\overline{CDEC}$	S13	ANYXNS	E16
V_{CC}	A4	RX4+	N2	$\overline{WR}$	R13	$\overline{PCOMP}$	D16
GND	B4	RX4−	M3	$\overline{RD}$	S14	RXI13−	D15
TXO8P−	C4	V_{CC}	P1	D7	P12	RXI13+	D14
TXO8+	A3	GND	R1	D6	R14	TXO13P+	C16
TXO8−	C3	RX3+	P2	D5	S15	TXO13−	C15
TXO8P+	D4	RX3−	N3	D4	P13	TXO13+	B16
RXI8−	B3	CD3+	P3	D3	P14	TXO13P−	B15
RXI8+	B2	CD3−	R2	D2	R15	V_{CC}	D13
V_{CC}	A2	TX3+	N4	D1	S16	GND	C14
GND	D3	TX3−	R3	D0	R16		

Note: NC = No Connect

2.0 Connection Diagram—160 Pin PGA Package (Continued)



TL/F/11096–4

Bottom View
1–7 AUI + 8–13 T.P. Ports

Order Number DP83950BNU
See NS Package Number UP159A

2.0 Connection Diagram—160 Pin PGA Package (Continued)

Pin Table (All AUI Ports)

Pin Name	Pin No.
TX12−	A15
TX12+	A14
CD12−	B14
CD12+	C13
RX12+	B13
RX12−	A13
V_{CC}	C12
GND	C11
RX11+	B12
RX11−	B11
CD11+	A12
CD11−	A11
TX11+	C10
TX11−	A10
V_{CC}	B10
GND	B9
TX10−	C9
TX10+	C8
CD10−	A9
CD10+	A8
RX10+	B8
RX10−	B7
V_{CC}	C7
GND	A7
RX9+	A6
RX9−	B6
CD9+	C6
CD9−	C5
TX9+	B5
TX9−	A5
V_{CC}	A4
GND	B4
TX8−	C4
TX8+	A3
CD8−	C3
CD8+	D4
RX8+	B3
RX8−	B2
V_{CC}	A2
GND	D3

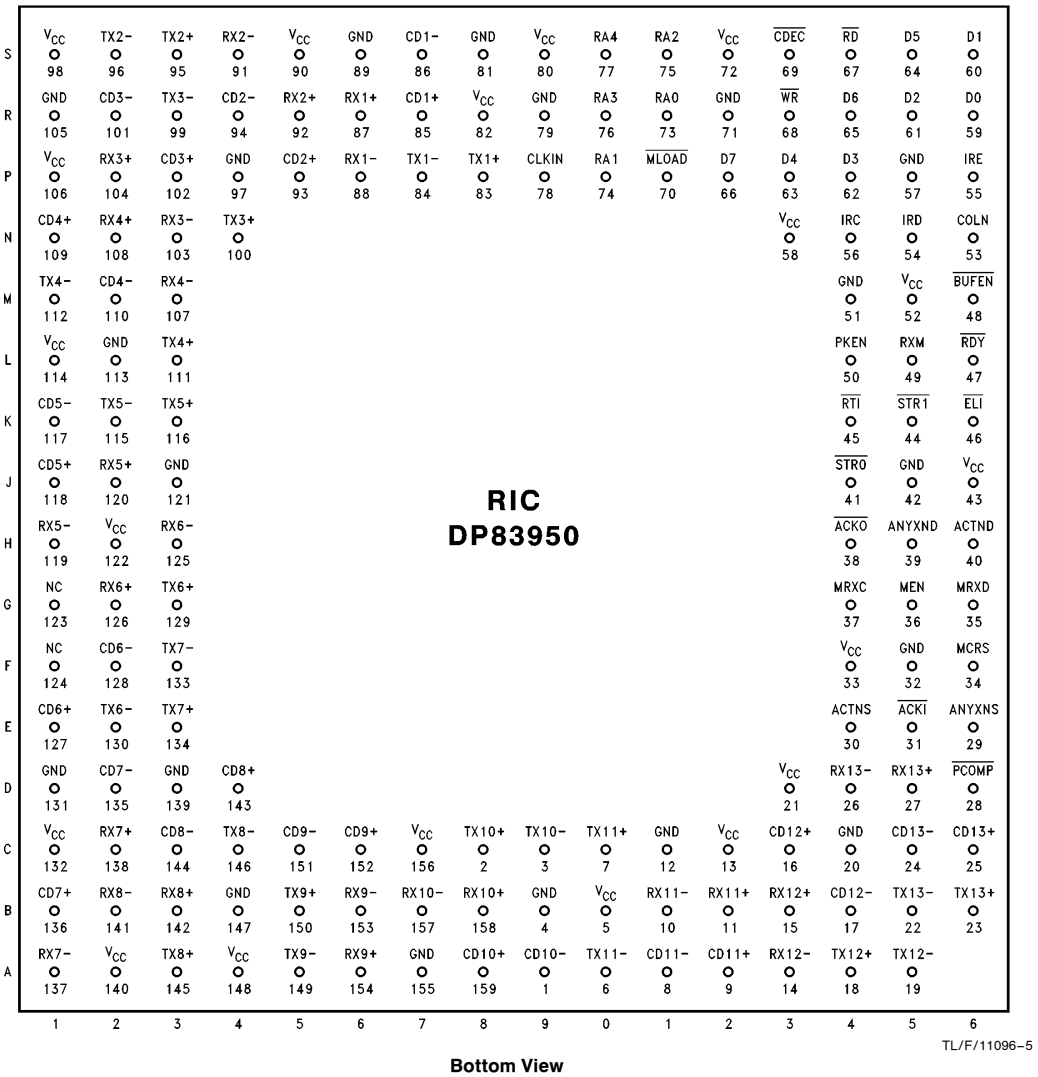
Pin Name	Pin No.
RX7+	C2
RX7−	A1
CD7+	B1
CD7−	D2
TX7+	E3
TX7−	F3
V_{CC}	C1
GND	D1
TX6−	E2
TX6+	G3
CD6−	F2
CD6+	E1
RX6+	G2
RX6−	H3
NC	F1
NC	G1
V_{CC}	H2
GND	J3
RX5+	J2
RX5−	H1
CD5+	J1
CD5−	K1
TX5+	K3
TX5−	K2
V_{CC}	L1
GND	L2
TX4−	M1
TX4+	L3
CD4−	M2
CD4+	N1
RX4+	N2
RX4−	M3
V_{CC}	P1
GND	R1
RX3+	P2
RX3−	N3
CD3+	P3
CD3−	R2
TX3+	N4
TX3−	R3

Pin Name	Pin No.
V_{CC}	S1
GND	P4
TX2−	S2
TX2+	S3
CD2−	R4
CD2+	P5
RX2+	R5
RX2−	S4
V_{CC}	S5
GND	S6
RX1−	P6
RX1+	R6
CD1−	S7
CD1+	R7
TX1−	P7
TX1+	P8
V_{CC}	R8
GND	S8
V_{CC}	S9
GND	R9
CLKIN	P9
RA4	S10
RA3	R10
RA2	S11
RA1	P10
RA0	R11
V_{CC}	S12
GND	R12
$\overline{MLOAD}$	P11
$\overline{CDEC}$	S13
$\overline{WR}$	R13
$\overline{RD}$	S14
D7	P12
D6	R14
D5	S15
D4	P13
D3	P14
D2	R15
D1	S16
D0	R16

Pin Name	Pin No.
V_{CC}	N13
GND	P15
IRC	N14
IRE	P16
IRD	N15
COLN	N16
V_{CC}	M15
GND	M14
PKEN	L14
RXM	L15
$\overline{BUFEN}$	M16
$\overline{RDY}$	L16
$\overline{ELI}$	K16
$\overline{RTI}$	K14
$\overline{STR1}$	K15
V_{CC}	J16
GND	J15
$\overline{STR0}$	J14
ACTND	H16
ANYXND	H15
$\overline{ACKO}$	H14
MRXC	G14
MEN	G15
MRXD	G16
MCRS	F16
V_{CC}	F14
GND	F15
$\overline{ACKI}$	E15
ACTNS	E14
ANYXNS	E16
$\overline{PCOMP}$	D16
RX13+	D15
RX13−	D14
CD13+	C16
CD13−	C15
TX13+	B16
TX13−	B15
V_{CC}	D13
GND	C14

Note: NC = No Connect

2.0 Connection Diagram—160 Pin PGA Package (Continued)



TL/F/11096–5

Bottom View
All AUI Ports

Order Number DP83950BNU
See NS Package Number UP159A

3.0 Pin Descriptions

Pin No.	Pin Name	Driver Type	I/O	Description
NETWORK INTERFACE PINS (On-Chip Transceiver Mode)				
	RXI2− to RXI13−	TP	I	Twisted Pair **R**eceive **I**nput Negative
	RXI2+ to RXI13+	TP	I	Twisted Pair **R**eceive **I**nput Positive
	TXOP2− to TXOP13−	TT	O	Twisted Pair **P**re-emphasis **T**ransmit **O**utput Negative
	TXO2− to TXO13−	TT	O	Twisted Pair **T**ransmit **O**utput Negative
	TXO2+ to TXO13+	TT	O	Twisted Pair **T**ransmit **O**utput Positive
	TXOP2+ to TXOP13+	TT	O	Twisted Pair **P**re-emphasis **T**ransmit **O**utput Positive
	CD1+	AL	I	AUI **C**ollision **D**etect Input Positive
	CD1−	AL	I	AUI **C**ollision **D**etect Input Negative
	RX1+	AL	I	AUI **R**eceive Input Positive
	RX1−	AL	I	AUI **R**eceive Input Negative
	TX1+	AD	O	AUI **T**ransmit Output Positive
	TX1−	AD	O	AUI **T**ransmit Output Negative
NETWORK INTERFACE PINS (External Transceiver Mode **AUI Signal Level Compatibility Selected)**				
	TX2+ to TX13+	AL	O	**T**ransmit Output Positive
	TX2− to TX13−	AL	O	**T**ransmit Output Negative
	CD2+ to CD13+	AL	I	**C**ollision Input Positive
	CD2− to CD13−	AL	I	**C**ollision Input Negative
	RX2+ to RX13+	AL	I	**R**eceive Input Positive
	RX2− to RX13−	AL	I	**R**eceive Input Negative
	CD1+	AL	I	AUI **C**ollision **D**etect Input Positive
	CD1−	AL	I	AUI **C**ollision **D**etect Input Negative
	RX1+	AL	I	AUI **R**eceive Input Positive
	RX1−	AL	I	AUI **R**eceive Input Negative
	TX1+	AD	O	AUI **T**ransmit Output Positive
	TX1−	AD	O	AUI **T**ransmit Output Negative

Note: AD = **A**UI level and **D**rive compatible, **TP** = **T**wisted **P**air interface compatible, **AL** = **A**UI **L**evel compatible, **TT** = **TT**L compatible, **I** = **I**nput, **O** = **O**utput.

3.0 Pin Descriptions (Continued)

Pin No.	Pin Name	Driver Type	I/O	Description
PROCESSOR BUS PINS				
	RA0–RA4	TT	I	**R**EGISTER **A**DDRESS INPUTS: These five pins are used to select a register to be read or written. The state of these inputs are ignored when the read, write and mode load input strobes are high. (Even under these conditions these inputs must not be allowed to float at an undefined logic state).
	$\overline{\text{STR0}}$	C	O	DISPLAY UPDATE **STR**OBE 0 **Maximum Display Mode:** This signal controls the latching of display data for network ports 1 to 7 into the off chip display latches. **Minimum Display Mode:** This signal controls the latching of display data for the RIC into the off chip display latch. During processor access cycles (read or write is asserted) this signal is inactive (high).
	$\overline{\text{STR1}}$	C	O	DISPLAY UPDATE **STR**OBE 1 **Maximum Display Mode:** This signal controls the latching of display data for network ports 8 to 13 into the off chip display latches. **Minimum Display Mode:** No operation During processor access cycles (read or write is asserted) this signal is inactive (high).
	D0–D7	TT	B, Z	**D**ATA BUS **Display Update Cycles:** These pins become outputs providing display data and port address information. Address information only available in Maximum Display mode. **Processor Access Cycles:** Data input or output is performed via these pins. The read, write and mode load inputs control the direction of the signals. **Note:** The data pins remain in their display update function, i.e., asserted as outputs unless either the read or write strobe is asserted.
	$\overline{\text{BUFEN}}$	C	O	**BUF**FER **EN**ABLE: This output controls the TRI-STATE® operation of the bus transceiver which provides the interface between the RIC's data pins and the processor's data bus. **Note:** The buffer enable output indicates the function of the data pins. When it is high they are performing display update cycles, when it is low a processor access or mode load cycle is occurring.
	$\overline{\text{RDY}}$	C	O	DATA **R**EA**DY** STROBE: The falling edge of this signal during a read cycle indicates that data is stable and valid for sampling. In write cycles the falling edge of $\overline{\text{RDY}}$ denotes that the write data has been latched by the RIC. Therefore data must have been available and stable for this operation to be successful.
	$\overline{\text{ELI}}$	C	O	**E**VENT **L**OGGING **I**NTERRUPT: A low level on the $\overline{\text{ELI}}$ output indicates the RIC's hub management logic requires CPU attention. The interrupt is cleared by accessing the Port Event Recording register or Event Counter that produced it. All interrupt sources may be masked.
	$\overline{\text{RTI}}$	C	O	**R**EAL **T**IME **I**NTERRUPT: A low level on the $\overline{\text{RTI}}$ output indicates the RIC's real time (packet specific) interrupt logic requires CPU attention. The interrupt is cleared by reading the Real Time Interrupt Status register. All interrupt sources may be masked.
	$\overline{\text{CDEC}}$	TT	I	**C**OUNTER **DEC**REMENT: A low level on the $\overline{\text{CDEC}}$ input strobe decrements all of the RIC's Port Event Counters by one. This input is internally synchronized and if necessary the operation of the signal is delayed if there is a simultaneous internally generated counting operation.
	$\overline{\text{WR}}$	TT	I	**WR**ITE STROBE: Strobe from the CPU used to write an internal register defined by the RA0–RA4 inputs.
	$\overline{\text{RD}}$	TT	I	**R**EA**D** STROBE: Strobe from the CPU used to read an internal register defined by the RA0–RA4 inputs.
	$\overline{\text{MLOAD}}$	TT	I	DEVICE RESET AND **M**ODE **LOAD**: When this input is low all of the RIC's state machines, counters and network ports are reset and held inactive. On the rising edge of $\overline{\text{MLOAD}}$ the logic levels present on the D0–7 pins and RA0–RA4 inputs are latched into the RIC's configuration registers. The rising edge of $\overline{\text{MLOAD}}$ also signals the beginning of the display test operation.

3.0 Pin Descriptions (Continued)

Pin No.	Pin Name	Driver Type	I/O	Description
INTER-RIC BUS PINS				
	$\overline{\text{ACKI}}$	TT	I	**ACK**NOWLEDGE **I**NPUT: Input to the network ports' arbitration chain.
	$\overline{\text{ACKO}}$	TT	O	**ACK**NOWLEDGE **O**UTPUT: Output from the network ports' arbitration chain.
	IRD	TT	B, Z	**I**NTER-**R**IC **D**ATA: When asserted as an output this signal provides a serial data stream in NRZ format. The signal is asserted by a RIC when it is receiving data from one of its network segments. The default condition of this signal is to be an input. In this state it may be driven by other devices on the Inter-RIC bus.
	IRE	TT	B, Z	**I**NTER-**R**IC **E**NABLE: When asserted as an output this signal provides an activity framing enable for the serial data stream. The signal is asserted by a RIC when it is receiving data from one of its network segments. The default condition of this signal is to be an input. In this state it may be driven by other devices on the Inter-RIC bus.
	IRC	TT	B, Z	**I**NTER-**R**IC **C**LOCK: When asserted as an output this signal provides a clock signal for the serial data stream. Data (IRD) is changed on the falling edge of the clock. The signal is asserted by a RIC when it is receiving data from one of its network segments. The default condition of this signal is to be an input. When an input IRD is sampled on the rising edge of the clock. In this state it may be driven by other devices on the Inter-RIC bus.
	COLN	TT	B, Z	**COL**LISION ON PORT **N**: This denotes that a collision is occurring on the port receiving the data packet. The default condition of this signal is to be an input. In this state it may be driven by other devices on the Inter-RIC bus.
	PKEN	C	O	**P**AC**K**ET **EN**ABLE: This output acts as an active high enable for an external bus transceiver (if required) for the IRE, IRC IRD and COLN signals. When high the bus transceiver should be transmitting on to the bus, i.e., this RIC is driving the IRD, IRE, IRC and COLN bus lines. When low the bus transceiver should receive from the bus.
	CLKIN	TT	I	40 MHz **CL**OC**K IN**PUT: This input is used to generate the RIC's timing reference for the state machines, and phase lock loop decoder.
	ACTND	OD	O	**ACT**IVITY ON PORT **N D**RIVE: This output is active when the RIC is receiving data or collision information from one of its network segments.
	ACTNS	TT	I	**ACT**IVITY ON PORT **N S**ENSE: This input senses when this or another RIC in a multi-RIC system is receiving data or collision information.
	ANYXND	OD	O	**A**CTIVITY ON A**NY** PORT E**X**CLUDING PORT **N D**RIVE: This output is active when a RIC is experiencing a transmit collision or multiple ports have active collisions on their network segments.
	ANYXNS	TT	I	**A**CTIVITY ON A**NY** PORT E**X**CLUDING PORT **N S**ENSE: This input senses when this RIC or other RICs in a multi-RIC system are experiencing transmit collisions or multiple ports have active collisions on their network segments.

3.0 Pin Descriptions (Continued)

Pin No.	Pin Name	Driver Type	I/O	Description
MANAGEMENT BUS PINS				
	MRXC	TT	O, Z	**M**ANAGEMENT **R**ECEIVE **C**LOCK: When asserted this signal provides a clock signal for the MRXD serial data stream. The MRXD signal is changed on the falling edge of this clock. The signal is asserted when a RIC is receiving data from one of its network segements. Otherwise the signal is inactive.
	MCRS	TT	B, Z	**M**ANAGEMENT **C**ARRIE**R** **S**ENSE: When asserted this signal provides an activity framing enable for the serial output data stream (MRXD). The signal is asserted when a RIC is receiving data from one of its network segments. Otherwise the signal is an input.
	MRXD	TT	O, Z	**M**ANAGEMENT **R**ECEIVE **D**ATA: When asserted this signal provides a serial data stream in NRZ format. The data stream is made up of the data packet and RIC status information. The signal is asserted when a RIC is receiving data from one of its network segments. Otherwise the signal is inactive.
	MEN	C	O	**M**ANAGEMENT BUS OUTPUT **EN**ABLE: This output acts as an active high enable for an external bus transceiver (if required) for the MRXC, MCRS and MRXD signals. When high the bus transceiver should be transmitting on to the bus.
	$\overline{\text{PCOMP}}$	TT	I	**P**ACKET **COMP**RESS: This input is used to activate the RIC's packet compress logic. A low level on this signal when MCRS is active will cause that packet to be compressed. If $\overline{\text{PCOMP}}$ is tied low all packets are compressed, if $\overline{\text{PCOMP}}$ is tied high packet compression is inhibited.
POWER AND GROUND PINS				
	V_{CC}			Positive Supply
	GND			Negative Supply
EXTERNAL DECODER PINS				
	RXM	TT	O	**R**ECEIVE DATA MANCHESTER FORMAT: This output makes the data, in Manchester format, received by port N available for test purposes. If not used for testing this pin should be left open.

Note: TT = **TT**L compatible, **B** = **B**i-directional, **C** = **C**MOS compatible, **OD** = **O**pen **D**rain, **I** = **I**nput, **O** = **O**utput, Z = TRI-STATE

4.0 Block Diagram

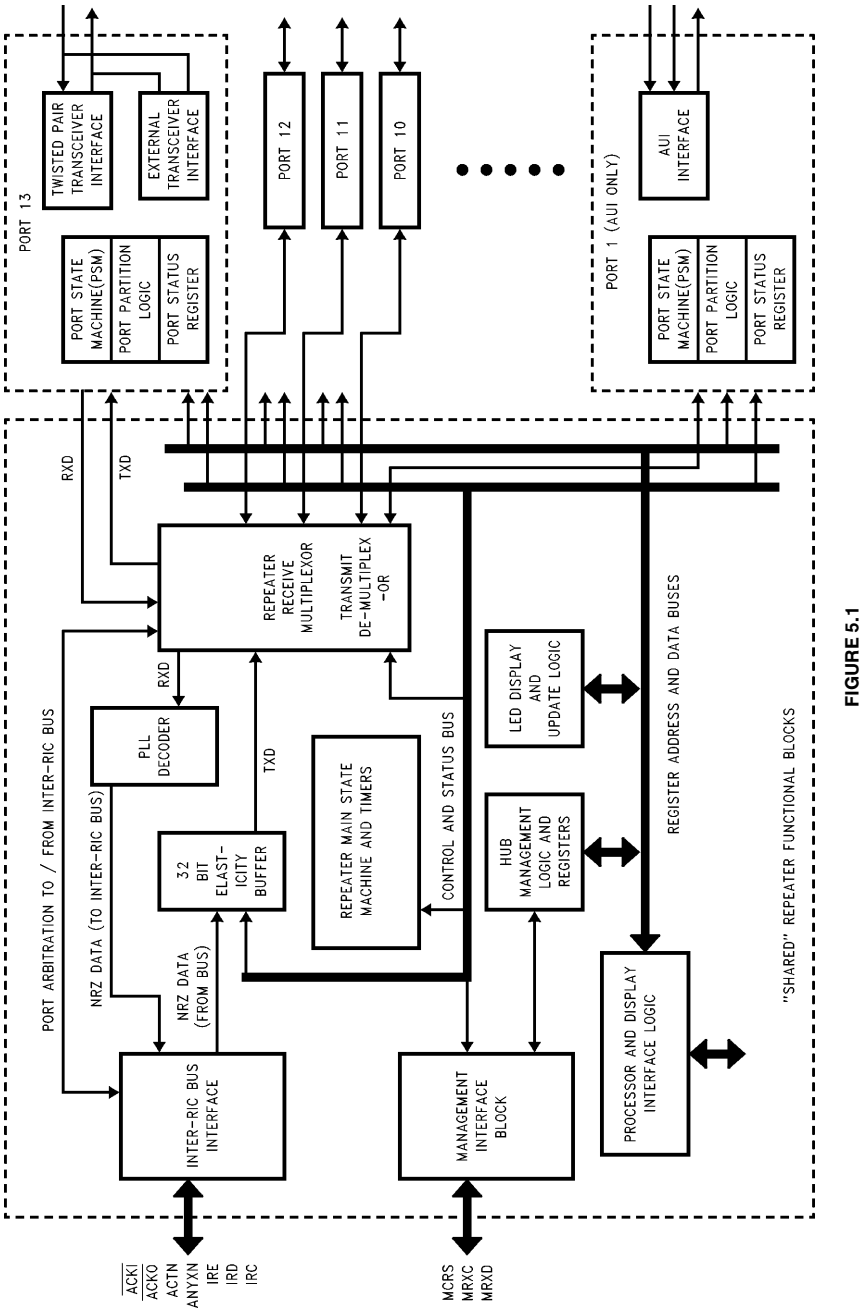


FIGURE 5.1

5.0 Functional Description

The I.E.E.E. repeater specification details a number of functions a repeater system must perform. These requirements allied with a need for the implementation to be multiport strongly favors the choice of a modular design style. In such a design, functionality is split between those tasks common to all data channels and those exclusive to each individual channel. The RIC follows this approach, certain functional blocks are replicated for each network attachment, (also known as a repeater port), and others are shared. The following section briefly describes the functional blocks in the RIC.

5.1 OVERVIEW OF RIC FUNCTIONS

Segment Specific Block: Network Port

As shown in the Block Diagram, the segment specific blocks consist of:

1. One or more physical layer interfaces.
2. A logic block required for performing repeater operations upon that particular segment. This is known as the ''port'' logic since it is the access ''port'' the segment has to the rest of the network.

This function is repeated 13 times in the RIC (one for each port) and is shown on the right side of the Block Diagram, *Figure 5.1*.

The physical layer interfaces provided depends upon the port under examination. Port 1 has an AUI compliant interface for use with AUI compatible transceiver boxes and cable. Ports 2 to 13 may be configured for use with one of two interfaces: twisted pair or an external transceiver. The former utilizes the RIC's on-chip 10BASE-T transceivers, the latter allows connection to external transceivers. When using the external transceiver mode the interface is AUI compatible. Although AUI compatible transceivers are supported the interface is not designed for use with an interface cable, thus the transceivers are necessarily internal to the repeater equipment.

Inside the port logic there are 3 distinct functions:

1. The port state machine ''PSM'' is required to perform data and collision repetition as described by the repeater specification, for example, it determines whether this port should be receiving from or transmitting to its network segment.
2. The port partition logic implements the segment partitioning algorithm. This algorithm is defined by the IEEE specification and is used to protect the network from malfunctioning segements.
3. The port status register reflects the current status of the port. It may be accessed by a system processor to obtain this status or to perform certain port configuration operations, such as port disable.

Shared Functional Blocks:
Repeater Core Logic

The shared functional blocks consist of the Repeater Main State Machine (MSM) and Timers, a 32 bit Elasticity Buffer, PLL Decoder, and Receive and Transmit Multiplexors. These blocks perform the majority of the operations needed to fulfill the requirements of the IEEE repeater specification.

When a packet is received by a port it is sent via the Receive Multiplexor to the PLL Decoder. Notification of the data and collision status is sent to the main state machine via the receive multiplexor and collision activity status signals. This enables the main state machine to determine the source of the data to be repeated and the type of data to be transmitted. The transmit data may be either the received packet's data field or a preamble/jam pattern consisting of a 1010 . . . bit pattern.

Associated with the main state machine are a series of timers. These ensure various IEEE specification times (referred to as the TW1 to TW6 times) are fulfilled.

A repeater unit is required to meet the same signal jitter performance as any receiving node attached to a network segment. Consequently, a phase locked loop Manchester decoder is required so that the packet may be decoded, and the jitter accumulated over the receiving segment recovered. The decode logic outputs data in NRZ format with an associated clock and enable. In this form the packet is in a convenient format for transfer to other devices, such as network controllers and other RICs, via the Inter-RIC bus (described later). The data may then be re-encoded into Manchester data and transmitted.

Reception and transmission via physical layer transceiver units causes a loss of bits in the preamble field of a data packet. The repeater specification requires this loss to be compensated for. To accomplish this an elasticity buffer is employed to temporarily store bits in the data field of the packet.

The sequence of operation is as follows:

Soon after the network segment receiving the data packet has been identified, the RIC begins to transmit the packet preamble pattern (1010 . . .) onto the other network segments. While the preamble is being transmitted the Elasticity Buffer monitors the decoded received clock and data signals (this is done via the Inter-RIC bus as described later). When the start of frame delimiter ''SFD'' is detected the received data stream is written into the elasticity buffer. Removal of data from the buffer for retransmission is not allowed until a valid length preamble pattern has been transmitted.

Inter-RIC Bus Interface

Using the RIC in a repeater system allows the design to be constructed with many more network attachments than can be supported by a single chip. The split of functions already described allows data packets and collision status to be transferred between multiple RICs, and at the same time the multiple RICs still behave as a single logical repeater. Since all RICs in a repeater system are identical and capable of performing any of the repetition operations, the failure of one RIC will not cause the failure of the entire system. This is an important issue in large multiport repeaters.

RICs communicate via a specialized interface known as the Inter-RIC bus. This allows the data packet to be transferred from the receiving RIC to the other RICs in the system. These RICs then transmit the data stream to their segments. Just as important as data transfer is the notification of collisions occurring across the network. The Inter-RIC bus has a set of status lines capable of conveying collision information between RICs to ensure their main state machines operate in the appropriate manner.

5.0 Functional Description (Continued)

LED Interface and Hub Management Function

Repeater systems usually possess optical displays indicating network activity and the status of specific repeater operations. The RIC's display update block provides the system designer with a wide variety of indicators. The display updates are completely autonomous and merely require SSI logic devices to drive the display devices, usually made up of light emitting diodes, LEDs. The status display is very flexible allowing the user to choose those indicators appropriate for the specification of the equipment.

The RIC has been designed with special awareness for system designers implementing large repeaters possessing hub management capabilities. Hub management uses the unique position of repeaters in a network to gather statistics about the network segments they are attached to. The RIC provides hub management statistical data in 3 steps. Important events are gathered by the management block from logic blocks throughout the chip. These events may then be stored in on-chip latches or counted in on-chip counters according to user supplied latching and counting masks.

The fundamental task of a hub management system implementation is to associate the current packet and any management status information with the network segment, i.e., repeater port where the packet was received. The ideal system would place this combined data packet and status field in system memory for examination by hub management software. The ultimate function of the RIC's hub management support logic is to provide this function.

To accomplish this the RIC utilizes a dedicated hub management interface. This is similar to the Inter-RIC bus since it allows the data packet to be recovered from the receiving RIC. Unlike the Inter-RIC bus the intended recipient is not another RIC but National Semiconductor's DP83932 ''SONIC™'' Network controller. The use of a dedicated bus allows a management status field to be appended at the end of the data packet. This can be done without affecting the operation of the repeater system.

Processor Interface

The RIC's processor interface allows connection to a system processor. Data transfer occurs via an octal bi-directional data bus. The RIC has a number of on-chip registers indicating the status of the hub management functions, chip configuration and port status. These may be accessed by providing the chosen address at the Register Address (RA4–RA0) input pins.

Display update cycles and processor accesses occur utilizing the same data bus. An on-chip arbiter in the processor/display block schedules and controls the accesses and ensures the correct information is written into the display latches. During the display update cycles the RIC behaves as a master of its data bus. This is the default state of the data bus. Consequently, a TRI-STATE buffer must be placed between the RIC and the system processor's data bus. This ensures bus contention is avoided during simultaneous display update cycles and processor accesses of other devices on the system bus. When the processor accesses a RIC register, the RIC enables the data buffer and selects the operation, either input or output, of the data pins.

5.2 DESCRIPTION OF REPEATER OPERATIONS

In order to implement a multi-chip repeater system which behaves as though it were a single logical repeater, special consideration must be paid to the data path used in packet repetition. For example, where in the path are specific operations such as Manchester decoding and elasticity buffering performed. Also the system's state machines which utilize available network activity signals, must be able to accommodate the various packet repetition and collision scenarios detailed in the repeater specification.

The RIC contains two types of inter-acting state machines. These are:

1. Port State Machines (PSMs). Every network attachment has its own PSM.
2. Main State Machine (MSM). This state machine controls the shared functional blocks as shown in the block diagram *Figure 5.1.*

Repeater Port and Main State Machines

These two state machines are described in the following sections. Reference is made to expressions used in the IEEE Repeater specification. For the precise definition of these terms please refer to the specification. To avoid confusion with the RIC's implementation, where references are made to repeater states or terms as described in the IEEE specification, these items are written in *italics.* The IEEE state diagram is shown in *Figure 5-3*, the Inter-RIC bus state diagram is shown in *Figure 5-2*.

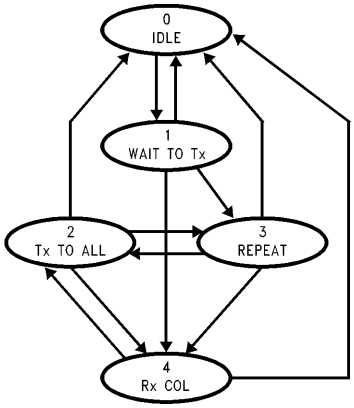


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FIGURE 5.2. Inter-RIC Bus State Diagram

5.0 Functional Description (Continued)

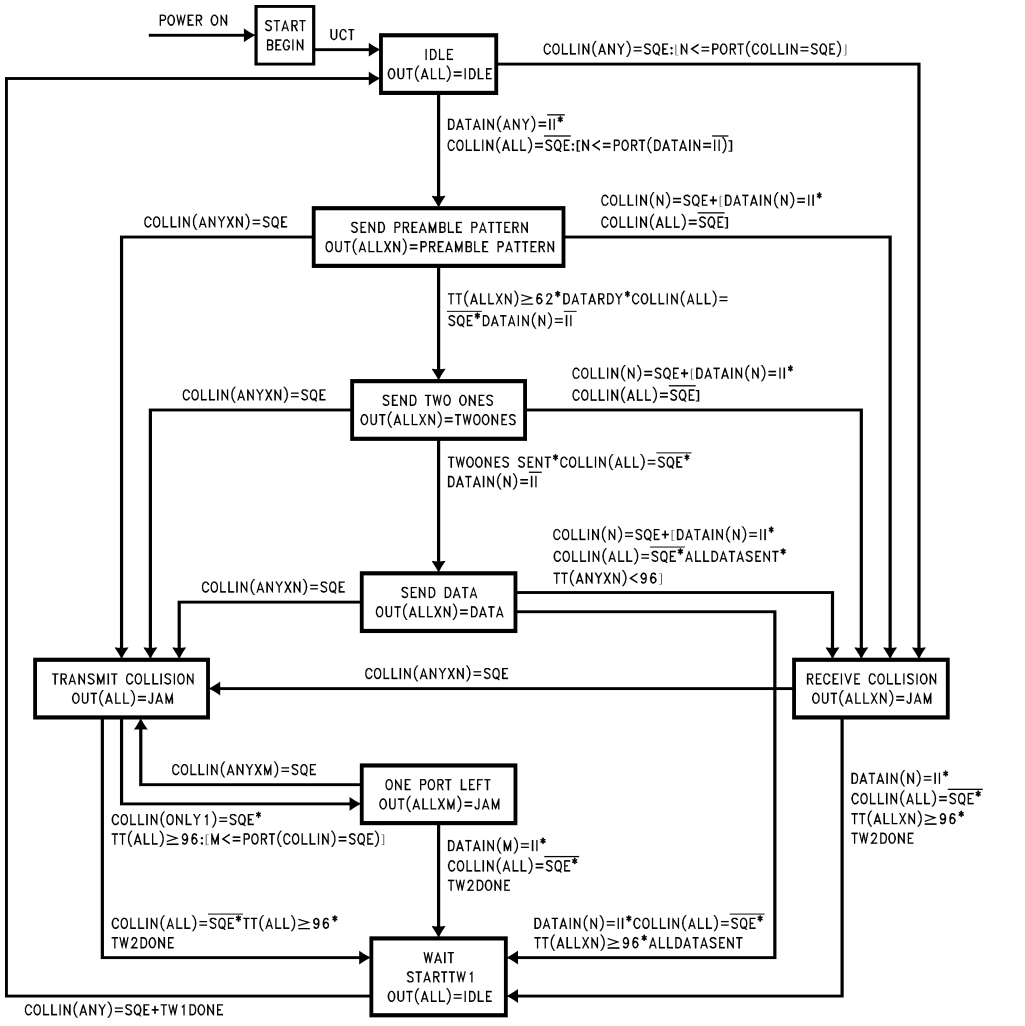


FIGURE 5.3. IEEE Repeater Main State Diagram

5.0 Functional Description (Continued)

Port State Machine (PSM)

There are two primary functions for the PSM as follows:

1. Control the transmission of repeated data and jam signals over the attached segment.
2. Decide whether a port will be the source of data or collision information which will be repeated over the network. This repeater port is known as *PORT N*. An arbitration process is required to enable the repeater to transition from the *IDLE* state to the *SEND PREAMBLE PATTERN* or *RECEIVE COLLISION* states, see *Figure 5.3*. This process is used to locate the port which will be *PORT N* for that particular packet. The data received from this port is directed to the PLL decoder and transmitted over the Inter-RIC bus. If the repeater enters the *TRANSMIT COLLISION* state a further arbitration operation is performed to determine which port is *PORT M*. *PORT M* is differentiated from the repeater's other ports if the repeater enters the *ONE PORT LEFT* state. In this state *PORT M* does not transmit to its segment; where as all other ports are still required to transmit to their segments.

Main State Machine (MSM)

The MSM controls the operation of the shared functional blocks in each RIC as shown in the block diagram, *Figure 5.1*, and it performs the majority of the data and collision propagation operations as defined by the IEEE specification, these include:

Function	Action
Preamble Regeneration	Restore the length of the preamble pattern to the defined size.
Fragment Extension	Extend received data or collision fragments to meet the minimum fragment length of 96 bits.
Elasticity Buffer Control	A portion of the received packet may require storage in an Elasticity Buffer to accommodate preamble regeneration.
Jam/ Preamble Pattern Generation	In cases of receive or transmit collisions a RIC is required to transmit a jam pattern (1010 . . .). **Note:** This pattern is the same as that used for preamble regeneration.
Transmit Collision Enforcement	Once the *TRANSMIT COLLISION* state is entered a repeater is required to stay in this state for at least 96 network bit times.
Data Encoding Control	NRZ format data from the elasticity buffer must be encoded into Manchester format data prior to retransmission.
Tw1 Enforcement	Enforce the Transmit Recovery Time specification.
Tw2 Enforcement	Enforce Carrier Recovery Time specification on all ports with active collisions.

The interaction of the main and port state machines is visible, in part, by observing the Inter-RIC bus.

Inter-RIC Bus Operation

Overview

The Inter-RIC Bus consists of eight signals. These signals implement a protocol which may be used to connect multiple RICs together. In this configuration, the logical function of a single repeater is maintained. The resulting multi-RIC system is compliant to the IEEE 802.3 repeater specification and may connect several hundred network segments. An example of a multi-RIC system is shown in *Figure 5.4*.

The Inter-RIC Bus connects multiple RICs to realize the following operations:

Port N Identification (which port the repeater receives data from)
Port M Identification (which port is the last one experiencing a collision)
Data Transfer
RECEIVE COLLISION identification
TRANSMIT COLLISION identification
DISABLE OUTPUT (jabber protection)

The following tables briefly describes the operation of each bus signal, the conditions required for a RIC to assert a signal and which RICs (in a multi-RIC system) would monitor a signal:

$\overline{\text{ACKI}}$	
Function	Input signal to the PSM arbitration chain. This chain is employed to identify *PORT N* and *PORT M*. **Note:** A RIC which contains *PORT N* or *PORT M* may be identified by its $\overline{\text{ACKO}}$ signal being low when its $\overline{\text{ACKI}}$ input is high.
Conditions required for a RIC to drive this signal	Not applicable
RIC Receiving the signal	This is dependent upon the method used to cascade RICs, described in a following section.

$\overline{\text{ACKO}}$	
Function	Output signal from the PSM arbitration chain.
Conditions required for a RIC to drive this signal	This is dependent upon the method used to cascade RICs, described in a following section.
RIC Receiving the Signal	Not applicable

5.0 Functional Description (Continued)

ACTN	
Function	This signal denotes there is activity on *PORT N* or *PORT M*.
Conditions required for a RIC to drive this signal	A RIC must contain *PORT N* or *PORT M*. **Note:** Although this signal normally has only one source asserting the signal active it is used in a wired-or configuration.
RIC Receiving the Signal	The signal is monitored by all RICs in the repeater system.

ANYXN	
Function	This signal denotes that a repeater port that is not *PORT N* or *PORT M* is experiencing a collision.
Conditions required for a RIC to drive this signal	Any RIC which satisfies the above condition. **Note:** This bus line is used in a wired-or configuration.
RIC Receiving the Signal	The signal is monitored by all RICs in the repeater system.

COLN	
Function	Denotes *PORT N* or *PORT M* is experiencing a collision.
Conditions required for a RIC to drive this signal	A RIC must contain *PORT N* or *PORT M*. (Note 1)
RIC Receiving the Signal	The Signal is monitored by all other RICs in the repeater system.

IRE	
Function	This signal acts as an activity framing signal for the IRC and IRD signals.
Conditions required for a RIC to drive this signal	A RIC must contain *PORT N*.
RIC Receiving the Signal	The Signal is monitored by all other RICs in the repeater system.

Note 1: Refer to note on page 25 for the transmit collision case.

IRD	
Function	Decoded serial data, in NRZ format, received from the network segment attached to *PORT N*.
Conditions required for a RIC to drive this signal	A RIC must contain *PORT N*.
RIC Receiving the Signal	The signal is monitored by all other RICs in the repeater system.

IRC	
Function	Clock signal associated with IRD and IRE.
Conditions required for a RIC to drive this signal	A RIC must contain *PORT N*.
RIC Receiving the Signal	The signal is monitored by all other RICs in the repeater system.

Methods of RIC Cascading

In order to build multi-RIC repeaters *PORT N* and *PORT M* identification must be performed across all the RICs in the system. Inside each RIC the PSMs are arranged in a logical arbitration chain where port 1 is the highest and port 13 the lowest. The top of the chain, the input to port 1 is accessible to the user via the RIC's $\overline{\text{ACKI}}$ input pin. The output from the bottom of the chain becomes the $\overline{\text{ACKO}}$ output pin. In a single RIC system *PORT N* is defined as the highest port in the arbitration chain with receive or collision activity. *Port N* identification is performed when the repeater is in the *IDLE* state. *PORT M* is defined as the highest port in the chain with a collision when the repeater leaves the *TRANSMIT COLLISION* state. In order for the arbitration chain to function, all that needs to be done is to tie the $\overline{\text{ACKI}}$ signal to a logic high state. In multi-RIC systems there are two methods to propagate the arbitration chain between RICs:

The first and most straight forward is to extend the arbitration chain by daisy chaining the $\overline{\text{ACKI}}$ $\overline{\text{ACKO}}$ signals between RICs. In this approach one RIC is placed at the top of the chain (its $\overline{\text{ACKI}}$ input is tied high), then the $\overline{\text{ACKO}}$ signal from this RIC is sent to the $\overline{\text{ACKI}}$ input of the next RIC and so on. This arrangement is simple to implement but it places some topological restrictions upon the repeater system. In particular, if the repeater is constructed using a backplane with removable printed circuit boards. (These boards contain the RICs and their associated components). If one of the boards is removed then the $\overline{\text{ACKI}}$ $\overline{\text{ACKO}}$ chain will be broken and the repeater will not operate correctly.

5.0 Functional Description (Continued)

The second method of *PORT N* or *M* identification avoids this problem. This second technique relies on an external parallel arbiter which monitors all of the RIC's $\overline{\text{ACKO}}$ signals and responds to the RIC with the highest priority. In this scheme each RIC is assigned with a priority level. One method of doing this is to assign a priority number which reflects the position of a RIC board on the repeater backplane, i.e., its slot number. When a RIC experiences receive activity and the repeater system is in the *IDLE* state, the RIC board will assert $\overline{\text{ACKO}}$. External arbitration logic drives the identification number onto an arbitration bus and the RIC containing *PORT N* will be identified. An identical procedure is used in the *TRANSMIT COLLISION* state to identify *PORT M*. This parallel means of arbitration is not subject to the problems caused by missing boards, i.e., empty slots in the backplane. The logic associated with asserting this arbitration vector in the various packet repetition scenarios could be implemented in programmable logic type devices.

To perform *PORT N* or *M* arbitration both of the above methods employ the same signals: $\overline{\text{ACKI}}$, $\overline{\text{ACKO}}$ and ACTN.

The Inter-RIC bus allows multi-RIC operations to be performed in exactly the same manner as if there is only a single RIC in the system. The simplest way to describe the operation of Inter-RIC bus is to see how it is used in a number of common packet repetition scenarios. Throughout this description the RICs are presumed to be operating in external transceiver mode. This is advantageous for the explanation since the receive, transmit and collision signals from each network segment are observable. In internal transceiver mode this is not the case, since the collision signal for the non-AUI ports is derived by the transceivers inside the RIC.

5.3 EXAMPLES OF PACKET REPETITION SCENARIOS

Data Repetition

The simplest packet operation performed over the Inter-RIC Bus is data repetition. In this operation a data packet is received at one port and transmitted to all other segments.

The first task to be performed is *PORT N* identification. This is an arbitration process performed by the Port State Machines in the system. In situations where two or more ports simultaneously receive packets the Inter-RIC bus operates by choosing one of the active ports and forcing the others to transmit data. This is done to faithfully follow the IEEE specification's allowed exit paths from the *IDLE* state, i.e., to the *SEND PREAMBLE PATTERN* or *RECEIVE COLLISION* states.

The packet begins with a preamble pattern derived from the RIC's on chip jam/preamble generator. The data received at *PORT N* is directed through the receive multiplexor to the PLL decoder. Once phase lock has been achieved, the decoded data, in NRZ format, with its associated clock and enable signals are asserted onto the IRD IRE and IRC Inter-RIC bus lines. This serial data stream is received from the bus by all RICs in the repeater and directed to their Elasticity Buffers. Logic circuits monitor the data stream and look for the Start of Frame Delimiter (SFD). When this has been detected data is loaded into the elasticity buffer for later transmission. This will occur when sufficient preamble has been transmitted and certain internal state machine operations have been fulfilled.

Figure 5.4 shows two RICs A and B, daisy chained together with RIC A positioned at the top of the chain. A packet is received at port B1 of RIC B and is then repeated by the other ports in the system. *Figure 5.5* shows the functional timing diagram for this packet repetition represented by the signals shown in *Figure 5.4*. In this example only two ports in the system are shown, obviously the other ports also repeat the packet. It also indicates the operation of the RICs' state machines in so far as can be seen by observing the Inter-RIC bus. For reference, the repeater's state transitions are shown in terms of the states defined by the IEEE specification. The location, i.e., which port it is, of *PORT N* is also shown. The following section describes the repeater and Inter-RIC bus transitions shown in *Figure 5.5*.

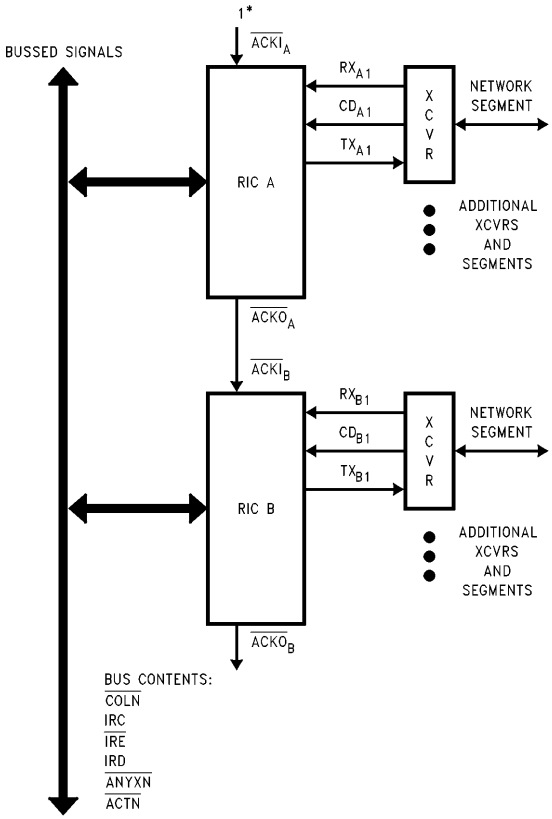
The repeater is stimulated into activity by the data signal received by port B1. The RICs in the system are alerted to forthcoming repeater operation by the falling edges on the $\overline{\text{ACKI}}$ $\overline{\text{ACKO}}$ daisy chain and the ACTN bus signal. Following a defined start up delay the repeater moves to the *SEND PREAMBLE* state. The RIC system utilizes the start up delay to perform port arbitration. When packet transmission begins the RIC system enter the REPEAT state.

The expected, for normal packet repetition, sequence of repeater states, *SEND PREAMBLE*, *SEND SFD* and *SEND DATA* is followed but is not visible upon the Inter-RIC bus. They are merged together into a single REPEAT state. This is also true for the *WAIT* and *IDLE* states, they appear as a combined Inter-RIC bus IDLE state.

Once a repeat operation has begun, i.e., the repeater leaves the *IDLE* state. It is required to transmit at least 96 bits of data or jam/preamble onto its network segments. If the duration of the received signal from *PORT N* is smaller than 96 bits, the repeater transitions to the *RECEIVE COLLISION* state (described later). This behavior is known as fragment extension.

After the packet data has been repeated, including the emptying of the RICs' elasticity buffers, the RIC performs the *Tw1* transmit recovery operation. This is performed during the *WAIT* state shown in the repeater state diagram.

5.0 Functional Description (Continued)



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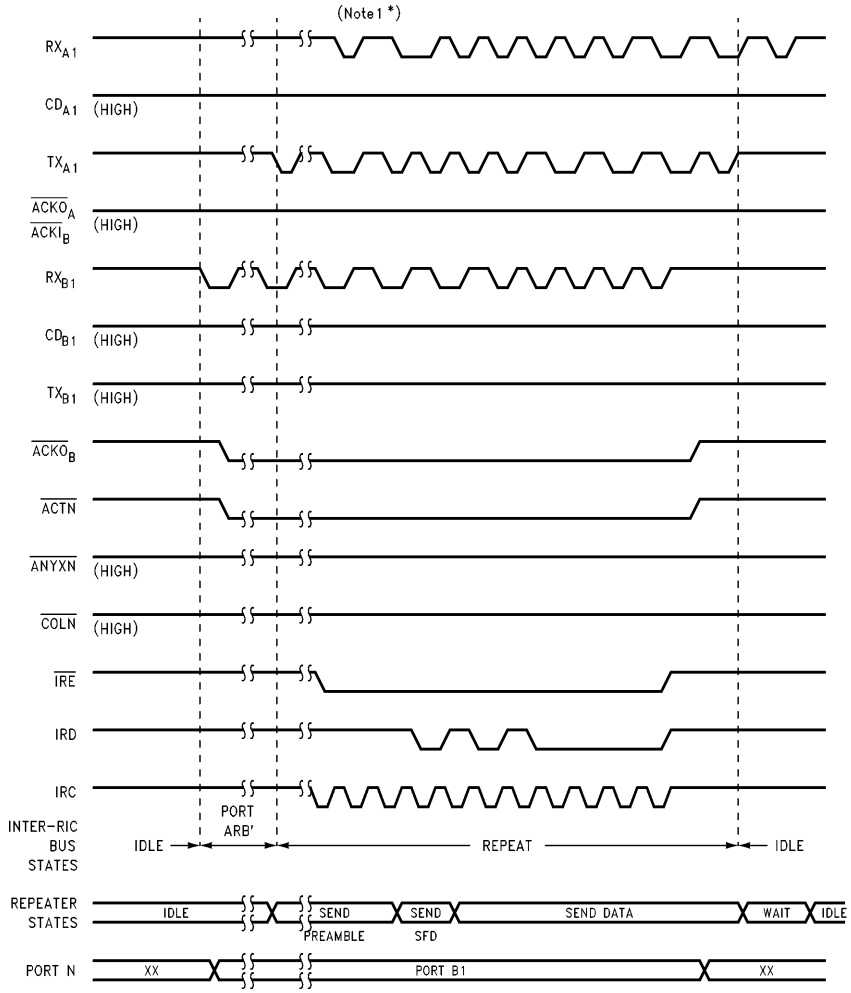
Note: In this example the Inter-RIC bus is configured to use active low signals.

FIGURE 5.4. RIC System Topology

5.0 Functional Description (Continued)



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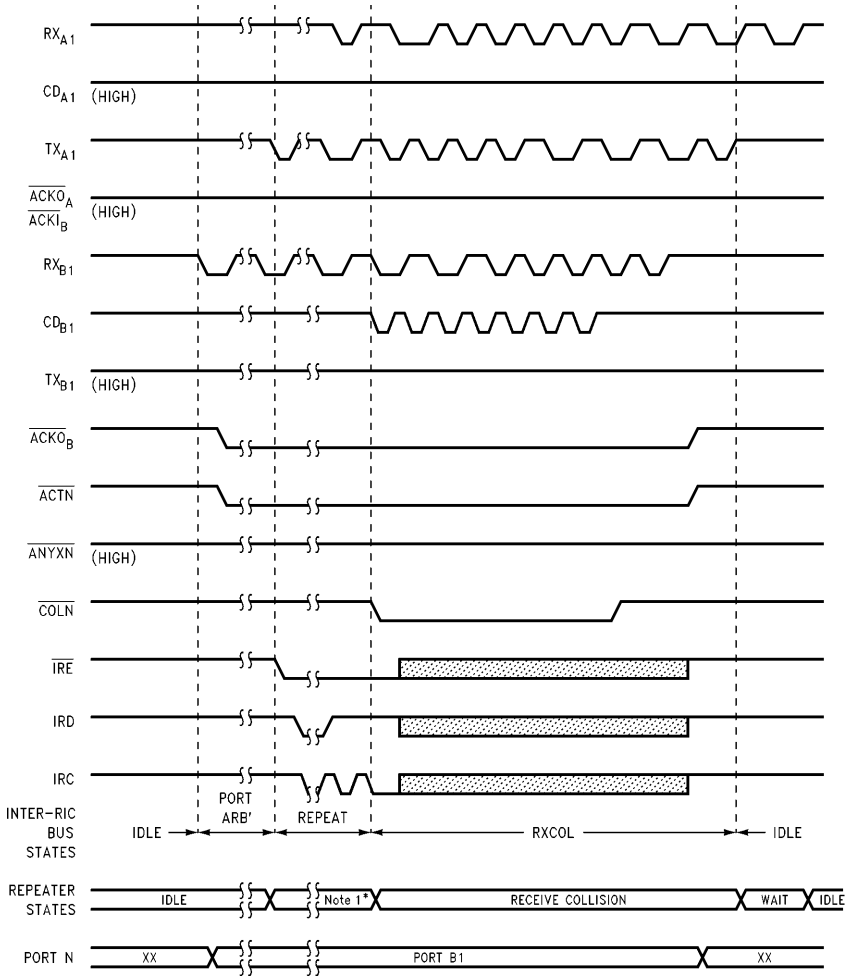
*__Note 1:__ The activity shown in RX_{A1} represents the transmitted signal on TX_{A1} after being looped back by the attached transceiver.

__Note:__ In this example the Inter-RIC bus is configured to use active low signals.

FIGURE 5.5. Data Repetition

5.0 Functional Description (Continued)



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*__Note 1:__ *SEND PREAMBLE, SEND SFD, SEND DATA*.

__Note:__ In this example the Inter-RIC bus is configured to use active low signals.

FIGURE 5.6. Receive Collision

5.0 Functional Description (Continued)

Receive Collisions

A receive collision is a collision which occurs on the network segment attached to *PORT N*, i.e., the collision is ''received'' in a similar manner as a data packet is received and then repeated to the other network segments. Not surprisingly receive collision propagation follows a similar sequence of operations as is found with data repetition:

An arbitration process is performed to find *PORT N* and a preamble/jam pattern is transmitted by the repeater's other ports. When *PORT N* detects a collision on its segment the COLN Inter-RIC bus signal is asserted. This forces all the RICs in the system to transmit a preamble/jam pattern to their segments. This is important since they may be already transmitting data from their elasticity buffers. The repeater moves to the *RECEIVE COLLISION* state when the RICs begin to transmit the jam pattern. The repeater remains in this state until both the following conditions have been fulfilled:

1. At least 96 bits have been transmitted onto the network,
2. The activity has ended.

Under close examination the repeater specification reveals that the actual end of activity has its own permutations of conditions:

1. Collision and receive data signals may end simultaneously,
2. Receive data may appear to end before collision signals,
3. Receive data may continue for some time after the end of the collision signal.

Network segments using coaxial media may experience spurious gaps in segment activity when the collision signal goes inactive. This arises from the inter-action between the receive and collision signal squelch circuits, implemented in coaxial transceivers, and the properties of the coaxial cable itself. The repeater specification avoids propagation of these activity gaps by extending collision activity by the *Tw2* wait time. Jam pattern transmission must be sustained throughout this period. After this, the repeater will move to the *WAIT* state unless there is a data signal being received by *PORT N*.

The functional timing diagram, *Figure 5.6*, shows the operation of a repeater system during a receive collision. The system configuration is the same as earlier described and is shown in *Figure 5.4*.

The RICs perform the same *PORT N* arbitration and data repetition operations as previously described. The system is notified of the receive collision on port B1 by the COLN bus signal going active. This is the signal which informs the main state machines to output the jam pattern rather than the data held in the elasticity buffers. Once a collision has occurred the IRC, IRD AND $\overline{\text{IRE}}$ bus signals may become undefined. When the collision has ended and the *Tw2* operation performed, the repeater moves to the *WAIT state.*

Transmit Collisions

A transmit collision is a collision that is detected upon a segment to which the repeater system is transmitting. The port state machine monitoring the colliding segment asserts the ANYXN bus signal. The assertion of ANYXN causes *PORT M* arbitration to begin. The repeater moves to the *TRANSMIT COLLISION* state when the port which has been *PORT N* starts to transmit a Manchester encoded 1 on to its network segment. Whilst in the *TRANSMIT COLLISION* state all ports of the repeater must transmit the 1010 . . . jam pattern and *PORT M* arbitration is performed. Each RIC is obliged, by the IEEE specification, to ensure all of its ports transmit for at least 96 bits once the *TRANSMIT COLLISION* state has been entered. This transmit activity is enforced by the ANYXN bus signal. Whilst ANYXN is active all RIC ports will transmit jam. To ensure this situation lasts for at least 96 bits, the MSMs inside the RICs assert the ANYXN signal throughout this period. After this period has elapsed, ANYXN will only be asserted if there are multiple ports with active collisions on their network segments.

There are two possible ways for a repeater to leave the *TRANSMIT COLLISION* state. The most straight forward is when network activity, i.e., collisions and their *Tw2* extensions, end before the 96 bit enforced period expires. Under these conditions the repeater system may move directly to the *WAIT* state when 96 bits have been transmitted to all ports. If the MSM enforced period ends and there is still one port experiencing a collision the *ONE PORT LEFT* state is entered. This may be seen on the Inter-RIC bus when ANYXN is deasserted and *PORT M* stops transmitting to its network segment. In this circumstance the Inter-RIC bus transitions to the RECEIVE COLLISION state. The repeater will remain in this state whilst *PORT M's* collision, *Tw2* collision extension and any receive signals are present. When these conditions are not true, packet repetition finishes and the repeater enters the *WAIT* state.

Figure 5.7 shows a multi-RIC system operating under transmit collision conditions. There are many different scenarios which may occur during a transmit collision, this figure illustrates one of these. The diagram begins with packet reception by port A1. Port B1 experiences a collision, since it is not *PORT N* it asserts ANYXN. This alerts the main state machines in the system to switch from data to jam pattern transmission.

Port A1 is also monitoring the ANYXN bus line. Its assertion forces A1 to relinquish its *PORT N* status, start transmitting, stop asserting ACTN and release its hold on the PSM arbitration signals ($\overline{\text{ACKO}}$ A and $\overline{\text{ACKI}}$ B). The first bit it transmit will be a Manchester encoded ''1'' in the jam pattern. Since port B1 is the only port with a collision it attains *PORT M* status and stops asserting ANYXN. It does however assert ACTN, and exert its presence upon the PSM arbitration chain (forces$\overline{\text{ACKO}}$ B low). The MSMs ensure that ANYXN stays active and thus force all of the ports, including *PORT M*, to transmit to their segments.

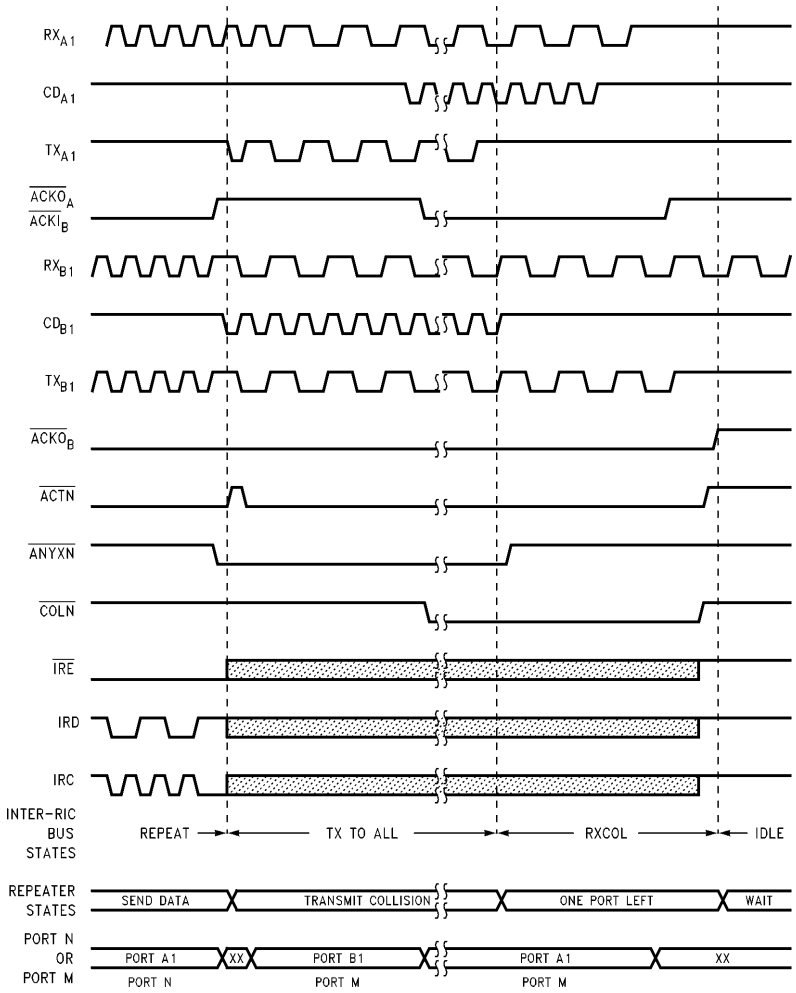
After some time port A1 experiences a collision. This arises from the presence of the packet being received from port A1's segment and the jam signal the repeater is now transmitting onto this segment. Two packets on one segment results in a collision. *PORT M* now moves from B1 to A1. Port A1 fulfills the same criteria as B1, i.e., it has an active collision on its segment, but in addition it is higher in the arbitration chain. This priority yields no benefits for port A1 since the ANYXN signal is still active. There are now two sources driving ANYXN, the MSMs and the collision on port B1.

Eventually the collision on port B1 ends and the ANYXN extension by the MSMs expires. There is only one collision

5.0 Functional Description (Continued)

on the network (this may be deduced since ANYXN is inactive) so the repeater will move to the *ONE PORT LEFT* state. The RIC system treats this state in a similar manner to a receive collision with *PORT M* fulfilling the role of the receiving port. The difference from a true receive collision is that the switch from packet data to the jam pattern has already been made (controlled by ANYXN). Thus the state of COLN has no effect upon repeater operations. In common with the operation of the *RECEIVE COLLISION* state, the repeater remains in this condition until the collision and receive activity on *PORT M* sibsides. The packet repetition operation completes when the *Tw1* recovery time in the *WAIT* state has been performed.

Note: In transmit collision conditions COLN will only go active if the RIC which contained *PORT N* at the start of packet repetition contains *PORT M* during the *TRANSMIT COLLISION* and *ONE PORT LEFT* states.



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Note: In this example the Inter-RIC bus is configured to use active low signals.

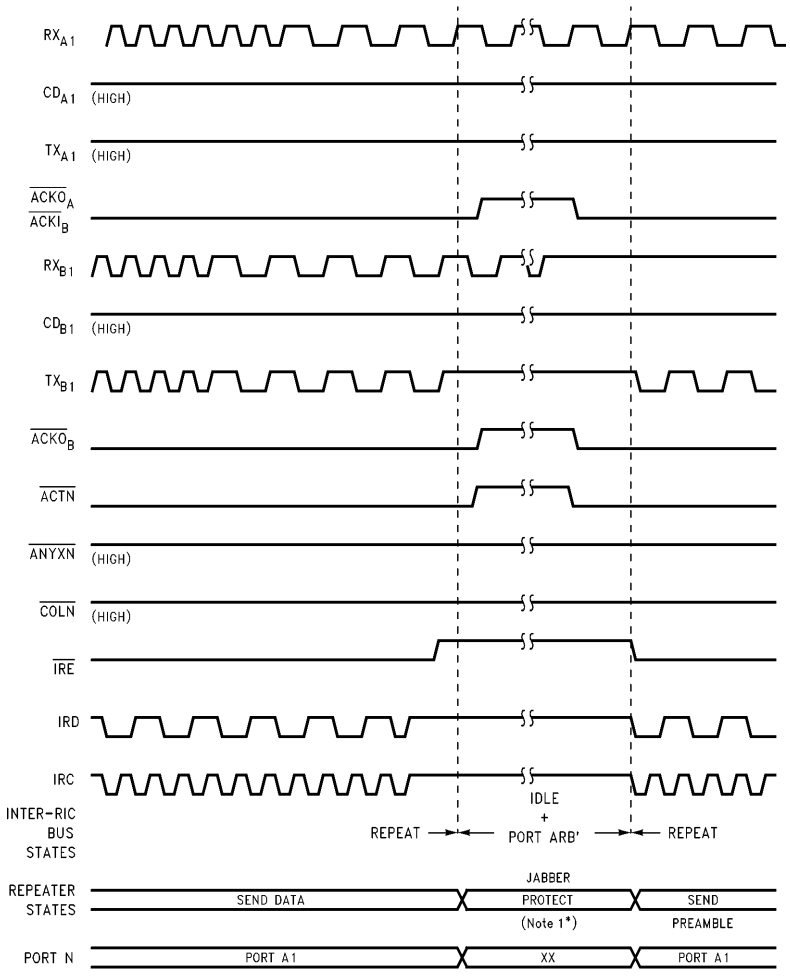
FIGURE 5.7. Transmit Collision

5.0 Functional Description (Continued)

Jabber Protection

A repeater is required to disable transmit activity if the length of its current transmission reaches the jabber protect limit. This is defined by the specification's *Tw3* time. The repeater disables output for a time period defined by the *Tw4* specification, after this period normal operation may resume.

Figure 5.8 shows the effect of a jabber length packet upon a RIC based repeater system. The **JABBER PROTECT** state is entered from the *SEND DATA* state. While the *Tw4* period is observed the Inter-RIC bus displays the IDLE state. This is misleading since new packet activity or continuous activity (as shown in the diagram) does not result in packet repetition. This may only occur when the *Tw4* requirement has been satisified.



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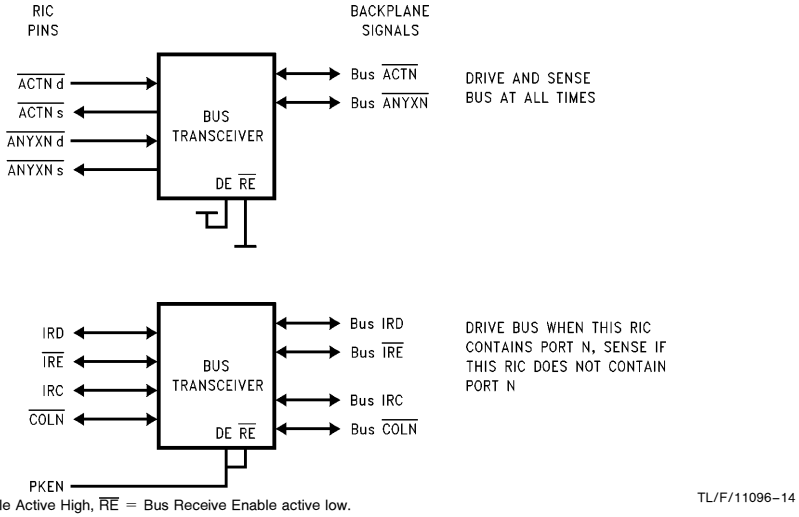
*__Note 1:__ The IEEE Specification does not have a jabber protect state defined in its main state diagram, this behaviour is defined in an additional MAU Jabber Lockup Protection state diagram.

Note: In this example the Inter-RIC bus is configured to use active low signals.

FIGURE 5.8. Jabber Protect

5.0 Functional Description (Continued)

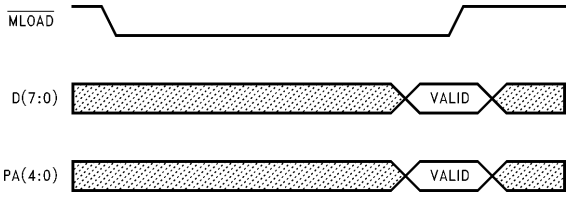


TL/F/11096–14

Note: DE = Bus Drive Enable Active High, $\overline{RE}$ = Bus Receive Enable active low.

Note: In this example the Inter-RIC bus is shown as using active low signals.

FIGURE 5.9. External Bus Transceiver Connection Diagram



TL/F/11096–15

FIGURE 5.10. Mode Load Operation

5.0 Functional Description (Continued)

5.4 DESCRIPTION OF HARDWARE CONNECTION FOR INTER-RIC BUS

When considering the hardware interface the Inter-RIC bus may be viewed as consisting of three groups of signals:

1. Port Arbitration chain, namely: $\overline{\text{ACKI}}$ and $\overline{\text{ACKO}}$.
2. Simultaneous drive and sense signals, i.e., ACTN and ANYXN. (Potentially these signals may be driven by multiple devices).
3. Drive or sense signals, i.e., IRE, IRD, IRC and COLN. (Only one device asserts these signals at any instance in time.)

The first set of signals are either used as point to point links or with external arbitration logic. In both cases the load on these signals will not be large so that the on-chip drivers are adequate. This may not be true for signal classes (2) and (3).

The Inter-RIC bus has been designed to connect RICs together directly or via external bus transceivers. The latter is advantageous in large repeaters. In the second application the backplane is often heavily loaded and is beyond the drive capability of the on-chip bus drivers. The need for simultaneous sense and drive capabilities on the ACTN and ANYXN signals and the desire to allow operation with external bus transceivers makes it necessary for these bus signals to each have a pair of pins on the RIC. One driving the bus the other sensing the bus signal. When external bus transceivers are used they must be open collector/open drain to allow wire-ORing of the signals. Additionally, the drive and sense enables of the bus transceiver should be tied in the active state.

When the RIC is used in a stand alone configuration, it is required to tie ACTN_D to ACTN_S and ANYXN_D to ANYXN_S.

The uni-directional nature of information transfer on the IRE, IRD, IRC and COLN signals, means a RIC is either driving these signals or receivng them from the bus but not both at the same time. Thus a single bi-directional input/output pin is adequate for each of these signals. In an external bus transceiver is used with these signals the Packet Enable ''PKEN'' RIC output pin performs the function of a drive enable and sense disable.

Figure 5.9 shows the RIC connected to the Inter-RIC bus via external bus transceivers, such as National's DS3893A bus transceivers.

Some bus transceivers are of the inverting type. To allow the Inter-RIC bus to utilize these transceivers the RIC may be configured to invert the active states of the ACTN, ANYXN, COLN and IRE signals. Instead of being active low they are active high.

Thus they become active low once more when passed through an inverting bus driver. This is particularly important for the ACTN and ANYXN bus lines, since these signals must be used in a wired-or configuration. Incorrect signal polarity would make the bus unusable.

5.5 PROCESSOR AND DISPLAY INTERFACE

The processor interface pins, which include the data bus, address bus and control signals, actually perform three operations which are multiplexed on these pins. These operations are:

1. The Mode Load Operation, which performs a power up initialization cycle upon the RIC.
2. Display Update Cycles, which are refresh operations for updating the display LEDs.
3. Processor Access Cycles, which allows μP's to communicate with the RIC's registers.

These three operations are described below.

Mode Load Operation

The Mode Load Operation is a hardware initialization procedure performed at power on. It loads vital device configuration information into on-chip configuration registers. In addition to its configuration function the $\overline{\text{MLOAD}}$ pin is the RIC's reset input. When $\overline{\text{MLOAD}}$ is low all of the RIC's repeater timers, state machines, segment partition logic and hub management logic are reset.

The Mode Load Operation may be accomplished by attaching the appropriate set of pull up and pull down resistors to the data and register address pins to assert logic high or low signals onto these pins, and the providing a rising edge on the $\overline{\text{MLOAD}}$ pin as is shown in *Figure 5.10*. The mapping of chip functions to the configuration inputs is shown in Table 5.1. Such an arrangement may be performed using a simple resistor, capacitor, diode network. Performing the Mode Load Operation in this way enables the configuration of a RIC that is in a simple repeater system (one without a processor).

Alternatively in a complex repeater system, the Mode Load Operation may be performed using a processor write cycle. This would require the $\overline{\text{MLOAD}}$ pin be connected to the CPU's write strobe via some decoding logic, and included in the processor's memory map.

5.0 Functional Description (Continued)

TABLE 5.1. Pin Definitions for Options in the Mode Load Operation

Pin Name	Programming Function	Effect When Bit is 0	Effect When Bit is 1	Function
D0	resv	Not Permitted	Required	To ensure correct device operation, this bit must be written with a logic one during the mode load operation.
D1	tw2	5 bits	3 bits	This allows the user to select one of two values for the repeater specification tw2 time. The lower limit (3 bits) meets the IEEE specification. The upper limit (5 bits) is not specification compliant but may provide users with higher network throughput by avoiding spurious network activity gaps when using coaxial (10BASE2, 10BASE5) network segments.
D2	$\overline{\text{CCLIM}}$	63	31	The partition specification requires a port to be partitioned after a certain number of consecutive collisions. The RIC has two values available to allow users to customize the partitioning algorithm to their environment. Please refer to the Partition State Machine, in data sheet Section 7.3.
D3	$\overline{\text{LPPART}}$	Selected	Not Selected	The RIC may be configured to partition a port if the segment transceiver does not loopback data to the port when the port is transmitting to it, as described in the Partition State Machine.
D4	$\overline{\text{OWCE}}$	Selected	Not Selected	This configuration bit allows the on-chip partition algorithm to include out of window collisions into the collisions it monitors, as described in the Partition State Machine.
D5	$\overline{\text{TXONLY}}$	Selected	Not Selected	This configuration bit allows the on-chip partition algorithm to restrict segment reconnection, as described in the Partition State Machine.
D6	$\overline{\text{DPART}}$	Selected	Not Selected	The Partition state machines for all ports may be disabled by writing a logic zero to this bit during the mode load operation.
D7	MIN/MAX	Minimum Mode	Maximum Mode	The operation of the display update block is controlled by the value of this configuration bit, as described in the Display Update Cycles section.

TABLE 5.1 Pin Definitions for Options in the Mode Load Operation (Continued)

<table>
<tr><th>Pin Name</th><th>Programming Function</th><th>Effect When Bit is 0</th><th>Effect When Bit is 1</th><th>Function</th></tr>
<tr><td>RA0</td><td>BYPAS1</td><td></td><td></td><td rowspan="2">These configuration bits select which of the repeater ports (numbers 2 to 13) are configured to use the on-chip internal 10BASE-T transceivers or the external transceiver interface. The external transceiver interface operates using AUI compatible signal levels.

<table>
<tr><th>BYPAS2</th><th>BYPAS1</th><th>Information</th></tr>
<tr><td>0</td><td>0</td><td>All ports (2 to 13) use the external Transceiver Interface.</td></tr>
<tr><td>0</td><td>1</td><td>Ports 2 to 7 use the external interface, 8 to 13 use the internal 10BASE-T transceivers.</td></tr>
<tr><td>1</td><td>0</td><td>Ports 2 to 5 use the external interface, 6 to 13 use the internal 10BASE-T transceivers.</td></tr>
<tr><td>1</td><td>1</td><td>All ports (2 to 13) use the internal 10BASE-T transceivers.</td></tr>
</table></td></tr>
<tr><td>RA1</td><td>BYPAS2</td><td></td><td></td></tr>
<tr><td>RA2</td><td>BINV</td><td>Active High Signals</td><td>Active Low Signals</td><td>This selection determines whether the Inter-RIC signals: IRE, ACTN, ANYXN, COLN and Management bus signal MCRS are active high or low.</td></tr>
<tr><td>RA3</td><td>EXPLL</td><td>External PLL</td><td>Internal PLL</td><td>If desired, the RIC may be used with an external decoder, this configuration bit performs the selection.</td></tr>
<tr><td>RA4</td><td>resv</td><td>Not Permitted</td><td>Required</td><td>To ensure correct device operation, this bit must be written with a logic one during the mode load operation.</td></tr>
</table>

5.0 Functional Description (Continued)

5.6 DESCRIPTION OF HARDWARE CONNECTION FOR PROCESSOR AND DISPLAY INTERFACE

Display Update Cycles

The RIC possesses control logic and interface pins which may be used to provide status information concerning activity on the attached network segments and the current status of repeater functions. These status cycles are completely autonomous and require only simple support circuitry to produce the data in a form suitable for a light emitting diode ''LED'' display. The display may be used in one of two modes:

1. Minimum Mode: General Repeater Status LEDs

2. Maximum Mode: Individual Port Status LEDs

Minimum mode, intended for simple LED displays, makes available four status indicators. The first LED denotes whether the RIC has been forced to activate its jabber protect functions. The remaining 3 LEDs indicate if any of the RIC's network segments are: (1) experiencing a collision, (2) receiving data, (3) currently partitioned. When minimum display mode is selected the only external components required are a 74LS374 type latch, the LEDs and their current limiting resistors.

Maximum mode differs from minimum mode by providing display information specific to individual network segments. This information denotes the collision activity, packet reception and partition status of each segment. In the case of 10BASE-T segments the link integrity status and polarity of the received data are also made available. The wide variety of information available in maximum mode may be used in its entirety or in part. Thus allowing the system designer to choose the appropriate complexity of status display commensurate with the specification of the end equipment.

The signals provided and their timing relationships have been designed to interface directly with 74LS259 type addressable latches. The number of latches used being dependant upon the complexity of the display. Since the latches are octal, a pair of latches is needed to display each type of segment specific data (13 ports means 13 latch bits). The accompanying tables (5.1 and 5.2) show the function of the interface pins in minimum and maximum modes. *Figure 5.12* shows the location of each port's status information when maximum mode is selected. This may be compared with the connection diagram *Figure 5.11*.

Immediately following the Mode Load Operation (when the $\overline{\text{MLOAD}}$ pin transitions to a high logic state), the display logic performs an LED test operation. This operation lasts one second and while it is in effect all of the utilized LEDs will blink on. Thus an installation engineer is able to test the operation of the display by forcing the RIC into a reset cycle ($\overline{\text{MLOAD}}$ forced low). The rising edge on the $\overline{\text{MLOAD}}$ pin starts the LED test cycle. **During the LED test cycle the RIC does not perform packet repetition operations.**

The status display possesses a capability to lengthen the time an LED is active. At the end of the repetition of a packet, the display is frozen showing the current activity. This freezing lasts for 30 milliseconds or until a subsequent packet is repeated. Thus at low levels of packet activity the display stretches activity information to make it discernable to the human eye. At high traffic rates the relative brightness of the LEDs indicates those segments with high or low activity.

It should be mentioned that when the Real Time Interrupt (RTI) occurs, the display update cycle will stop and after RTI is serviced, the display update cycle will resume activity.

TABLE 5.2. Status Display Pin Functions in Minimum Mode

Signal Pin Name	Function in MINIMUM MODE
D0	No operation
D1	Provides status information indicating if there is a collision occurring on one of the segments attached to this RIC.
D2	Provides status information indicating if one of this RIC's ports is receiving a data or collision packet from a segment attached to this RIC.
D3	Provides status information indicating that the RIC has experienced a jabber protect condition.
D4	Provides Status information indicating if one of the RIC's segments is partitioned.
D(7:5)	No operation
$\overline{\text{STR0}}$	This signal is the latch enable for the 374 type latch.
$\overline{\text{STR1}}$	This signal is held at a logic one.

5.0 Functional Description (Continued)

Table 5.3 Status Display Pin Functions in MAXIMUM MODE

Signal Pin Name	Function in Maximum Mode
D0	Provides status information concerning the Link Integrity status of 10BASE-T segments. This signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D1	Provides status information indicating if there is a collision occurring on one of the segments attached to this RIC. This signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D2	Provides status information indicating if one of this RIC's ports is receiving a data or a collision packet from its segment. This signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D3	Provides Status information indicating that the RIC has experienced a jabber protect condition. Additionally it denotes which of its ports are partitioned. This signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D4	Provides status information indicating if one of this RIC's ports is receiving data of inverse polarity. This status output is only valid if the port is configured to use its internal 10BASE-T transceiver. The signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D(7:5)	These signals provide the repeater port address corresponding to the data available on D(4:0).
$\overline{STR0}$	This signal is the latch enable for the lower byte latches, that is the 74LS259s which display information concerning ports 1 to 7.
$\overline{STR1}$	This signal is the latch enable for the upper byte latches, that is the 74LS259s which display information concerning ports 8 to 13.

Maximum Mode LED Definitions

74LS259 Latch Inputs = $\overline{STR0}$

259 Output	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
259 Addr S2–0	000	001	010	011	100	101	110	111
RIC Port Number		1 (AUI)	2	3	4	5	6	7
RIC D0 259 #1			LINK	LINK	LINK	LINK	LINK	LINK
RIC D1 259 #2	ACOL	COL	COL	COL	COL	COL	COL	COL
RIC D2 259 #3	AREC	REC	REC	REC	REC	REC	REC	REC
RIC D3 259 #4	JAB	PART	PART	PART	PART	PART	PART	PART
RIC D4 259 #5			BDPOL	BDPOL	BDPOL	BDPOL	BDPOL	BDPOL

74LS259 (or Equiv.) Latch Inputs = $\overline{STR1}$

259 Output	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
259 Addr S2–0	000	001	010	011	100	101	110	111
RIC Port Number	8	9	10	11	12	13		
RIC D0 259 #6	LINK	LINK	LINK	LINK	LINK	LINK		
RIC D1 259 #7	COL	COL	COL	COL	COL	COL		
RIC D2 259 #8	REC	REC	REC	REC	REC	REC		
RIC D3 259 #9	PART	PART	PART	PART	PART	PART		
RIC D4 259 #10	BDPOL	BDPOL	BDPOL	BDPOL	BDPOL	BDPOL		

This shows the LED Output Functions for the LED Drivers when 74LS259s are used. The top table refers to the bank of 4 74LS259s latched with $\overline{STR0}$, and the lower table refers to the bank of 4 74LS259s latched with $\overline{STR1}$. For example the RIC's D0 data signal goes to 259 #1 and #5. These two 74LS259s then drive the LINK LEDs).

Note: ACOL = Any Port Collision, AREC = Any Port Reception, JAB = Any Port Jabbering, LINK = Port Link, COL = Port Collision, REC = Port Reception, PART = Port Partitioned, BDPOL = Bad (inverse) Polarity or received data.

FIGURE 5.12

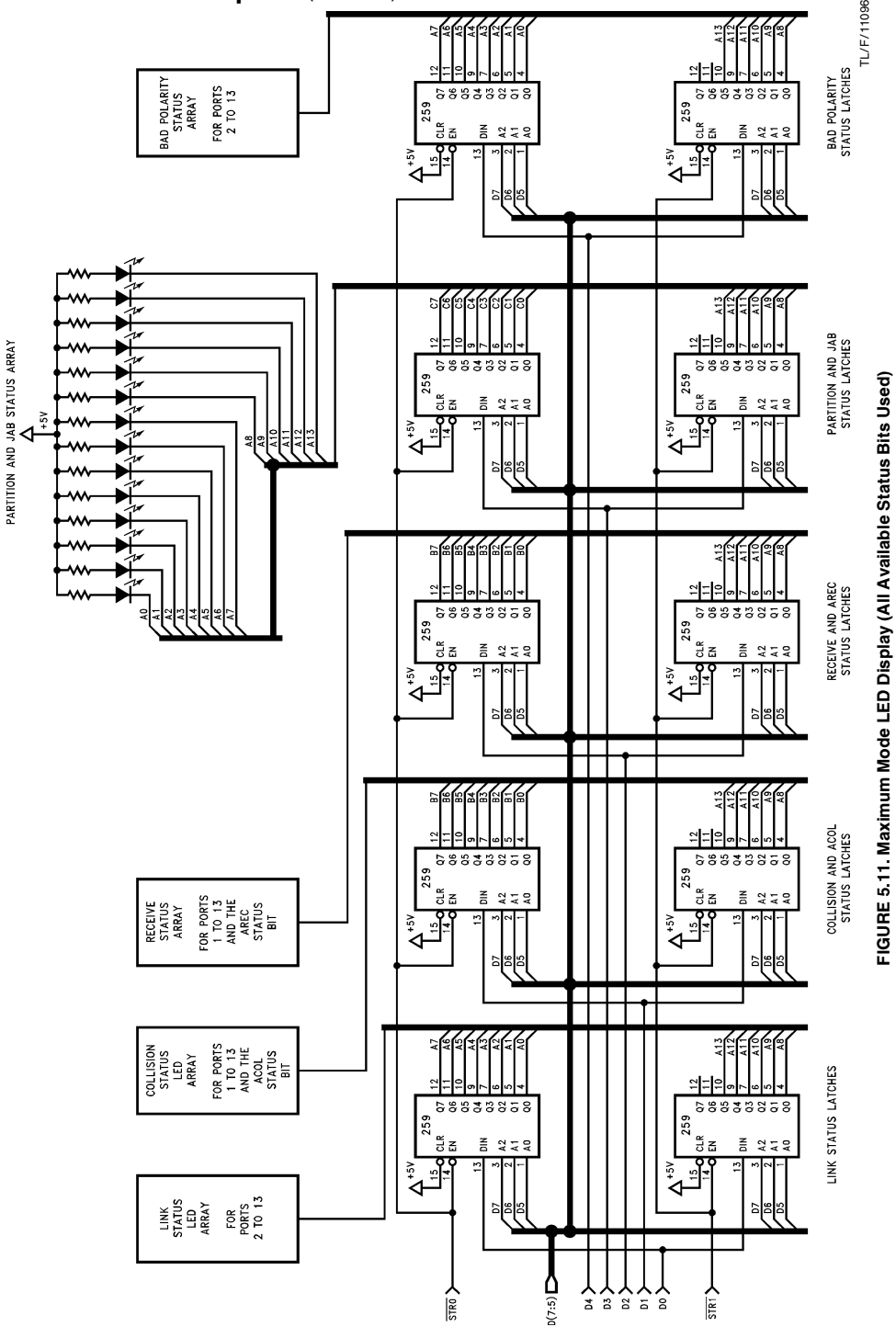


FIGURE 5.11. Maximum Mode LED Display (All Available Status Bits Used)

5.0 Functional Description (Continued)

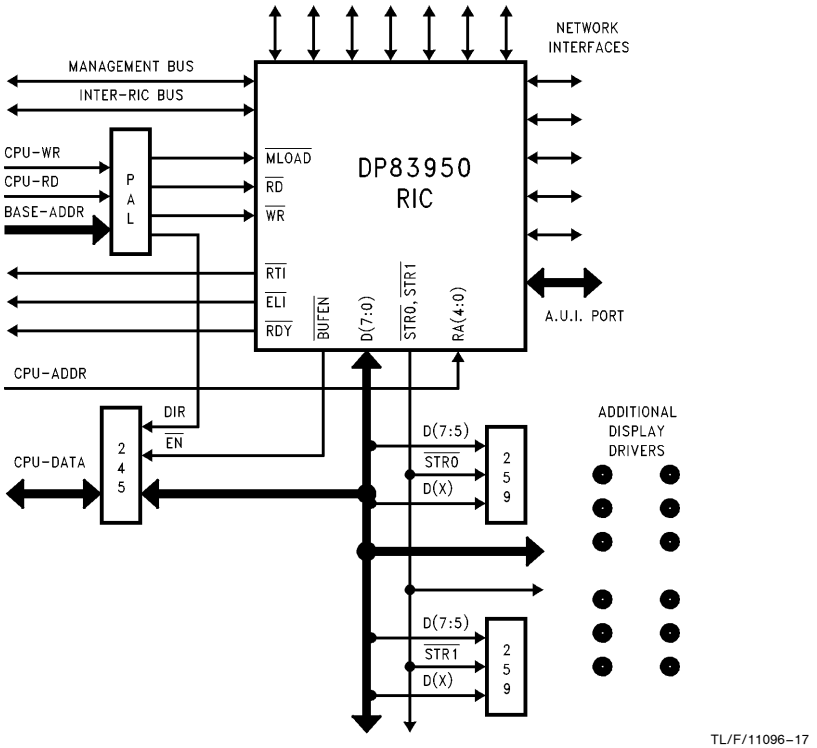


FIGURE 5.13. Processor Connection Diagram

5.0 Functional Description (Continued)

Processor Access Cycles

Access to the RIC's on-chip registers is made via its processor interface. This utilizes conventional non-multiplexed address (five bit) and data (eight bit) busses. The data bus is also used to provide data and address information to off chip display latches during display update cycles. While performing these cycles the RIC behaves as a master of its data bus. Consequently a TRI-STATE bi-directional bus transceiver, e.g., 74LS245 must be placed between the RIC and any processor bus.

The processor requests a register access by asserting the read "$\overline{RD}$" or write "$\overline{WR}$" input strobes. The RIC responds by finishing any current display update cycle and asserts the tri-state buffer enable signal "$\overline{BUFFEN}$". If the processor cycle is a write cycle then the RIC's data buffers are disabled to prevent contention. In order to interface to the RIC in a processor controlled system it is likely a PAL device will be used to perform the following operations:

1. Locate the RIC in the processor's memory map (address decode),
2. Generate the RIC's read and write strobes,
3. Control the direction signal for the 74LS245.

An example of the processor and display interfaces is shown in *Figure 5.13*.

6.0 Hub Management Support

The RIC provides information regarding the status of its ports and the packets it is repeating. This data is available in three forms:

1. Counted Events—Network events accumulated into the RIC's 16-bit Event Counter Registers.
2. Recorded Events—Network events that set bits in the Event Record Registers.
3. Hub Management Status Packets—This is information sent over the Management Bus in a serial function to be decoded by an Ethernet Controller board.

The counted and recorded event information is available through the processor interface. This data is port specific and may be used to generate interrupts via the Event Logging Interrupt "$\overline{ELI}$" pin. Since the information is specific to each port, each repeater port has its own event record register and event counter. The counters and event record registers have user definable masks which enable them to be configured to count and record a variety of events. The counters and record registers are designed to be used together so that detailed information, i.e., a count value can be held on-chip for a specific network condition, and more general information, i.e., certain types of events have occurred, may be retained in on-chip latches. Thus the user may configure the counters to increment upon a rapidly occurring event (most likely to be used to count collisions), and the record registers may log the occurrence of less frequent error conditions such as jabber protect packets.

6.1 EVENT COUNTING FUNCTION

The counters may increment upon the occurrence of one of the categories of event as described below.

Potential sources for Counter increment:

Jabber Protection (JAB): The port counter increments if the length of a received packet from its associated port, causes the repeater state machine to enter the jabber protect state.

Elasticity Buffer Error (ELBER): The port counter increments if a Elasticity Buffer underflow or overflow occurs during packet reception. The flag is held inactive if a collision occurs during packet reception or if a phase lock error, described below, has already occurred during the repetition of the packet.

Phase Lock Error (PLER): A phase lock error is caused if the phase lock loop decoder looses lock during packet reception. Phase lock onto the received data stream may or may not be recovered later in the packet and data errors may have occurred. This flag is held inactive if a collision occurs.

Non SFD Packet (NSFD): If a packet is received and the start of frame delimiter is not found, the port counter will increment. Counting is inhibited if the packet suffers a collision.

Out of Window Collision (OWC): The out of window collision flag for a port goes active when a collision is experienced outside of the network slot time.

Transmit Collision (TXCOL): The transmit collision flag for a port is enabled when a transmit collision is experienced by the repeater. Each port experiencing a collision under these conditions is said to have suffered a transmit collision.

Receive Collision (RXCOL): The receive collision flag for a port goes active when the port is the receive source of network activity and suffers a collision, provided no other network segments experience collision then the receive collision flag for the receiving port will be set.

Partition (PART): The port counter increments when a port becomes partitioned.

Bad Link (BDLNK): The port counter increments when a port is configured for 10BASE-T operation has entered the link lost state.

Short Event reception (SE): The port counter increments if the received packet is less than 74 bits long and no collision occurs during reception.

Packet Reception (REC): When a packet is received the port counter increments.

In order to utilize the counters the user must choose, from the above list, the desired statistic for counting. This counter mask information must be written to the appropriate, Event Count Mask Register. There are two of these registers, the Upper and Lower, Event Count Mask registers. For the exact bit patterns of these registers please see Section 8 of the data sheet.

For example if the counters are configured to count network collisions and the appropriate masks have been set, then whenever a collision occurs on a segment, this information is latched by the hub management support logic. At the end of repetition of the packet the collision status, respective to each port, is loaded into that port's counter. This operation is completely autonomous and requires no processor intervention.

6.0 Hub Management Support (Continued)

Each counter is 16 bits long and may be directly read by the processor. Additionally each counter has a number of decodes to indicate the current value of the count. There are three decodes:

Low Count (a value of 00FF Hex and under),
High Count (a value of C000 Hex and above),
Full Count (a value of FFFF Hex).

The decodes from each counter are logically ''ORed'' together and may be used as interrupt sources for the $\overline{ELI}$ interrupt pin. Additionally the status of these bits may be observed by reading the Page Select Register (PSR), (see Section 8 for register details). In order to enable any of these threshold interrupts, the appropriate interrupt mask bit must be written to the Management and Interrupt Configuration Register; see Section 8 for register details.

In addition to their event masking functions the Upper Event Counting Mask Register (UECMR) possesses two bits which control the operation of the counters. When written to a logic one, the reset on read bit ''ROR'' resets the counter after a processor read cycle is performed. If this operation is not selected then in order to zero the counters they must either be written with zeros by the processor or allowed to roll over to all zeros. The freeze when full bit ''FWF'' prevents counter roll over by inhibiting count up cycles (these happen when chosen events occur), thus freezing the particular counter at FFFF Hex.

The port event counters may also be controlled by the Counter Decrement ($\overline{CDEC}$) pin. As its name suggests a logic low state on this pin will decrement all the counters by a single value. The pulses on $\overline{CDEC}$ are internally synchronized and scheduled so as not to conflict with any ''up counting'' activity. If an up count and a down count occur simultaneously then the down count is delayed until the up count has completed. This combination of up and down counting capability enables the RIC's on-chip counters to provide a simple rolling average or be used as extensions of larger off chip counters.

Note: If the FWF option is enabled then the count down operation is disabled from those registers which have reached FFFF Hex and consequently have been frozen. Thus, if FWF is set and $\overline{CDEC}$ has been employed to provide a rate indication. A frozen counter indicates that a rate has been detected which has gone out of bounds, i.e., too fast increment or too slow increment. If the low count and high count decodes are employed as either interrupt sources or in a polling cycle, the direction of the rate excursion may be determined.

Reading the Event Counters

The RIC's external data bus is eight bits wide, since the event counters are 16 bits long two processor read cycles are required to yield the counter value. In order to ensure that the read value is correct and to allow simultaneous event counts with processor accesses, a temporary holding register is employed. A read cycle to either the lower or upper byte of a counter, causes both bytes to be latched into the holding register. Thus when the other byte of the counter is obtained the holding register is accessed and not the actual counter register. This ensures that the upper and lower bytes contain the value sampled at the same instance in time, i.e., when the first read cycle to that counter occurred.

There is no restriction concerning whether the upper or lower byte is read first. However to ensure the ''same instance value'' is obtained, the reads of the upper then lower byte (or vice versa) should be performed as consecutive reads of the counter array. Other NON COUNTER registers may be read in between these read cycles and also write cycles may be performed. If another counter is read or the same byte of the original counter is read, then the holding register is updated from the counter array and the unread byte is lost.

If the reset on read option is employed then the counter is reset after the transfer to the holding register is performed. Processor read and write cycles are scheduled in such a manner that they do not conflict with count up or count down operations. That is to say, in the case of a processor read the count value is stable when it is loaded into the holding register. In the case of a processor write, the newly written value is stable so it maybe incremented or decrement by any subsequent count operation. During the period the $\overline{MLOAD}$ pin is low, (power on reset) all counters are reset to zero and all count masks are forced into the disabled state. Section 8 of the data sheet details the address location of the port event counters.

6.2 EVENT RECORD FUNCTION

As previously stated each repeater port has its own Event Recording Register. This is an 8-bit status register each bit is dedicated to logging the occurrence of a particular event (see Section 8 for detailed description). The logging of these events is controlled by the Event Recording Mask Register, for an event to be recorded the particular mask bit must be set, (see Section 8 description of this register). Similar to the scheme employed for the event counters, the recorded events are latched during the repetition of a packet and then automatically loaded into the recording registers at the end of transmission of a packet. When one of the unmasked events occurs, the particular port register bit is set. This status is visible to the user. All of the register bits for all of the ports are logically ''ORed'' together to produce a Flag Found ''FF'' signal. This indicator may be found by reading the Page Select Register. Additionally an interrupt may be generated if the appropriate mask bit is enabled in the Management and Interrupt Configuration Register.

A processor read cycle to a Event Record Register resets any of the bits set in that register. Read operations are scheduled to guarantee non changing data during a read cycle. Any internal bit setting event which immediately follows a processor read will be successful. The events which may be recorded are described below:

Jabber Protection (JAB): This flag goes active if the length of a received packet from the relevant port, causes the repeater state machine to enter the Jabber Protect state.

Elasticity Buffer Error (ELBER): This condition occurs if an Elasticity Buffer full or overflow occurs during packet reception. The flag is held inactive if a collision occurs during packet reception or if a phase lock error has already occurred during the repetition of the packet.

Phase Lock Error (PLER): A phase lock error is caused if the phase lock loop decoder loses lock during packet reception. Phase lock onto the received data stream may or may not be recovered later in the packet and data errors may have occurred. This flag is held inactive if a collision occurs.

Non SFD Packet (NSFD): If a packet is received and the start of frame delimiter is not found, the flag will go active. The flag is held inactive if a collision occurs in during packet repetition.

6.0 Hub Management Support (Continued)

Out of Window Collision (OWC): The out of window collision flag for a port goes active when a collision is experienced outside of the network slot time.

Partition (PART): This flag goes active when a port becomes partitioned.

Bad Link (BDLNK): The flag goes active when a port is configured for 10BASE-T operation has entered the link lost state.

Short Event reception (SE): This flag goes active if the received packet is less than 74 bits long and no collision occurs during reception.

6.3 MANAGEMENT INTERFACE OPERATION

The HUB Management interface provides a mechanism to combine repeater status information with packet information to form a hub management status packet. The interface, a serial bus consisting of carrier sense, received clock and received data, is designed to connect one or multiple RIC's over a backplane bus to a DP83932 ''SONIC'' network controller. The SONIC and the RICs form a powerful entity for network statistics gathering.

The interface consists of four pins:

MRXC	Management Receive Clock—10 MHz NRZ Clock output.
MCRS	Management Carrier Sense—Input/Output indicating of valid data stream.
MRXD	Management Receive Data—NRZ Data output synchronous to MRXC.
$\overline{\text{PCOMP}}$	Packet Compress—Input to truncate the packet's data field.

The first three signals mimic the interface between an Ethernet controller and a phase locked loop decoder (specifically the DP83932 SONIC and DP83910 SNI), these signals are driven by the RIC receiving the packet. MRXC and MRXD compose an NRZ serial data stream compatible with the DP83932. The $\overline{\text{PCOMP}}$ signal is driven by logic on the processor board. The actual data stream transferred over MRXD is derived from data transferred over the IRD Inter-RIC bus line. These two data streams differ in two important characteristics:

1. At the end of packet repetition a hub management status field is appended to the data stream. This status field, consisting of 7 bytes is shown in *Figure 6.1* and *6.2*. The information field is obtained from a number of packet status registers described below. In common with the 802.3 protocol the least significant bit of a byte is transmitted first.
2. While the data field of the repeated packet is being transferred over the management bus, received clock signals on the MRXC pin may be inhibited. This operation is under the control of the Packet Compress pin $\overline{\text{PCOMP}}$. If $\overline{\text{PCOMP}}$ is asserted during repetition of the packet then MRXC signals are inhibited when the number of bytes (after SFD) transferred over the management bus equals the number indicated in the Packet Compress Decode Register. This register provides a means to delay the effect of the $\overline{\text{PCOMP}}$ signal, which may be generated early in the packet's repetition, until the desired moment. Packet compression may be used to reduce the amount of memory required to buffer packets when they are received and are waiting to be processed by hub management software. In this kind of application an address decoder, which forms part of the packet compress logic, would monitor the address fields as they are received over the management bus. If the destination address is not the address of the management node inside the hub, then packet compression could be employed. In this manner only the portion of the packet meaningful for hub management interrogation, i.e., the address fields, is transferred to the SONIC and is buffered in memory.

   If the repeated packet ends before $\overline{\text{PCOMP}}$ is asserted or before the required number of bytes have been transferred, then the hub management status field is directly appended to the received data at a byte boundary. If the repeated packet is significantly longer than the value in the Decode Register requires and $\overline{\text{PCOMP}}$ is asserted the status fields will be delayed until the end of packet repetition. During this delay period MRXC clocks are inhibited but the MCRS signal remains asserted.

Note: If $\overline{\text{PCOMP}}$ is asserted late in the packet, i.e., after the number of bytes defined by the packet compression register, then packet compression will not occur.

The Management Interface may be fine tuned to meet the timing consideration of the SONIC and the access time of its associated packet memory. This refinement may be performed in two ways:

1. The default mode of operation of the Management interface is to only transfer packets over the bus which have a start of frame delimiter. Thus ''packets'' that are only preamble/jam and do not convey any source or destination address information are inhibited. This filtering may be disabled by writing a logic zero to the Management Interface Configuration or ''MIFCON'' bit in the Management and Interrupt Configuration Register. See Section 8 for details.
2. The Management bus has been designed to accommodate situations of maximum network utilization, for example when collision generated fragments occur; (these collision fragments may violate the IEEE802.3 IFG specification). The IFG required by the SONIC is a function of the time taken to release space in the receive FIFO and to perform end of packet processing (write status information into memory). These functions are primarily memory operations and consequently depend upon the bus latency and the memory access time of the system. In order to allow the system designer some discretion in choosing the speed of this memory, the RIC may be configured to protect the SONIC from a potential FIFO overflow. This is performed by utilizing the Inter Frame Gap Threshold Select Register.

   The value held in this register, plus one, defines, in network bit times, the minimum allowed gap between frames on the management bus. If the gap is smaller than this number then MCRS is asserted but MRXC clocks are inhibited. Consequently no data transfer is performed.

   Thus the system designer may make the decision whether to gather statistics on all packets even if they occur with very small IFGs or to monitor a subset.

The status field, shown in *Figure 6.1*, contains information which may be conveniently analyzed by considering it as

6.0 Hub Management Support (Continued)

providing information of six different types. They are held in seven Packet Status Registers ''PSRs'':

1. The RIC and port address fields [PSR(0) and (1)] can uniquely identify the repeater port receiving the packet out of a potential maximum of 832 ports sharing the same management bus (64 RICs each with 13 ports). Thus all of the other status fields can be correctly attributed to the relevant port.
2. The status flags the RIC produces for the event counters or recording latches are supplied with each packet [PSR(2)]. Additionally the clean receive CLN status is supplied to allow the user to determine the reliability of the address fields in the packet. The CLN status bit [PSR(1)] is set if no collisions are experienced during the repetition of the address fields.
3. The RIC has an on-chip timer to indicate when, relative to the start of packet repetition, a collision, if any, occurred [PSR(3)]. There is also a timer which indicates how many bit times of IFG was seen on the network between repetition of this packet and the preceding one. This is provided by [PSR(6)].
4. If packet compression is employed, the receive byte count contained in the SONIC's packet descriptor will indicate the number of bytes transferred over the management bus rather than the number of bytes in the packet. For this reason the RIC which receives the packet, counts the number of received bytes and transfers this over the management bus [PSR(4), (5)].
5. Appending a status field to a data packet will obviously result in a CRC error being flagged by the SONIC. For this reason the RIC monitors the repeated data stream to check for CRC and FAE errors. In the case of FAE errors the RIC provides additional dummy data bits, so that the status fields are always byte aligned.
6. As a final check upon the effectiveness of the management interface, the RIC transfers a bus specific status bit to the SONIC. This flag Packet Compress Done PCOMPD [PSR(0)], may be monitored by hub management software to check if the packet compression operation is enabled.

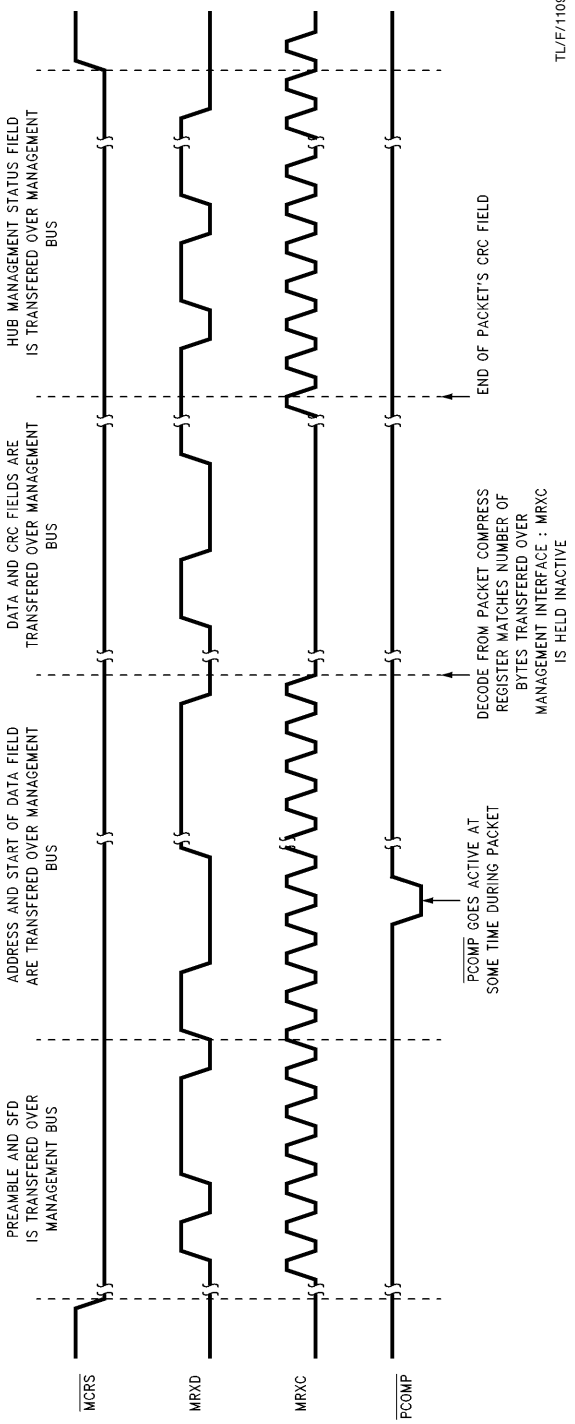
Figure 6.2 shows an example of a packet being transmitted over the management bus. The first section of the diagram (moving from left to right) shows a short preamble and SFD pattern. The second region contains the packet's address and the start of the data fields. During this time logic on the processor/SONIC card would determine if packet compression should be used on this packet. The $\overline{\text{PCOMP}}$ signal is asserted and packet transfer stops when the number of bytes transmitted equals the value defined in the decode register. Hence the MRXC signal is idle for the remainder of the packet's data and CRC fields. The final region shows the transfer of the RIC's seven bytes of packet status.

The following pages describe these Hub Management registers which constitute the management status field.

Packet Status Register PSR	D7	D6	D5	D4	D3	D2	D1	D0
PSR(0)	A5	A4	A3	A2	A1	A0	PCOMPD	TXCOL
PSR(1)	CRCER	FAE	COL	CLN	PA3	PA2	PA1	PA0
PSR(2)	SE	OWC	NSFD	PLER	ELBER	JAB	CBT9	CBT8
PSR(3) Collision Bit Timer	CBT7	CBT6	CBT5	CBT4	CBT3	CBT2	CBT1	CBT0
PSR(4) Lower Repeat Byte Count	RBY7	RBY6	RBY5	RBY4	RBY3	RBY2	RBY1	RBY0
PSR(5) Upper Repeat Byte Count	RBY15	RBY14	RBY13	RBY12	RBY11	RBY10	RBY9	RBY8
PSR(6) Inter Frame Gap Bit Timer	IBT7	IBT6	IBT5	IBT4	IBT3	IBT2	IBT1	IBT0

Note: These registers may only be reliably accessed via the management interface. Due to the nature of these registers they may not be accessed (read or write cycles) via the processor interface.

FIGURE 6.1. Hub Management Status Field



Note: In this example the Management Bus is configured to use active low signals.

FIGURE 6.2. Operation of the Management Bus

6.0 Hub Management Support (Continued)

Packet Status Register 0

D7	D6	D5	D4	D3	D2	D1	D0
A5	A4	A3	A2	A1	A0	PCOMPD	resv

Bit	Symbol	Description
D0	resv	**RESERVED FOR FUTURE USE:** This bit is currently undefined, management software should not examine the state of this bit.
D1	PCOMPD	**PACKET COMPRESSION DONE:** If packet compression is utilized, this bit informs the user that compression was performed, i.e., the packet was long enough to require compression.
D(7:2)	A(5:0)	**RIC ADDRESS (5:0):** This address is defined by the user and is supplied when writing to the RIC Address Register. It is used by hub management software to distinguish between RICs in a multi-RIC system.

Packet Status Register 1

D7	D6	D5	D4	D3	D2	D1	D0
CRCER	FAE	COL	CLN	PA3	PA2	PA1	PA0

Bit	Symbol	Description
D(3:0)	PA(3:0)	**PORT ADDRESS:** This field defines the port which is receiving the packet.
D4	CLN	**CLEAN RECEIVE:** This bit is asserted from the start of reception, and is deasserted if a collision occurs within a window from the start of reception to the end of the 13th byte after SFD detection. If no SFD is detected the window is extended to the end of reception.
D5	COL	**COLLISION:** If a receive or transmit collision occurs during packet repetition the collision bit is asserted.
D6	FAE	**FRAME ALIGNMENT ERROR:** This bit is asserted if a Frame Alignment Error occurred in the repeated packet.
D7	CRCER	**CRC ERROR:** This bit is asserted if a CRC Error occurred in the repeated packet. This status flag should not be tested if the COL bit is asserted since the error may be simply due to the collision.

6.0 Hub Management Support (Continued)

Packet Status Register 2

D7	D6	D5	D4	D3	D2	D1	D0
SE	OWC	NSFD	PLER	ELBER	JAB	CBT9	CBT8

Bit	Symbol	Description
D(1:0)	CT(9:8)	**COLLISION TIMER BITS 9 AND 8:** These two bits are the upper bits of the collision bit timer.
D2	JAB	**JABBER EVENT:** This bit indicates that the receive packet was so long the repeater was forced to go into a jabber protect condition.
D3	ELBER	**ELASTICITY BUFFER ERROR:** During the packet an Elasticity Buffer under/overflow occurred.
D4	PLER	**PHASE LOCK LOOP ERROR:** The packet suffered sufficient jitter/noise corruption to cause the phase lock loop decoder to lose lock.
D5	NSFD	**NON SFD:** The repeated packet did not contain a Start of Frame Delimiter. When this bit is set the Repeat Byte Counter counts the length of the entire packet. When this bit is not set the byte counter only counts post SFD bytes. **Note:** The operation of this bit is not inhibited by the occurrence of a collision during packet repetition (see description of the Repeat Byte Counter below).
D6	OWC	**OUT OF WINDOW COLLISION:** The packet suffered an out of window collision.
D7	SE	**SHORT EVENT:** The receive activity was so small it met the criteria to be classed as a short event.

The other registers comprise the remainder of the collision timer register [PSR(3)], the Repeat Byte Count registers [PSR(4), (5)], and the Inter Frame Gap Counter ''IFG'' register [PSR(6)].

Collision Bit Timer

The Collision Timer counts in bit times the time between the start of repetition of the packet and the detection of the packet's first collision. The Collision counter increments as the packet is repeated and freezes when a collision occurs. The value in the counter is only valid when the collision bit ''COL'' in [PSR(1)] is set.

Repeat Byte Counter

The Repeat Byte Counter is a 16 bit counter which can perform two functions. In cases where the transmitted packet possesses an SFD, the byte counter counts the number of received bytes after the SFD field. Alternatively if no SFD is repeated the counter reflects the length of the packet, counted in bytes, starting at the beginning of the preamble field. When performing the latter function the counter is shortened to 7 bits. Thus the maximum count value is 127 bytes. The mode of counting is indicated by the ''NSFD'' bit in [PSR(2)]. In order to check if the received packet was genuinely a Non-SFD packet, the status of the COL bit should be checked. During collisions SFD fields may be lost or created, Management software should be robust to this kind of behaviour.

Inter Frame Gap (IFG) Bit Timer

The IFG counter counts in bit times the period in between repeater transmissions. The IFG counter increments whenever the RIC is not transmitting a packet. If the IFG is long, i.e., greater than 255 bits the counter sticks at this value. Thus an apparent count value of 255 should be interpreted as 255 or more bit times.

6.4 DESCRIPTION OF HARDWARE CONNECTION FOR MANAGEMENT INTERFACE

The RIC has been designed so it may be connected to the Management bus directly or via external bus transceivers. The latter is advantageous in large repeaters. In this application the system backplane is often heavily loaded beyond the drive capabilities of the on-chip bus drivers.

The uni-directional nature of information transfer on the MCRS, MRXD and MRXC signals, means a single open drain output pin is adequate for each of these signals. The Management Enable (MEN) RIC output pin performs the function of a drive enable for an external bus transceiver if one is required.

In common with the Inter-RIC bus signals ACTN, ANYXN, COLN and IRE the MCRS active level asserted by the MCRS output is determined by the state of the BINV Mode Load configuration bit.

7.0 Port Block Functions

The RIC has 13 port logic blocks (one for each network connection). In addition to the packet repetition operations already described, the port block performs two other functions:

1. The physical connection to the network segment (transceiver function).
2. It provides a means to protect the network from malfunctioning segments (segment partition).

Each port has its own status register. This register allows the user to determine the current status of the port and configure a number of port specific functions.

7.0 Port Block Functions (Continued)

7.1 TRANSCEIVER FUNCTIONS

The RIC may connect to network segments in three ways:

1. Over AUI cable to transceiver boxes,

2. Directly to board mounted transceivers,

3. To twisted pair cable via a simple interface.

The first method is only supported by RIC port 1 (the AUI port). Options (2) and (3) are available on ports 2 to 13. The selection of the desired option is made at device initialization during the Mode Load operation. The Transceiver Bypass XBYPAS configuration bits are used to determine whether the ports will utilize the on-chip 10BASE-T transceiver or bypass these in favour of external transceivers. Four possible combinations of port utilization are supported:

All ports (2 to 13) use the external Transceiver Interface.

Ports 2 to 5 use the external interface, 6 to 13 use the internal 10BASE-T transceivers.

Ports 2 to 7 use the external interface, 8 to 13 use the internal 10BASE-T transceivers.

All ports (2 to 13) use the internal 10BASE-T transceivers.

10BASE-T Transceiver Operation

The RIC contains virtually all the digital and analog circuits required for connection to 10BASE-T network segments. The only additional active component is an external driver packet. The connection for a RIC port to a 10BASE-T segment is shown in *Figure 7.1*. The diagram shows the components required to connect one of the RIC's ports to a 10BASE-T segment. The major components are the driver package, a member of the 74ACT family, and an integrated filter/choke network.

The operation of the 10BASE-T transceiver's logical functions may be modified by software control. The default mode of operation is for the transceivers to transmit and expect reception of link pulses. This may be modified if a logic one is written to the $\overline{\text{GDLNK}}$ bit of a port's status register. The port's transceiver will operate normally but will not transmit link pulses nor monitor their reception. Thus the entry to a link fail state and the associated modification of transceiver operation will not occur.

The on-chip 10BASE-T transceivers automatically detect and correct the polarity of the received data stream. This polarity detection scheme relies upon the polarity of the received link pulses and the end of the packet waveform. Polarity detection and correction may be disabled under software control as follows:

1) Write the value 07H to the Page Select Register (address 10H).

2) Write the value 02H to the address 11H. (Note that address 11H will read back 00H after writing 02H to it).

This is the only exception for accessing any of the reserved pages 4 to 7.

External Transceiver Operation

RIC ports 2 to 13 may be connected to media other than twisted-pair by opting to bypass the on-chip transceivers. When using external transceivers the user must have the external transceivers perform collision detection and the other functions associated with an IEEE 802.2 Media Access Unit. *Figure 7.2* shows the connection between a repeater port and a coaxial transceiver using the AUI type interface.

7.2 SEGMENT PARTITION

Each of the RIC's ports has a dedicated state machine to perform the functions defined by the IEEE partition algorithm as shown in *Figure 7.3*. To allow users to customize this algorithm for different applications a number of user selected options are available during device configuration at power up (the Mode Load Cycle).

Five different options are provided:

1. Operation of the 13 partition state machines may be disabled via the disable partition $\overline{\text{DPART}}$ configuration bit (Pin D6).

2. The value of consecutive counts required to partition a segment (the CCLimit specification) may be set at either 31 or 63 consecutive collisions.

3. The use of the TW5 specification in the partition algorithm differentiates between collisions which occur early in a packet (before TW5 has elapsed) and those which occur late in the packet (after TW5 has elapsed). These late or ''out of window'' collisions can be regarded in the same manner as early collisions if the Out of Window Collision Enable $\overline{\text{OWCE}}$ option is selected. This configuration bit is applied to the D4 pin during the Mode Load operation. The use of $\overline{\text{OWCE}}$ delays until the end of the packet the operation of the state diagram branch marked (1) and enables the branch marked (2) in *Figure 7.3*.

4. The operation of the ports' state machines when reconnecting a segment may also be modified by the user. The Transmit Only $\overline{\text{TXONLY}}$ configuration bit allows the user to prevent segment reconnection unless the reconnecting packet is being sourced by the repeater. In this case the repeater is transmitting on to the segment, rather than the segment transmitting when the repeater is idle. The normal mode of reconnection does not differentiate between such packets. The $\overline{\text{TXONLY}}$ configuration bit is input on Pin D5 during the Mode Load cycle. If this option is selected the operation of the state machine branch marked (3) in *Figure 7.3* is affected.

5. The RIC may be configured to use an additional criterion for segment partition. This is referred to as loop back partition. If this operation is selected the partition state machine monitors the receive and collision inputs from a network segment to discover if they are active when the port is transmitting. Thus determining if the network transceiver is looping back the data pattern from the cable. A port may be partitioned if no data or collision signals are seen by the partition logic in the following window: 61 to 96 network bit times after the start of transmission see data sheet Section 8 for details. A segment partitioned by this operation may be reconnected in the normal manner.

In addition to the autonomous operation of the partition state machines, the user may reset these state machines. This may be done individually to each port by writing a logic one to the $\overline{\text{PART}}$ bit in its status register. The port's partition state machine and associated counters are reset and the port is reconnected to the network. The reason why a port become partitioned may be discovered by the user by reading the port's status register.

7.0 Port Block Functions (Continued)

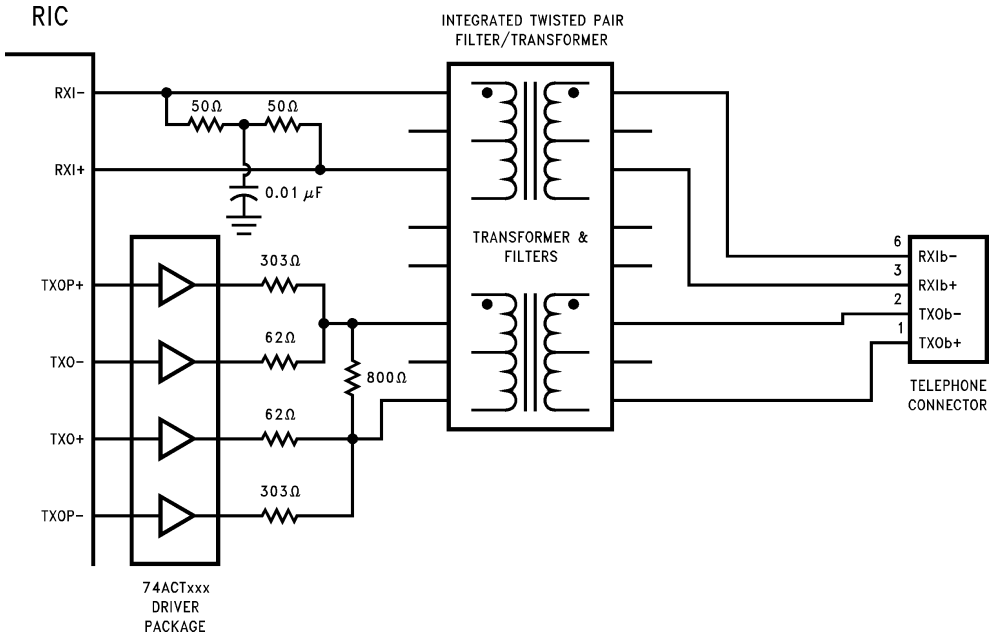
7.3 PORT STATUS REGISTER FUNCTIONS

Each RIC port has its own status register. In addition to providing status concerning the port and its network segment the register allows the following operations to be performed upon the port:

1. Port disable
2. Link Disable
3. Partition reconnection
4. Selection between normal and reduced squelch levels

Note that the link disable and port disable functions are mutually exclusive functions, i.e., disabling link does not affect receiving and transmitting from/to that port and disabling a port does not disable link.

When a port is disabled packet transmission and reception between the port's segment and the rest of the network is prevented.



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Note: For recommended modules, see "Ethernet Magnetics Vendors for 10BASE-T, 10BASE2, and 10BASE5" in Section 5 of this Databook.

FIGURE 7.1. Port Connection to a 10BASE-T Segment

7.0 Port Block Functions (Continued)

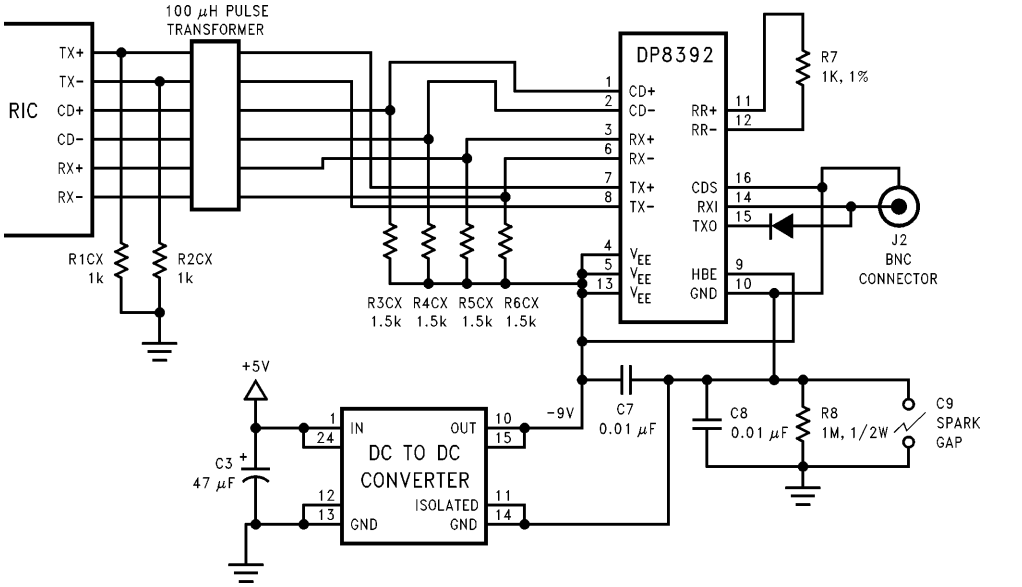

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FIGURE 7.2. Port Connection to a 10BASE2 Segment (AUI Interface Selected)

The preceding diagrams show a RIC port (Numbers 2 to 13) connected to a 10BASE-T and a 10BASE2 segment. The values of any components not indicated above are to be determined.

7.0 Port Block Functions (Continued)

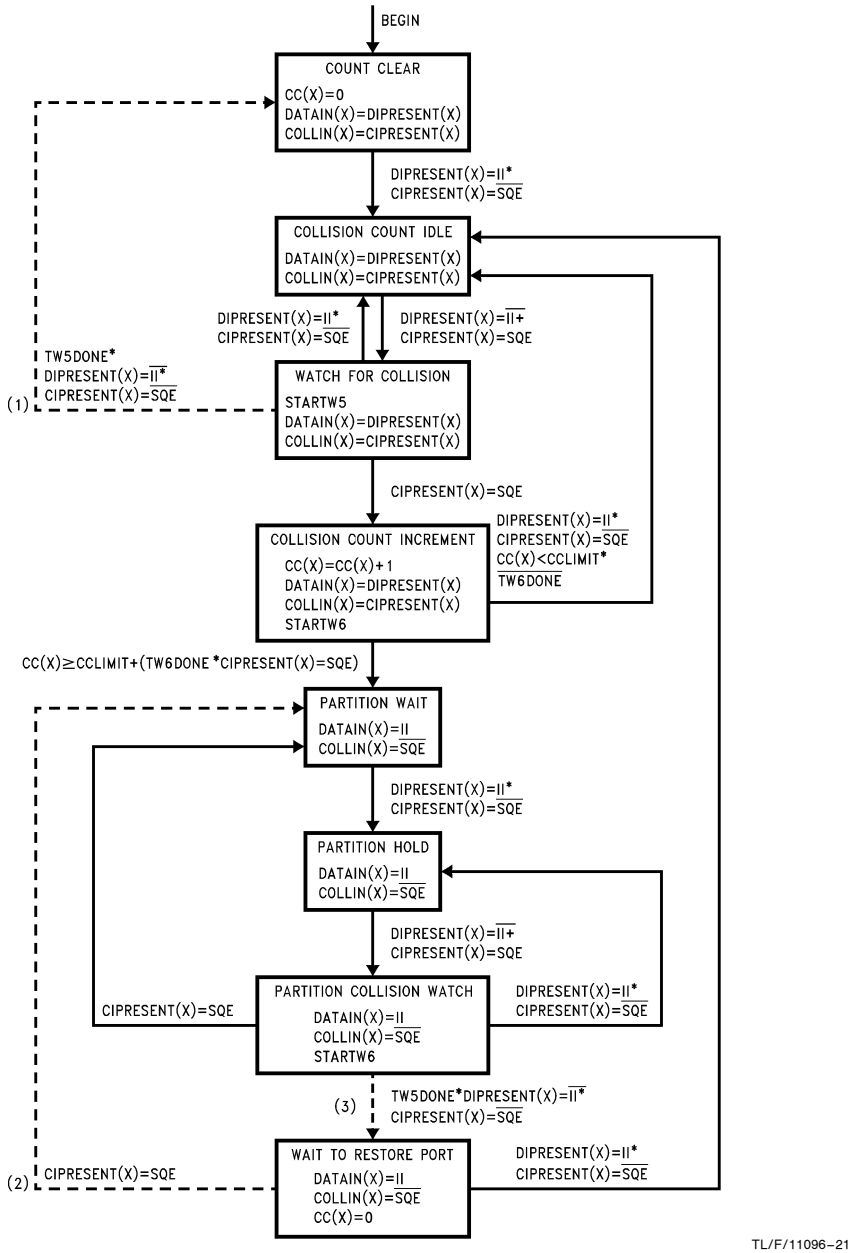


FIGURE 7.3. IEEE Segment Partition Algorithm

8.0 RIC Registers

RIC Register Address Map

The RIC's registers may be accessed by applying the required address to the five Register Address (RA(4:0)) input pins. Pin RA4 makes the selection between the upper and lower halves of the register array. The lower half of the register map consists of 16 registers:

1 RIC Real Time Status and Configuration register,
13 Port Real Time Status registers,
1 RIC Configuration Register
1 Real Time Interrupt Status Register.

These registers may be directly accessed at any time via the RA(4:0) pins, (RA4 = 0). The upper half of the register map, (RA4 = 1), is organized as 4 pages of registers:

Event Count Configuration page (0),
Event Record page (1),
Lower Event Count page (2)
Upper Event Count page (3)

Register access within these pages is also performed using the RA(4:0) pins, (RA4 = 1). Page switching is performed by writing to the Page Selection bits (PSEL2, 1, 0). These bits are found in the Page Select Register, located at address 10 hex on each page of the upper half of the register array. AT power on these bits default to 0 Hex, i.e., page zero.

8.0 RIC Registers (Continued)

Register Memory Map

Address	Name			
	Page (0)	Page (1)	Page (2)	Page (3)
00H	RIC Status and Configuration Register			
01H	Port 1 Status Register			
02H	Port 2 Status Register			
03H	Port 3 Status Register			
04H	Port 4 Status Register			
05H	Port 5 Status Register			
06H	Port 6 Status Register			
07H	Port 7 Status Register			
08H	Port 8 Status Register			
09H	Port 9 Status Register			
0AH	Port 10 Status Register			
0BH	Port 11 Status Register			
0CH	Port 12 Status Register			
0DH	Port 13 Status Register			
0EH	RIC Configuration Register			
0FH	Real Time Interrupt Register			
10H	Page Select Register			
11H	Device Type Register	Port 1 Event Record Register (ERR)		
12H	Lower Event Count Mask Register (ECMR)	Port 2 ERR	Port 1 Lower Event Count Register (ECR)	Port 8 Lower ECR
13H	Upper ECMR	Port 3 ERR	Port 1 Upper ECR	Port 8 Upper ECR
14H	Event Record Mask Register	Port 4 ERR	Port 2 Lower ECR	Port 9 Lower ECR
15H	resv	Port 5 ERR	Port 2 Upper ECR	Port 9 Upper ECR
16H	Management/Interrupt Configuration Register	Port 6 ERR	Port 3 Lower ECR	Port 10 Lower ECR
17H	RIC Address Register	Port 7 ERR	Port 3 Upper ECR	Port 10 Upper ECR
18H	Packet Compress Decode Register	Port 8 ERR	Port 4 Lower ECR	Port 11 Lower ECR
19H	resv	Port 9 ERR	Port 4 Upper ECR	Port 11 Upper ECR
1AH	resv	Port 10 ERR	Port 5 Lower ECR	Port 12 Lower ECR
1BH	resv	Port 11 ERR	Port 5 Upper ECR	Port 12 Upper ECR
1CH	resv	Port 12 ERR	Port 6 Lower ECR	Port 13 Lower ECR
1DH	resv	Port 13 ERR	Port 6 Upper ECR	Port 13 Upper ECR
1EH	resv		Port 7 Lower ECR	
1FH	IFG Threshold		Port 7 Upper ECR	

Note: All registers marked resv on pages 0 to 3 must not be accessed by the user. The other register pages, 4 to 7, are also reserved.

8.0 RIC Registers (Continued)

Register Array Bit Map Addresses 00H to 10H

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	BINV	BYPAS2	BYPAS1	$\overline{\text{APART}}$	$\overline{\text{JAB}}$	$\overline{\text{AREC}}$	$\overline{\text{ACOL}}$	resv
01 to 0D	DISPT	SQL	PTYPE1	PTYPE0	$\overline{\text{PART}}$	$\overline{\text{REC}}$	$\overline{\text{COL}}$	$\overline{\text{GDLNK}}$
0E	MINMAX	$\overline{\text{DPART}}$	$\overline{\text{TXONLY}}$	$\overline{\text{OWCE}}$	$\overline{\text{LPPART}}$	$\overline{\text{CCLIM}}$	Tw2	resv
0F	IVCTR3	IVCTR2	IVCTR1	IVCTR0	ISRC3	ISRC2	ISRC1	ISRC0

Register Array Bit Map Addresses 10H to 1FH Page (0)

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
10	FC	HC	LC	FF	resv	PSEL2	PSEL1	PSEL0
11	0	0	0	0	0	0	0	0
12	BDLNKC	PARTC	RECC	SEC	NSFDC	PLERC	ELBERC	JABC
13	resv	resv	OWCC	RXCOLC	TXCOLC	resv	FWF	ROR
14	BDLNKE	PARTE	OWCE	SEE	NSFDE	PLERE	ELBERE	JABE
16	$\overline{\text{IFC}}$	$\overline{\text{IHC}}$	$\overline{\text{ILC}}$	$\overline{\text{IFF}}$	$\overline{\text{IREC}}$	$\overline{\text{ICOL}}$	$\overline{\text{IPART}}$	MIFCON
17	A5	A4	A3	A2	A1	A0	resv	resv
18	PCD7	PCD6	PCD5	PCD4	PCD3	PCD2	PCD1	PCD0
1F	IFGT7	IFGT6	IFGT5	IFGT4	IFGT3	IFGT2	IFGT1	IFGT0

Register Array Bit Map Addresses 10H to 1FH Page (1)

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
10	FC	HC	LC	FF	resv	PSEL2	PSEL1	PSEL0
11 to 1D	BDLNK	PART	OWC	SE	NSFD	PLER	ELBER	JAB

Register Array Bit Map Addresses 10H to 1FH Pages (2) and (3)

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
10	FC	HC	LC	FF	resv	PSEL2	PSEL1	PSEL0
11	—	—	—	—	—	—	—	—
Even Locations	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
Odd Locations	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8

8.0 RIC Registers (Continued)

RIC Status and Configuration Register (Address 00H)

The lower portion of this register contains real time information concerning the operation of the RIC. The upper three bits represent the chosen configuration of the transceiver interface employed.

D7	D6	D5	D4	D3	D2	D1	D0
BINV	BYPAS2	BYPAS1	$\overline{\text{APART}}$	$\overline{\text{JAB}}$	$\overline{\text{AREC}}$	$\overline{\text{ACOL}}$	resv

Bit	R/W	Symbol Access	Description
D0	R	resv	**RESERVED FOR FUTURE USE:** Reads as a logic 0.
D1	R	$\overline{\text{ACOL}}$	**ANY COLLISIONS:** 0: A collision is occurring at one or more of the RIC's ports. 1: No collisions.
D2	R	$\overline{\text{AREC}}$	**ANY RECEIVE:** 0: One of the RIC's ports is the current packet or collision receiver. 1: No packet or collision reception within this RIC.
D3	R	$\overline{\text{JAB}}$	**JABBER PROTECT:** 0: The RIC has been forced into jabber protect state by one of its ports or by another port on the Inter-RIC bus, (Multi-RIC operations). 1: No jabber protect conditions exist.
D4	R	$\overline{\text{APART}}$	**ANY PARTITION:** 0: One or more ports are partitioned. 1: No ports are partitioned.
D5	R	BYPAS1	These bits define the configuration of ports 2 to 13 i.e., their use if the internal 10BASE-T transceivers or the external (AUI-like) transceiver interface.
D6	R	BYPAS2	
D7	R	BINV	**BUS INVERT:** This register bit informs whether the Inter-RIC signals: IRE, ACTN, ANYXN, COLN and Management bus signal MCRS are active high or low. 0: Active high 1: Active low

8.0 RIC Registers (Continued)

Port Real Time Status Registers (Address 01H to 0DH)

D7	D6	D5	D4	D3	D2	D1	D0
DISPT	EGP	PTYPE1	PTYPE0	$\overline{\text{PART}}$	$\overline{\text{REC}}$	$\overline{\text{COL}}$	$\overline{\text{GDLNK}}$

Bit	R/W	Symbol	Description
D0	R/W	$\overline{\text{GDLNK}}$	**GOOD LINK:** 0: Link pulses are being received by the port. 1: Link pulses are not being received by the port logic. **Note:** Writing a 1 to this bit will cause the 10BASE-T transceiver not the transmit or monitor the reception of link pulses. If the internal 10BASE-T transceivers are not selected or if port 1 (AUI port) is read, then this bit is undefined.
D1	R	$\overline{\text{COL}}$	**COLLISION:** 0: A collision is happening or has occurred during the current packet. 1: No collisions have occurred as yet during this packet.
D2	R	$\overline{\text{REC}}$	**RECEIVE:** 0: This port is now or has been the receive source of packet or collision information for the current packet. 1: This port has not been the receive source during the current packet.
D3	R/W	$\overline{\text{PART}}$	**PARTITION:** 0: This port is partitioned. 1: This port is not partitioned. Writing a logic one to this bit forces segment reconnection and partition state machine reset. Writing a zero to this bit has no effect.
D(5, 4)	R	PTYPE0 PTYPE1	**PARTITION TYPE 0** **PARTITION TYPE 1** The partition type bits provide information specifying why the port is partitioned.

PTYPE1	PTYPE0	Information
0	0	Consecutive Collision Limit Reached
0	1	Excessive Length of Collision Limit Reached
1	0	Failure to See Data Loopback from Transceiver in Monitored Window
1	1	Processor Forced Reconnection

D6	R/W	SQL	**SQUELCH LEVEL:** 0: Port operates with normal IEEE receive squelch level. 1: Port operates with reduced receive squelch level. Note: This bit has no effect when the external transceiver is selected.
D7	R/W	DISPT	**DISABLE PORT:** 0: Port operates as defined by repeater operations. 1: All port activity is prevented.

8.0 RIC Registers (Continued)

RIC Configuration Register (Address 0EH)

This register displays the state of a number of RIC configuration bits loaded during the Mode Load operation.

D7	D6	D5	D4	D3	D2	D1	D0
MINMAX	$\overline{\text{DPART}}$	$\overline{\text{TX ONLY}}$	$\overline{\text{OWCE}}$	$\overline{\text{LPPART}}$	$\overline{\text{CCLIM}}$	Tw2	resv

Bit	R/W	Symbol	Description
D0	R	resv	**RESERVED FOR FUTURE USE:** Value set at logic one.
D1	R	Tw2	**CARRIER RECOVERY TIME:** 0: Tw2 set at 5 bits. 1: Tw2 set at 3 bits.
D2	R	$\overline{\text{CCLIM}}$	**CONSECUTIVE COLLISION LIMIT:** 0: Consecutive collision limit set at 63 collisions. 1: Consecutive collision limit set at 31 collisions.
D3	R	$\overline{\text{LPPART}}$	**LOOPBACK PARTITION:** 0: Partitioning upon lack of loopback from transceivers is enabled. 1: Partitioning upon lack of loopback from transceivers is disabled.
D4	R	$\overline{\text{OWCE}}$	**OUT OF WINDOW COLLISION ENABLE:** 0: Out of window collisions are treated as in window collisions by the segment partition state machines. 1: Out of window collisions are treated as out of window collisions by the segment partition state machines.
D5	R	$\overline{\text{TXONLY}}$	**ONLY RECONNECT UPON SEGMENT TRANSMISSION:** 0: A segment will only be reconnected to the network if a packet transmitted by the RIC onto that segment fulfills the requirements of the segment reconnection algorithm. 1: A segment will be reconnected to the network by any packet on the network which fullfills the requirements of the segment reconnection algorithm.
D6	R	$\overline{\text{DPART}}$	**DISABLE PARTITION:** 0: Partitioning of ports by on-chip algorithms is prevented. 1: Partitioning of ports by on-chip algorithms is enabled.
D7	R	MINMAX	**MINIMUM/MAXIMUM DISPLAY MODE:** 0: LED display set in minimum display mode. 1: LED display set in maximum display mode.

8.0 RIC Registers (Continued)

Real Time Interrupt Register (Address 0FH)

The Real Time Interrupt register (RTI) contains information which may change on a packet by packet basis. Any remaining interrupts which have not been serviced before the following packet is transmitted are cleared. Since multiple interrupt sources may be displayed by the RTI a priority scheme is implemented. A read cycle to the RTI gives the interrupt source and an address vector indicating the RIC port which generated the interrupt. The order of priority for the display of interrupt information is as follows:

1. The receive source of network activity (Port N),
2. The first RIC port showing collision
3. A port partitioned or reconnected.

During the repetition of a single packet it is possible that multiple ports may be partitioned or alternatively reconnected. The ports have equal priority in displaying partition/reconnection information. This data is derived from the ports by the RTI register as it polls consecutively around the ports.

Reading the RTI clears the particular interrupt. If no interrupt sources are active the RTI returns a no valid interrupt status.

D7	D6	D5	D4	D3	D2	D1	D0
IVCTR3	IVCTR2	IVCTR1	IVCTR0	ISRC3	ISRC2	ISRC1	ISRC0

Bit	R/W	Symbol Access	Description
D(3:0)	R	ISCR(3:0)	**INTERRUPT SOURCE:** These four bits indicate the reason why the interrupt was generated.
D(7:4)	R	IVCTR(3:0)	**INTERRUPT VECTOR:** This field defines the port address responsible for generating the interrupt.

The following table shows the mapping of interrupt sources onto the D3 to D0 pins. Essentially each of the three interrupt sources has a dedicated bit in this field. If a read to the RTI produces a low logic level on one of these bits then the interrupt source may be directly decoded. Associated with the source of the interrupt is the port where the event is occurring. If no unmasked events (receive, collision, etc.), have occurred when the RTI is read then an all ones pattern is driven by the RIC onto the data pins.

D7	D6	D5	D4	D3	D2	D1	D0	Comments
PA3	PA2	PA1	PA0	1	1	0	1	First Collision PA(3:0) = Collision Port Address
PA3	PA2	PA1	PA0	1	0	1	1	Receive PA(3:0) = Receive Port Address
PA3	PA2	PA1	PA0	0	1	1	1	Partition Reconnection PA(3:0) = Partition Port Address
1	1	1	1	1	1	1	1	No Valid Interrupt

8.0 RIC Registers (Continued)

Page Select Register ((All Pages) Address 10H)

The Page Select register performs two functions:

1. It enables switches to be made between register pages,
2. It provides status information regarding the Event Logging Interrupts.

D7	D6	D5	D4	D3	D2	D1	D0
FC	HC	LC	FF	resv	PSEL2	PSEL1	PSEL0

Bit	R/W	Symbol	Description
D(2:0)	R/W	PSEL(2:0)	**PAGE SELECT BITS:** When read these bits indicate the currently selected Upper Register Array Page. Write cycles to these locations facilitates page swapping.
D3	R	resv	**RESERVED FOR FUTURE USE**
D4	R	FF	**FLAG FOUND:** This indicates one of the unmasked event recording latches has been set.
D5	R	LC	**LOW COUNT:** This indicates one of the port event counters has a value less than 00FF Hex.
D6	R	HC	**HIGH COUNT:** This indicates one of the port event counters has a value greater than C000 Hex.
D7	R	FC	**FULL COUNTER:** This indicates one of the port event counters has a value equal to FFFF Hex.

Device Type Register (Page 0H Address 11H)

This register may be used to distinguish different revisions of RIC. If this register is read it will return a different value each for DP83950 revisions. (Contact National Semiconductor for revision information.) Write operations to this register have no effect upon the contents.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	X	X

8.0 RIC Registers (Continued)

Lower Event Count Mask Register (Page 0H Address 12H)

D7	D6	D5	D4	D3	D2	D1	D0
BDLNKC	PARTC	RECC	SEC	NSFDC	PLERC	ELBER C	JABC

Bit	R/W	Symbol	Description
D0	R/W	JABC	**JABBER COUNT ENABLE:** Enables recording of Jabber Protect events.
D1	R/W	ELBERC	**ELASTICITY BUFFER ERROR COUNT ENABLE:** Enables recording of Elasticity Buffer Error events.
D2	R/W	PLERC	**PHASE LOCK ERROR COUNT ENABLE:** Enables recording of Carrier Error events.
D3	R/W	NSFDC	**NON SFD COUNT ENABLE:** Enables recording of Non SFD packet events.
D4	R/W	SEC	**SHORT EVENT COUNT ENABLE:** Enables recording of Short events.
D5	R/W	RECC	**RECEIVE COUNT ENABLE:** Enables recording of Packet Receive (port N status) events that do not suffer collisions.
D6	R/W	PARTC	**PARTITION COUNT ENABLE:** Enables recording of Partition events.
D7	R/W	BDLNKC	**BAD LINK COUNT ENABLE:** Enables recording of Bad Link events.

Upper Event Count Mask Register (Page 0H Address 13H)

D7	D6	D5	D4	D3	D2	D1	D0
resv	resv	OWCC	RXCOLC	TXCOLC	resv	FWF	ROR

Bit	R/W	Symbol	Description
D0	R/W	ROR	**RESET ON READ:** This bit selects the action a read operation has upon a port's event counter: 0: No effect upon register contents. 1: The counter register is reset.
D1	R/W	FWF	**FREEZE WHEN FULL:** This bit controls the freezing of the Event Count registers when the counter is full (FFFF Hex)
D2	R	resv	**RESERVED FOR FUTURE USE:** This bit should be written with a low logic level.
D3	R/W	TXCOLC	**TRANSMIT COLLISION COUNT ENABLE:** Enables recording of transmit collision events only.
D4	R/W	RXCOLC	**RECEIVE COLLISION COUNT ENABLE:** Enables recording of receive collision events only.
D5	R/W	OWCC	**OUT OF WINDOW COLLISION COUNT ENABLE:** Enables recording of out of window collision events only.
D(7: 6)	R	resv	**RESERVED FOR FUTURE USE:** These bits should be written with a low logic level.

Note 1: To count all collisions then both the TXCOLC and RXCOLC bits must be set. The OWCC bit should not be set otherwise the port counter will be incremented twice when an out of collision window collision occurs. The OWCC bit alone should be set if only out of window collision are to be counted.

Note 2: Writing a 1 enables the event to be counted.

8.0 RIC Registers (Continued)

Event Record Mask Register (Page 0H Address 14H)

D7	D6	D5	D4	D3	D2	D1	D0
BDLNKE	PARTE	OWCE	SEE	NSFDE	PLERE	ELBERE	JABE

Bit	R/W	Symbol	Description
D0	R/W	JABE	**JABBER ENABLE:** Enables recording of Jabber Protect events.
D1	R/W	ELBERE	**ELASTICITY BUFFER ERROR ENABLE:** Enables recording of Elasticity Buffer Error events.
D2	R/W	PLERE	**PHASE LOCK ERROR ENABLE:** Enables recording of Carrier Error events.
D3	R/W	NSFDE	**NON SFD ENABLE:** Enables recording of Non SFD packet events.
D4	R/W	SEE	**SHORT EVENT ENABLE:** Enables recording of Short Events.
D5	R/W	OWCE	**OUT OF WINDOW COLLISION COUNT ENABLE:** Enables recording of Out of Window Collision events only.
D6	R/W	PARTE	**PARTITION ENABLE:** Enables recording of Partition events.
D7	R/W	BDLNKE	**BAD LINK ENABLE:** Enables recording of Bad Link Events.

Note: Writing a 1 enables the event to be recorded.

8.0 RIC Registers (Continued)

Interrupt and Management Configuration Register (Page 0H Address 16H)

This register powers up with all bits set to one and must be initialized by a processor write cycle before any events will generate interrupts.

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{IFC}$	$\overline{IHC}$	$\overline{ILC}$	$\overline{IFF}$	$\overline{IREC}$	$\overline{ICOL}$	$\overline{IPART}$	MIFCON

Bit	R/W	Symbol	Description
D0	R/W	MIFCON	**MANAGEMENT INTERFACE CONFIGURATION:** 0: All Packets repeated are transmitted over the Management bus. 1: Packets repeated by the RIC which do not have a Start of Frame Delimiters are not transmitted over the Management bus.
D1	R/W	$\overline{IPART}$	**INTERRUPT ON PARTITION:** 0: Interrupts will be generated(1) if a port becomes Partitioned. 1: No interrupts are generated by this condition.
D2	R/W	$\overline{ICOL}$	**INTERRUPT ON COLLISION:** 0: Interrupts will be generated(1) if this RIC has a port which experiences a collision, Single RIC applications, or contains a port which experiences a receive collision or is the first port to suffer a transmit collision in a packet in Multi-RIC applications. 1: No interrupts are generated by this condition.
D3	R/W	$\overline{IREC}$	**INTERRUPT ON RECEIVE:** 0: Interrupts will be generated(1) if this RIC contains the receive port for packet or collision activity. 1: No interrupts are generated by this condition.
D4	R/W	$\overline{IFF}$	**INTERRUPT ON FLAG FOUND:** 0: Interrupts will be generated(2) if one or more than one of the flags in the flag array is true. 1: No interrupts are generated by this condition.
D5	R/W	$\overline{ILC}$	**INTERRUPT ON LOW COUNT:** 0: Interrupt generated(2) when one or more of the Event Counters holds a value less than 256 counts. 1: No effect
D6	R/W	$\overline{IHC}$	**INTERRUPT ON HIGH COUNT:** 0: Interrupt generated(2) when one or more of the Event Counters holds a value in excess of 49152 counts. 1: No effect
D7	R/W	$\overline{IFC}$	**INTERRUPT ON FULL COUNTER:** 0: Interrupt generated(2) when one or more of the Event Counters is full. 1: No effect

Note 1: ($\overline{RTI}$ pin goes active)

Note 2: ($\overline{ELI}$ pin goes active)

8.0 RIC Registers (Continued)

RIC Address Register (Page 0H Address 17H)

This register may be used to differentiate between RICs in a multi-RIC repeater system. The contents of this register form part of the information available through the management bus.

D7	D6	D5	D4	D3	D2	D1	D0
A5	A4	A3	A2	A1	A0	res	res

Packet Compress Decode Register (Page 0H Address 18H)

This register is used to determine the number of bytes in the data field of a packet which are transferred over the management bus when the packet compress option is employed. The register bits perform the function of a direct binary decode. Thus up to 255 bytes of data may be transferred over the management bus if packet compression is selected.

D7	D6	D5	D4	D3	D2	D1	D0
PCD7	PCD6	PCD5	PCD4	PCD3	PCD2	PCD1	PCD0

Inter Frame Gap Threshold Select Register (Page 0H Address 1FH)

This register is used to configure the hub management interface to provide a certain minimum inter frame gap between packets transmitted over the management bus. The value written to this register, plus one, is the magnitude in bit times of the minimum IFG allowed on the management bus.

D7	D6	D5	D4	D3	D2	D1	D0
IFGT7	IFGT6	IFGT5	IFGT4	IFGT3	IFGT2	IFGT1	IFGT0

Port Event Record Registers (Page 1H Address 11H to 1DH)

These registers hold the recorded events for the specified RIC port. The flags are cleared when the register is read.

D7	D6	D5	D4	D3	D2	D1	D0
BDLNK	PART	OWC	SE	NSFD	PLER	ELBER	JAB

Bit	R/W	Symbol	Description
D0	R	JAB	**JABBER:** A Jabber Protect event has occurred.
D1	R	ELBER	**ELASTICITY BUFFER ERROR:** A Elasticity Buffer Error has occurred.
D2	R	PLER	**PHASE LOCK ERROR:** A Phase Lock Error event has occurred.
D3	R	NSFD	**NON SFD:** A Non SFD packet event has occurred.
D4	R	SE	**SHORT EVENT:** A Short event has occurred.
D5	R	OWC	**OUT OF WINDOW COLLISION:** An out of window collision event has occurred.
D6	R	PART	**PARTITION:** A partition event has occurred.
D7	R	BDLNK	**BAD LINK:** A link failure event has occurred.

Port Event Count Register (Pages 2H and 3H)

The Event Count (EC) register shows the instantaneous value of the specified port's 16-bit counter. The counter increments when an enabled event occurs. The counter may be cleared when it is read and prevented from rolling over when the maximum count is reached by setting the appropriate control bits in the Upper Event Count mask register. Since the RIC's processor port is octal and the counters are 16 bits long a temporary holding register is employed for register reads. When one of the counters is read, either high or low byte first, all 16 bits of the counter are transferred to a holding register. Provided the next read cycle to the counter array accesses the same counter's, other byte, then the read cycle accesses the holding register. This avoids the problem of events occurring in between the two processor reads and indicating a false count value. In order to enter a new value to the holding register a different counter must be accessed or the same counter byte must be re-read.

Lower Byte

D7	D6	D5	D4	D3	D2	D1	D0
EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Upper Byte

D7	D6	D5	D4	D3	D2	D1	D0
EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8

9.0 AC and DC Specifications

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	0.5V to 7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} +0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	2W
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
ESD Rating (R_{zap} = 1.5k, C_{zap} = 120 pF)	1500V

DC Specifications T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

PROCESSOR, LED, TWISTED PAIR PORTS, INTER-RIC AND MANAGEMENT INTERFACES

Symbol	Description	Conditions	Min	Max	Units
V_{OH}	Minimum High Level Output Voltage	I_{OH} = −8 mA	3.5		V
V_{OL}	Minimum Low Level Output Voltage	I_{OL} = 8 mA		0.4	V
V_{IH}	Minimum High Level Input Voltage		2.0		V
V_{IL}	Maximum Low Level Input Voltage			0.8	V
I_{IN}	Input Current	V_{IN} = V_{CC} or GND	−1.0	1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND	−10	10	μA
I_{CC}	Average Supply Current	V_{IN} = V_{CC} or GND V_{CC} = 5.25V		380	mA
AUI (PORT 1)					
V_{OD}	Differential Output Voltage (TX±)	78Ω Termination and 270Ω Pulldowns	±550	±1200	mV
V_{OB}	Differential Output Voltage Imbalance (TX±)	78Ω Termination and 270Ω Pulldowns	Typical: 40 mV		
V_U	Undershoot Voltage (TX±)	78Ω Termination and 270Ω Pulldowns	Typical: 80 mV		
V_{DS}	Differential Squelch Threshold (RX±, CD±)		−175	−300	mV
V_{CM}	Differential Input Common Mode Voltage (RX±, CD±) (Note 1)		0	5.5	V

Note 1: This parameter is guaranteed by design and is not tested.

9.0 AC and DC Specifications (Continued)

DC Specifications $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified (Continued)

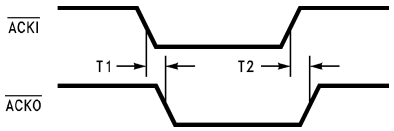
Symbol	Description	Conditions	Min	Max	Units
PSEUDO AUI (PORTS 2–13)					
V_{POD}	Differential Output Voltage (TX±)	270Ω Termination and 1 kΩ Pulldowns	±450	±1200	mV
V_{POB}	Differential Output Voltage Imbalance (TX±)	270Ω Termination and 1 kΩ Pulldowns	Typical: 40 mV		
V_{PU}	Undershoot Voltage (TX±)	270Ω Termination and 1 kΩ Pulldowns	Typical: 80 mV		
V_{PDS}	Differential Squelch Threshold (RX±, CD±)		−175	−300	mV
V_{PCM}	Differential Input Common Mode Voltage (Rx±, CD±) (Note 1)		0	5.5	V
TWISTED PAIR (PORTS 2–13)					
V_{RON}	Minimum Receive Squelch Threshold	Normal Mode Reduced Mode	±300 (Note 2) 	±585 ±340	mV mV

Note 1: This parameter is guaranteed by design and is not tested.

Note 2: The operation in Reduced Mode is not guaranteed below 300 mV.

AC Specifications

PORT ARBITRATION TIMING



TL/F/11096–22

Number	Symbol	Parameter	Min	Max	Units
T1	ackilackol	ACKI Low to $\overline{ACKO}$ Low		24	ns
T2	ackihackoh	ACKI High to $\overline{ACKO}$ High		21	ns

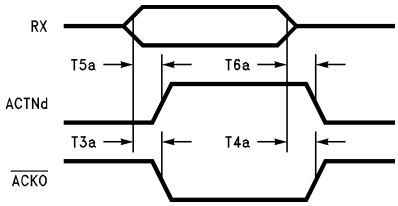
Note: Timing valid with no receive or collision activities.

Note: In these diagrams the Inter-RIC and Management Busses are shown using active high signals, active low signals may also be used. See Section 5.5 Mode Load Operation.

9.0 AC and DC Specifications (Continued)

RECEIVING TIMINGS—AUI PORTS

Receive activity propagation start up and end delays for ports in **non** 10BASE-T mode



TL/F/11096–23

Number	Symbol	Parameter	Min	Max	Units
T3a	rxaackol	RX Active to $\overline{\text{ACKO}}$ Low		66	ns
T4a	rxiackoh	RX Inactive to $\overline{\text{ACKO}}$ High		325	ns
T5a	rxaactna	RX Active to ACTNd Active		105	ns
T6a	rxiactni	RX Inactive to ACTNd Inactive		325	ns

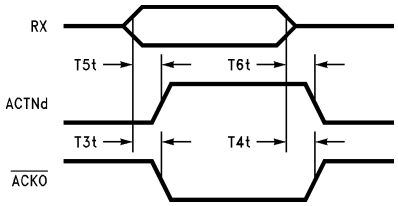
Note: $\overline{\text{ACKI}}$ assumed high.

Note: In these diagrams the Inter-RIC and Management Busses are shown using active high signals, active low signals may also be used. See Section 5.5 Mode Load Operation.

9.0 AC and DC Specifications (Continued)

RECEIVE TIMING—10BASE-T PORTS

Receive activity propagation start up and end delays for ports in 10BASE-T mode



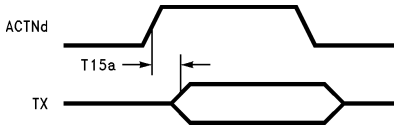
TL/F/11096–24

Number	Symbol	Parameter	Min	Max	Units
T3t	rxaackol	RX Active to $\overline{\text{ACKO}}$ Low		240	ns
T4t	rxiackoh	RX Inactive to $\overline{\text{ACKO}}$ High		255	ns
T5t	rxaactna	RX Active to ACTNd Active		270	ns
T6t	rxiactni	RX Inactive to ACTNd Inactive		265	ns

Note: $\overline{\text{ACKI}}$ assumed high.

TRANSMIT TIMING—AUI PORTS

Transmit activity propagation start up and end delays for ports in **non** 10BASE-T mode



TL/F/11096–25

Number	Symbol	Parameter	Min	Max	Units
T15a	actnatxa	ACTNd Active to TX Active		585	ns

Note: $\overline{\text{ACKI}}$ assumed high.

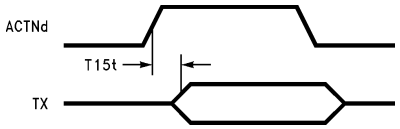
Note: ACTN_d and ACTN_s are tied together.

Note: In these diagrams the Inter-RIC and Management Busses are shown using active high signals, active low signals may also be used. See Section 5.5 Mode Load Operation.

9.0 AC and DC Specifications (Continued)

TRANSMIT TIMING—10BASE-T PORTS

Receive activity propagation start up and end delays for ports in 10BASE-T mode



TL/F/11096–26

Number	Symbol	Parameter	Min	Max	Units
T15t	actnatxa	ACTNd Active to TX Active		790	ns

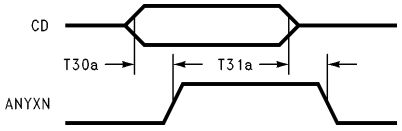
Note: $\overline{ACKI}$ assumed high.

Note: $ACTN_d$ and $ACTN_s$ are tied together.

COLLISION TIMING—AUI PORTS

Collision activity propagation start up and end delays for ports in **non** 10BASE-T mode

TRANSMIT COLLISION TIMING



TL/F/11096–27

Number	Symbol	Parameter	Min	Max	Units
T30a	cdaanyxna	CD Active to ANYXN Active		65	ns
T31a	cdianyxni	CD Inactive to ANYXN Inactive (Notes 1, 2)		400	ns

Note 1: TX collision extension has already been performed and no other port is driving ANYXN.

Note 2: Includes TW2.

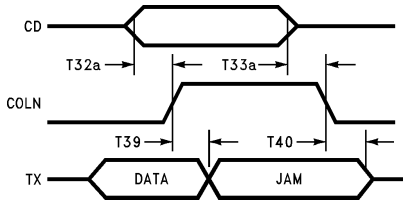
Note: In these diagrams the Inter-RIC and Management Busses are shown using active high signals, active low signals may also be used. See Section 5.5 Mode Load Operation.

9.0 AC and DC Specifications (Continued)

COLLISION TIMING—AUI PORTS

Collision activity propagation start up and end delays for ports in **non** 10BASE-T mode.

RECEIVE COLLISION TIMING



TL/F/11096–28

Number	Symbol	Parameter	Min	Max	Units
T32a	cdacolna	CD Active to COLN Active (Note 1)		55	ns
T33a	cdicolni	CD Inactive to COLN Inactive		215	ns
T39	colnajs	COLN Active to Start of Jam		400	ns
T40	colnije	COLN Inactive to End of Jam (Note 2)		800	ns

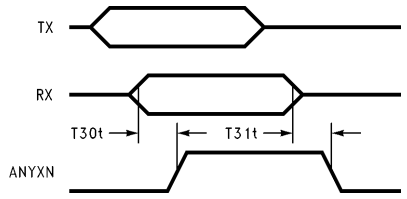
Note 1: PKEN assumed high.

Note 2: Assuming reception ended before COLN goes inactive. TW2 is included in this parameter. Assuming $ACTN_d$ to $ACTN_s$ delay is 0.

Note: In these diagrams the Inter-RIC and Management Busses are shown using active high signals, active low signals may also be used. See Section 5.5 Mode Load Operation.

COLLISION TIMING—10BASE-T PORTS

Collision activity propagation start up and end delays for ports in 10BASE-T mode



TL/F/11096–29

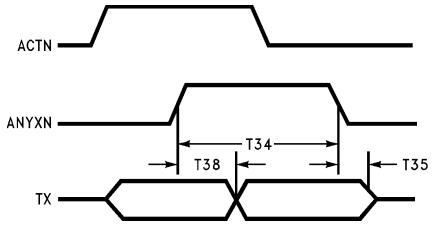
Number	Symbol	Parameter	Min	Max	Units
T30t	colaanya	Collision Active to ANYXN Active		800	ns
T31t	colianyi	Collision Inactive to ANYXN Inactive (Note 1)		400	ns

Note 1: TX collision extension has alreay been performed and no other port is asserting ANYXN.

Note: In these diagrams the Inter-RIC and Management Busses are shown using active high signals, active low signals may also be used. See Section 5.5 Mode Load Operation.

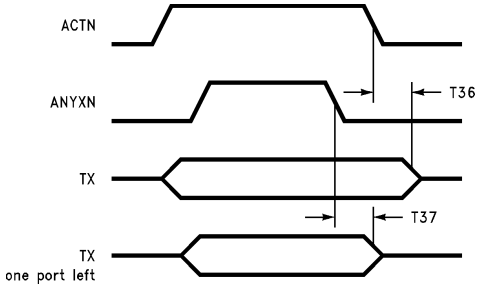
9.0 AC and DC Specifications (Continued)

COLLISION TIMING—ALL PORTS



TL/F/11096–38

Number	Symbol	Parameter	Min	Max	Units
T34	anyamin	ANYXN Active Time	96		Bits
T35	anyitxai	ANYXN Inactive to TX to all Inactive	120	170	ns
T38	anyasj	ANYXN Active to Start of Jam		400	ns



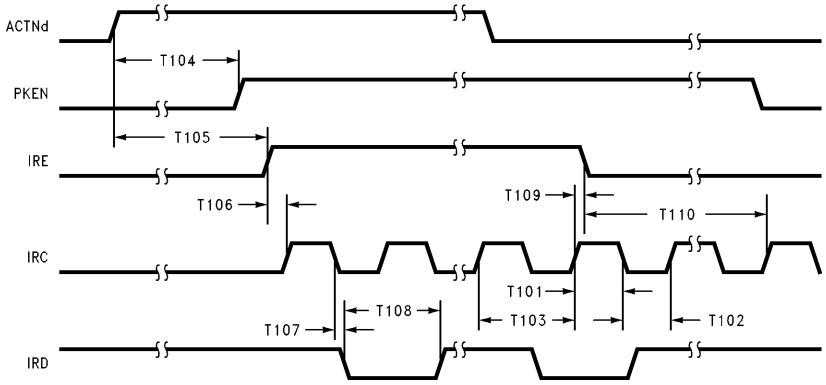
TL/F/11096–39

Number	Symbol	Parameter	Min	Max	Units
T36	actnitxi	ACTN Inactive to TX Inactive		405	ns
T37	anyitxoi	ANYXN Inactive to TX "One Port Left" Inactive	120	170	ns

Note: In these diagrams the Inter-RIC and Management Busses are shown using active high signals, active low signals may also be used. See Section 5.5 Mode Load Operation.

9.0 AC and DC Specifications (Continued)

INTER RIC BUS OUTPUT TIMING



TL/F/11096–35

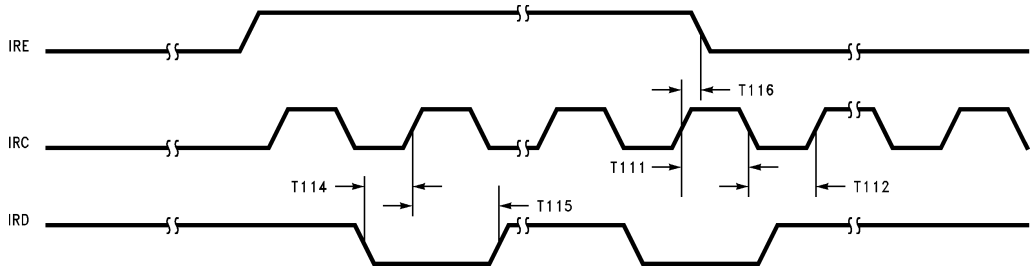
Number	Symbol	Parameter	Min	Max	Units
T101	ircoh	IRC Output High Time	45	55	ns
T102	ircol	IRC Output Low Time	45	55	ns
T103	ircoc	IRC Output Cycle Time	90	110	ns
T104	actndapkena	ACTNd Active to PKEN Active	555		ns
T105	actndairea	ACTNd Active to IRE Active	560		ns
T106	ireoairca	IRE Output Active to IRC Active		1.8	μs
T107	irdov	IRD Output Valid from IRC		10	ns
T108	irdos	IRD Output Stable Valid Time	90		ns
T109	ircohirei	IRC Output High to IRE Inactive	30	70	ns
T110	ircclks	Number of IRCs after IRE Inactive	5		clks

Note: In these diagrams the Inter-RIC and Management Busses are shown using active high signals, active low signals may also be used. See Section 5.5 Mode Load Operation.

Note: In a Multi-RIC system, the PKEN signal is valid only for the first receiving RIC.

9.0 AC and DC Specifications (Continued)

INTER RIC BUS INPUT TIMING



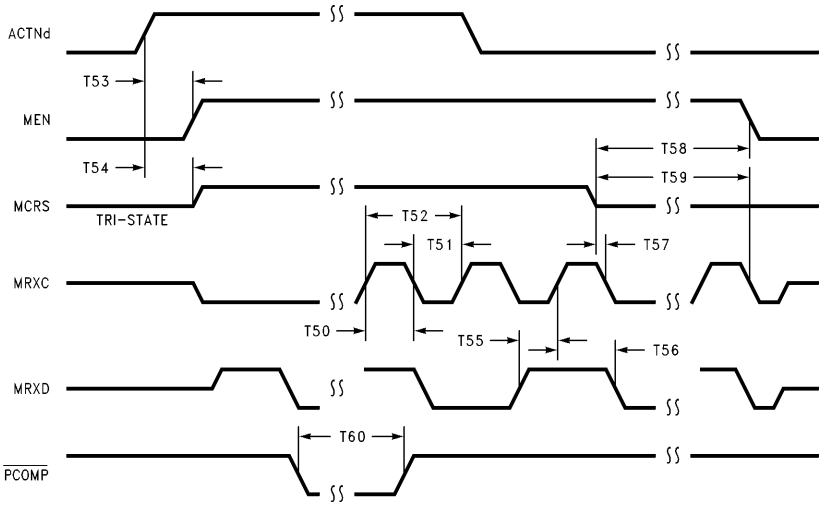
TL/F/11096–40

Number	Symbol	Parameter	Min	Max	Units
T111	ircih	IRC Input High Time	20		ns
T112	ircil	IRC Input Low Time	20		ns
T114	irdisirc	IRD Input Setup to IRC	5		ns
T115	irdihirc	IRD Input Hold from IRC	10		ns
T116	irchiire	IRC Input High to IRE Inactive	10	90	ns

Note: In these diagrams the Inter-RIC and Management Busses are shown using active high signals, active low signals may also be used. See Section 5.5 Mode Load Operation.

9.0 AC and DC Specifications (Continued)

MANAGEMENT BUS TIMING



TL/F/11096–30

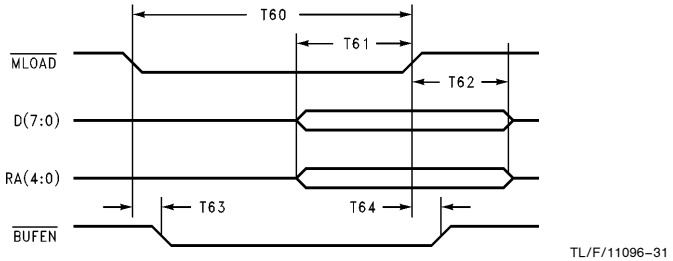
Number	Symbol	Parameter	Min	Max	Units
T50	mrxch	MRXC High Time	45	55	ns
T51	mrxcl	MRXC Low Time	45	55	ns
T52	mrxcd	MRXC Cycle Time	90	110	ns
T53	actndamena	ACTNd Active to MEN Active		715	ns
T54	actndamcrsa	ACTNd Active to MCRS Active		720	ns
T55	mrxds	MRXD Setup	40		ns
T56	mrxdh	MRXD Hold	45		ns
T57	mrxclmcrsi	MRXC Low to MCRS Inactive	−5	6	ns
T58	mcrsimenl	MCRS Inactive to MEN Low		510	ns
T59	mrxcclks	Min Number of MRXCs after MCRS Inactive	5	5	Clks
T60	pcompw	PCOMP Pulse Width	20		ns

Note: The preamble on this bus consists of the following string: 01011.

Note: In these diagrams the Inter-RIC and Management Busses are shown using active high signals, active low signals may also be used. See Section 5.5 Mode Load Operation.

9.0 AC and DC Specifications (Continued)

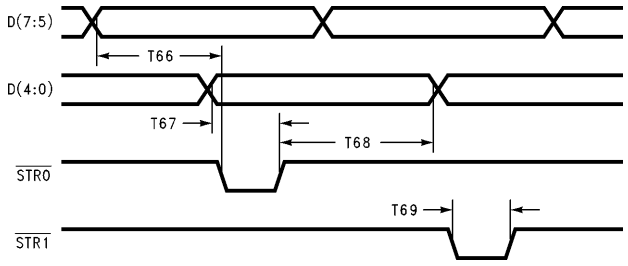
MLOAD TIMING



TL/F/11096–31

Number	Symbol	Parameter	Min	Max	Units
T61	mldats	Data Setup	10		ns
T62	mldath	Data Hold	10		ns
T63	mlabufa	MLOAD Active to BUFEN Active		35	ns
T64	mlibufi	MLOAD Inactive to BUFEN Inactive		35	ns
T65	mlw	MLOAD Width	800		ns

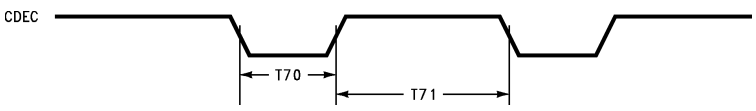
STROBE TIMING



TL/F/11096–32

Number	Symbol	Parameter	Min	Max	Units
T66	stradrs	Strobe Address Setup	80	115	ns
T67	strdats	Strobe Data Setup	40	65	ns
T68	strdath	Strobe Data Hold	135	160	ns
T69	strw	Strobe Width	30	65	ns

CDEC TIMING

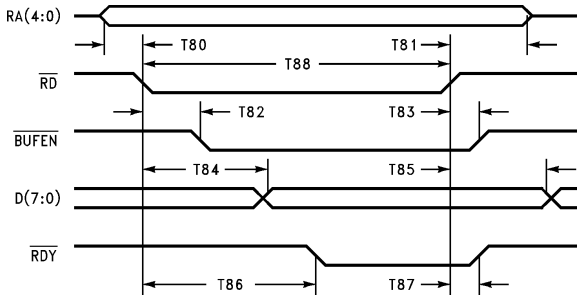


TL/F/11096–41

Number	Symbol	Parameter	Min	Max	Units
T70	cdecpw	CDEC Pulse Width	20	100	ns
T71	cdeccdec	CDEC to CDEC Width	200		ns

9.0 AC and DC Specifications (Continued)

REGISTER READ TIMING



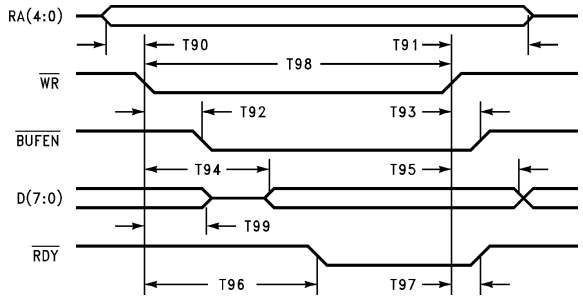
TL/F/11096–33

Number	Symbol	Parameter	Min	Max	Units
T80	rdadrs	Read Address Setup	0		ns
T81	rdadrh	Read Address Hold	0		ns
T82	rdabufa	Read Active to $\overline{\text{BUFEN}}$ Active	95	345	ns
T83	rdibufi	Read Inactive to $\overline{\text{BUFEN}}$ Inactive		35	ns
T84	rdadatv	Read Active to Data Invalid	245		ns
T85	rddath	Read Data Hold	75		ns
T86	rdardya	Read Active to $\overline{\text{RDY}}$ Active	340	585	ns
T87	rdirdyi	Read Inactive to $\overline{\text{RDY}}$ Inactive		30	ns
T88	rdw	Read Width	600		ns

Note: Minimum high time between read/write cycles is 100 ns.

9.0 AC and DC Specifications (Continued)

REGISTER WRITE TIMING



TL/F/11096–34

Number	Symbol	Parameter	Min	Max	Units
T90	wradrs	Write Address Setup	0		ns
T91	wradrh	Write Address Hold	0		ns
T92	wrabufa	Write Active to $\overline{\text{BUFEN}}$ Active	95	355	ns
T93	wribufi	Write Inactive to $\overline{\text{BUFEN}}$ Inactive		35	ns
T94	wradatv	Write Active to Data Valid		275	ns
T95	wrdath	Write Data Hold	0		ns
T96	wrardya	Write Active to $\overline{\text{RDY}}$ Active	340	585	ns
T97	wrirdyi	Write Inactive to $\overline{\text{RDY}}$ Inactive		30	ns
T98	wrw	Write Width	600		ns
T99	wradt	Write Active to Data TRI-STATE		350	ns

Note: Assuming zero propagation delay on external buffer.

Note: Minimum high time between read/write cycles is 100 ns.

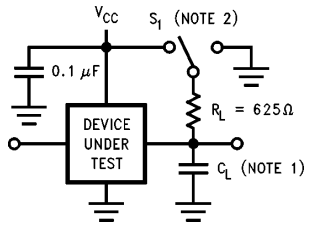
Note: The data will always TRI-STATE before $\overline{\text{BUFEN}}$ goes active with a load of 100 pF on the data bus.

Note: When $\overline{\text{RDY}}$ is used, the minimum 600 ns write width does not have to be maintained.

10.0 AC Timing Test Conditions

All specifications are valid only if the mandatory isolation is employed and all differential signals are taken to be at the AUI side of the pulse transformer.

Input Pulse Levels (TTL/CMOS)	GND to 3.0V
Input Rise and Fall Times (TTL/CMOS)	5 ns
Input and Output Reference Levels (TTL/CMOS)	1.5V
Input Pulse Levels (Diff.)	2.0 V_{P-P}
Input and Output Reference Levels (Diff.)	50% Point of the Differential
TRI-STATE Reference Levels	Float (ΔV) $\pm$0.5V
Output Load (See *Figure* Below)	



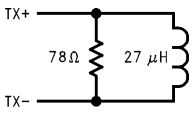
TL/F/11096–36

Note 1: 100 pF, includes scope and jig capacitance.

Note 2: S1 = Open for timing tests for push pull outputs.
S1 = V_{CC} for V_{OL} test.
S1 = GND for V_{OH} test.
S1 = V_{CC} for High Impedance to active low and active low to High Impedance measurements.
S1 = GND for High Impedance to active high and active high to High Impedance measurements.

Capacitance T_A = 25°C, f = 1 MHz

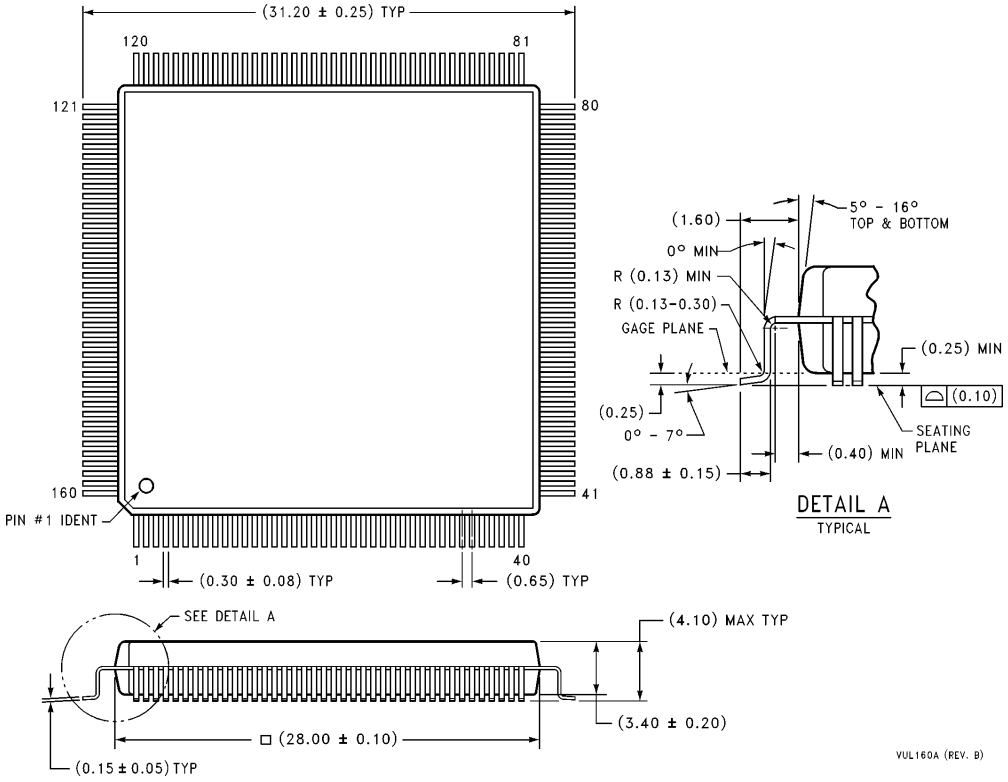
Symbol	Parameter	Typ	Units
C_{IN}	Input Capacitance	7	pF
C_{OUT}	Output Capacitance	7	pF



TL/F/11096–37

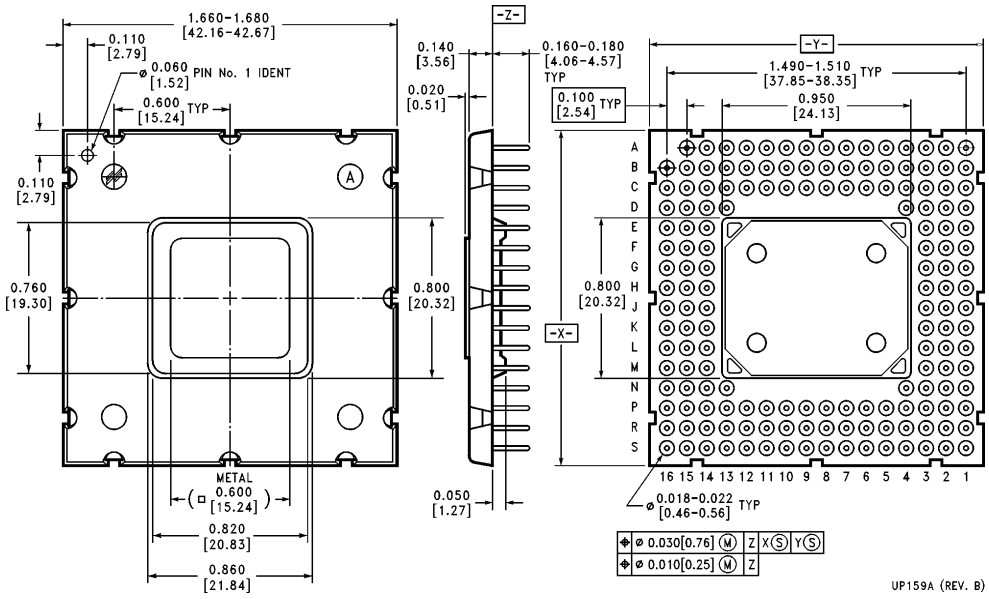
Note: In the above diagram, the TX+ and TX− signals are taken from the AUI side of the isolation (pulse transformer). The pulse transformer used for all testing is the Pulse Engineering PE64103.

11.0 Physical Dimensions inches (millimeters)



JEDEC, Molded Plastic Quad Flat Package (VUL)
Order Number DP83950BVQB
NS Package Number VUL160A

11.0 Physical Dimensions inches (millimeters) (Continued)



Pin Grid Array (U)
Order Number DP83950BNU
NS Package Number UP159A

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