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REV. 1

SEMICONDUCTOR

TECHNICAL DATA

MC68HC05P1
MC68HCL05P1
MC68HSC05P1

Addendum to
MC68HC05P1
HCMOS Microcontroller Unit
Technical Data

This addendum supplements *MC68HC05P1 Technical Data* (Motorola document number MC68HC05P1/D REV. 1) with the following additional information:

- Corrections to *MC68HC05P1 Technical Data* REV. 1
- New Ordering Information — **SECTION 10 ORDERING INFORMATION** in this addendum replaces **SECTION 10 ORDERING INFORMATION** in *MC68HC05P1 Technical Data* REV. 1
- MC68HCL05P1 data — APPENDIX A contains data for the MC68HCL05P1, a low-power version of the MC68HC05P1
- MC68HSC05P1 data — APPENDIX B contains data for the MC68HSC05P1, a high-speed version of the MC68HC05P1

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CORRECTIONS TO *MC68HC05P1 Technical Data* REV. 1

Corrections to *MC68HC05P1 Technical Data* REV. 1 are as follows:

1. Page 3-25, **3.5.2 WAIT Mode** — Delete the following sentence from the first paragraph:

   If the A/D converter is enabled, it is also active in WAIT mode.

2. Page 3-25, **3.5.2 WAIT Mode** — Delete the second paragraph.

3. Page 6-9, **6.7 Timer during WAIT Mode** — The first sentence should read as follows:

   The internal clock halts during WAIT mode, but the capture/compare timer remains active.

4. Page 6-9, **6.8 Timer during STOP Mode** —The second sentence should read as follows:

   If $\overline{IRQ}$ is used to exit STOP mode, the timer resumes counting from the count value that was present when STOP mode was entered.

5. Page 8-4, **Table 8-4. DC Electrical Characteristics (V_{DD} = 3.3 Vdc)** — NOTE 2 at the bottom of Table 8-4 should read as follows:

   2. Run (operating) I_{DD} and WAIT I_{DD} measured using external square wave clock source (f_{OSC} = 2.1 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.

6. Page 8-6, **Figure 8-5. Maximum Supply Current vs Clock Frequency** — Internal clock frequency scale at bottom of V_{DD} = 3.3 V 10% graph should read as follows:

   0 250 kHz 500 kHz 750 kHz 1 MHz

SECTION 10
ORDERING INFORMATION

This section contains information for ordering custom-masked ROM MCUs.

10.1 MCU Ordering Forms

To initiate an order for a ROM-based MCU, first obtain the current ordering form for the MCU from a Motorola representative. Submit the following items when ordering MCUs:

- A current MCU ordering form that is **completely filled out** (Contact your Motorola sales office for assistance.)
- A copy of the customer specification if the customer specification deviates from the Motorola specification for the MCU
- Customer's application program on one of the media listed in **10.2 Application Program Media**. The current MCU ordering form is also available through the Motorola Freeware Bulletin Board Service (BBS). The telephone number is (512) 891-FREE. After making the connection, type `bbs` in lowercase letters and press the return key to start the BBS software.

10.2 Application Program Media

Please deliver the application program to Motorola in one of the following media:

- Macintosh®[1] 3-1/2-inch diskette (double-sided 800K or double-sided high-density 1.4M)
- MS-DOS®[2] or PC-DOS®[3] 3-1/2-inch diskette (double-sided 720K or double-sided high-density 1.44M)
- MS-DOS® or PC-DOS® 5-1/4-inch diskette (double-sided double-density 360K or double-sided high-density 1.2M)
- EPROM(s) 2716, 2732, 2764, 27128, 27256, or 27512 (depending on the size of the memory map of the MCU)

Use positive logic for data and addresses.

1. Macintosh is a registered trademark of Apple Computer, Inc.
2. MS-DOS is a registered trademark of Microsoft, Inc.
3. PC-DOS is a registered trademark of International Business Machines Corporation.

10.2.1 Diskettes

If submitting the application program on a diskette, clearly label the diskette with the following information:

- Customer name
- Customer part number
- Project or product name
- File name of object code
- Date
- Name of operating system that formatted diskette
- Formatted capacity of diskette

On diskettes, the application program must be in Motorola's S-record format (S1 and S9 records), a character-based object file format generated by M6805 cross assemblers and linkers.

NOTE

Begin the application program at the first user ROM location. Program addresses must correspond exactly to the available on-chip user ROM addresses as shown in the memory map. **Write $00 in all non-user ROM locations, or leave all non-user ROM locations blank.** See the current MCU ordering form for additional requirements.

If the memory map has two user ROM areas with the same addresses, write the two areas in separate files on the diskette. Label the diskette with both file names.

In addition to the object code, a file containing the source code can be included. Motorola keeps this code confidential and uses it only to expedite ROM pattern generation in case of any difficulty with the object code. Label the diskette with the file name of the source code.

10.2.2 EPROMs

If submitting the application program in an EPROM, clearly label the EPROM with the following information:

- Customer name
- Customer part number
- Checksum
- Project or product name
- Date

NOTE

Begin the application program at the first user ROM location. Program addresses must correspond exactly to the available on-chip user ROM addresses as shown in the memory map. **Write $00 in all non-user ROM locations.** See the current MCU ordering form for additional requirements.

Submit the application program in one EPROM large enough to contain the entire memory map. If the memory map has two user ROM areas with the same addresses, write the two areas on separate EPROMs. Label the EPROMs with the addresses they contain.

Pack EPROMs securely in a conductive IC carrier for shipment. Do not use Styrofoam.

10.3 ROM Program Verification

The primary use for the on-chip ROM is to hold the customer's application program. The customer develops and debugs the application program, and then submits the MCU order along with the application program.

Motorola inputs the customer's application program code into a computer program that generates a listing verify file. The listing verify file represents the memory map of the MCU. The listing verify file contains the user ROM code and may also contain non-user ROM code, such as self-check code. Motorola sends the customer a computer printout of the listing verify file along with a listing verify form.

To aid the customer in checking the listing verify file, Motorola will program the listing verify file into customer-supplied blank EPROMs or preformatted Macintosh or DOS disks. All original pattern media is filed for contractual purposes and is not returned.

Check the listing verify file thoroughly, then complete and sign the listing verify form and return the listing verify form to Motorola. The signed listing verify form constitutes the contractual agreement for the creation of the custom mask.

10.4 ROM Verification Units

After receiving the signed listing verify form, Motorola manufactures a custom photographic mask. The mask contains the customer's application program and is used to process silicon wafers. The application program cannot be changed after the manufacture of the mask begins. Motorola then produces ten MCUs, called ROM verification units (RVUs), and sends the RVUs to the customer. RVUs are usually packaged in unmarked ceramic and tested to 5 Vdc at room temperature. RVUs are not tested to environmental extremes because their sole purpose is to demonstrate that the customer's user ROM pattern was properly implemented.

The ten RVUs are free of charge with the minimum order quantity but are not production parts. RVUs are not guaranteed by Motorola Quality Assurance.

10.5 MC Order Numbers

Table 10-1 provides ordering information for available package types.

Table 10-1. MC Order Numbers

Package Type	Temperature	MC Order Number
28-Pin Plastic Dual In-Line Package (DIP)	0 C to +70 C -40 C to +85 C	MC68HC05P1P MC68HC05P1CP
28-Pin Small Outline Integrated Circuit (SOIC)	0 C to +70 C -40 C to +85 C	MC68HC05P1DW MC68HC05P1CDW

APPENDIX A
MC68HCL05P1

This appendix introduces the MC68HCL05P1, a low-power version of the MC68HC05P1. All of the information in *MC68HC05P1 Technical Data* applies to the MC68HCL05P1 with the exceptions given in this appendix.

A.1 DC ELECTRICAL CHARACTERISTICS

The data in Table 8-3 and Table 8-4 of *MC68HC05P1 Technical Data* applies to the MC68HCL05P1 with the exceptions given in **Table A-1**, **Table A-2**, and **Table A-3**.

Table A-1. Low-Power Output Voltage (V_{DD} = 1.8–2.4 Vdc)

Characteristic	Symbol	Min	Typ	Max	Unit
Output High Voltage (I_{LOAD} = -0.1 mA) PA7–PA0, PB7–PB5, PC5–PC0, PD5, TCMP	V_{OH}	V_{DD} - 0.3	—	—	V
Output Low Voltage (I_{LOAD} = 0.2 mA) PA3–PA0, PB7–PB5, PC5–PC0, PD5, TCMP	V_{OL}	—	—	0.3	V

Table A-2. Low-Power Output Voltage (V_{DD} = 2.5–3.6 Vdc)

Characteristic	Symbol	Min	Typ	Max	Unit
Output High Voltage (I_{LOAD} = -0.2 mA) PA7–PA0, PB7–PB5, PC5–PC0, PD5, TCMP	V_{OH}	V_{DD} - 0.3	—	—	V
Output Low Voltage (I_{LOAD} = 0.4 mA) PA7–PA0, PB7–PB5, PC5–PC0, PD5, TCMP	V_{OL}	—	—	0.3	V

Table A-3. Low-Power Supply Current

Characteristic	Symbol	Min	Typ(1)	Max	Unit
Supply Current (V_{DD} = 4.5–5.5 Vdc, f_{OP} = 2.1 MHz)					
Run(2)	I_{DD}	—	3.0	4.25	mA
WAIT(3)		—	1.6	2.25	mA
STOP(4)					
25 C		—	0.5	15	µA
0 C to 70 C (Standard)		—	2.0	25	µA
Supply Current (V_{DD} = 2.5–3.6 Vdc, f_{OP} = 1.0 MHz)					
Run(2)	I_{DD}	—	1.0	1.6	mA
WAIT(3)		—	0.7	1.0	mA
STOP(4)					
25 C		—	0.2	5.0	µA
0 C to 70 C (Standard)		—	2.0	10.0	µA
Supply Current (V_{DD} = 2.5–3.6 Vdc, f_{OP} = 500 kHz)					
Run(2)	I_{DD}	—	600	800	µA
WAIT(3)		—	350	500	µA
STOP(4)					
25 C		—	0.2	5.0	µA
0 C to 70 C (Standard)		—	2.0	10.0	µA
Supply Current (V_{DD} = 1.8–2.4 Vdc, f_{OP} = 500 kHz)					
Run(2)	I_{DD}	—	300	600	µA
WAIT(3)		—	200	400	µA
STOP(4)					
25 C		—	0.1	2	µA
0 C to 70 C (Standard)		—	2.0	5	µA

1. Typical values reflect average measurements at midpoint of voltage range at 25 C.
2. Run (operating) I_{DD} measured using external square wave clock source with all inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.
3. WAIT I_{DD} measured using external square wave clock source with all inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. V_{IL} = 0.2 V, V_{IH} = V_{DD} - 0.2 V. OSC2 capacitance linearly affects WAIT I_{DD}.
4. STOP I_{DD} measured with OSC1 = V_{DD}. All ports configured as inputs. V_{IL} = 0.2 V, V_{IH} = V_{DD} - 0.2 V.

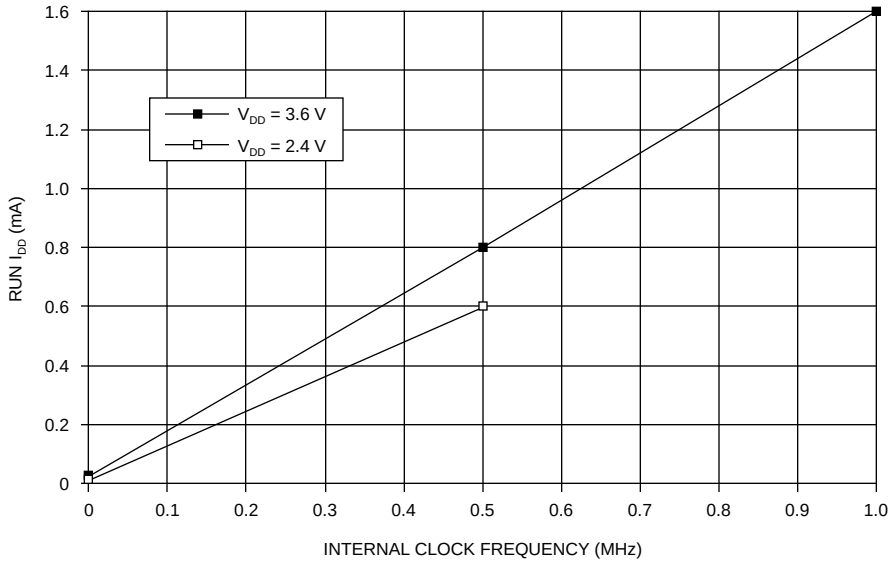

Figure A-1. Maximum Run Mode I_{DD} vs Frequency

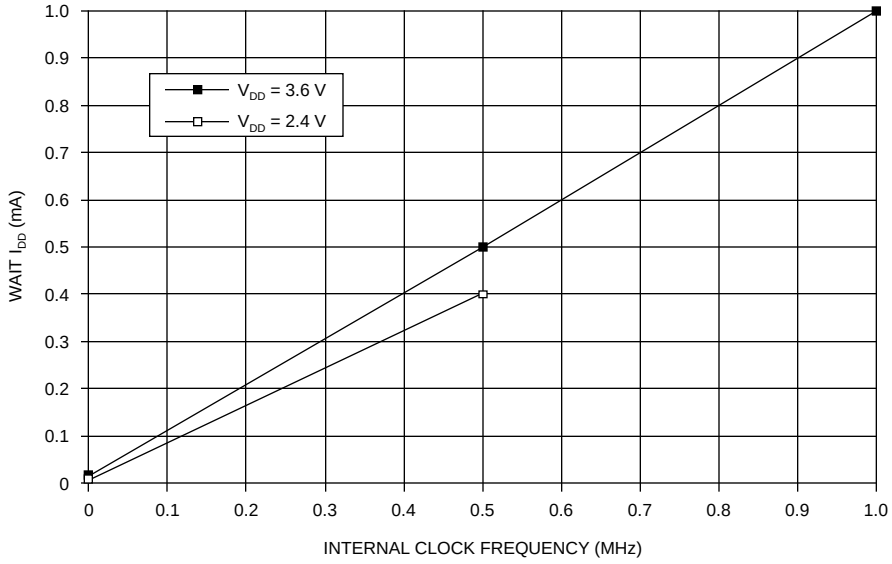

Figure A-2. Maximum WAIT Mode I_{DD} vs Frequency

A.2 MC ORDERING INFORMATION

Table A-4 provides ordering information for available package types.

Table A-4. MC Order Numbers

Package Type	Temperature	MC Order Number
28-Pin Plastic Dual In-Line Package (DIP)	0 C to +70 C	MC68HCL05P1P
28-Pin Small Outline Integrated Circuit (SOIC)	0 C to +70 C	MC68HCL05P1DW

APPENDIX B
MC68HSC05P1 MCU

This appendix introduces the MC68HSC05P1, a high-speed version of the MC68HC05P1. All of the information in *MC68HC05P1 Technical Data* applies to the MC68HSC05P1 with the exceptions given in this appendix.

B.1 DC ELECTRICAL CHARACTERISTICS

The data in Table 8-3 and Table 8-4 of *MC68HC05P1 Technical Data* applies to the MC68HSC05P1 with the exceptions given in **Table B-1**.

Table B-1. High-Speed Supply Current(1)

Characteristic	Symbol	Min	Typ(2)	Max	Unit
Supply Current (V_{DD} = 4.5–5.5 Vdc, f_{OP} = 4.0 MHz)					
Run(3)	I_{DD}	—	6.7	8.0	mA
WAIT(4)		—	3.5	4.0	mA
STOP(5)			2.0	25	µA
Supply Current (V_{DD} = 3.0–3.6 Vdc, f_{OP} = 2.1 MHz)					
Run(3)	I_{DD}	—	2.5	4.0	mA
WAIT(4)		—	1.3	3.0	mA
STOP(5)			2.0	10	µA

1. T_A = 0 C to 70 C
2. Typical values at midpoint of voltage range, 25 C only.
3. Run (operating) I_{DD} measured using external square wave clock source. All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.
4. WAIT I_{DD} measured using external square wave clock source. All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. V_{IL} = 0.2 V. V_{IH} = V_{DD} - 0.2 V. OSC2 capacitance linearly affects WAIT I_{DD}.
5. STOP I_{DD} measured with OSC1 = V_{SS}. All ports configured as inputs. V_{IL} = 0.2 V. V_{IH} = V_{DD} - 0.2 V.

B.2 CONTROL TIMING

The data in Table 8-6 and Table 8-7 of *MC68HC05P1 Technical Data* applies to the MC68HSC05P1 with the exceptions given in **Table B-2** and **Table B-3**.

Table B-2. High-Speed Control Timing (V_{DD} = 5.0 Vdc 10%)

Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal Oscillator External Clock	f_{OSC}	 — dc	 8.0 8.0	 MHz MHz
Internal Operating Frequency (f_{OSC} Ö2) Crystal Oscillator External Clock	f_{OP}	 — dc	 4.0 4.0	 MHz MHz
Internal Clock Cycle Time	t_{CYC}	250	—	ns
Input Capture Pulse Width	t_{TH}, t_{TL}	63	—	ns
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	63	—	ns
OSC1 Pulse Width	t_{OH}, t_{OL}	45	—	ns

Table B-3. High-Speed Control Timing (V_{DD} = 3.3 Vdc 10%)

Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal Oscillator External Clock	f_{OSC}	 — dc	 4.2 4.2	 MHz MHz
Internal Operating Frequency (f_{OSC} Ö2) Crystal Oscillator External Clock	f_{OP}	 — dc	 2.1 2.1	 MHz MHz
Internal Clock Cycle Time	t_{CYC}	480	—	ns
Input Capture Pulse Width	t_{TH}, t_{TL}	125	—	ns
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	125	—	ns
OSC1 Pulse Width	t_{OH}, t_{OL}	90	—	ns

B.3 MC ORDERING INFORMATION

Table B-4 provides ordering information for available package types.

Table B-4. MC Order Numbers

Package Type	Temperature	MC Order Number
28-Pin Plastic Dual In-Line Package (DIP)	0 C to +70 C	MC68HSC05P1P
28-Pin Small Outline Integrated Circuit (SOIC)	0 C to +70 C	MC68HSC05P1DW

MC68HC05P1AD/D