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PowerPC™

Technical Data

MPC106 PCI Bridge/Memory Controller Hardware Specifications

The Motorola MPC106 PCI bridge/memory controller provides a PowerPC™ microprocessor common hardware reference platform (CHRP™) compliant bridge between the PowerPC microprocessor family and the Peripheral Component Interconnect (PCI) bus. In this document, the term ‘106’ is used as an abbreviation for the phrase ‘MPC106 PCI bridge/memory controller.’ This document contains pertinent physical characteristics of the 106. For functional characteristics, refer to the *MPC106 PCI Bridge/Memory Controller User’s Manual*.

This document contains the following topics:

This document contains information on a new product under development by Motorola.
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In this document, the term ‘60x’ is used to denote a 32-bit microprocessor from the PowerPC architecture family that conforms to the bus interface of the PowerPC 601™, PowerPC 603™, or PowerPC 604™ microprocessors. Note that this does not include the PowerPC 602™ microprocessor which has a multiplexed address/data bus. 60x processors implement the PowerPC architecture as it is specified for 32-bit addressing, which provides 32-bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits (single-precision and double-precision).

To locate any published errata or updates for this document, refer to the website at http://www.mot.com/SPS/PowerPC/.

1.1 Overview

The MPC106 provides an integrated high-bandwidth, high-performance, TTL-compatible interface between a 60x processor, a secondary (L2) cache or additional (up to four total) 60x processors, the PCI bus, and main memory. This section provides a block diagram showing the major functional units of the 106 and describes briefly how those units interact.

Figure 1 shows the major functional units within the 106. Note that this is a conceptual block diagram intended to show the basic features rather than how these features are physically implemented on the device.

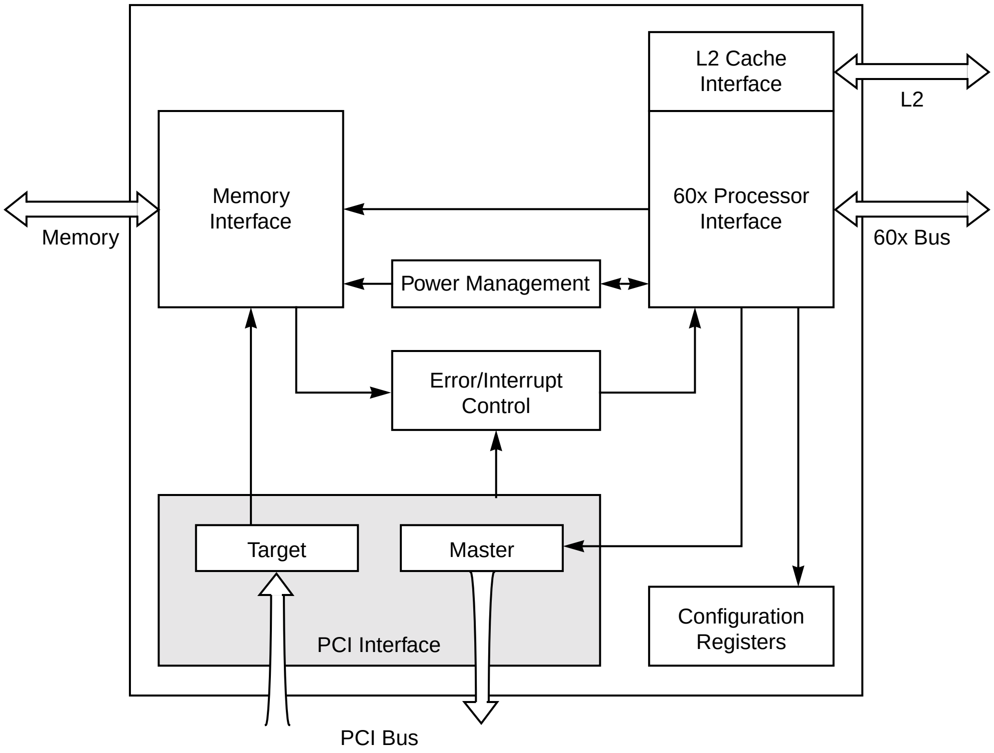

Figure 1. Block Diagram

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The 106 provides a PowerPC microprocessor CHRP-compliant bridge between the PowerPC microprocessor family and the PCI bus. CHRP documentation provides a set of specifications that define a unified personal computer architecture. PCI support allows the rapid design of systems using peripherals already designed for PCI and the other standard interfaces available in the personal computer hardware environment. The 106 integrates secondary cache control and a high-performance memory controller, uses an advanced, 3.3-V CMOS process technology, and is fully compatible with TTL devices.

The 106 supports a programmable interface to a variety of PowerPC microprocessors operating at select bus speeds. The 60x address bus is 32 bits wide and the data bus is 64 bits wide. The 60x processor interface of the 106 uses a subset of the 60x bus protocol, supporting single-beat and burst data transfers. The address and data buses are decoupled to support pipelined transactions.

The 106 provides support for the following configurations of 60x processors and L2 cache:

- Up to four 60x processors with no L2 cache
- A single 60x processor plus a direct-mapped, lookaside L2 cache using the internal L2 cache controller of the 106
- Up to four 60x processors plus an externally controlled L2 cache (such as the Motorola MPC2605 integrated secondary cache)

The memory interface controls processor and PCI interactions to main memory and is capable of supporting a variety of configurations using DRAM, EDO, SDRAM, ROM, or Flash ROM.

The PCI interface of the 106 complies with the *PCI Local Bus Specification*, Revision 2.1, and follows the guidelines in the *PCI System Design Guide*, Revision 1.0, for host bridge architecture. The PCI interface connects the processor and memory buses to the PCI bus, to which I/O components are connected. The PCI bus uses a 32-bit multiplexed address/data bus, plus various control and error signals.

The PCI interface of the 106 functions as both a master and target device. As a master, the 106 supports read and write operations to the PCI memory space, the PCI I/O space, and the PCI configuration space. The 106 also supports PCI special-cycle and interrupt-acknowledge commands. As a target, the 106 supports read and write operations to system memory.

The 106 provides hardware support for four levels of power reduction: doze, nap, sleep, and suspend. The design of the MPC106 is fully static, allowing internal logic states to be preserved during all power-saving modes.

1.2 Features

This section summarizes the major features of the 106, as follows:

- 60x processor interface
  - Supports up to four 60x processors
  - Supports various operating frequencies and bus divider ratios
  - 32-bit address bus, 64-bit data bus
  - Supports full memory coherency
  - Supports optional 60x local bus slave
  - Decoupled address and data buses for pipelining of 60x accesses
  - Store gathering on 60x-to-PCI writes

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- Secondary (L2) cache control
  - Configurable for write-through or write-back operation
  - Supports cache sizes of 256 Kbytes, 512 Kbytes, and 1 Mbyte
  - Up to 4 Gbytes of cacheable space
  - Direct-mapped
  - Supports byte parity
  - Supports partial update with external byte decode for write enables
  - Programmable interface timing
  - Supports pipelined burst, synchronous burst, or asynchronous SRAMs
  - Alternately supports an external L2 cache controller or integrated L2 cache module
- Memory interface
  - 1 Gbyte of RAM space, 16 Mbytes of ROM space
  - Supports parity or error checking and correction (ECC)
  - High-bandwidth, 64-bit data bus (72 bits including parity or ECC)
  - Supports fast page mode DRAMs, extended data out (EDO) DRAMs, and synchronous DRAMs (SDRAMs)
  - Supports 1 to 8 banks of DRAM/EDO/SDRAM with sizes ranging from 2 Mbyte to 128 Mbytes per bank
  - ROM space may be split between the PCI bus and the 60x/memory bus (8 Mbytes each)
  - Supports 8-bit asynchronous ROM or 64-bit burst-mode ROM
  - Supports writing to Flash ROM
  - Configurable external buffer control logic
  - Programmable interface timing
- PCI interface
  - Compliant with *PCI Local Bus Specification*, Revision 2.1
  - Supports PCI interlocked accesses to memory using $\overline{\text{LOCK}}$ signal and protocol
  - Supports accesses to all PCI address spaces
  - Selectable big- or little-endian operation
  - Store gathering on PCI writes to memory
  - Selectable memory prefetching of PCI read accesses
  - Only one external load presented by the MPC106 to the PCI bus
  - Interface operates at 20–33 MHz
  - Word parity supported
  - 3.3 V/5.0 V-compatible
- Support for concurrent transactions on 60x and PCI buses
- Power management
  - Fully-static 3.3-V CMOS design
  - Supports 60x nap, doze, and sleep power management modes and suspend mode
- IEEE 1149.1-compliant, JTAG boundary-scan interface
- 304-pin ceramic ball grid array (CBGA) package

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1.3 General Parameters

The following list provides a summary of the general parameters of the 106:

Technology	0.5 µm CMOS, four-layer metal
Die size	5.8 mm x 7.2 mm (41.8 mm^2)
Transistor count	250,000
Logic design	Fully-static
Packages	Surface mount 304-lead C4 ceramic ball grid array (CBGA)
Power supply	3.3 V ± 5% V DC
Maximum input rating	5.0 V ± 10% V DC

1.4 Electrical and Thermal Characteristics

This section provides both the AC and DC electrical specifications and thermal characteristics for the 106.

1.4.1 DC Electrical Characteristics

The tables in this section describe the 106 DC electrical characteristics. Table 1 provides the absolute maximum ratings. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause it permanent damage.

Table 1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit	Notes
Supply voltage	Vdd	–0.3 to 3.6	V	—
PLL supply voltage	AVdd	–0.3 to 3.6	V	—
Input voltage	V_{in}	–0.3 to 5.5	V	1
Junction temperature	T_j	0 to 105	°C	2
Storage temperature range	T_{stg}	–55 to 150	°C	—

Notes:

[1] **Caution**: V_{in} must not exceed Vdd by more than 2.5 V at all times including during power-on reset.

[2] The extended temperature parts have die junction temperature of -40 to 105°C. See MPC106ARXTGPNS/D for more information.

Table 2 provides the recommended operating conditions for the 106. Proper device operation outside of these recommended and tested conditions is not guaranteed.

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Table 2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit	Notes
Supply voltage	Vdd	3.3 ± 165 mv	V	—
PLL supply voltage	AVdd	3.3 ± 165 mv	V	—
Input voltage	V_{in}	0 to 5.5	V	—
Die junction temperature	T_j	0 to 105	°C	The extended temperature parts have die junction temperature of -40 to 105°C

Table 3 provides the package thermal characteristics for the 106.

Table 3. Package Thermal Characteristics

Characteristic	Symbol	Value	Rating
CBGA package thermal resistance, junction-to-top of die	θ_{JC}	0.133	°C/W

Note: Refer to Section 1.8, “System Design Information,” for more details about thermal management.

Table 4 provides the DC electrical characteristics for the 106, assuming Vdd = AVdd = 3.3 ± 5% V DC, GND = 0 V DC, and $0 \leq T_j \leq 105$ °C.

Table 4. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSCLK)	V_{IH}	2	5.5	V
Input low voltage (all inputs except SYSCLK)	V_{IL}	GND	0.8	V
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V
SYSCLK input low voltage	CV_{IL}	GND	0.4	V
Input leakage current, V_{in} =3.3 V[1]	I_{in}	—	15.0	µA
Hi-Z (off-state) leakage current, V_{in} = 3.3 V[1]	I_{TSI}	—	15.0	µA
Output high voltage, $I_{OH} = -7$ mA[2]	V_{OH}	2.4	—	V
Output low voltage, $I_{OL} = 7$ mA[2]	V_{OL}	—	0.5	V
PCI 3.3 V signaling output high voltage, $I_{OH} = -0.5$ mA[2]	V_{OH}	2.7	—	V
PCI 3.3 V signaling output low voltage, $I_{OL} = 1.5$ mA[2]	V_{OL}	—	0.3	V
Capacitance, V_{in} = 0 V, f = 1 MHz[3]	C_{in}	—	7.0	pF

Notes:

[1] Excludes test signals (LSSD_MODE and JTAG signals).

[2] This value represents worst case 40-ohm drivers (default value for Processor/L2 control signals $\overline{\text{CI}}$, $\overline{\text{WT}}$, $\overline{\text{GBL}}$, $\overline{\text{TBST}}$, TSIZ[0–2], TT[0–4], $\overline{\text{TWE}}$, and $\overline{\text{TV}}$) only. Other signals have lower default driver impedance and will support larger I_{OH} and I_{OL}. All drivers may optionally be programmed to different driver strengths.

[3] Capacitance is periodically sampled rather than 100% tested.

Table 5 lists the power consumption of the 106.

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Table 5. Power Consumption

Mode	SYSCLK/Core 33/66 MHz	SYSCLK/Core 33/83.3 MHz	Unit
Full-On			
Typical	1.2	2.2	W
Maximum	1.4	2.4	W
Doze			
Typical	1.0	1.1	W
Maximum	1.2	1.4	W
Nap			
Typical	1.0	1.1	W
Maximum	1.2	1.4	W
Sleep			
Typical	260	330	mW
Maximum	360	450	mW
Suspend			
Typical	140	220	mW
Maximum	190	270	mW

Notes:

- Power consumption for common system configurations assuming 50 pF loads
- Suspend power-saving mode assumes SYSCLK off and PLL in bypass mode.
- Typical power is an average value measured at Vdd = AVdd = 3.30 V and T_A = 25 °C.
- Maximum power is measured at Vdd = AVdd = 3.45 V and T_A = 25 °C.

1.4.2 AC Electrical Characteristics

This section provides AC electrical characteristics for the 106. After fabrication, parts are sorted by maximum 60x processor bus frequency, as shown in Section 1.4.2.1, “Clock AC Specifications,” and tested for conformance to the AC specifications for that frequency. These specifications are for operation between 16.67 and 33.33 MHz PCI bus (SYSCLK) frequencies. The 60x processor bus frequency is determined by the PCI bus (SYSCLK) frequency and the settings of the PLL[0–3] signals. All timings are specified relative to the rising edge of SYSCLK.

1.4.2.1 Clock AC Specifications

Table 6 provides the clock AC timing specifications as shown in Figure 2, and assumes Vdd = AVdd = 3.3 ± 5% V DC, GND = 0 V DC, and $0 \leq T_j \leq 105$ °C.

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Table 6. Clock AC Timing Specifications

Num	Characteristic	SYSCLK/Core 33/66 MHz		SYSCLK/Core 33/83.3 MHz		Unit	Notes
		Min	Max	Min	Max		
—	60x processor bus (core) frequency	16.67	66	16.67	83.3	MHz	1
—	VCO frequency	120	200	120	200	MHz	1, 2
—	SYSCLK frequency	16.67	33.33	16.67	33.33	MHz	1
1	SYSCLK cycle time	30.0	60.0	30.0	60.0	ns	—
2, 3	SYSCLK rise and fall time	—	2.0	—	2.0	ns	3
4	SYSCLK duty cycle measured at 1.4 V	40	60	40	60	%	4
—	SYSCLK jitter	—	±200	—	±200	ps	5
—	106 internal PLL relock time	—	100	—	100	µs	4, 6

Notes:

[1] **Caution**: The SYSCLK frequency and PLL[0–3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL[0–3] signal description in Section 1.8, “System Design Information,” for valid PLL[0–3] settings, and to Section 1.9, “Document Revision History,” for available frequencies and part numbers.

[2] VCO operating range for extended temperature devices is different. Refer to MPC106ARXTGPNS/D for more information.

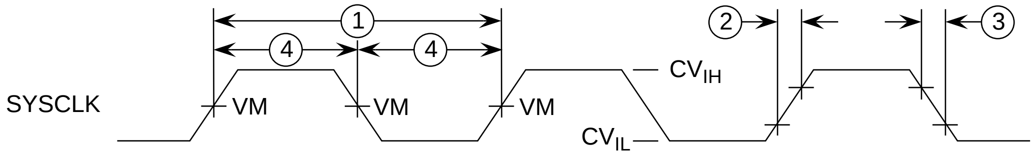
[3] Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.

[4] Timing is guaranteed by design and characterization and is not tested.

[5] The total input jitter (short-term and long-term combined) must be under ±200 ps.

[6] PLL-relock time is the maximum time required for PLL lock after a stable Vdd, AVdd, and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during the sleep and suspend power-saving modes. Also note that $\overline{\text{HRST}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time (100 µs) during the power-on reset sequence.

Figure 2 provides the SYSCLK input timing diagram.



VM = Midpoint Voltage (1.4 V)

Figure 2. SYSCLK Input Timing Diagram

1.4.2.2 Input AC Specifications

Table 7 provides the input AC timing specifications for the 106 as defined in Figure 3 and Figure 4. These specifications are for operation between 16.67 and 33.33 MHz PCI bus clock (SYSCLK) frequencies. Assume Vdd = AVdd = 3.3 ± 5% V DC, GND = 0 V DC, and $0 \leq T_j \leq 105$ °C.

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Table 7. Input AC Timing Specifications

Num	Characteristic	66 MHz		83.3 MHz		Unit	Notes
		Min	Max	Min	Max		
10a	Group I input signals valid to 60x Bus Clock (input setup)	4.0		3.5		ns	1,2,3
10a	Group II input signals valid to 60x Bus Clock (input setup)	3.5		3.5		ns	1,2,4
10a	Group III input signals valid to 60x Bus Clock (input setup)	3.0		2.5		ns	1,2,5
10a	Group IV input signals valid to 60x Bus Clock (input setup)	5.0		4.0		ns	1,2,6
10b	Group V input signals valid to SYSCLK (input setup)	7.0		7.0		ns	7,8
10b	Group VI input signals valid to SYSCLK (input setup)	7.0		7.0		ns	7,9
11a	60x Bus Clock to group I–IV inputs invalid (input hold)	0	—	0	—	ns	3,4,5,6
11b	SYSCLK to group V–VI inputs invalid (input hold)	–0.5	—	–0.5	—	ns	8,9
	$\overline{\text{HRST}}$ pulse width	255 x t_{sysclk} + 100 µs	—	255 x t_{sysclk} + 100 µs	—		—
10c	Mode select inputs valid to $\overline{\text{HRST}}$ (input setup)	3 x t_{sysclk}	—	3 x t_{sysclk}	—	ns	10, 11,12
11c	$\overline{\text{HRST}}$ to mode select input invalid (input hold)	1.0	—	1.0	—	ns	10, 12

Notes:

[1] Input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of SYSCLK. Both input and output timings are measured at the pin (see Figure 3).

[2] Processor and memory interface signals are specified from the rising edge of the 60x bus clock (which is internally synchronized to SYSCLK).

[3] Group I input signals include the following processor, L2, and memory interface signals: A[0–31], PAR[0–7]/AR[1–8], $\overline{\text{BR}}$[0–4], $\overline{\text{BRL2}}$, $\overline{\text{XATS}}$, $\overline{\text{LBCLAIM}}$, $\overline{\text{ADS}}$, BA0, TV and $\overline{\text{HIT}}$ (when configured for external L2)

[4] Group II input signals include the following processor and memory interface signals: $\overline{\text{TBST}}$, TT[0–4], TSIZ[0–2], $\overline{\text{WT}}$, $\overline{\text{CI}}$, $\overline{\text{GBL}}$, $\overline{\text{AACK}}$, and $\overline{\text{TA}}$.

[5] Group III input signals include the following processor and memory interface signals: DL[0–31] and DH[0–31].

[6] Group IV input signals include the following processor and L2 interface signals: $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DIRTY\_IN}}$, and $\overline{\text{HIT}}$ (when configured for internal L2 controller).

[7] PCI 3.3 V signaling environment signals are measured from 1.65 V (Vdd ÷ 2) on the rising edge of SYSCLK to V_{OH} = 3.0 V or V_{OL} = 0.3 V. PCI 5 V signaling environment signals are measured from 1.65 V (Vdd ÷ 2) on the rising edge of SYSCLK to V_{OH} = 2.4 V or V_{OL} = 0.55 V.

[8] Group V input signals include the following bussed PCI interface signals: $\overline{\text{FRAME}}$, $\overline{\text{C/BE}}$[0–3], AD[0–31], $\overline{\text{DEVSEL}}$, $\overline{\text{IRDY}}$, $\overline{\text{TRDY}}$, $\overline{\text{STOP}}$, $\overline{\text{PAR}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{LOCK}}$, $\overline{\text{FLSHREQ}}$, and $\overline{\text{ISA\_MASTER}}$.

[9] Group VI input signal is the point-to-point PCI $\overline{\text{GNT}}$ input signal.

[10] The setup and hold time is with respect to the rising edge of $\overline{\text{HRST}}$ (see Figure 4). Mode select inputs include the $\overline{\text{RCS0}}$, $\overline{\text{FOE}}$, and $\overline{\text{DBG0}}$ configuration inputs.

[11] t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds (ns). When the unit is given as t_{sysclk}, the numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.

[12] These values are guaranteed by design and are not tested.

Figure 3 provides the input timing diagram for the 106.

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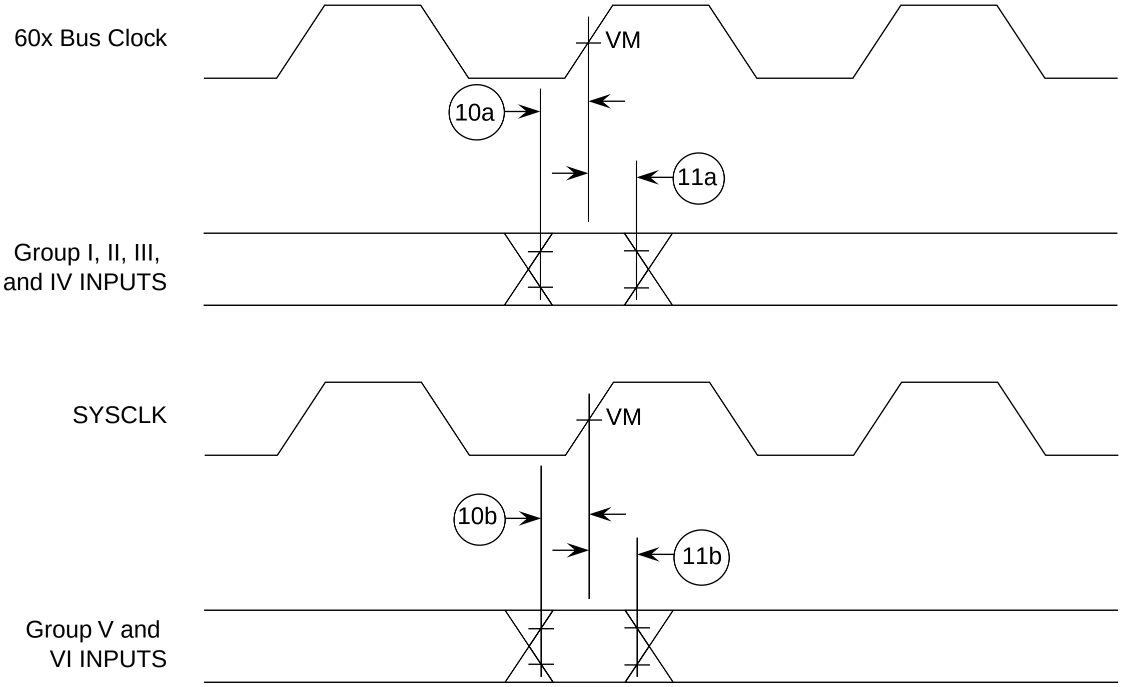
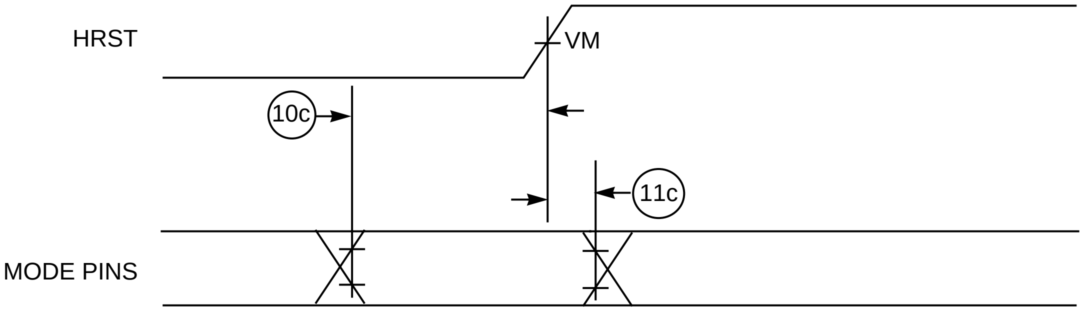


VM = Midpoint Voltage (1.4 V)

Figure 3. Input Timing Diagram

Figure 4 provides the mode select input timing diagram for the 106.



VM = Midpoint Voltage (1.4 V)

Figure 4. Mode Select Input Timing Diagram

1.4.2.3 Output AC Specifications

Table 8 provides the output AC timing specifications for 106 (shown in Table 5). Assume Vdd = AVdd = 3.3 ± 5% V DC, GND = 0 V DC, CL = 50 pF, and $0 \le T_j \le 105$ °C. Processor and memory interface signals are specified from the rising edge of the 60x bus clock (which is internally synchronized to SYSCLK). All units are nanoseconds.

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Table 8. Output AC Timing Specifications

Num	Characteristic	66 MHz		83.3 MHz		Notes
		Min	Max	Min	Max	
12	SYSCLK to output driven (output enable time)	2.0	—	2.0	—	1
13a	SYSCLK to output valid for $\overline{\text{TS}}$ and $\overline{\text{ARTRY}}$	—	7.0	—	6.0	2, 3, 4
13b	SYSCLK to output valid for all non-PCI signals except $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{RAS}}$[0–7], $\overline{\text{CAS}}$[0–7], and DWE[0-2]	—	7.0	—	6.0	2, 3, 5
14a	SYSCLK to output valid (for RAS[0–7] and CAS[0–7])	—	7.0	—	6.0	2, 3
14b	SYSCLK to output valid for PCI signals	—	11.0	—	11.0	3, 6
15a	SYSCLK to output invalid for all non-PCI signals (output hold)	1.0	—	1.0	—	7, 10
15b	SYSCLK to output invalid for PCI signals (output hold)	1.0	—	1.0	—	7
18	SYSCLK to $\overline{\text{ARTRY}}$ high impedance before precharge (output hold)	—	8.0	—	8.0	1
19	SYSCLK to $\overline{\text{ARTRY}}$ precharge enable	(0.4 * t_{sysclk}) + 2.0	—	(0.4 x t_{sysclk}) + 2.0	—	8, 1
21	SYSCLK to $\overline{\text{ARTRY}}$ high impedance after precharge	—	(1.5 * t_{sysclk}) + 8.0	—	(1.5 x t_{sysclk}) + 8.0	8, 1

Notes:

[1] These values are guaranteed by design and are not tested.

[2] Output specifications are measured from 1.4 V on the rising edge of the appropriate clock to the TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin (see Figure 5).

[3] The maximum timing specification assumes C_L = 50 pF.

[4] The shared outputs $\overline{\text{TS}}$ and $\overline{\text{ARTRY}}$ require pull-up resistors to hold them negated when there is no bus master driving them.

[5] When the 106 is configured for asynchronous L2 cache SRAMs, the DWE[0–2] signals have a maximum SYSCLK to output valid time of (0.5 x t_{PROC}) + 8.0 ns (where t_{PROC} is the 60x bus clock cycle time).

[6] PCI 3.3 V signaling environment signals are measured from 1.65 V (Vdd ÷ 2) on the rising edge of SYSCLK to V_{OH} = 3.0 V or V_{OL} = 0.3 V.

[7] The minimum timing specification assumes C_L = 0 pF.

[8] t_{sysclk} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). When the unit is given as t_{sysclk} the numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.

[9] PCI devices which require more than the PCI-specified hold time of T_h = 0ns or systems where clock skew approaches the PCI-specified allowance of 2ns may not work with the MPC106. For workarounds, see Motorola application note *Designing PCI 2.1-Compliant MPC106 Systems* (order number AN1727/D).

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Figure 5 provides the output timing diagram for the 106.

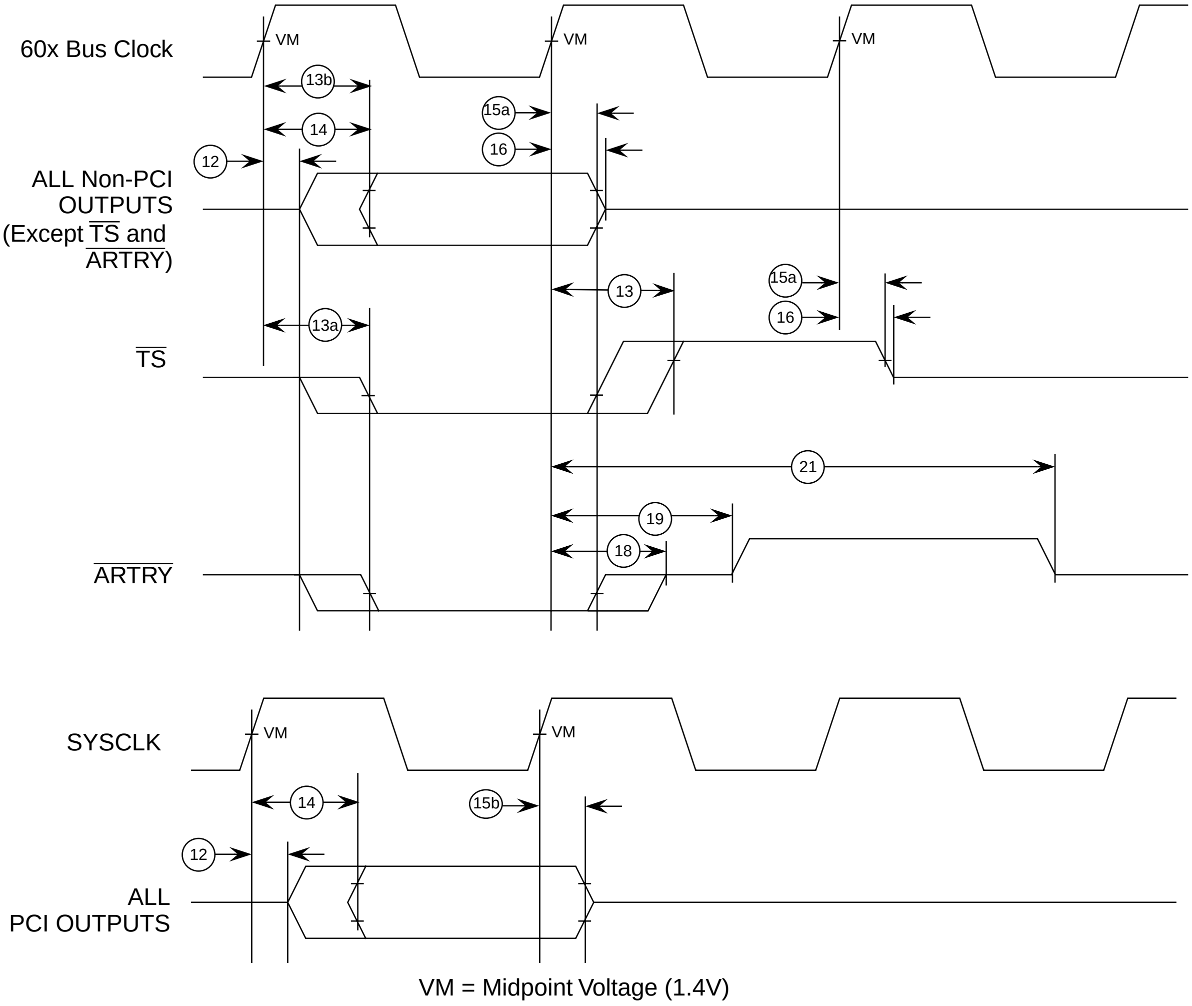

Figure 5. Output Timing Diagram

1.4.3 JTAG AC Timing Specifications

Table 9 provides the JTAG AC timing specifications. Assume Vdd = AVdd = 3.3 ± 5% V DC, GND = 0 V DC, CL = 50 pF, and $0 \leq T_j \leq 105$ °C.

Table 9. JTAG AC Timing Specifications (Independent of SYSCLK)

Num	Characteristic	Min	Max	Unit	Notes
—	TCK frequency of operation	0	25	MHz	—
1	TCK cycle time	40	—	ns	—
2	TCK clock pulse width measured at 1.4 V	20	—	ns	—
3	TCK rise and fall times	0	3	ns	1
4	$\overline{\text{TRST}}$ setup time to TCK rising edge	10	—	ns	2
5	$\overline{\text{TRST}}$ assert time	10	—	ns	1

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Table 9. JTAG AC Timing Specifications (Independent of SYSCLK) (Continued)

Num	Characteristic	Min	Max	Unit	Notes
6	Boundary-scan input data setup time	5	—	ns	3
7	Boundary-scan input data hold time	15	—	ns	3
8	TCK to output data valid	0	30	ns	4
9	TCK to output high impedance	0	30	ns	4
10	TMS, TDI data setup time	5	—	ns	—
11	TMS, TDI data hold time	15	—	ns	1
12	TCK to TDO data valid	0	15	ns	—
13	TCK to TDO high impedance	0	15	ns	—

Notes:

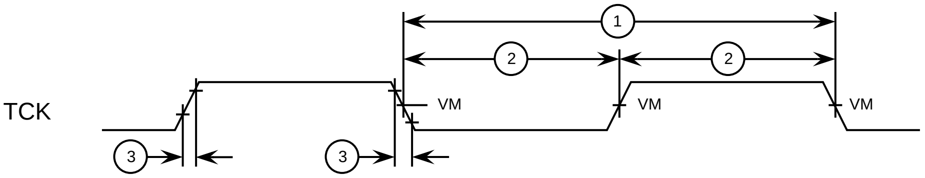
[1] These values are guaranteed by design, and are not tested

[2] $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.

[3] Non-test signal input timing with respect to TCK.

[4] Non-test signal output timing with respect to TCK.

Figure 6 provides the JTAG clock input timing diagram.



VM = Midpoint Voltage (1.4 V)

Figure 6. JTAG Clock Input Timing Diagram

Figure 7 provides the $\overline{\text{TRST}}$ timing diagram.

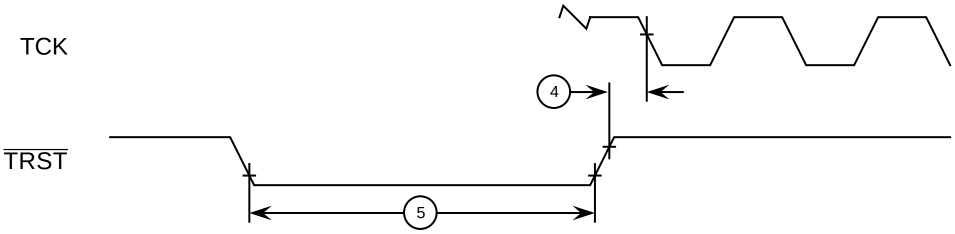


Figure 7. $\overline{\text{TRST}}$ Timing Diagram

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Figure 8 provides the boundary-scan timing diagram.

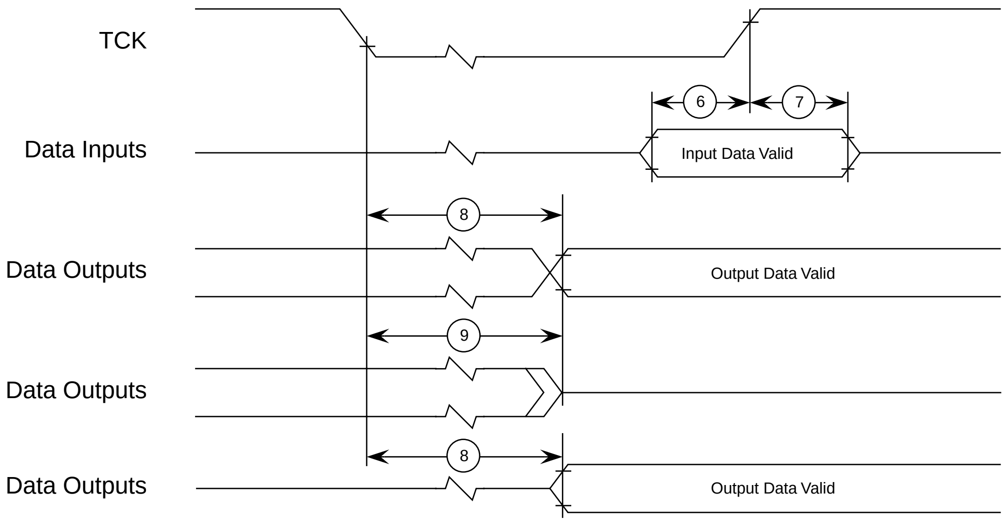

Figure 8. Boundary-Scan Timing Diagram

Figure 9 provides the test access port timing diagram.

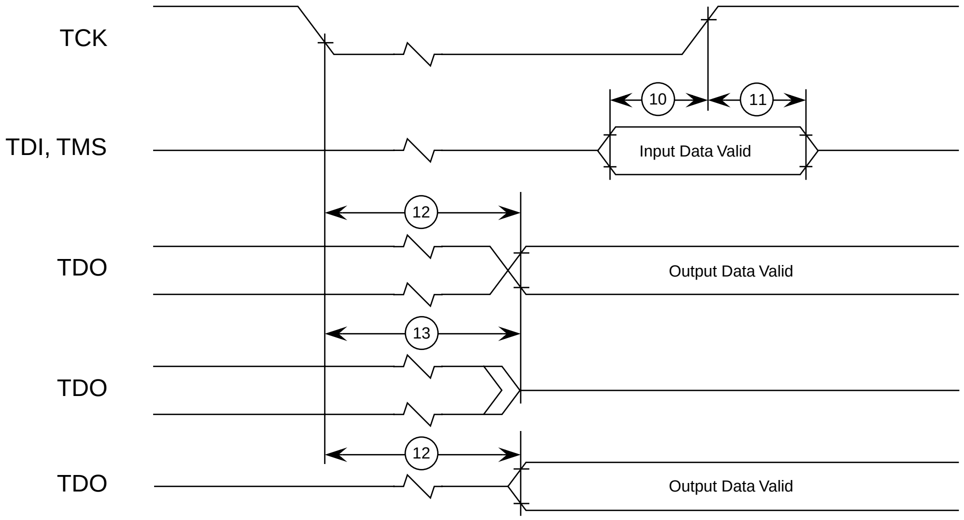

Figure 9. Test Access Port Timing Diagram

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1.5 Pin Assignments

Figure 10 contains the pin assignments for the MPC106, and Figure 11 provides a key to the shading.

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
W	DL26	DL28	DL30	DH31	DH29	DH27	DH25	DH23	DH21	DH19	DH17	DH15	DH13	DH11	DH9	DH7	W
V	DL24	DL27	DL29	DL31	DH30	DH28	DH26	DH24	DH20	DH18	DH16	DH14	DH12	DH10	DH8	DL22	V
U	MA1/SDBA0/AR9	DL23	DL25	DL14	PLL2	PLL0	DL12	DL10	DL4	DL2	DL0	DOE/DBGL2	TOE DBG1	DH6	DL21	DL20	U
T	MA2/SDMA2/AR10	WE	DH0	DL15	PLL3	PLL1	DL13	DL11	DL3	DL1	TV/BR2	BA0/BR3	HIT	DIRTY_IN/BR1	DL19	DCS/BG3	T
R	MA3/SDMA3/AR11	RCS0	DH2	DH1	DL16	Vss	Vdd	DL9	DL5	Vss	Vdd	TWE/BG2	DIRTY_OUT/BG1	ADS/DALE/BRL2	A0	TS	R
P	MA5/SDMA5/AR13	MA4/SDMA4/AR12	DH4	DH3	Vss	Vdd	Vss	DL8	DL6	Vdd	Vss	Vdd	BA1/BAA/BGL2	DWE0/DBG2	A1	XATS/SDMA1	P
N	MA6/SDMA6/AR14	MA0/SDBA1/SDMA0/AR0	DL17	DH5	Vdd	Vss	Vdd	DL7	DH22	Vss	Vdd	Vss	LBCLAIM	CI	A2	TA	N
M	MA8/SDMA8/AR16	MA7/SDMA7/AR15	RAS0/CS0	DL18	Vss	Vdd	Vss	NC	NC	Vdd	Vss	Vdd	WT	GBL	A3	TT4	M
L	HRST	MA9/SDMA9/AR17	QACK	RAS1/CS1	Vdd	CKO/DWE2	RAS5/CS5	Vss	Vdd	Vss	SYSCLK	DBG0	TBST	BR0	A4	TT3	L
K	MA11/SDMA11/AR19	MA10/SDMA10/AR18	RAS3/CS3	RAS2/CS2	RAS4/CS4	RAS7/CS7	Vdd	AVdd	Vss	Vdd	A9	A8	A7	BG0	A5	TT2	K
J	MA12/SDMA12/AR20	CAS0/DQM0	PPEN	RCS1	RAS6/CS6	MCP	DBGLB/CKE	Vss	Vdd	Vss	A11	A6	A13	A12	A10	TEA	J
H	QREQ	CAS1/DQM1	SUSPEND	TRST	Vss	DWE1/DBG3	PIRQ/SDRAS	NC	NC	Vdd	Vss	Vdd	A15	A14	A16	TT1	H
G	CAS2/DQM2	RTC	CAS4/DQM4	CAS5/DQM5	Vdd	LSSD_MODE	Vdd	PAR	LOCK	Vss	Vdd	Vss	TSIZ1	TSIZ0	A17	TT0	G
F	BCTL0	BCTL1	CAS6/DQM6	TCK	Vss	Vdd	Vss	PERR	DEVSEL	Vdd	Vss	Vdd	A21	TSIZ2	ARTRY	A18	F
E	CAS3/DQM3	NMI	CAS7/DQM7	MDLE/SDCAS	TDO	Vss	Vdd	SERR	IRDY	Vss	Vdd	A31	A29	A22	A20	A19	E
D	PAR0/AR1	PAR1/AR2	TMS	FOE	AD28	AD24	AD21	AD17	AD14	AD10	C/BE0	AD4	AD0	A30	AACK	A23	D
C	PAR2/AR3	PAR3/AR4	PAR5/AR6	AD30	AD26	AD23	AD19	C/BE2	C/BE1	AD12	AD8	AD6	AD2	A27	A25	A24	C
B	PAR4/AR5	PAR7/AR8	AD1	TDI	AD7	AD11	AD15	TRDY	AD18	AD22	AD25	AD29	REQ	ISA_MASTER/BERR	A28	A26	B
A	PAR6/AR7	GNT	AD3	AD5	AD9	AD13	FRAME	STOP	AD16	AD20	C/BE3	AD27	AD31	FLSHREQ	MEMACK		A
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 10. Pin Assignments

NC	No Connect
Vss	Power Supply Ground
Vdd	Power Supply Positive
AVdd	Clock Power Supply Positive (K9)
☐	Signals

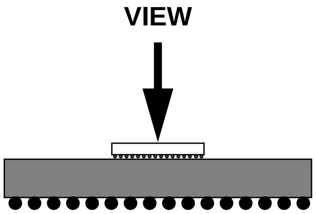

Figure 11. Pin Assignments Shading Key

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1.6 Pinout Listings

Table 10 provides the pinout listing for the MPC106. Some signals have dual functions and are shown more than once.

Table 10. Pinout Listing

Signal Name	Pin Number	Active	I/O
60x Processor Interface Signals			
A[0–31]	R2, P2, N2, M2, L2, K2, J5, K4, K5, K6, J2, J6, J3, J4, H3, H4, H2, G2, F1, E1, E2, F4, E3, D1, C1, C2, B1, C3, B2, E4, D3, E5	High	I/O
$\overline{\mathrm{AACK}}$	D2	Low	I/O
$\overline{\mathrm{ARTRY}}$	F2	Low	I/O
$\overline{\mathrm{BG0}}$	K3	Low	Output
$\overline{\mathrm{BG1}}$ ($\overline{\mathrm{DIRTY\_OUT}}$)	R4	Low	Output
$\overline{\mathrm{BG2}}$ ($\overline{\mathrm{TWE}}$)	R5	Low	Output
$\overline{\mathrm{BG3}}$ ($\overline{\mathrm{DCS}}$)	T1	Low	Output
$\overline{\mathrm{BR0}}$	L3	Low	Input
$\overline{\mathrm{BR1}}$ ($\overline{\mathrm{DIRTY\_IN}}$)	T3	Low	Input
$\overline{\mathrm{BR2}}$ (TV)	T6	Low	Input
$\overline{\mathrm{BR3}}$ (BA0)	T5	Low	Input
$\overline{\mathrm{CI}}$	N3	Low	I/O
$\overline{\mathrm{DBG0}}$	L5	Low	Output
$\overline{\mathrm{DBG1}}$ ($\overline{\mathrm{TOE}}$)	U4	Low	Output
$\overline{\mathrm{DBG2}}$ ($\overline{\mathrm{DWE0}}$)	P3	Low	Output
$\overline{\mathrm{DBG3}}$ ($\overline{\mathrm{DWE1}}$)	H11	Low	Output
$\overline{\mathrm{DBGLB}}$ (CKE)	J10	Low	Output
DH[0–31]	T14, R13, R14, P13, P14, N13, U3, W1, V2, W2, V3, W3, V4, W4, V5, W5, V6, W6, V7, W7, V8, W8, N8, W9, V9, W10, V10, W11, V11, W12, V12, W13	High	I/O
DL[0–31]	U6, T7, U7, T8, U8, R8, P8, N9, P9, R9, U9, T9, U10, T10, U13, T13, R12, N14, M13, T2, U1, U2, V1, U15, V16, U14, W16, V15, W15, V14, W14, V13	High	I/O
$\overline{\mathrm{GBL}}$	M3	Low	I/O

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Table 10. Pinout Listing (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{LBCLAIM}}$	N4	Low	Input
$\overline{\text{MCP}}$	J11	Low	Output
$\overline{\text{TA}}$	N1	Low	I/O
$\overline{\text{TBST}}$	L4	Low	I/O
$\overline{\text{TEA}}$	J1	Low	Output
$\overline{\text{TS}}$	R1	Low	I/O
TSIZ[0–2]	G3, G4, F3	High	I/O
TT[0–4]	G1, H1, K1, L1, M1	High	I/O
$\overline{\text{WT}}$	M4	Low	I/O
$\overline{\text{XATS}}$ (SDMA1)	P1	Low	Input
L2 Cache Interface Signals			
$\overline{\text{ADS}}$/$\overline{\text{DALE}}$/$\overline{\text{BRL2}}$	R3	Low	I/O
BA0 ($\overline{\text{BR3}}$)	T5	Low	Output
BA1/$\overline{\text{BAA}}$/$\overline{\text{BGL2}}$	P4	Low	Output
$\overline{\text{DBGL2}}$/$\overline{\text{DOE}}$	U5	Low	Output
$\overline{\text{DCS}}$ ($\overline{\text{BG3}}$)	T1	Low	Output
$\overline{\text{DIRTY\_IN}}$ ($\overline{\text{BR1}}$)	T3	Low	Input
$\overline{\text{DIRTY\_OUT}}$ ($\overline{\text{BG1}}$)	R4	Low	Output
$\overline{\text{DWE0}}$ ($\overline{\text{DBG2}}$)	P3	Low	Output
$\overline{\text{DWE1}}$ (DBG3)	H11	Low	Output
$\overline{\text{DWE2}}$ (CKO)	L11	Low	Output
$\overline{\text{HIT}}$	T4	Low	Input
$\overline{\text{TOE}}$ ($\overline{\text{DBG1}}$)	U4	Low	Output
TV ($\overline{\text{BR2}}$)	T6	High	I/O
$\overline{\text{TWE}}$ ($\overline{\text{BG2}}$)	R5	Low	Output
Memory Interface Signals			
$\overline{\text{BCTL}}$[0–1]	F16, F15	Low	Output
$\overline{\text{BERR}}$ ($\overline{\text{ISA\_MASTER}}$)	B3	Low	Input

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Table 10. Pinout Listing (Continued)

Signal Name	Pin Number	Active	I/O
CAS/DQM[0–7]	J15, H15, G16, E16, G14, G13, F14, E14	Low	Output
CKE/DBGLB	J10	High	Output
FOE	D13	Low	Output
MA0/SDBA1/SDMA0/AR0	N15	High	Output
SDMA1 (XATS)	P1	High	Output
MA1/SDBA0/AR9	U16	High	Output
MA[2–12]/SDMA[2–12]/AR[10–20]	T16, R16, P15, P16, N16, M15, M16, L15, K15, K16, J16	High	Output
MDLE/SDCAS	E13	Low	Output
PAR[0–7]/AR[1–8]	D16, D15, C16, C15, B16, C14, A16, B15	High	I/O
PPEN	J14	Low	Output
RAS/CS[0–7]	M14, L13, K13, K14, K12, L10, J12, K11	Low	Output
RCS0	R15	Low	I/O
RCS1	J13	Low	Output
RTC	G15	High	Input
SDRAS (PIRQ)	H10	Low	Output
WE	T15	Low	Output
PCI Interface Signals1			
AD[31–0]	A4, C13, B5, D12, A5, C12, B6, D11, C11, B7, D10, A7, C10, B8, D9, A8, B10, D8, A11, C7, B11, D7, A12, C6, B12, C5, A13, D5, A14, C4, B14, D4	High	I/O
C/BE[3–0]	A6, C9, C8, D6	Low	I/O
DEVSEL	F8	Low	I/O
FLSHREQ	A3	Low	Input
FRAME	A10	Low	I/O
GNT	A15	Low	Input
IRDY	E8	Low	I/O
ISA_MASTER (BERR)	B3	Low	Input
LOCK	G8	Low	Input
MEMACK	A2	Low	Output
PAR	G9	High	I/O
PERR	F9	Low	I/O
PIRQ (SDRAS)	H10	Low	Output
REQ	B4	Low	Output

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Table 10. Pinout Listing (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{SERR}}$	E9	Low	I/O
$\overline{\text{STOP}}$	A9	Low	I/O
$\overline{\text{TRDY}}$	B9	Low	I/O
Interrupt, Clock, and Power Management Signals			
CKO ($\overline{\text{DWE2}}$)	L11	High	Output
$\overline{\text{HRST}}$	L16	Low	Input
NMI	E15	High	Input
$\overline{\text{QACK}}$	L14	Low	Output
$\overline{\text{QREQ}}$	H16	Low	Input
SYSCLK	L6	Clock	Input
$\overline{\text{SUSPEND}}$	H14	Low	Input
Test/Configuration Signals			
PLL[0–3]	U11, T11, U12, T12	High	Input
TCK	F13	Clock	Input
TDI	B13	High	Input
TDO	E12	High	Output
TMS	D14	High	Input
$\overline{\text{TRST}}$	H13	Low	Input
Power and Ground Signals			
AVdd	K9	High	Clock Power
$\overline{\text{LSSD\_MODE}}$ [2]	G11	Low	Input
Vdd	E10, E6, F11, F5, F7, G10, G12, G6, H5, H7, K10, K7, L12, M11, M5, M7, N10, N12, N6, P11, P5, P7, R10, R6, J8, L8	High	Power
Vss	E11, E7, F10, F12, F6, G5, G7, H12, H6, J7, L7, M10, M12, M6, N11, N5, N7, P10, P12, P6, R11, R7, K8, J9, L9	Low	Ground
NC	H8, H9, M8, M9	—	—

Note:

[1] All PCI signals are in little-endian bit order.

[2] This test signal is for factory use only. It must be pulled up to Vdd for normal device operation.

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1.7 Package Description

The following sections provide the package parameters and the mechanical dimensions for the 106.

1.7.1 Package Parameters

The package parameters are as provided in the following list. The package type is a 21 mm x 25 mm, 304-lead C4 ceramic ball grid array (CBGA).

Package outline	21 mm x 25 mm
Interconnects	303 (16 x 19 ball array minus one)
Pitch	1.27 mm
Solder attach	63/37 Sn/Pb
Solder balls	10/90 Sn/Pb, 0.89 mm diameter
Maximum module height	3.16 mm
Co-planarity specification	0.15 mm

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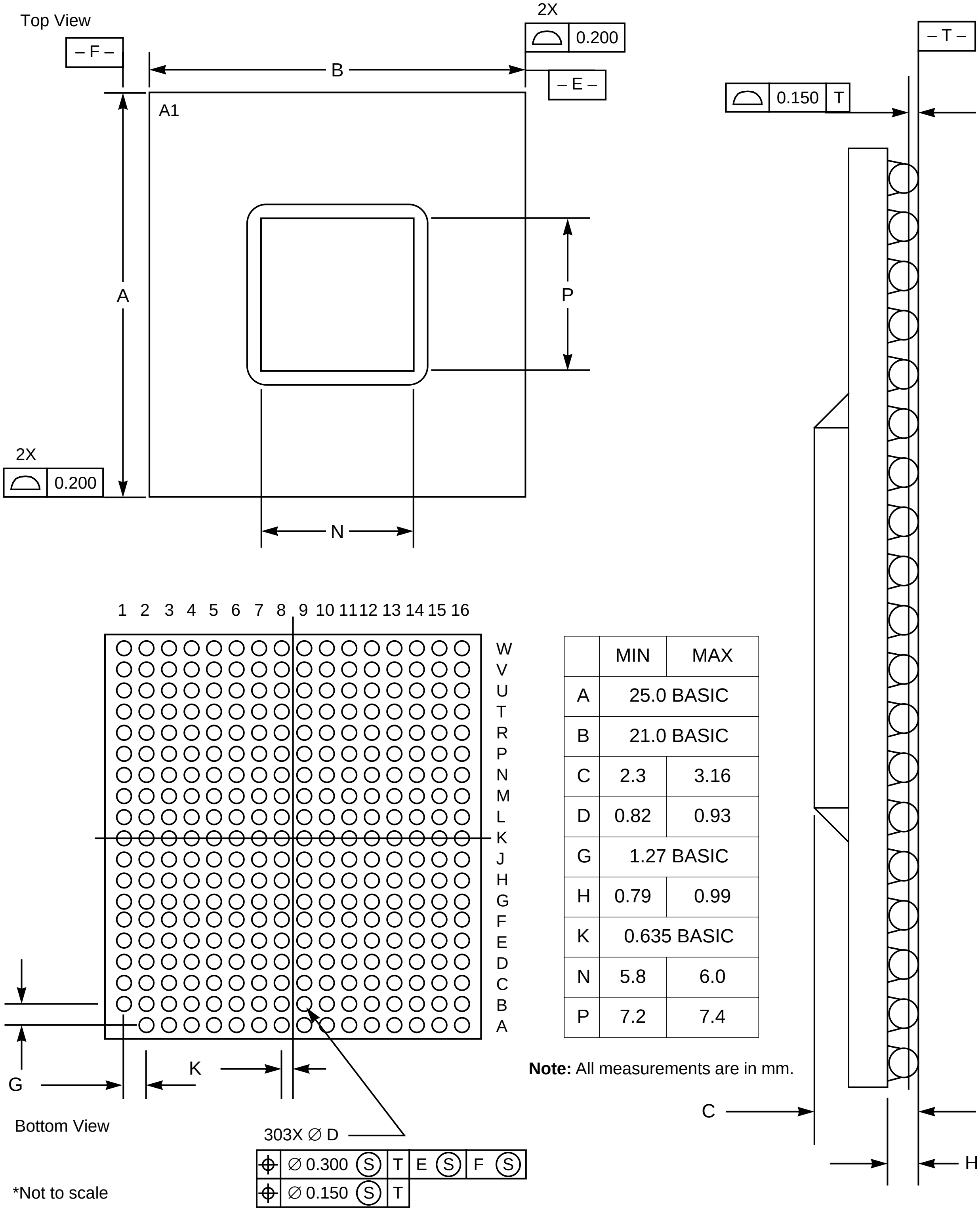
1.7.2 Mechanical Dimensions

Figure 12 shows the mechanical dimensions for the MPC106.



	MIN	MAX
A	25.0 BASIC	
B	21.0 BASIC	
C	2.3	3.16
D	0.82	0.93
G	1.27 BASIC	
H	0.79	0.99
K	0.635 BASIC	
N	5.8	6.0
P	7.2	7.4

Note: All measurements are in mm.

*Not to scale

Figure 12. Mechanical Dimensions

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1.8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the 106.

1.8.1 PLL Configuration

The 106 requires a single system clock input, SYSCLK. The SYSCLK frequency dictates the frequency of operation for the PCI bus. An internal PLL on the MPC106 generates a master clock that is used for all of the internal (core) logic. The master clock provides the core frequency reference and is phase-locked to the SYSCLK input. The 60x processor, L2 cache, and memory interfaces operate at the core frequency. In the 5:2 clock mode (Rev. 4.0 only), the MPC106 needs to sample the 60x bus clock (on the $\overline{\text{LBCLAIM}}$ configuration input) to resolve clock phasing with the PCI bus clock (SYSCLK).

The PLL is configured by the PLL[0–3] signals. For a given SYSCLK (PCI bus) frequency, the clock mode configuration signals (PLL[0–3]) set the core frequency (and the frequency of the VCO controlling the PLL lock). The supported core and VCO frequencies and the corresponding PLL[0–3] settings are provided in Table 11.

Table 11. PLL Configuration

PLL[0–3][1]	Core/SYSCLK Ratio	VCO Multiplier	Core Frequency (VCO Frequency) in MHz			
			PCI Bus 16.6 MHz	PCI Bus 20 MHz	PCI Bus 25 MHz	PCI Bus 33.3 MHz
0001	1:1	x4	—	—	—	33.3 (133)
0100	2:1	x2	—	—	—	66.6 (133)
0101	2:1	x4	33.3 (133)	40 (160)	50 (200)	—
0110	5:2 [2]	x2	—	—	—	83.3 (166)
0111	5:2 [2]	x4	41.6 (166)	—	—	—
1000	3:1	x2	—	60(120)	75 (150)	—
0011	PLL-bypass [3]		PLL off SYSCLK clocks core circuitry directly 1x core/SYSCLK ratio implied			
1111	Clock off [4]		PLL off no core clocking occurs			

Notes:

[1] PLL[0–3] settings not listed are reserved. Some PLL configurations may select bus, CPU, or VCO frequencies which are not useful, not supported, or not tested. See Section 1.4.2.1, “Clock AC Specifications,” for valid SYSCLK and VCO frequencies.

[2] 5:2 clock modes are only supported by MPC106 Rev 4.0; earlier revisions do not support 5:2 clock modes. The 5:2 modes require a 60x bus clock applied to the 60x clock phase ($\overline{\text{LBCLAIM}}$) configuration input signal during power-on reset, hard reset, and coming out of sleep and suspend power-saving modes.

[3] In PLL-bypass mode, the SYSCLK input signal clocks the internal circuitry directly, the PLL is disabled, and the core/SYSCLK ratio is set for 1:1 mode operation. This mode is intended for factory use and third-party tool vendors only. **Note also**: The AC timing specifications given in this document do not apply in PLL-bypass mode.

[4] In clock-off mode, no clocking occurs inside the MPC106 regardless of the SYSCLK input.

[5] PLL[0-3] = 0010 (2:1 Core/SYSCLK Ratio; X8 VCO multiplier) exists on the chip but will fail to lock 50% of the time. Therefore, this configuration should not be used and 1:1 modes between 16-25MHz are not supported.

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1.8.2 PLL Power Supply Filtering

The AVdd power signal is provided on the 106 to provide power to the clock generation phase-locked loop. To ensure stability of the internal clock, the power supplied to the AVdd input signal should be filtered using a circuit similar to the one shown in Figure 13. The circuit should be placed as close as possible to the AVdd pin to ensure it filters out as much noise as possible.

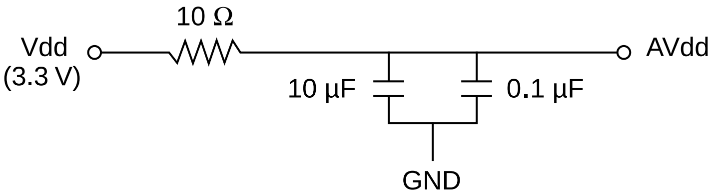

Figure 13. PLL Power Supply Filter Circuit

1.8.3 Decoupling Recommendations

Due to the 106's large address and data buses and high operating frequencies, it can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the system, and the 106 itself requires a clean, tightly regulated source of power.

It is strongly recommended that the system design include six to eight 0.1 µF (ceramic) and 10 µF (tantalum) decoupling capacitors to provide both high- and low-frequency filtering. These capacitors should be placed closely around the perimeter of the 106 package (or on the underside of the PCB). It is also recommended that these decoupling capacitors receive their power from separate Vdd and GND power planes in the PCB, utilizing short traces to minimize inductance. Only surface mount technology (SMT) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the Vdd plane, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 µF (AVX TPS tantalum) or 330 µF (AVX TPS tantalum).

1.8.4 Connection Recommendations

To ensure reliable operation, it is recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied (using pull-up resistors) to Vdd. Unused active high inputs should be tied (using pull-down resistors) to GND. All no-connect (NC) signals must remain unconnected.

Power and ground connections must be made to all external Vdd, AVdd, and GND pins of the 106.

1.8.4.1 Pull-up Resistor Recommendations

The MPC106 requires pull-up (or pull-down) resistors on several control signals of the 60x and PCI buses to maintain the control signals in the negated state after they have been actively negated and released by the 106 or other bus masters. The JTAG test reset signal, $\overline{\text{TRST}}$, should be pulled down during normal system operation. Also, as indicated in Table 10, the factory test signal, $\overline{\text{LSSD\_MODE}}$, must be pulled up for normal device operation

During inactive periods on the bus, the address and transfer attributes on the bus (A[0–31], TT[0–4], $\overline{\text{TBST}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, and $\overline{\text{GBL}}$) are not driven by any master and may float in the high-impedance state for relatively long periods of time. Since the MPC106 must continually monitor these signals, this float

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condition may cause excessive power draw by the input receivers on the MPC106 or by other receivers in the system. It is recommended that these signals be pulled up or restored in some manner by the system.

The 60x data bus input receivers on the MPC106 do not require pull-up resistors on the data bus signals (DH[0–31], DL[0–31], and PAR[0–7]). However, other data bus receivers in the system may require pull-up resistors on these signals.

In general, the 60x address and control signals are pulled up to 3.3 VDC and the PCI control signals are pulled up to 5 VDC through weak (2–10 kΩ) resistors. Resistor values may need to be adjusted stronger to reduce induced noise on specific board designs. Table 12 summarizes the pull-up/pull-down recommendations for the MPC106.

Table 12. Pull-Up/Pull-Down Recommendations

Signal Type	Signals	Pull-Up/Pull-Down
60x bus control	$\overline{\mathrm{BR}n}$ $\overline{\mathrm{TS}}$, $\overline{\mathrm{XATS}}$, $\overline{\mathrm{AACK}}$ $\overline{\mathrm{ARTRY}}$ $\overline{\mathrm{TA}}$	Pull up to 3.3 VDC
60x bus address/transfer attributes	A[0–31], TT[0–4], $\overline{\mathrm{TBST}}$ $\overline{\mathrm{WT}}$, $\overline{\mathrm{CI}}$, $\overline{\mathrm{GBL}}$	Pull up to 3.3 VDC
Cache control	ADS	Pull up to 3.3 VDC
	HIT, TV	Pull up to 3.3 VDC or pull-down to GND depending on programmed polarity
PCI bus control	$\overline{\mathrm{REQ}}$ $\overline{\mathrm{FRAME}}$, $\overline{\mathrm{IRDY}}$ $\overline{\mathrm{DEVSEL}}$, $\overline{\mathrm{TRDY}}$, $\overline{\mathrm{STOP}}$ $\overline{\mathrm{SERR}}$, $\overline{\mathrm{PERR}}$ $\overline{\mathrm{LOCK}}$ $\overline{\mathrm{FLSHREQ}}$, $\overline{\mathrm{ISA\_MASTER}}$.	Typically pull up to 5 VDC Note: For closed systems not requiring 5V power, these may be pulled up to 3.3 VDC.
JTAG	TRST	Pull down to GND (during normal system operation)
Factory test	LSSD_MODE	Pull up to 3.3 VDC

1.8.5 Thermal Management Information

This section provides thermal management information for the C4/CBGA package. Proper thermal control design is primarily dependent on the system-level design.

The use of C4 die on a CBGA interconnect technology offers significant reduction in both the signal delay and the microelectronic packaging volume. Figure 14 shows the salient features of the C4/CBGA interconnect technology. The C4 interconnection provides both the electrical and the mechanical connections for the die to the ceramic substrate. After the C4 solder bump is reflowed, epoxy (encapsulant) is under-filled between the die and the substrate. Under-fill material is commonly used on large high-power die; however, this is not a requirement of the C4 technology. The package substrate is a multilayer-cofired ceramic. The package-to-board interconnection is by an array of orthogonal 90/10 (lead/tin) solder balls on 1.27 mm pitch. During assembly of the C4/CBGA package to the board, the high-melt balls do not collapse.

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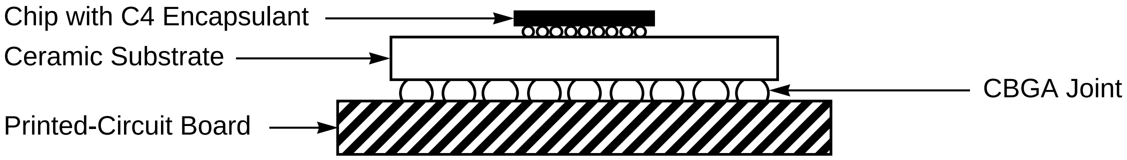

Figure 14. Exploded Cross-Sectional View

1.8.5.1 Internal Package Conduction Resistance

For this C4/CBGA packaging technology, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lead thermal resistance

These parameters are shown in Table 13. In this C4/CBGA package, the silicon chip is exposed; therefore, the package "case" is the top of the silicon.

Table 13. Thermal Resistance

Thermal Metric	Effective Thermal Resistance
Junction-to-case thermal resistance	0.133 °C/W
Junction-to-lead (ball) thermal resistance	3.8 °C/W

Figure 15 provides a simplified thermal network in which a C4/CBGA package is mounted to a printed-circuit board.

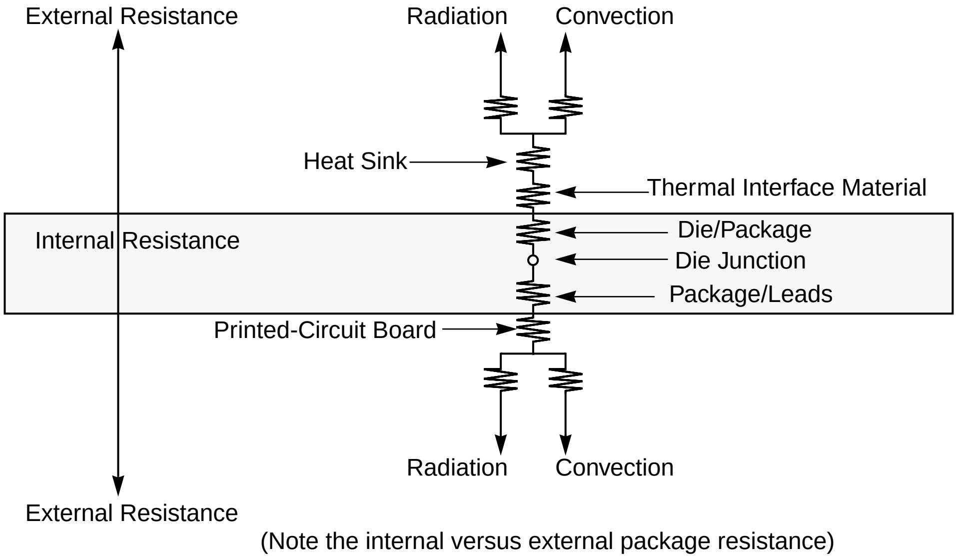

Figure 15. C4/CBGA Package Mounted to a Printed-Circuit Board

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1.8.5.2 Board and System-Level Modeling

A common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies is the junction-to-ambient thermal resistance. The final chip-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature. For example, these factors might include airflow, board population, heat sink efficiency, heat sink attach, next-level interconnect technology, and system air temperature rise.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For this reason, we recommend using conjugate heat transfer models for the board as well as system-level designs. To expedite system-level thermal analysis, several "compact" CBGA thermal models are available on request within FLOTHERM®.

The die junction-to-ambient thermal resistance is shown in Table 14. The model results are in accordance with SEMI specification G38. This standard specifies a single component be placed on a 7.5 cm x 10 cm single-layer printed-circuit card. Note that this single metric may not adequately describe three-dimensional heat flow.

Table 14. Die Junction-to-Ambient Thermal Resistance

Airflow Velocity (Meter/Second)	Airflow Velocity (Feet/Minute)	Die Junction-to-Ambient Thermal Resistance (SEMI G38) (°C/W)
1	196.8	22.0
2	393.7	18.5
3	590.0	17.0

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1.9 Document Revision History

Table 15 lists significant changes between revisions of this document.

Table 15. Document Revision History

Document Revision	Substantive Change(s)
Rev 0	Initial release
Rev 1	Changed VCO maximum frequency in Table 6 to 200 MHz
	Changed input and Hi-Z leakage current in Table 4. from 10µA to 15µA
	Changed I_{OH} and I_{OL} in Table 4 from 18mA and 14mA respectively to -7mA and 7mA to correct the sign and reduce the current to worst case value for the lowest strength default driver
	Changed footnote 4 to Table 6 to be consistent with SYSCLK jitter spec of 200ps
	Modified Table 7, Figure 3, Table 8, and Figure 5 to clarify reference clock (60x Bus Clock or SYSCLK) for input and output specifications
	Changed Group I and Group II signals input setup requirement for 83 MHz in Table 7 from 3.0 ns to 3.5 ns min.
	Changed Group I-IV (non-PCI signals) input hold requirement (Spec 11a) in Table 7 from 1.0 ns to 0 ns
	Changed Group V and VI (PCI signals) input hold requirement (Spec 11b) in Table 7 from 1.0ns to -0.5ns
	Changed output valid times for all non-PCI signals (Specs 13a, 13b and 14a) from 8 ns to 7 ns at 66 Mhz and from 7 ns to 6 ns at 83 MHz
	Corrected Figure 10 to reflect TOE signal is shared with DBG1 on pin U5
Rev 2	Changed input and Hi-Z leakage current, V_{in} in Table 4 from 5.5V to 3.3V
	Changed the power consumption data in Table 5
	Changed note 7 of Table 8 to show the minimum timing specification assumes CL=0 pF
Rev 3	Deleted PLL[0-3] = 0010 from Table 11 to remove 1:1 mode operation between 16MHz and 25MHz
	Added note 10 to Table 8 regarding PCI hold time
	Lowered PCI 3.3V signalling output high voltage from 3.0 V to 2.7V and added current conditions for PCI 3.3V VOH and VOL in Table 4 to reflect current production test
	Included note 12 in Specification 10c of Table 4; Clarified note 9 in Table 8 and included in Specification 12 and 18; Added a similar “guaranteed by design and not tested” note to Table 9 and included in Specifications 3, 7, and 11. All to reflect current production test.
	Corrected Figure 12 dimensions from TBD to actual die size
	Table 1 and Table 2 include notes on extended temperature parts.
Rev 4	Table 8, Note 8 changed to include: “These values are guaranteed by design and are not tested.”
Rev 5	Added PNS references below Table 1 and Table 6. Changed footnote ordering in Table 8, Table 9, and Table 10. Added new footnote 2 to Table 6. Changed part number key.

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1.10 Ordering Information

Figure 16 provides the Motorola part-numbering nomenclature for the 106. In addition to the core frequency, the part numbering scheme also consists of a part modifier and application modifier. The part modifier indicates any enhancements in the part from the original production design. The application modifier may specify special bus frequencies or application conditions. Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part-numbering scheme for identification purposes only.

MPC	**106**	**A**	**RX**	***xx***	***x***	***x***
Product Code	**Part Identifier**	**Part Modifier**	**Package**	**Frequency**	**Application Modifier**	**Revision Level**[2]
			RX = BGA	66 or 83	C No 5:2 mode D 5:2 mode T Extended temperature[1]	E 3.0 G 4.0

Notes:

[1] See Part Number Specifications (MPC106ARXTGPNS/D).

[2] For current revision level, contact local Motorola sales office.

Figure 16. Part Number Key

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