FINAL

# Am386®SX/SXL/SXLV

## High-Performance, Low-Power, Embedded Microprocessors

## DISTINCTIVE CHARACTERISTICS

- **Member of the E86™ CPU series**
  - 16-bit data bus
  - 24-bit address bus
  - 16-Mbyte address range
  - Long-term stable supply from AMD
- **40-, 33- and 25-MHz operating speeds**
- **Ideal for embedded applications**
  - True Static design for low-power applications
  - 3–5 V operation (at 25 MHz)
  - Ideal for cost-sensitive designs
  - True DC (0 MHz) operation
- **Industry Standard Architecture**
  - Supports world's largest software base for x86 architectures
  - Wide range of chipsets and BIOS available
  - Fully compatible with all 386SX systems and software
- **System Management Mode (SMM) for system and power management (Am386SXLV only)**
  - System Management Interrupt (SMI) for power management independent of processor operating mode and operating system
  - SMI coupled with I/O instruction break feature provides transparent power off and auto resume of peripherals which may not be "power aware"
  - SMI is non-maskable and has higher priority than Non-Maskable Interrupt (NMI)
  - Automatic save and restore of the microprocessor state
- **100-lead Plastic Quad Flat Pack (PQFP) package**
- **Extended temperature version available**

## GENERAL DESCRIPTION

The Am386®SX/SXL/SXLV microprocessors are low-cost, high-performance CPUs for embedded applications. Embedded customers benefit from using the Am386 microprocessor in a number of ways.

The Am386SX/SXL/SXLV microprocessors provide embedded customers access to very inexpensive processors and the highest performance of any 386SX available anywhere. The 16-bit data path allows for inexpensive memory design. Full static operation, coupled with 3-V supplies, benefit customers who desire low-power designs. Standby Mode allows the Am386SXL/SXLV microprocessors to be clocked down to 0 MHz (DC) and retain full register contents. A float pin places all outputs in a three-state mode to facilitate board test and debug.

Additionally, the Am386SXLV microprocessor comes with System Management Mode (SMM) for system and power management. SMI (System Management Interrupt) is a non-maskable, higher priority interrupt than NMI and has its own code space (1 Mbyte in Real Mode and 16 Mbyte in Protected Mode). SMI can be coupled with the I/O instruction break feature to implement transparent power management of peripherals. SMM can be used by system designers to implement system and power management code independent of the operating system or the processor mode.

Since the Am386SX/SXL/SXLV microprocessors are supported as an embedded product in the E86 family, customers can rely on long-term supply of product, and extended temperature products.

In addition, customers have access to the largest selection of inexpensive development tools, compilers, and chipsets. A large number of PC operating systems and Real Time Operating Systems (RTOS) support the Am386SX/SXL/SXLV microprocessors. This means cheaper development costs, and improved time to market.

The Am386SX/SXL/SXLV microprocessor is available in a small footprint 100-pin Plastic Quad Flat Pack (PQFP) package.

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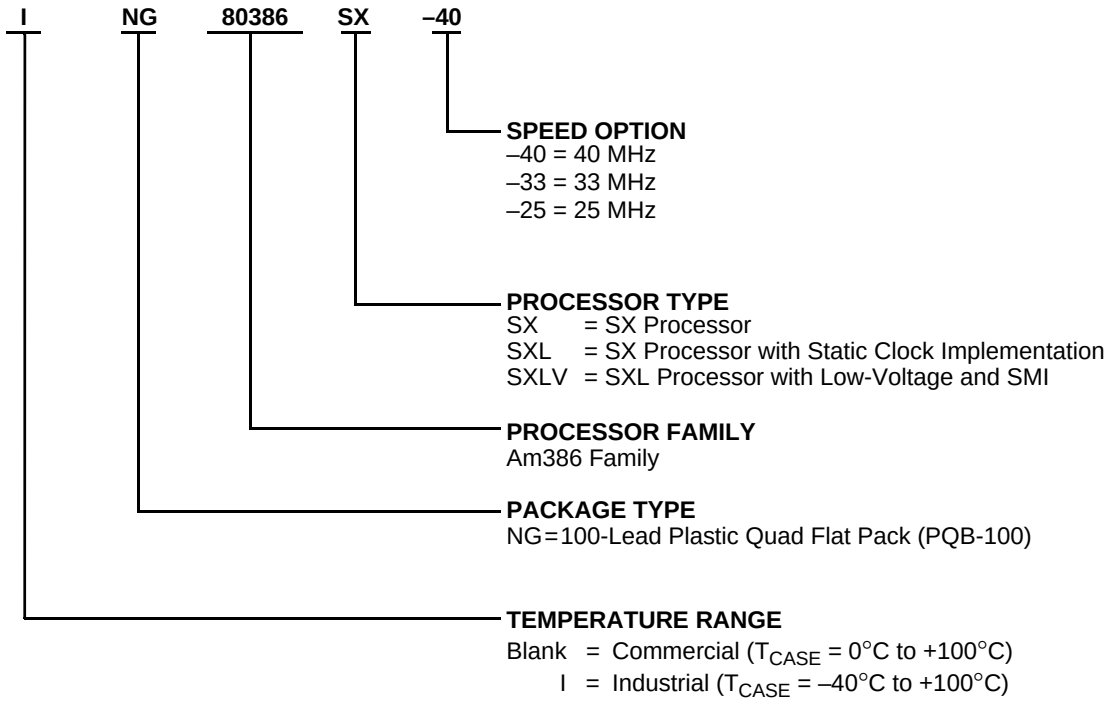
# ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

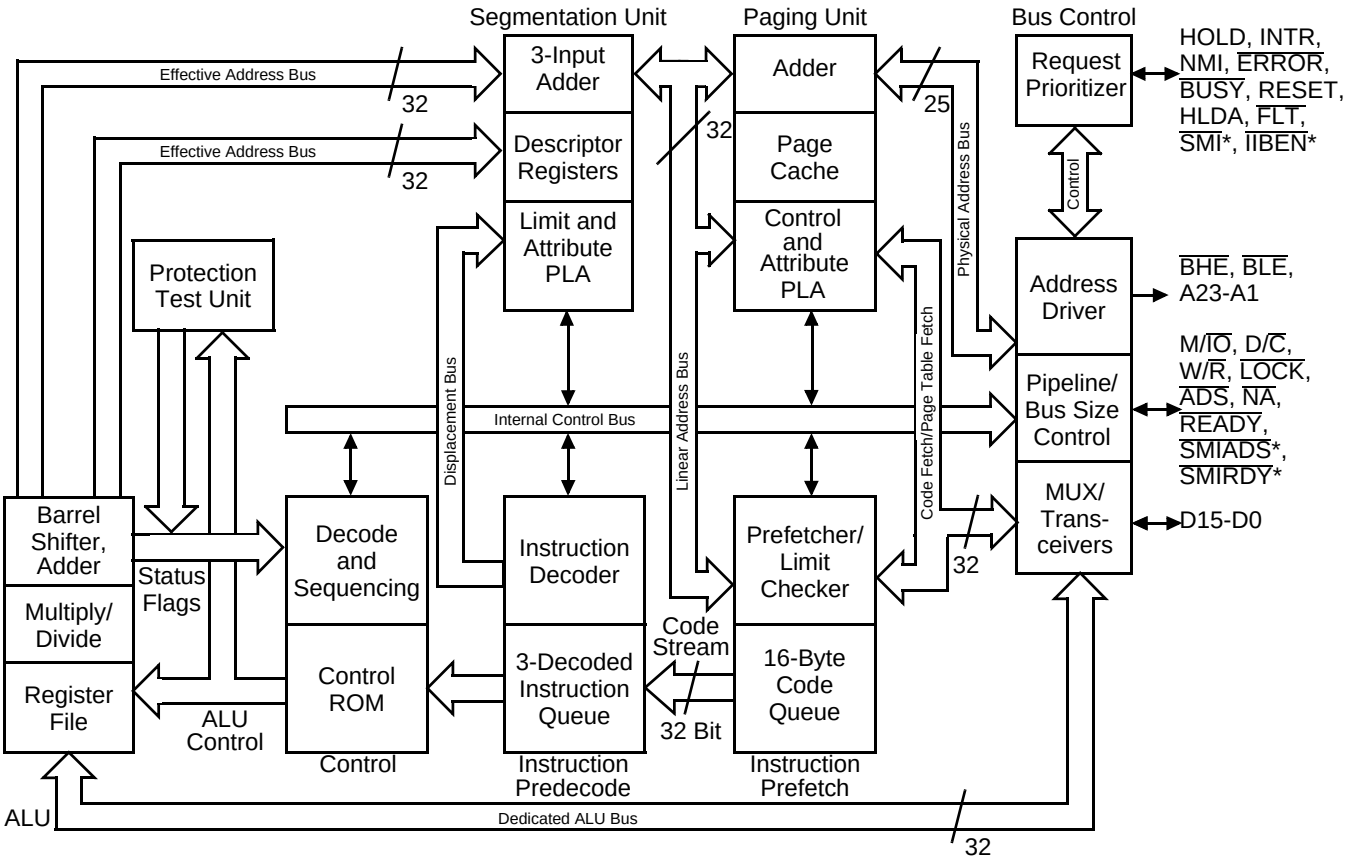



| Valid Combinations | | |
|---|---|---|
| NG80386 | SX | –25<br>–33<br>–40 |
| | SXL | –25<br>–33 |
| | SXLV | –25 |
| ING80386 | SX | –25 |

### Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## BLOCK DIAGRAM




* – On Am386SXLV only

## FUNCTIONAL DESCRIPTION

### True Static Operation (Am386SXL/SXLV Only)

The Am386SXL/SXLV microprocessor incorporates a true static design. Unlike dynamic circuit design, the Am386SXL/SXLV device eliminates the minimum operating frequency restriction. It may be clocked from its maximum speed all the way down to 0 MHz (DC). System designers can use this feature to design portable applications with long battery life.

### Standby Mode (Am386SXL/SXLV Only)

The true static design of the Am386SXL/SXLV microprocessor allows for a Standby Mode. At any operating speed, the microprocessor will retain its state (i.e., the contents of all its registers). By shutting off the clock completely, the device enters Standby Mode. Since power consumption is proportional to clock frequency, operating power consumption is reduced as the frequency is lowered. In Standby Mode, typical current draw is reduced to less than 20 microamps at DC. Not only does this feature save battery life, but it also simplifies the design of power-conscious portable applications in the following ways.

- Eliminates the need for software in BIOS to save and restore the contents of registers.
- Allows simpler circuitry to control stopping of the clock since the system does not need to know the state of the processor.

### Lower Operating Icc (Am386SXL/SXLV Only)

True static design also allows lower operating Icc when operating at any speed.

### Performance on Demand (Am386SXL/SXLV Only)

The Am386SXL/SXLV microprocessor retains its state at any speed from 0 MHz (DC) to its maximum operating speed. With this feature, system designers may vary the operating speed of the system to extend the battery life in portable systems.

For example, the system could operate at low speeds during inactivity or polling operations. However, upon interrupt, the system clock can be increased up to its maximum speed. After a user-defined time-out period, the system can be returned to a low (or 0 MHz) operating speed without losing its state. This design maximizes battery life while achieving optimal performance.

## Benefits of Lower Operating Voltage (Am386SXLV Only)

The Am386SXLV microprocessor has an operating voltage range of 3.0 V to 5.5 V. Low voltage allows for lower operating power consumption, longer battery life, and/or smaller batteries for portable applications.

Because power is proportional to the square of the voltage, reduction of the supply voltage from 5.0 V to 3.3 V reduces power consumption by 56%. This directly translates to a doubling of battery life for portable applications. Lower power consumption can also be used to reduce the size and weight of the battery. Thus, 3.3-V designs facilitate a reduction in the form factor.

A lower operating voltage results in a reduction of I/O voltage swings. This reduces noise generation and provides a less hostile environment for board design. Lower operating voltage also reduces electromagnetic radiation noise and makes FCC approval easier to obtain.

## SMM—System Management Mode (Am386SXLV Only)

The Am386SXLV microprocessor has a System Management Mode (SMM) for system and power management. This mode consists of two features: System Management Interrupt (SMI) and I/O instruction break.

### SMI—System Management Interrupt

SMI is implemented by using special bus interface pins. This interrupt method can be used to perform system management functions such as power management independent of processor operating mode (Real, Protected, or Virtual 8086 modes).

SMI can also be invoked in software. This allows system software to communicate with SMI power management code. In addition, the UMOV instruction allows data transfers between SMI and normal system memory spaces.

Activating the $\overline{\text{SMI}}$ pin invokes a sequence that saves the operating state of the processor into a separate SMM memory space, independent of the main system memory. After the state is saved, the processor is forced into Real mode and begins execution at address FFFFF0h in the SMM memory space where a far jump to the SMM code is executed. This Real mode code can perform its system management function and then resume execution of the normal system software by executing an RES3 instruction which will reload the saved processor state and continue execution in the main system memory space. See Figure 1 for a general flowchart of an SMM operation.

### CPU Interface—Pin Functions

The CPU interface for SMM consists of three pins dedicated to the SMI function. One pin, $\overline{\text{SMI}}$, is the interrupt input. The other two pins, $\overline{\text{SMIADS}}$ and $\overline{\text{SMIRDY}}$, provide the control signals necessary for the separate SMM mode memory space.

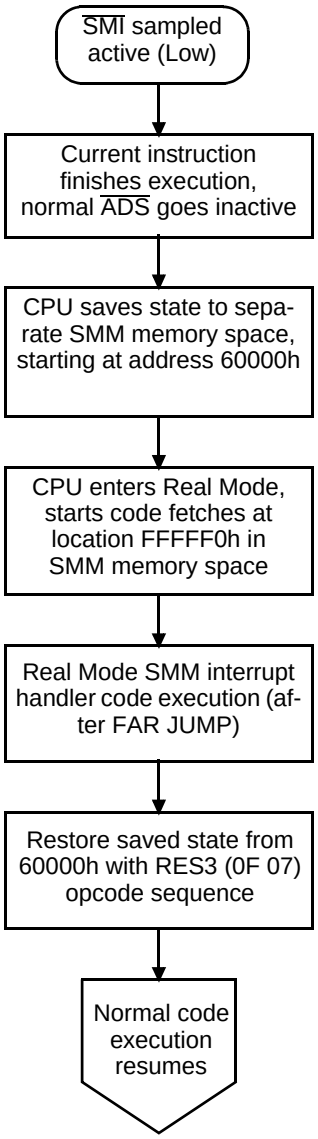



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**Figure 1. SMM Flow**

## Description of SMM Operation (Am386SXLV Only)

The execution of a System Management Interrupt has four distinct phases: the initiation of the interrupt via $\overline{SMI}$, a processor state save, execution of the SMM interrupt code, and a processor state restore (to resume normal operation).

### Interrupt Initiation

A System Management Interrupt is initiated by the driving of a synchronous, active Low pulse on the $\overline{SMI}$ pin until the first $\overline{SMIADS}$ is asserted. This pulse period will ensure recognition of the interrupt. The CPU drives the $\overline{SMI}$ pin active after the completion of the current operation (active bus cycle, instruction execution, or both). The active drive of the pin by the CPU is released at the end of the interrupt routine following the last register read of the saved state. The CPU drives $\overline{SMI}$ High for two CLK2 cycles prior to releasing the drive of $\overline{SMI}$.

An SMI cannot be masked off by the CPU, and it will always be recognized by the CPU, regardless of operating modes. This includes the Real, Protected, and Virtual-8086 modes of the processor.

While the CPU is in SMM, a bus hold request via the HOLD pin is granted**.** The HLDA pin goes active after bus release and the $\overline{SMIADS}$ pin floats along with the other pins that normally float during a bus hold cycle. SMI does not float during a Bus Hold cycle.

### Processor State Save

The first set of SMM bus transfer cycles after the CPU's recognition of an active SMI is the processor saving its state to an external RAM array in a separate address space from main system memory. This is accomplished by using the $\overline{SMIADS}$ and $\overline{SMIRDY}$ pins for initiation and termination of bus cycles, instead of the $\overline{ADS}$ and $\overline{READY}$ pins. The 24-bit addresses to which the CPU saves its state are 60000h–600CBh and 60100h–60127h. These are fixed address locations for each register saved.

To ensure valid operation, pipelining must be disabled while the processor is in SMM. There are 114 data transfer cycles.

### SMI Code Execution

After the processor state is saved to the separate SMM memory space, the execution of the SMM interrupt routine code begins. The processor enters Real mode, sets most of the register values to "reset" values (those values normally seen after a CPU reset), and begins fetching code from address FFFFF0h in the separate SMM memory space. Normally, the first thing the interrupt routine code does is a FAR JUMP to the Real mode entry point for the SMM interrupt routine, which is also in SMM memory space.

Both INTR and NMI are disabled upon entry into SMM. The SMM code can be located anywhere within the 1-Mbyte Real mode address space, except for where the processor state is saved. I/O cycles, as a result of the IN, OUT, INS, and OUTS instructions, will go to the normal address space, utilizing the normal $\overline{ADS}$ and $\overline{READY}$ bus interface signals. This facilitates power management code manipulating system hardware registers as needed through the standard I/O subsystem; a separate I/O space is not implemented.

### Processor State Restore (Resuming Normal Execution)

Returning to normal code execution in the main system memory, including restoring the processor operating mode, is accomplished by executing a special code sequence. This code invokes a restore CPU state operation that reloads the CPU registers from the saved data in the RAM controlled by $\overline{SMIADS}$ and $\overline{SMIRDY}$.

The ES:EDI register pair must point to the physical address of the processor save state (6000h). In Real mode the address is calculated as ES•16 + EDI offset. The saved state should not cross a 64K boundary. The RES3 instruction (0F 07) should be executed to start the restore state operation. After completion of the restore state operation, the $\overline{SMI}$ pin will be deactivated by the CPU and normal code execution will continue at the point where it left off before the SMI occurred. There are 114 data transfer cycles in the restore operation.

## Software Features (Am386SXLV Only)

Several features of the SMI function provide support for special operations during the execution of the system's software. These features involve the execution of reserved opcodes to induce specific SMI-related operations.

### Software SMI Generation

Besides hardware initiation of the SMI via the $\overline{SMI}$ pin, there is also a software-induced SMI mechanism. Generating a soft SMI involves setting a control bit (Bit 12) in the Debug Control Register (DR7) and executing an SMI instruction (opcode F1h).

The functional sequence of the software-based SMI is identical to the hardware-based SMI with the exception that the $\overline{SMI}$ pin is not initially driven active by an external source. Upon execution of a soft SMI opcode, the $\overline{SMI}$ pin is driven active (Low) by the processor before the save state operation begins.

### Memory Transfers to Main System Memory

While executing an SMI routine, the interrupt code can initiate memory data reads and writes to the main system memory using the normal $\overline{ADS}$ and $\overline{READY}$ pins. This initiation is accomplished by using reserved opcodes that are special forms of the MOV instruction (called UMOV). The UMOV opcodes can move byte,

word, or double word register operands to or from main system memory. Multiple data transfers using the normal $\overline{ADS}$ and $\overline{READY}$ pins will occur if the operands are misaligned relative to the effective address used. The UMOV opcodes are 0F 10h, 0F 11h, 0F 12h, and 0F 13h. The UMOV instruction can use any of the 386 addressing modes, as specified in the ModR/M byte of the opcode. Note that the 16- and 32-bit versions are the same opcodes with the exception of the 66h operand size prefix.

## I/O Instruction Break (Am386SXLV Only)

The Am386SXLV microprocessor has an I/O instruction break feature that allows the system logic to implement I/O trapping for peripheral devices. To enable the I/O Instruction break feature, $\overline{IIBEN}$ must first be asserted active Low. On detecting an I/O instruction, the processor prevents the execution unit from executing further instructions until $\overline{READY}$ is driven active Low by the system. Once $\overline{READY}$ is driven active, the execution unit either immediately responds to any active interrupt request or continues executing instructions following the I/O instruction that caused the break.

The I/O instruction break feature can be used to allow system logic to implement I/O trapping for peripheral devices. On sensing an I/O instruction, the system drives the $\overline{SMI}$ pin active before driving $\overline{READY}$ active. This ensures that the interrupt service routine is executed immediately following the I/O instruction that caused the break. (If the I/O instruction break feature is not enabled via $\overline{IIBEN}$, several instructions could execute before the SMI service routine is executed.)

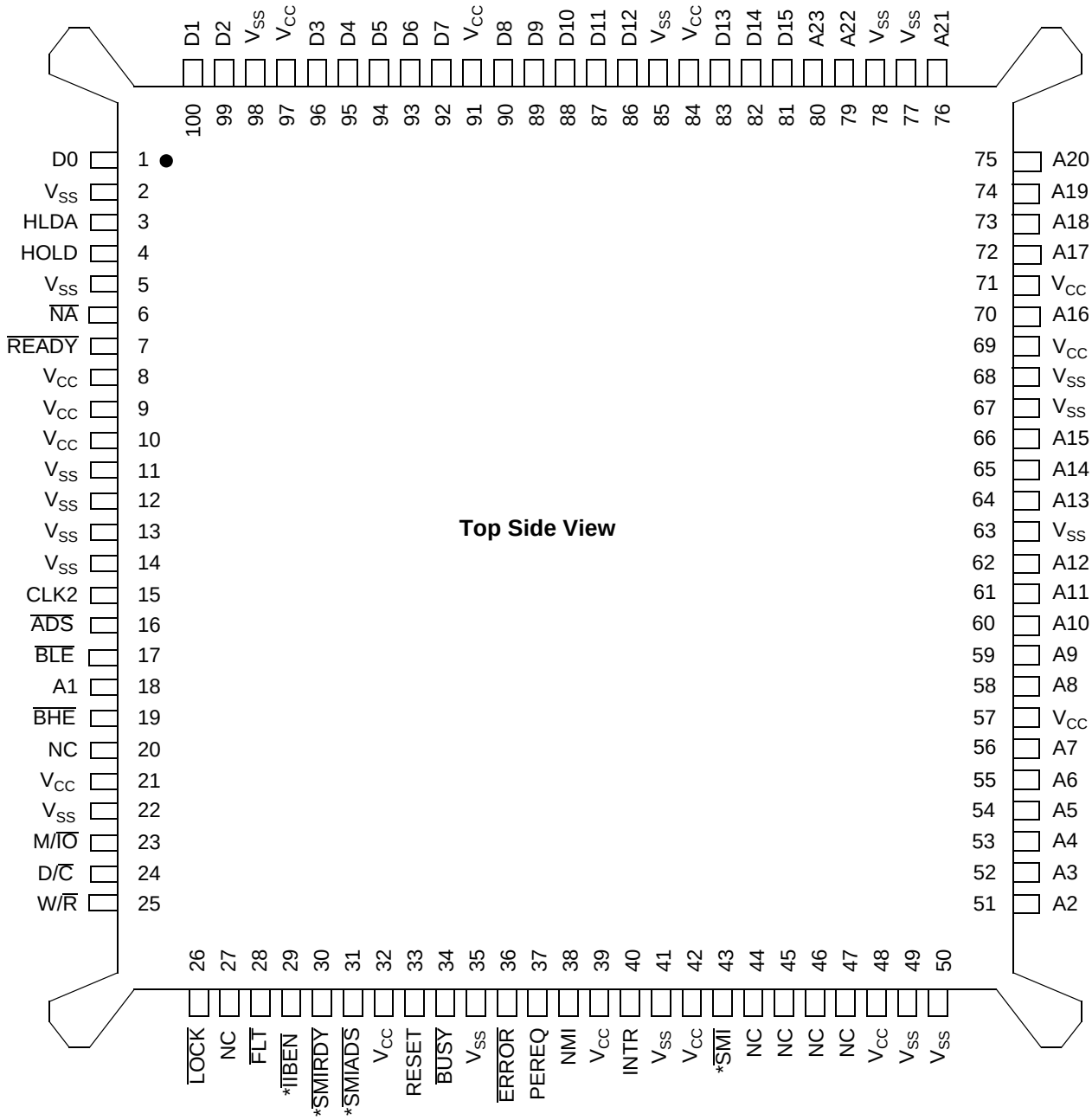
The SMI service routine can access the peripheral for which $\overline{SMI}$ was asserted and modify its state.The SMI service routine normally returns to the instruction following the I/O instruction that caused the break. By modifying the saved state instruction pointer, the routine can choose to return to the I/O instruction that caused the break and re-execute that instruction. The default is to return to the following instruction (except for REP I/O string instruction). To re-execute the I/O instruction that caused the break, the SMI service routine must copy the I/O instruction pointer over the default pointer. This feature is particularly useful when an application program requests an access to a peripheral that has been powered down. The SMI service routine can restore power to the peripheral and initiate a re-execution sequence transparent to the application program. This re-execution feature should only be used if the SMI is in response to an I/O trap with $\overline{IIBEN}$ active. Note that the I/O instruction break feature is not enabled for memory mapped I/O devices or for coprocessor bus cycles even if $\overline{IIBEN}$ is active.

### I/O Instruction Break Timing

The I/O Instruction Break feature requires that $\overline{SMI}$ be sampled active (Low) by the processor at least three CLK2 edges before the CLK2 edge that ends the I/O cycle with an active $\overline{READY}$ signal. This timing applies for both pipelined and non-pipelined cycles. If this timing constraint is not met, additional instructions may be executed by the internal execution unit prior to entering SMM. Depending on the state of the prefetch queue at the time the $\overline{SMI}$ is asserted, instruction fetch cycles may occur on the normal $\overline{ADS}$ interface before the SMM save state process begins with the assertion of $\overline{SMIADS}$. However, this fetched code will not be executed.

## CONNECTION DIAGRAM

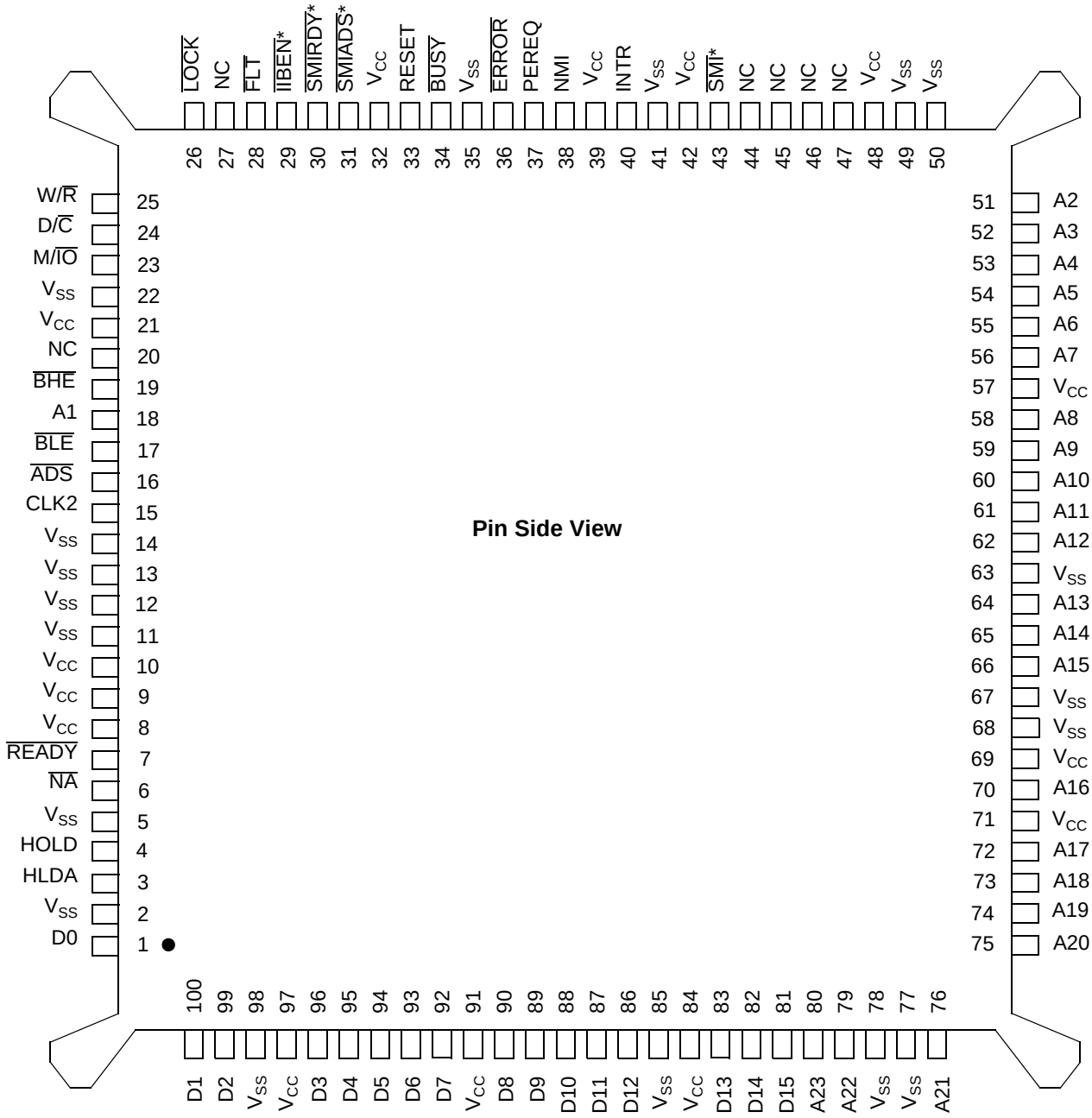
### 100-Lead Plastic Quad Flat Pack (PQFP) Package—Top Side View




***Notes*:**
*Pin 1 is marked for orientation*
*NC = Not connected; connection of an NC pin may cause a malfunction or incompatibility with future shippings of the Am386SX/SXL/SXLV microprocessors*
** = On Am386SXLV only; NC on Am386SX/SXL*

## CONNECTION DIAGRAM

### 100-Lead Plastic Quad Flat Pack (PQFP) Package—Pin Side View

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** = On Am386SXLV only; NC on Am386SX/SXL*

## PIN DESIGNATION TABLE (Sorted by Functional Grouping)

| Address | | Data | | Control | | NC | $V_{CC}$ | $V_{SS}$ |
|---|---|---|---|---|---|---|---|---|
| Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin No. | Pin No. | Pin No. |
| A1 | 18 | D0 | 1 | $\overline{ADS}$ | 16 | 20 | 8 | 2 |
| A2 | 51 | D1 | 100 | $\overline{BHE}$ | 19 | 27 | 9 | 5 |
| A3 | 52 | D2 | 99 | $\overline{BLE}$ | 17 | 44 | 10 | 11 |
| A4 | 53 | D3 | 96 | $\overline{BUSY}$ | 34 | 45 | 21 | 12 |
| A5 | 54 | D4 | 95 | CLK2 | 15 | 46 | 32 | 13 |
| A6 | 55 | D5 | 94 | D/$\overline{C}$ | 24 | 47 | 39 | 14 |
| A7 | 56 | D6 | 93 | $\overline{ERROR}$ | 36 | | 42 | 22 |
| A8 | 58 | D7 | 92 | $\overline{FLT}$ | 28 | | 48 | 35 |
| A9 | 59 | D8 | 90 | HLDA | 3 | | 57 | 41 |
| A10 | 60 | D9 | 89 | HOLD | 4 | | 69 | 49 |
| A11 | 61 | D10 | 88 | $\overline{IIBEN}$* | 29 | | 71 | 50 |
| A12 | 62 | D11 | 87 | INTR | 40 | | 84 | 63 |
| A13 | 64 | D12 | 86 | $\overline{LOCK}$ | 26 | | 91 | 67 |
| A14 | 65 | D13 | 83 | M/$\overline{IO}$ | 23 | | 97 | 68 |
| A15 | 66 | D14 | 82 | $\overline{NA}$ | 6 | | | 77 |
| A16 | 70 | D15 | 81 | NMI | 38 | | | 78 |
| A17 | 72 | | | PEREQ | 37 | | | 85 |
| A18 | 73 | | | $\overline{READY}$ | 7 | | | 98 |
| A19 | 74 | | | RESET | 33 | | | |
| A20 | 75 | | | $\overline{SMI}$* | 43 | | | |
| A21 | 76 | | | $\overline{SMIADS}$* | 31 | | | |
| A22 | 79 | | | $\overline{SMIRDY}$* | 30 | | | |
| A23 | 80 | | | W/$\overline{R}$ | 25 | | | |

** On Am386SXLV only; NC on Am386SX/SXL*

## PIN DESIGNATION TABLE (Sorted by Pin Number)

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|---|---|---|---|---|---|
| 1 | D0 | 21 | $V_{CC}$ | 41 | $V_{SS}$ | 61 | A11 | 81 | D15 |
| 2 | $V_{SS}$ | 22 | $V_{SS}$ | 42 | $V_{CC}$ | 62 | A12 | 82 | D14 |
| 3 | HLDA | 23 | M/$\overline{IO}$ | 43 | $\overline{SMI}$* | 63 | $V_{SS}$ | 83 | D13 |
| 4 | HOLD | 24 | D/$\overline{C}$ | 44 | NC | 64 | A13 | 84 | $V_{CC}$ |
| 5 | $V_{SS}$ | 25 | W/$\overline{R}$ | 45 | NC | 65 | A14 | 85 | $V_{SS}$ |
| 6 | $\overline{NA}$ | 26 | $\overline{LOCK}$ | 46 | NC | 66 | A15 | 86 | D12 |
| 7 | $\overline{READY}$ | 27 | NC | 47 | NC | 67 | $V_{SS}$ | 87 | D11 |
| 8 | $V_{CC}$ | 28 | $\overline{FLT}$ | 48 | $V_{CC}$ | 68 | $V_{SS}$ | 88 | D10 |
| 9 | $V_{CC}$ | 29 | $\overline{IIBEN}$* | 49 | $V_{SS}$ | 69 | $V_{CC}$ | 89 | D9 |
| 10 | $V_{CC}$ | 30 | $\overline{SMIRDY}$* | 50 | $V_{SS}$ | 70 | A16 | 90 | D8 |
| 11 | $V_{SS}$ | 31 | $\overline{SMIADS}$* | 51 | A2 | 71 | $V_{CC}$ | 91 | $V_{CC}$ |
| 12 | $V_{SS}$ | 32 | $V_{CC}$ | 52 | A3 | 72 | A17 | 92 | D7 |
| 13 | $V_{SS}$ | 33 | RESET | 53 | A4 | 73 | A18 | 93 | D6 |
| 14 | $V_{SS}$ | 34 | $\overline{BUSY}$ | 54 | A5 | 74 | A19 | 94 | D5 |
| 15 | CLK2 | 35 | $V_{SS}$ | 55 | A6 | 75 | A20 | 95 | D4 |
| 16 | $\overline{ADS}$ | 36 | $\overline{ERROR}$ | 56 | A7 | 76 | A21 | 96 | D3 |
| 17 | $\overline{BLE}$ | 37 | PEREQ | 57 | $V_{CC}$ | 77 | $V_{SS}$ | 97 | $V_{CC}$ |
| 18 | A1 | 38 | NMI | 58 | A8 | 78 | $V_{SS}$ | 98 | $V_{SS}$ |
| 19 | $\overline{BHE}$ | 39 | $V_{CC}$ | 59 | A9 | 79 | A22 | 99 | D2 |
| 20 | NC | 40 | INTR | 60 | A10 | 80 | A23 | 100 | D1 |

** On Am386SXLV only; NC on Am386SX/SXL*

## PIN DESCRIPTIONS

**A23–A1**
**Address Bus (Outputs)**

Outputs physical memory or port I/O addresses.

**$\overline{\text{ADS}}$**
**Address Status (Active Low; Output)**

Indicates that a valid bus cycle definition and address (W/$\overline{\text{R}}$, D/$\overline{\text{C}}$, M/$\overline{\text{IO}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, and A23–A1) are being driven at the Am386SX/SXL/SXLV microprocessor pins. Bus cycles initiated by $\overline{\text{ADS}}$ must be terminated by $\overline{\text{READY}}$.

**$\overline{\text{BHE}}$, $\overline{\text{BLE}}$**
**Byte Enables (Active Low; Outputs)**

Indicate which data bytes of the data bus take part in a bus cycle.

**$\overline{\text{BUSY}}$**
**Busy (Active Low; Input)**

Signals a busy condition from a processor extension. $\overline{\text{BUSY}}$ has an internal pull-up resistor.

**CLK2**
**CLK2 (Input)**

Provides the fundamental timing for the Am386SX/SXL/SXLV microprocessor.

**D15–D0**
**Data Bus (Inputs/Outputs)**

Inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles.

**D/$\overline{\text{C}}$**
**Data/Control (Output)**

A bus cycle definition pin that distinguishes data cycles, either memory or I/O, from control cycles which are interrupt acknowledge, halt, and code fetch.

**$\overline{\text{ERROR}}$**
**Error (Active Low; Input)**

Signals an error condition from a processor extension. $\overline{\text{ERROR}}$ has an internal pull-up resistor.

**$\overline{\text{FLT}}$**
**Float (Active Low; Input)**

An input which forces all bidirectional and output signals, including HLDA, to the three-state condition. $\overline{\text{FLT}}$ has an internal pull-up resistor. The pin, if not used, should be disconnected.

**HLDA**
**Bus Hold Acknowledge (Active High; Output)**

Output indicates that the Am386SX/SXL/SXLV microprocessor has surrendered control of its logical bus to another bus master.

**HOLD**
**Bus Hold Request (Active High; Input)**

Input allows another bus master to request control of the local bus.

**$\overline{\text{IIBEN}}$ (Am386SXLV Only)**
**I/O Instruction Break Enable (Active Low; Input)**

Enables the I/O instruction break feature. $\overline{\text{IIBEN}}$ has a dynamic internal pull-up resistor. The $\overline{\text{IIBEN}}$ pull-up is active during RESET and whenever the signal is not driven active Low by the system.

**INTR**
**Interrupt Request (Active High; Input)**

A maskable input that signals the Am386SX/SXL/SXLV microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

**$\overline{\text{LOCK}}$**
**Bus Lock (Active Low; Output)**

A bus cycle definition pin that indicates that other system bus masters are not to gain control of the system bus while it is active.

**M/$\overline{\text{IO}}$**
**Memory/IO (Output)**

A bus cycle definition pin that distinguishes memory cycles from input/output cycles.

**$\overline{\text{NA}}$**
**Next Address (Active Low; Input)**

Used to request address pipelining.

**NC**
**No Connect**

Should always be left unconnected. Connection of an NC pin may cause the processor to malfunction or be incompatible with future steppings of the Am386SX/SXL/SXLV microprocessor.

**NMI**
**Non-Maskable Interrupt Request**
**(Active High; Input)**

A non-maskable input that signals to the Am386SX/SXL/SXLV microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

**PEREQ**
**Processor Extension Request (Active High; Input)**

Indicates that the processor has data to be transferred by the Am386SX/SXL/SXLV microprocessor. PEREQ has an internal pull-down resistor.

**$\overline{\text{READY}}$**
**Bus Ready (Active Low; Input)**

Terminates the bus cycle initiated by $\overline{\text{ADS}}$.

**RESET**
**Reset (Active High; Input)**

Suspends any operation in progress and places the Am386SX/SXL/SXLV microprocessor in a known reset state.

**$\overline{\text{SMI}}$ (Am386SXLV Only)**
**System Management Interrupt (Active Low; I/O)**

A non-maskable interrupt pin that signals to the Am386SXLV microprocessor to suspend execution and enter System Management Mode. $\overline{\text{SMI}}$ has an internal pull-up resistor. $\overline{\text{SMI}}$ has a dynamic internal pull-up resistor that is disabled when the processor is in SMM. $\overline{\text{SMI}}$ is not three-stated during Hold Acknowledge bus cycles.

**$\overline{\text{SMIADS}}$ (Am386SXLV Only)**
**SMI Address Status (Active Low; Output)**

When active, this pin indicates that a valid bus cycle definition and address (W/$\overline{\text{R}}$, D/$\overline{\text{C}}$, M/$\overline{\text{IO}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, and A23–A1) are being driven at the Am386SXLV microprocessor pins while in the System Management mode. Bus cycles initiated by $\overline{\text{SMIADS}}$ must be terminated by $\overline{\text{SMIRDY}}$.

**$\overline{\text{SMIRDY}}$ (Am386SXLV Only)**
**SMI Ready (Active Low; Input)**

This input terminates the current bus cycle to the SMM mode address space in the same manner the $\overline{\text{READY}}$ pin does for the normal mode address space. $\overline{\text{SMIRDY}}$ has an internal pull-up resistor. $\overline{\text{READY}}$ and $\overline{\text{SMIRDY}}$ must not be tied together.

**$V_{CC}$**
**System Power (Input)**

Provides the 5 V nominal DC supply input.

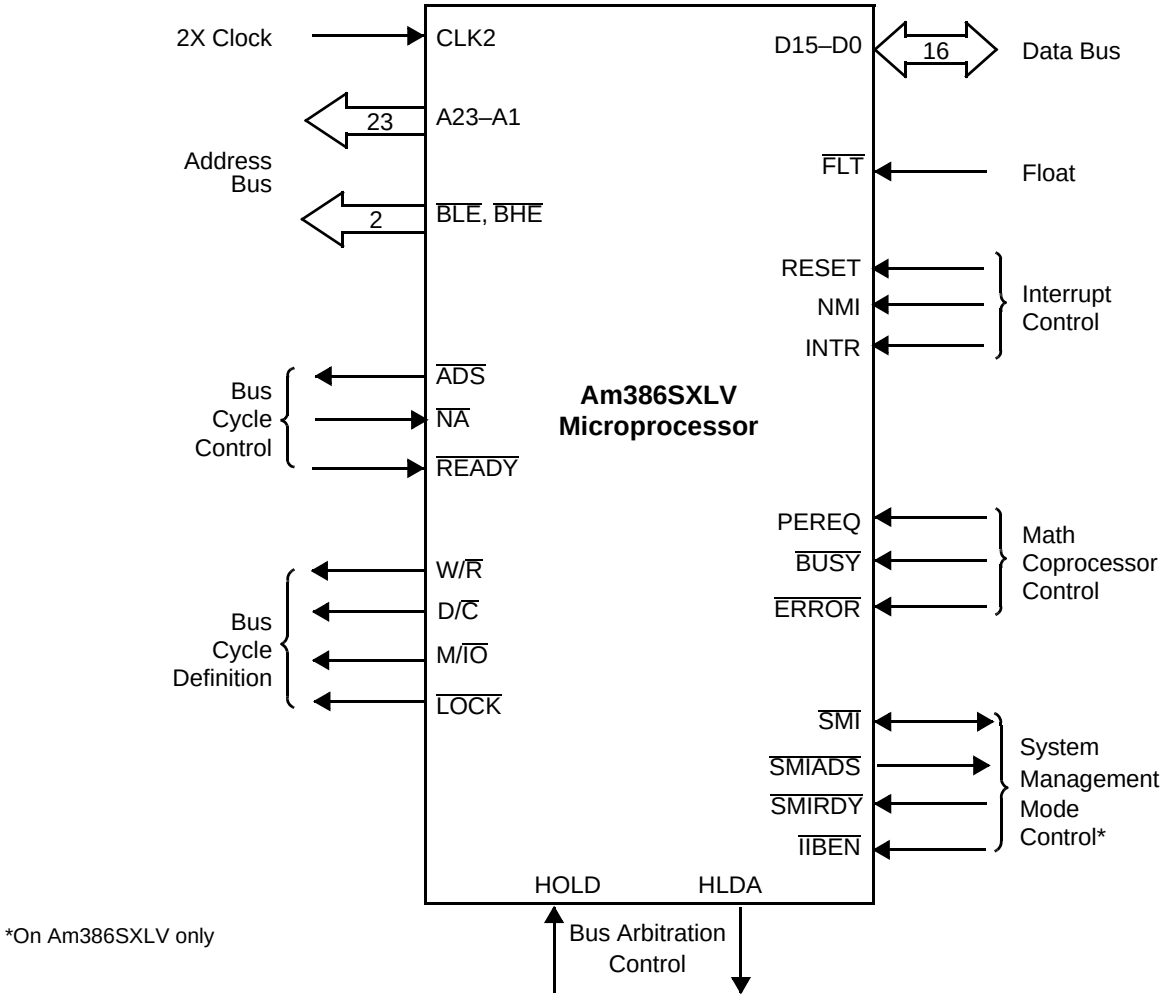
**$V_{SS}$**
**System Ground (Input)**

Provides the 0-V connection from which all inputs and outputs are measured.

**W/$\overline{\text{R}}$**
**Write/Read (Output)**

A bus cycle definition pin that distinguishes write cycles from read cycles.

## LOGIC SYMBOL



## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C
Ambient Temperature Under Bias .... –65°C to +125°C

*Stresses above those listed may cause permanent damage to the device. Functionality at or above these limits is not implied. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.*

## OPERATING RANGES

Supply Voltage with respect to $V_{SS}$..... –0.5 V to +7.0 V
Voltage on Other Pins..... –0.5 V to ($V_{CC}$ +0.5) V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges for 25 MHz Am386SXLV

$V_{CC}$=3.0 V to 3.6 V; $T_{CASE}$=0°C to +100°C

| Symbol | Parameter Description | Notes | Final | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IL}$ | Input Low Voltage | (Note 1) | –0.3 | +0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | $V_{CC}$+0.3 | V |
| $V_{ILC}$ | CLK2 Input Low Voltage | (Note 1) | –0.3 | +0.8 | V |
| $V_{IHC}$ | CLK2 Input High Voltage | | 2.4 | $V_{CC}$+0.3 | V |
| $V_{OL}$ | Output Low Voltage<br>$I_{OL}$ = 0.5 mA: A23–A1, D15–D0<br>$I_{OL}$ = 0.5 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, $\overline{SMIADS}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, HLDA, $\overline{SMI}$<br>$I_{OL}$ = 2 mA: A23–A1, D15–D0<br>$I_{OL}$ = 2.5 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, $\overline{SMIADS}$, $\overline{LOCK}$, $\overline{ADS}$, M/$\overline{IO}$, HLDA, $\overline{SMI}$ | (Note 5) | | 0.2<br>0.2<br>0.45<br>0.45 | V<br>V<br>V<br>V |
| $V_{OH}$ | Output High Voltage<br>$I_{OH}$ = 0.1 mA: A23–A1, D15–D0<br>$I_{OH}$ = 0.1 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, $\overline{SMIADS}$, $\overline{LOCK}$, $\overline{ADS}$, M/$\overline{IO}$, HLDA, $\overline{SMI}$<br>$I_{OH}$ = 0.5 mA: A23–A1, D15–D0<br>$I_{OH}$ = 0.5 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, $\overline{SMIADS}$, $\overline{LOCK}$, $\overline{ADS}$, M/$\overline{IO}$, HLDA, $\overline{SMI}$ | (Note 5)<br>(Note 6) | $V_{CC}$–0.2<br>$V_{CC}$–0.2<br>$V_{CC}$–0.45<br>$V_{CC}$–0.45 | | V<br>V<br>V<br>V |
| $I_{LI}$ | Input Leakage Current (All pins except PEREQ, $\overline{BUSY}$, $\overline{ERROR}$, $\overline{SMI}$, $\overline{SMIRDY}$, $\overline{FLT}$, $\overline{IIBEN}$) | 0 V ≤ $V_{IN}$ ≤ $V_{CC}$<br>(Note 7) | | ±10 | µA |
| $I_{IH}$ | Input Leakage Current<br>(PEREQ pin) | $V_{IH}$ = $V_{CC}$–0.1 V<br>$V_{IH}$ = 2.4 V (Note 2) | | 300<br>200 | µA<br>µA |
| $I_{IL}$ | Input Leakage Current<br>($\overline{BUSY}$, $\overline{ERROR}$, $\overline{SMI}$, $\overline{SMIRDY}$, $\overline{FLT}$, $\overline{IIBEN}$) | $V_{IL}$ = 0.1 V<br>$V_{IL}$ = 0.45 V (Note 3) | | –300<br>–200 | µA<br>µA |
| $I_{LO}$ | Output Leakage Current | 0.1 V ≤ $V_{OUT}$ ≤ $V_{CC}$ | | ±15 | µA |
| $I_{CC}$ | Supply Current (Note 8)<br>CLK2 = 50 MHz: Oper. Freq. 25 MHz | $V_{CC}$ = 3.3 V<br>$I_{CC}$ Typ = 95 | | $V_{CC}$ = 3.6 V<br>115 | mA |
| $I_{CCSB}$ | Standby Current (Note 8) | $I_{CCSB}$ Typ = 10µA | | 150 | µA |
| $C_{IN}$ | Input or I/O Capacitance | $F_C$ = 1 MHz (Note 4) | | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $F_C$ = 1 MHz (Note 4) | | 12 | pF |
| $C_{CLK}$ | CLK2 Capacitance | $F_C$ = 1 MHz (Note 4) | | 20 | pF |

***Notes:***

1. *The Min value, –0.3, is not 100% tested.*
2. *PEREQ input has an internal pull-down resistor.*
3. *$\overline{BUSY}$, $\overline{ERROR}$, $\overline{FLT}$, $\overline{SMI}$, $\overline{IIBEN}$, and $\overline{SMIRDY}$ inputs each have an internal pull-up resistor.*
4. *Not 100% tested.*
5. *Outputs are CMOS and will pull rail-to-rail if the load is not resistive.*
6. *$V_{OH}$ $\overline{SMI}$ only valid on $\overline{SMI}$ output when exiting SMM for two CLK2 periods.*
7. *$\overline{SMI}$ and $\overline{IIBEN}$ leakage Low will be $I_{LI}$ when pull-up is inactive and $I_{IL}$ when pull-up is active.*
8. *Inputs at rails ($V_{CC}$ or $V_{SS}$).*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C
Ambient Temperature under Bias .... –65°C to +125°C

*Stresses above those listed may cause permanent damage to the device. Functionality at or above these limits is not implied. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.*

## OPERATING RANGES

Supply Voltage with respect to $V_{SS}$.... –0.5 V to +7.0 V
Voltage on Other Pins.....–0.5 V to ($V_{cc}$ +0.5) V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

25 and 33 MHz: $V_{cc}$ = 5 V ± 10%; $T_{CASE}$ = 0°C to +100°C (commercial); $T_{CASE}$ = –40°C to +100°C (industrial)
40 MHz: $V_{cc}$ = 5 V ± 5%; $T_{CASE}$ = 0°C to +100°C

| Symbol | Parameter Description | Notes | Final Min | Final Max | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | (Note 1) | –0.3 | +0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | $V_{CC}$+0.3 | V |
| $V_{ILC}$ | CLK2 Input Low Voltage | (Note 1) | –0.3 | +0.8 | V |
| $V_{IHC}$ | CLK2 Input High Voltage | | 2.7 | $V_{CC}$+0.3 | V |
| $V_{OL}$ | Output Low Voltage<br>$I_{OL}$ = 4 mA: A23–A1, D15–D0<br>$I_{OL}$ = 5 mA: $\overline{BHE}$, $\overline{BLE}$,W/$\overline{R}$, D/$\overline{C}$, $\overline{SMIADS}$*, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, HLDA, $\overline{SMI}$* | (Note 5) | | <br>0.45<br>0.45 | <br>V<br>V |
| $V_{OH}$ | Output High Voltage<br>$I_{OH}$ = 1.0 mA: A23–A1, D15–D0<br>$I_{OH}$ = 0.2 mA: A23–A1, D15–D0<br>$I_{OH}$ = 0.9 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, $\overline{SMIADS}$*, $\overline{LOCK}$, $\overline{ADS}$, M/$\overline{IO}$, HLDA, $\overline{SMI}$*<br>$I_{OH}$ = 0.18 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, $\overline{SMIADS}$*, $\overline{LOCK}$, $\overline{ADS}$, M/$\overline{IO}$, HLDA, $\overline{SMI}$* | <br>(Note 5)<br><br>(Note 6*)<br><br> | <br>2.4<br>$V_{CC}$ –0.5<br>2.4<br><br>$V_{CC}$ –0.5 | <br><br><br><br> | <br>V<br>V<br>V<br><br>V |
| $I_{LI}$ | Input Leakage Current (All pins except PEREQ, $\overline{BUSY}$, $\overline{ERROR}$, $\overline{SMI}$*, $\overline{SMIRDY}$*, $\overline{FLT}$, and $\overline{IIBEN}$*) | 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ (Note 7) | | ±15 | µA |
| $I_{IH}$ | Input Leakage Current (PEREQ pin) | $V_{IH}$ = 2.4 V (Note 2) | | 200 | µA |
| $I_{IL}$ | Input Leakage Current ($\overline{BUSY}$, $\overline{ERROR}$, $\overline{SMI}$*, $\overline{SMIRDY}$*, $\overline{FLT}$, $\overline{IIBEN}$*) | $V_{IL}$ = 0.45 V (Note 3) | | –400 | µA |
| $I_{LO}$ | Output Leakage Current: Am386SX/SXL<br>Am386SXLV | 0.1 V ≤ $V_{OUT}$ ≤ $V_{CC}$<br>0.45 V ≤ $V_{OUT}$ ≤ $V_{CC}$ | | ±15<br>±15 | µA<br>µA |
| $I_{CC}$ | Supply Current (Note 8)<br>CLK2 = 50 MHz: Oper. Freq. 25 MHz<br>CLK2 = 66 MHz: Oper. Freq. 33 MHz<br>CLK2 = 80 MHz: Oper. Freq. 40 MHz | $V_{CC}$ Typ = 5.0 V<br>$I_{CC}$ Typ = 160<br>$I_{CC}$ Typ = 210<br>$I_{CC}$ Typ = 255 | | $V_{CC}$ = 5.5<br>190<br>245<br>295 | V<br>mA<br>mA<br>mA |
| $I_{CCSB}$ | Standby Current (Note 8) | $I_{CCSB}$ Typ = 20 µA | | 150 | µA |
| $C_{IN}$ | Input or I/O Capacitance | $F_C$ = 1 MHz (Note 4) | | 10 | pF |
| $C_{OUT}$ | Output or I/O Capacitance | $F_C$ = 1 MHz (Note 4) | | 12 | pF |
| $C_{CLK}$ | CLK2 Capacitance | $F_C$ = 1 MHz (Note 4) | | 20 | pF |

***Notes:***
** On Am386SXLV only*
1. *The Min value, –0.3, is not 100% tested.*
2. *PEREQ input has an internal pull-down resistor.*
3. *$\overline{BUSY}$, $\overline{ERROR}$, $\overline{FLT}$, $\overline{SMI}$*, $\overline{IIBEN}$*, and $\overline{SMIRDY}$* inputs each have an internal pull-up resistor.*
4. *Not 100% tested.*
5. *Outputs are CMOS and will pull rail-to-rail if the load is not resistive.*
6. *$V_{OH}$ $\overline{SMI}$ only valid on $\overline{SMI}$ output when exiting SMM for two CLK2 periods (on Am386SXLV only).*
7. *$\overline{SMI}$ and $\overline{IIBEN}$ leakage Low will be $I_{LI}$ when pull-up is inactive and $I_{IL}$ when pull-up is active (on Am386SXLV only).*
8. *Inputs at rails ($V_{CC}$ or $V_{SS}$), outputs unloaded, PEREQ Low, $\overline{ERROR}$ High, $\overline{BUSY}$ High, and $\overline{FLT}$ High.*

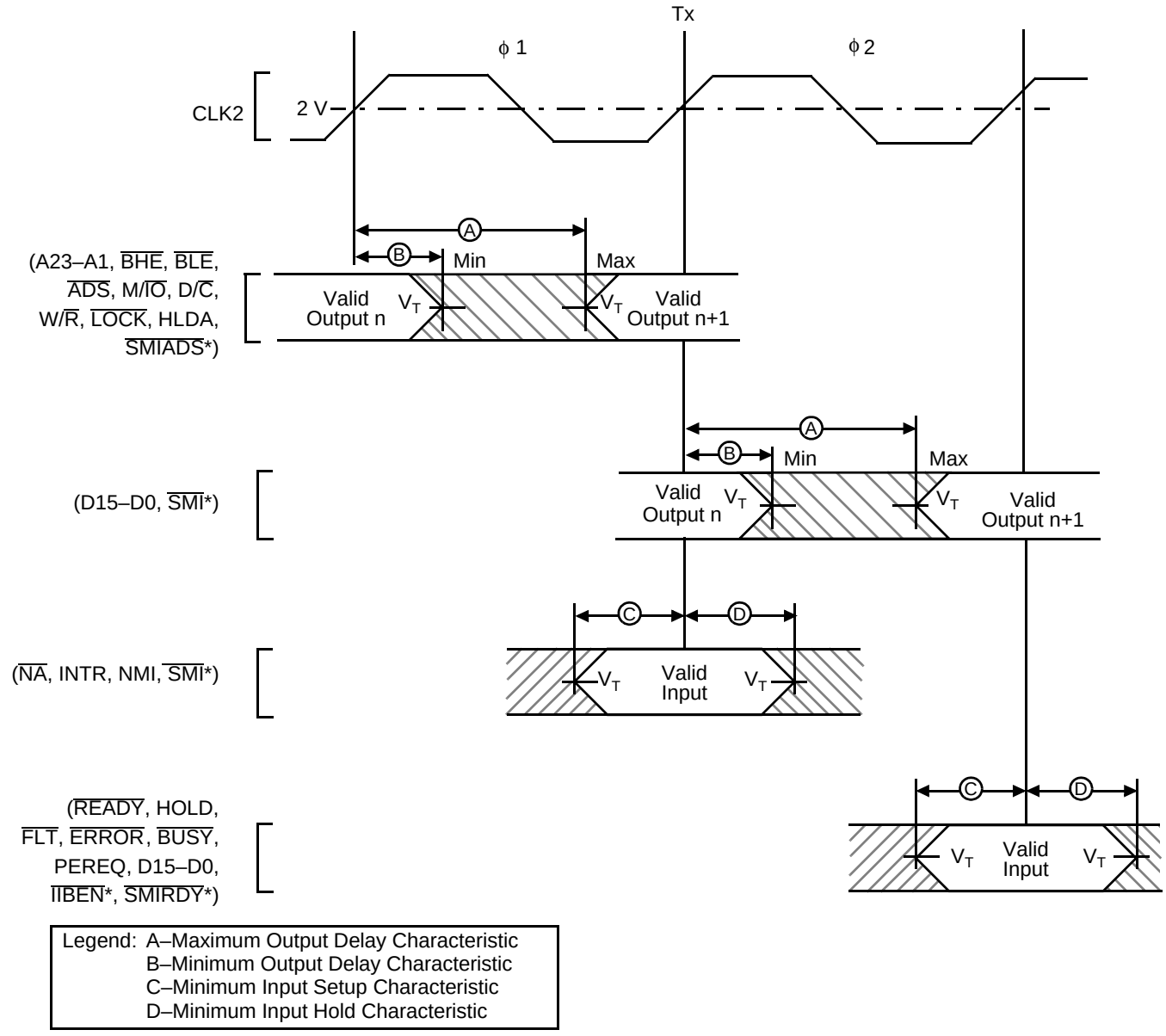
## SWITCHING CHARACTERISTICS

The switching characteristics given consist of output delays, input setup requirements, and input hold requirements. All switching characteristics are relative to the CLK2 rising edge crossing the 2.0-V level.

Switching characteristic measurement is defined in Figure 2. Inputs must be driven to the voltage levels indicated by Figure 2 when switching characteristics are measured. Output delays are specified with minimum and maximum limits measured, as shown. The minimum delay times are hold times provided to external circuitry. Input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct operation.

Outputs $\overline{ADS}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{BHE}$, $\overline{BLE}$, A23–A1, HLDA, and $\overline{SMIADS}$* only change at the beginning of phase one. D15–D0 and $\overline{SMI}$* write cycles only change at the beginning of phase two. The $\overline{READY}$, HOLD, $\overline{BUSY}$, $\overline{ERROR}$, PEREQ, $\overline{FLT}$, D15–D0, $\overline{IIBEN}$*, and $\overline{SMIRDY}$* read cycles inputs are sampled at the beginning of phase one. The $\overline{NA}$, INTR, NMI, and $\overline{SMI}$* inputs are sampled at the beginning of phase two.

** – On Am386SXLV only; NC on Am386SX/SXL*




***Notes:***

1. *Input waveforms have tr ≤ 2.0 ns from 0.8 V–2.0 V (on Am386SXLV only).*
2. *On Am386SX/SXL, $V_T$ = 1.5; on Am386SXLV, $V_T$ = 1.0 V for $V_{CC} \leq 3.6$ V and 1.5 V for $V_{CC} > 3.6$ V.*
3. ** = On Am386SXLV only.*

16305C–003

**Figure 2. Drive Levels and Measurement Points for Switching Characteristics**

## SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges at 25 MHz

$V_{CC}$ = 5.0 V ± 10%; $T_{CASE}$ = 0°C to +100°C (Commercial); $T_{CASE}$ = –40°C to +100°C (Industrial)
$V_{CC}$ = 3.0 V–5.5 V; $T_{CASE}$ = 0°C to +100°C (Am386SXLV only)

| Symbol | Parameter Description | Notes | Ref. Figures | Final Min | Final Max | Unit |
|---|---|---|---|---|---|---|
| | Operating Frequency: Am386SX CPU | Half CLK2 freq. | | 2 | 25 | MHz |
| | Am386SXL/SXLV CPU | Half CLK2 freq. | | 0 | 25 | |
| 1 | CLK2 Period | | 3, 4 | 20 | | ns |
| 2 | CLK2 High Time: Am386SXLV CPU | at $V_{IHC}$ | 3 | 4 | | ns |
| 2a | CLK2 High Time: Am386SX/SXL CPU | at 2 V | 4 | 7 | | ns |
| 2b | CLK2 High Time: Am386SX/SXL CPU | at ($V_{CC}$–0.8 V) | 4 | 4 | | ns |
| 3 | CLK2 Low Time: Am386SXLV CPU | at 0.8 V | 3 | 5 | | ns |
| 3a | CLK2 Low Time: Am386SX/SXL CPU | at 2 V | 4 | 7 | | ns |
| 3b | CLK2 Low Time: Am386SX/SXL CPU | at 0.8 V | 4 | 5 | | ns |
| 4 | CLK2 Fall Time: Am386SX/SXL CPU | ($V_{CC}$–0.8 V) to 0.8 V (Note 3) | 4 | | 7 | ns |
| | Am386SXLV CPU | 2.4 V to 0.8 V (Note 3) | 3 | | | |
| 5 | CLK2 Rise Time: Am386SX/SXL CPU | 0.8 V to 2.4 V (Note 3) | 4 | | 7 | ns |
| | Am386SXLV CPU | 0.8 V to ($V_{CC}$–0.8 V) (Note 3) | 3 | | | |
| 6 | A23–A1 Valid Delay | $C_L$ = 50 pF | 8 | 4 | 17 | ns |
| 7 | A23–A1 Float Delay | (Note 1) | 15 | 4 | 30 | ns |
| 8 | $\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Valid Delay | $C_L$ = 50 pF | 8 | 4 | 17 | ns |
| 9 | $\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Float Delay | (Note 1) | 15 | 4 | 30 | ns |
| 10 | M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$ Valid Delay | $C_L$ = 50 pF | 8 | 4 | 17 | ns |
| 10s | $\overline{SMIADS}$ Valid Delay | $C_L$ = 50 pF (Note 5) | 8 | 4 | 25 | ns |
| 11 | W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay | (Note 1) | 15, 18 | 4 | 30 | ns |
| 11s | $\overline{SMIADS}$ Float Delay | (Notes 1, 5) | 15 | 4 | 30 | ns |
| 12 | D15–D0 Write Data Valid Delay | $C_L$ = 50 pF | 8, 9 | 7 | 23 | ns |
| 12a | D15–D0 Write Data Hold Time | $C_L$ = 50 pF | 10 | 2 | | ns |
| 13 | D15–D0 Write Data Float Delay | (Note 1) | 15 | 4 | 22 | ns |
| 14 | HLDA Valid Delay | $C_L$ = 50 pF | 8 | 4 | 22 | ns |
| 14f | HLDA Float Delay: Am386SX/SXL | | 15, 16 | 4 | 22 | ns |
| | Am386SXLV | (Notes 1, 4) | | 4 | 30 | |
| 15 | $\overline{NA}$ Setup Time | | 7 | 5 | | ns |
| 16 | $\overline{NA}$ Hold Time | | 7 | 3 | | ns |
| 19 | $\overline{READY}$ Setup Time | | 7 | 9 | | ns |
| 19s | $\overline{SMIRDY}$ Setup Time | (Note 5) | 7 | 9 | | ns |
| 20 | $\overline{READY}$ Hold Time | | 7 | 4 | | ns |
| 20s | $\overline{SMIRDY}$ Hold Time | (Note 5) | 7 | 4 | | ns |
| 21 | D15–D0 Read Data Setup Time | | 7 | 7 | | ns |
| 22 | D15–D0 Read Data Hold Time | | 7 | 5 | | ns |
| 23 | HOLD Setup Time | | 7 | 9 | | ns |
| 24 | HOLD Hold Time | | 7 | 3 | | ns |
| 25 | RESET Setup Time | | 17 | 8 | | ns |
| 26 | RESET Hold Time | | 17 | 3 | | ns |
| 27 | NMI, INTR Setup Time | (Note 2) | 7 | 6 | | ns |
| 27s | $\overline{SMI}$ Setup Time | (Note 5) | 7 | 6 | | ns |
| 28 | NMI, INTR Hold Time | (Note 2) | 7 | 6 | | ns |
| 28s | $\overline{SMI}$ Hold Time | (Note 5) | 7 | 4 | | ns |
| 29 | PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$, $\overline{IIBEN}$[5] Setup Time | (Note 2) | 7 | 6 | | ns |
| 30 | PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$, $\overline{IIBEN}$[5] Hold Time | (Note 2) | 7 | 5 | | ns |
| 31 | $\overline{SMI}$ Valid Delay | (Note 5) | 8, 15 | 4 | 22 | ns |
| 32 | $\overline{SMI}$ Float Delay | (Notes 1, 4, 5) | 16 | 4 | 30 | ns |

***Notes:***

1. *Float condition occurs when maximum output current becomes less than $I_{LO}$ in magnitude. Float delay is not 100% tested.*
2. *These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.*
3. *Rise and Fall times are not tested. They are guaranteed by design characterization.*
4. *Only during $\overline{FLT}$ assertion.*
5. *On Am386SXLV only.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges at 33 MHz

$V_{CC}$ = 5.0 V ± 10%; $T_{CASE}$ = 0°C to +100°C

| Symbol | Parameter Description | Notes | Ref. Figures | Final Min | Final Max | Unit |
|---|---|---|---|---|---|---|
| | Operating Frequency: Am386SX CPU<br>Am386SXL CPU | Half CLK2 freq.<br>Half CLK2 freq. | | 2<br>0 | 33<br>33 | MHz |
| 1 | CLK2 Period | | 4 | 15 | | ns |
| 2a | CLK2 High Time | at 2 V | 4 | 6.25 | | ns |
| 2b | CLK2 High Time | at 3.7 V | 4 | 4 | | ns |
| 3a | CLK2 Low Time | at 2 V | 4 | 6.25 | | ns |
| 3b | CLK2 Low Time | at 0.8 V | 4 | 4.5 | | ns |
| 4 | CLK2 Fall Time | 3.7 V to 0.8 V (Note 3) | 4 | | 4 | ns |
| 5 | CLK2 Rise Time | 0.8 V to 3.7 V (Note 3) | 4 | | 4 | ns |
| 6 | A23–A1 Valid Delay | $C_L$ = 50 pF | 8 | 4 | 15 | ns |
| 7 | A23–A1 Float Delay | (Note 1) | 15 | 4 | 20 | ns |
| 8 | $\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Valid Delay | $C_L$ = 50 pF | 8 | 4 | 15 | ns |
| 9 | $\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Float Delay | (Note 1) | 15 | 4 | 20 | ns |
| 10 | M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$ Valid Delay | $C_L$ = 50 pF | 8 | 4 | 15 | ns |
| 11 | W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay | (Note 1) | 15 | 4 | 20 | ns |
| 12 | D15–D0 Write Data Valid Delay | $C_L$ = 50 pF | 8 | 7 | 23 | ns |
| 12a | D15–D0 Write Data Hold Time | $C_L$ = 50 pF | 10 | 2 | | ns |
| 13 | D15–D0 Write Data Float Delay | (Note 1) | 15 | 4 | 17 | ns |
| 14 | HLDA Valid Delay | $C_L$ = 50 pF | 8 | 4 | 20 | ns |
| 14f | HLDA Float Delay | | 15 | 4 | 20 | ns |
| 15 | $\overline{NA}$ Setup Time | | 7 | 5 | | ns |
| 16 | $\overline{NA}$ Hold Time | | 7 | 2 | | ns |
| 19 | $\overline{READY}$ Setup Time | | 7 | 7 | | ns |
| 20 | $\overline{READY}$ Hold Time | | 7 | 4 | | ns |
| 21 | D15–D0 Read Data Setup Time | | 7 | 5 | | ns |
| 22 | D15–D0 Read Data Hold Time | | 7 | 3 | | ns |
| 23 | HOLD Setup Time | | 7 | 9 | | ns |
| 24 | HOLD Hold Time | | 7 | 2 | | ns |
| 25 | RESET Setup Time | | 17 | 5 | | ns |
| 26 | RESET Hold Time | | 17 | 2 | | ns |
| 27 | NMI, INTR Setup Time | (Note 2) | 7 | 5 | | ns |
| 28 | NMI, INTR Hold Time | (Note 2) | 7 | 5 | | ns |
| 29 | PEREQ, $\overline{ERROR}$, $\overline{BUSY}$ Setup Time | (Note 2) | 7 | 5 | | ns |
| 30 | PEREQ, $\overline{ERROR}$, $\overline{BUSY}$ Hold Time | (Note 2) | 7 | 4 | | ns |

***Notes:***

1. *Float condition occurs when maximum output current becomes less than $I_{LO}$ in magnitude. Float delay is not 100% tested.*
2. *These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.*
3. *Rise and Fall times are not tested. They are guaranteed by design characterization.*
4. *Min time is not 100% tested.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges at 40 MHz

$V_{CC}$ = 5.0 V ± 5%; $T_{CASE}$ = 0°C to +100°C (Am386SX only)

| Symbol | Parameter Description | Notes | Ref. Figures | Final Min | Final Max | Unit |
|---|---|---|---|---|---|---|
| | Operating Frequency | Half CLK2 frequency | | 2 | 40 | MHz |
| 1 | CLK2 Period | | 5 | 12.5 | 250 | ns |
| 2 | CLK2 High Time | at 2.7 V | 5 | 4.5 | | ns |
| 3 | CLK2 Low Time | at 0.8 V | 5 | 4.5 | | ns |
| 4 | CLK2 Fall Time | 2.7 V to 0.8 V (Note 3) | 5 | | 4 | ns |
| 5 | CLK2 Rise Time | 0.8 V to 2.7 V (Note 3) | 5 | | 4 | ns |
| 6 | A23–A1 Valid Delay | $C_L$ = 50 pF | 8 | 4 | 13 | ns |
| 7 | A23–A1 Float Delay | (Note 1) | 15 | 4 | 20 | ns |
| 8 | $\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Valid Delay | $C_L$ = 50 pF | 8 | 4 | 13 | ns |
| 9 | $\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Float Delay | (Note 1) | 15 | 4 | 20 | ns |
| 10 | M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$ Valid Delay | $C_L$ = 50 pF | 8 | 4 | 13 | ns |
| 11 | W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay | (Note 1) | 15 | 4 | 20 | ns |
| 12 | D15–D0 Write Data Valid Delay | $C_L$ = 50 pF (Note 4) | 8 | 7 | 18 | ns |
| 12a | D15–D0 Write Data Hold Time | $C_L$ = 50 pF | 10 | 2 | | ns |
| 13 | D15–D0 Write Data Float Delay | (Note 1) | 15 | 4 | 17 | ns |
| 14 | HLDA Valid Delay | $C_L$ = 50 pF | 15 | 4 | 17 | ns |
| 14f | HLDA Float Delay | | 15 | 4 | 17 | ns |
| 15 | $\overline{NA}$ Setup Time | | 7 | 5 | | ns |
| 16 | $\overline{NA}$ Hold Time | | 7 | 2 | | ns |
| 19 | $\overline{READY}$ Setup Time | | 7 | 7 | | ns |
| 20 | $\overline{READY}$ Hold Time | | 7 | 4 | | ns |
| 21 | D15–D0 Read Data Setup Time | | 7 | 4 | | ns |
| 22 | D15–D0 Read Data Hold Time | | 7 | 3 | | ns |
| 23 | HOLD Setup Time | | 7 | 4 | | ns |
| 24 | HOLD Hold Time | | 7 | 2 | | ns |
| 25 | RESET Setup Time | | 17 | 4 | | ns |
| 26 | RESET Hold Time | | 17 | 2 | | ns |
| 27 | NMI, INTR Setup Time | (Note 2) | 7 | 5 | | ns |
| 28 | NMI, INTR Hold Time | (Note 2) | 7 | 5 | | ns |
| 29 | PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Setup Time | (Note 2) | 7 | 5 | | ns |
| 30 | PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Hold Time | (Note 2) | 7 | 4 | | ns |

***Notes:***

1. *Float condition occurs when maximum output current becomes less than $I_{LO}$ in magnitude. Float delay is not 100% tested.*
2. *These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.*
3. *Rise and Fall times are not tested. They are guaranteed by design characterization.*
4. *Min time is not 100% tested.*

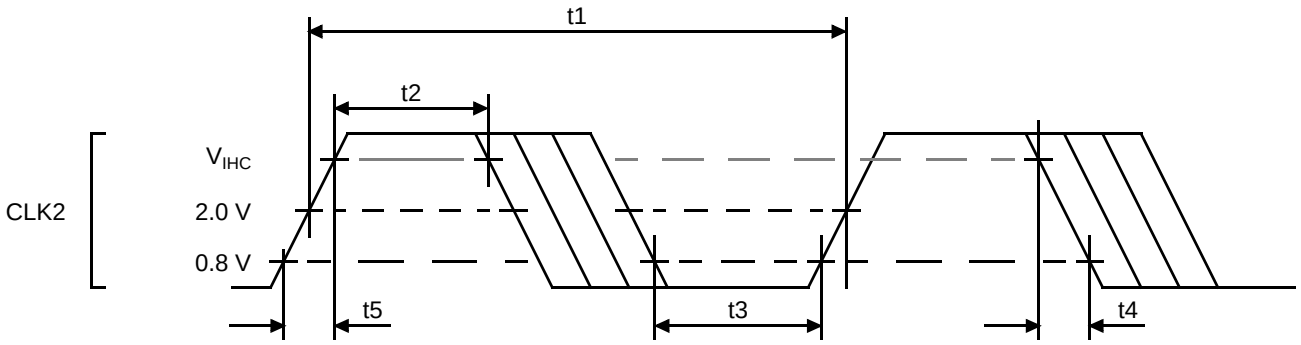
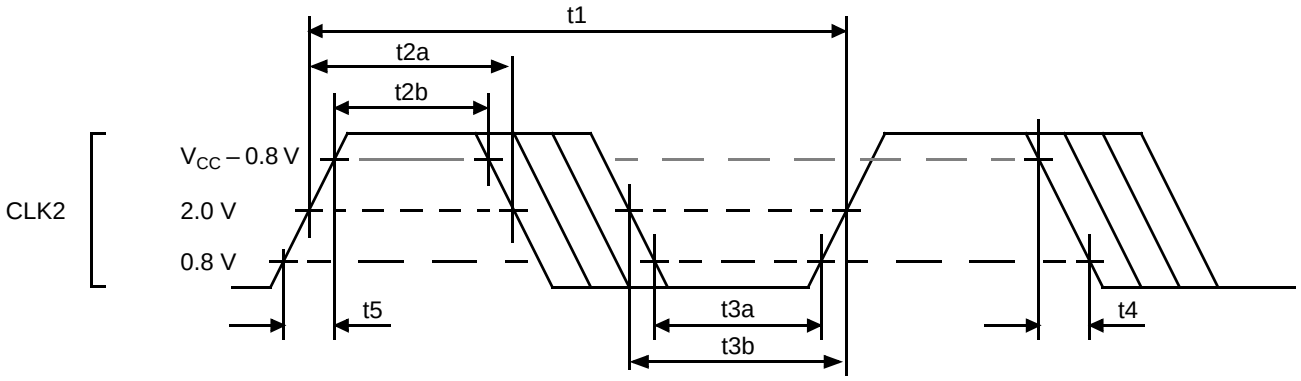


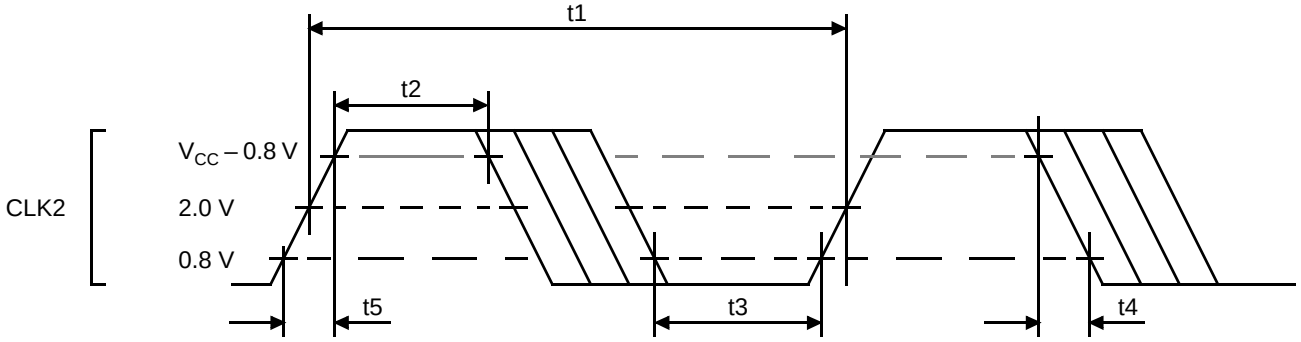

**Figure 3. CLK2 Timing (Am386SXLV 25 MHz)**

16305C–004



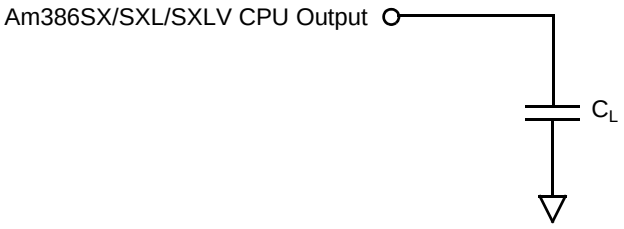

15022B-031

**Figure 4. CLK2 Timing (Am386SX/SXL 25 and 33 MHz)**




15022B-031a

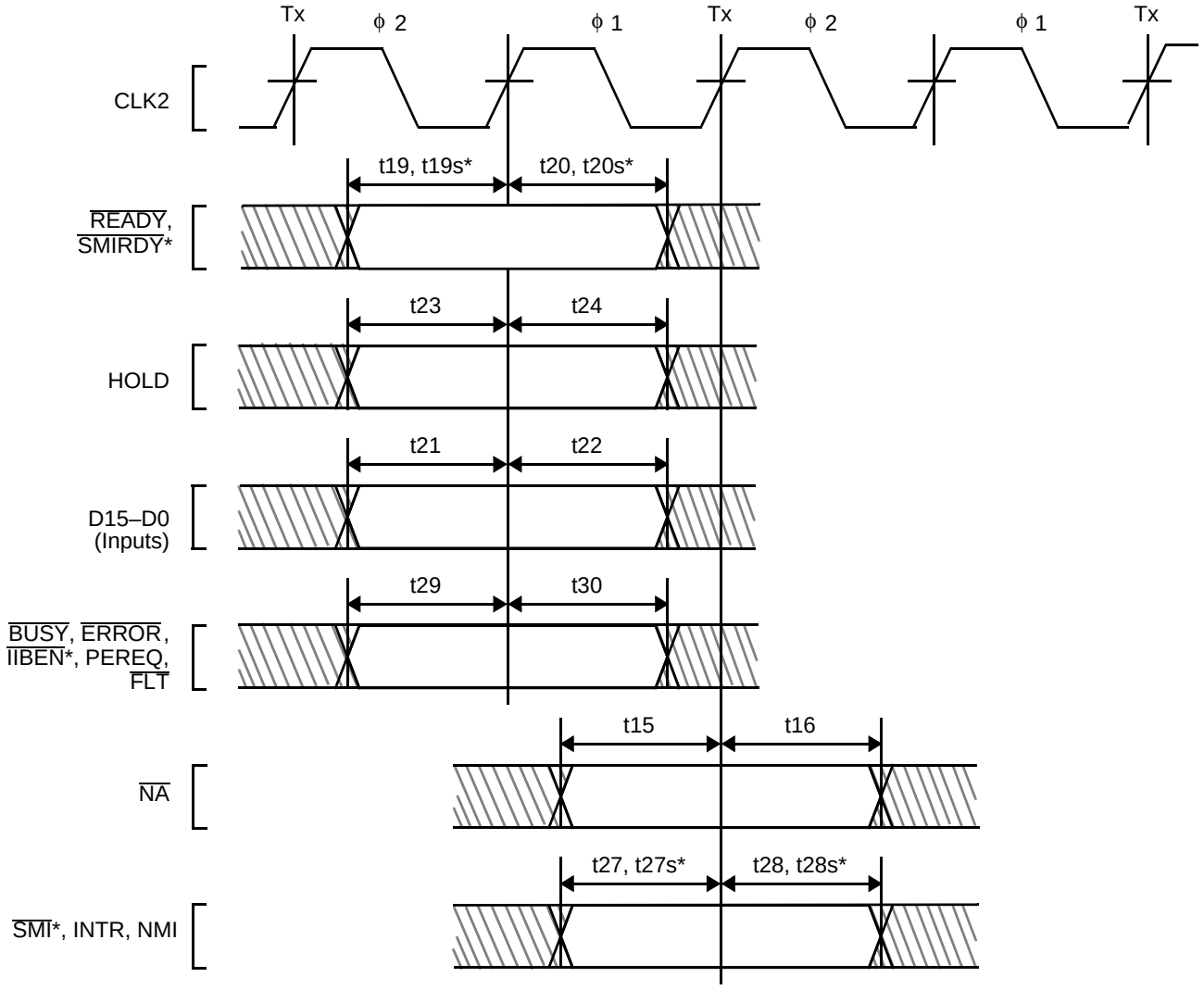
**Figure 5. CLK2 Timing (Am386SX 40 MHz)**




15022B–032

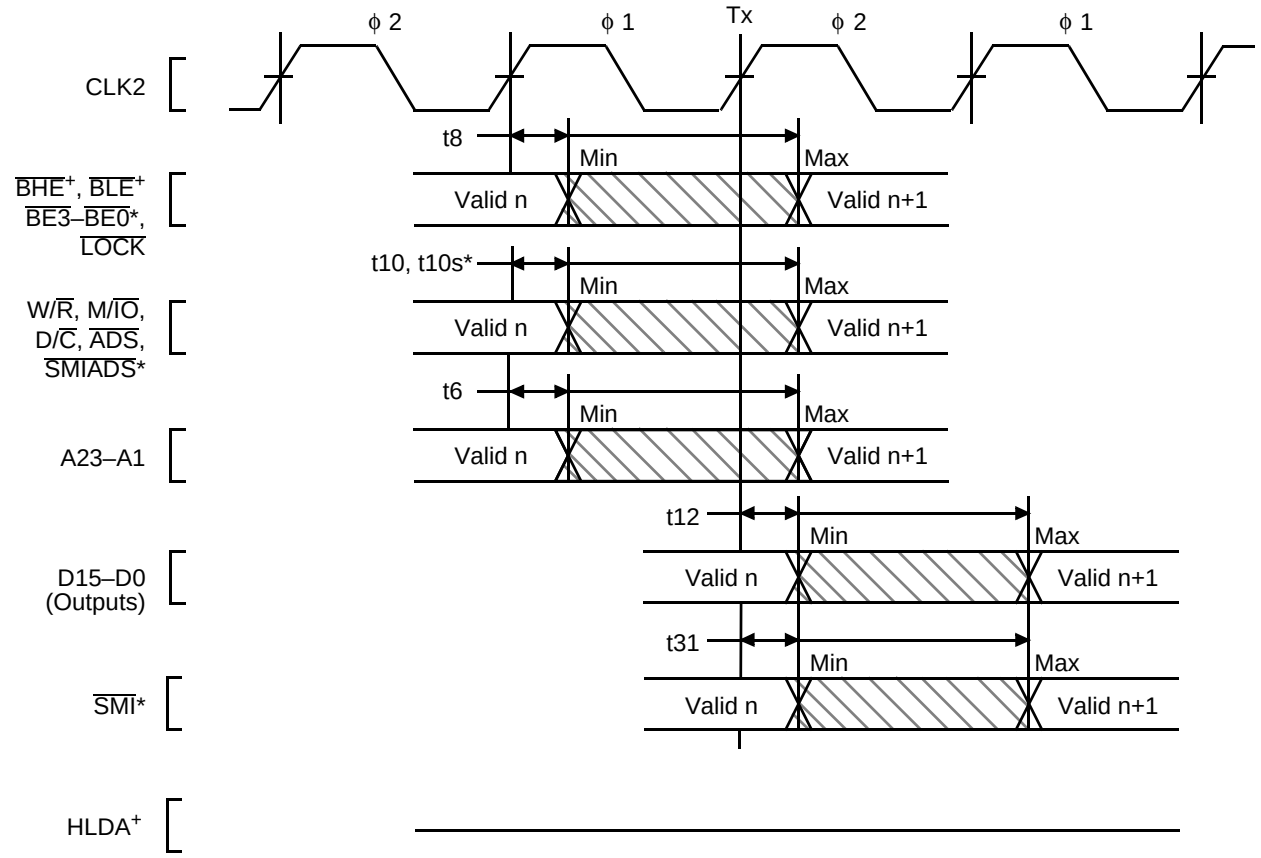
**Figure 6. AC Test Circuit**

## SWITCHING WAVEFORMS




** – On Am386SXLV only*

**Figure 7. Input Setup and Hold Timing**




*+ – On Am386SX/SXL only*
** – On Am386SXLV only*

**Figure 8. Output Valid Delay Timing**

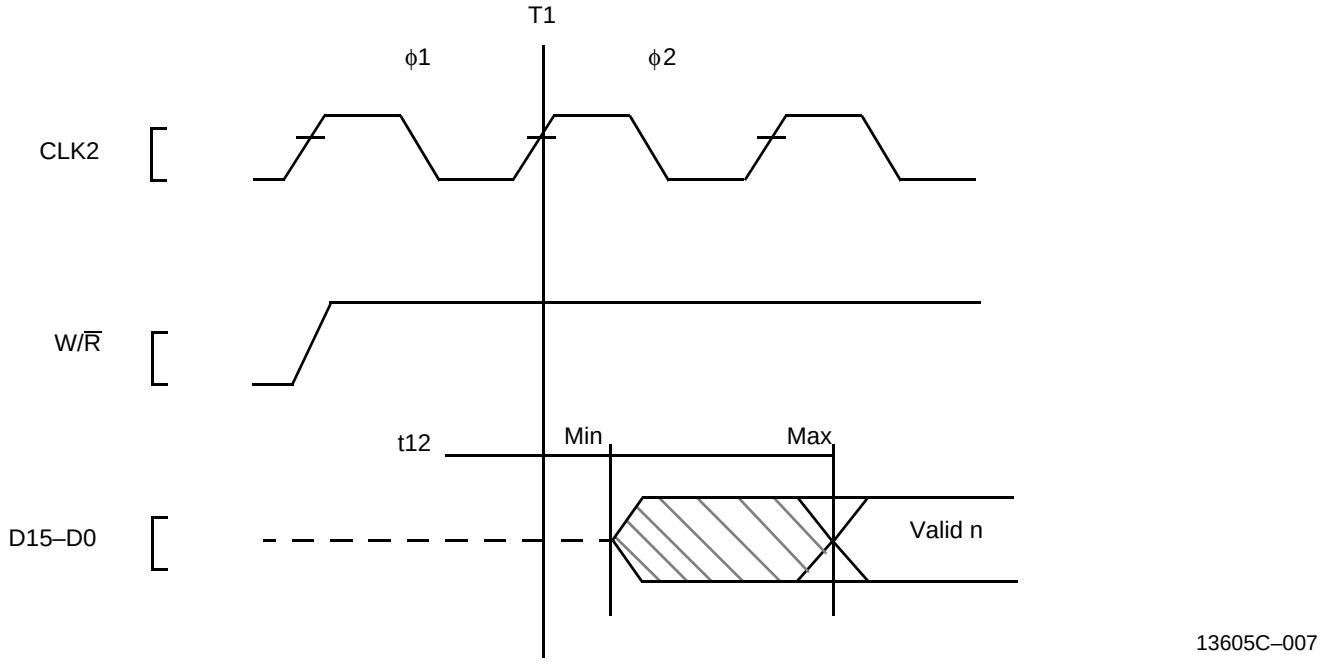



**Figure 9. Write Data Valid Delay Timing**

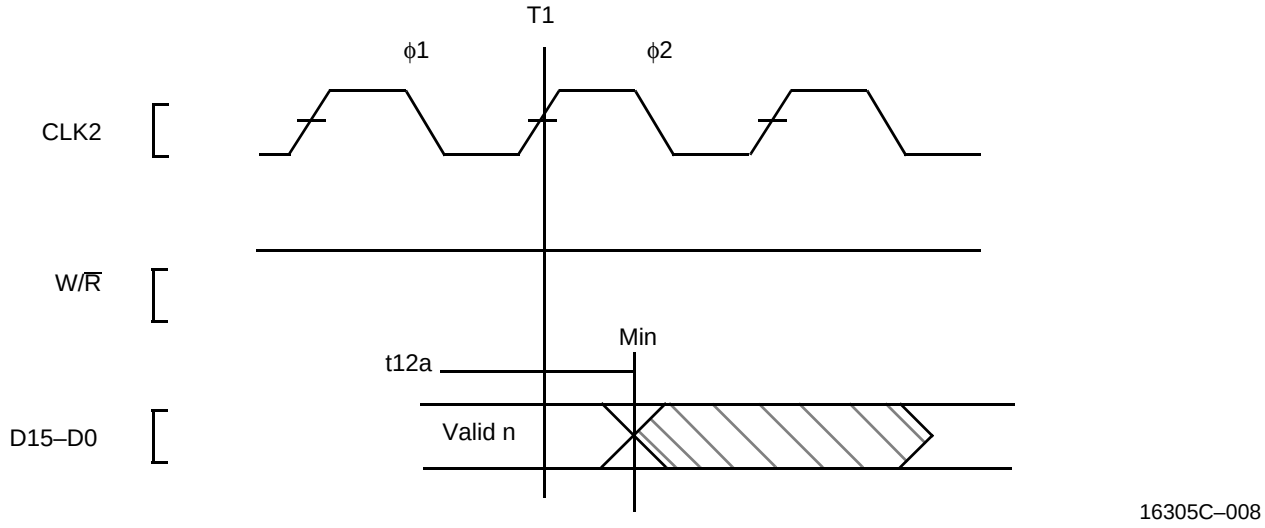
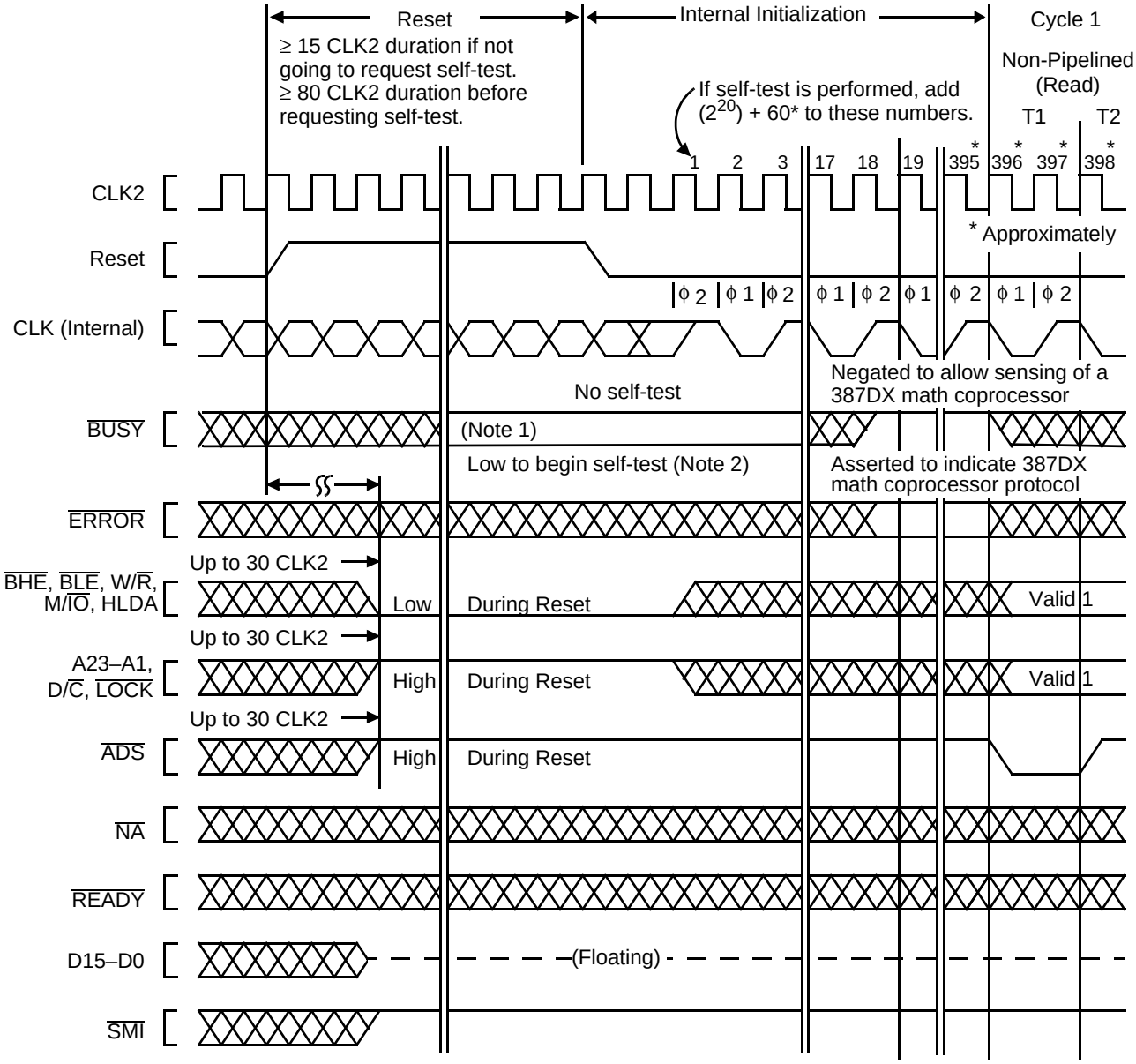



**Figure 10. Write Data Hold Timing**

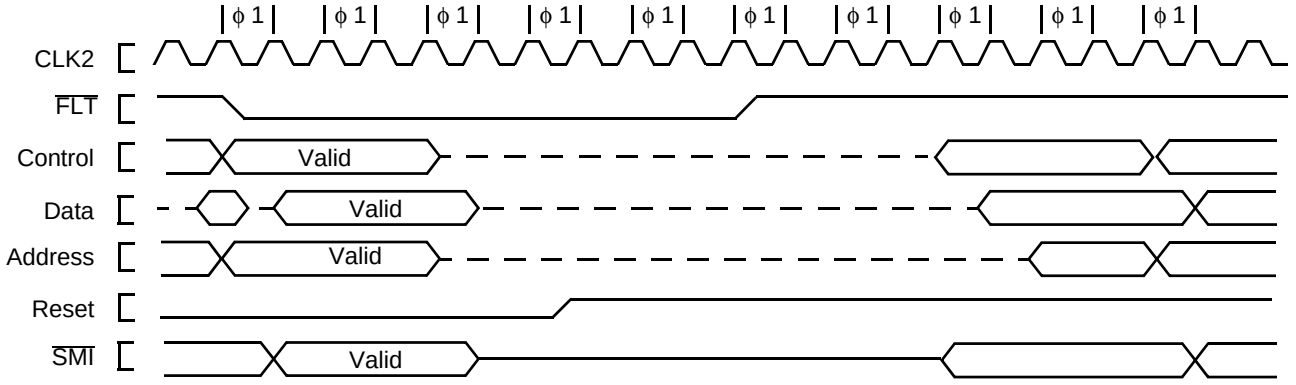



***Notes:***

1. *BUSY should be held stable for eight CLK2 periods before and after the CLK2 period in which the RESET falling edge occurs.*
2. *If self-test is requested, the Am386SXLV microprocessor outputs remain in their reset state as shown here.*

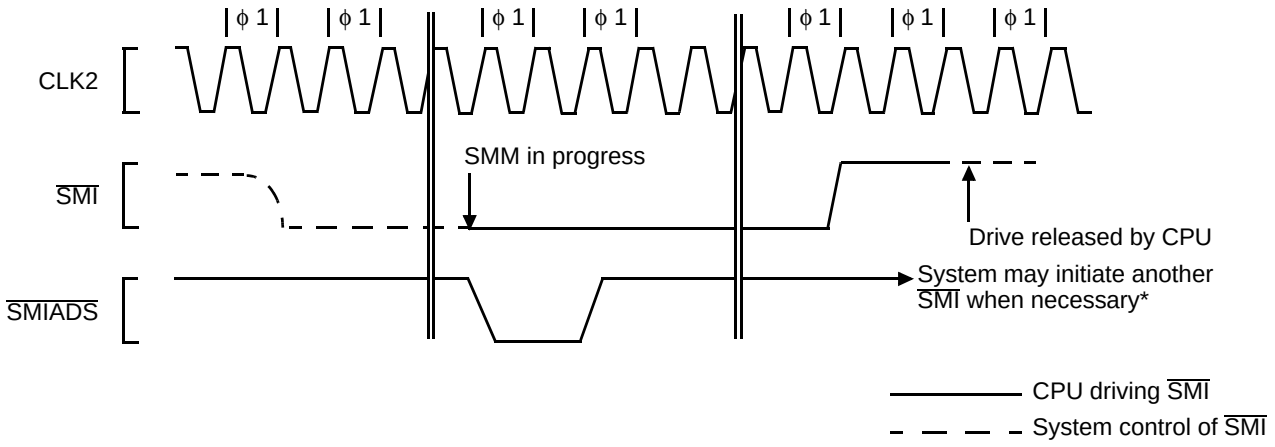
16305C–009

**Figure 11. Bus Activity from Reset Until First Code Fetch (Am386SXLV Only)**




16306B–008

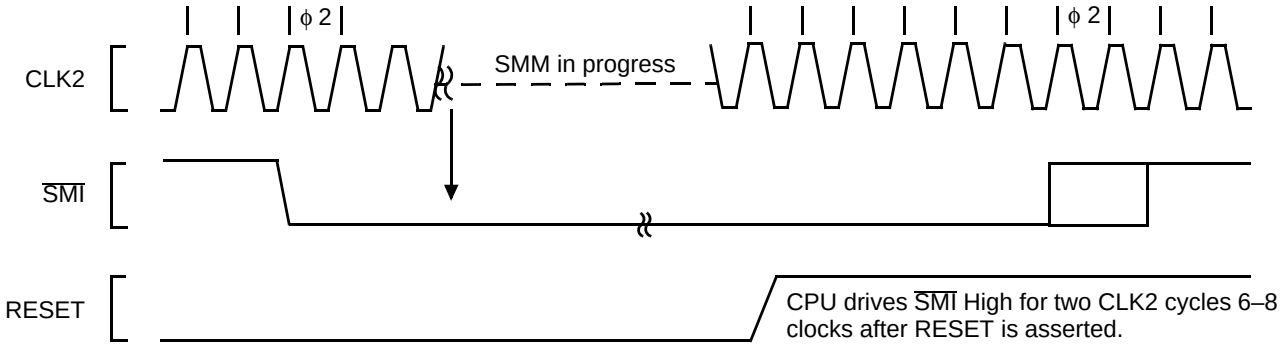
**Figure 12. Entering and Exiting $\overline{\text{FLT}}$ (Am386SXLV Only)**




*Once initiated, the system must hold $\overline{\text{SMI}}$ Low until the first $\overline{\text{SMIADS}}$. At this time, the system cannot drive $\overline{\text{SMI}}$ until three CLK2 cycles after the CPU drives $\overline{\text{SMI}}$ High. (The CPU will drive $\overline{\text{SMI}}$ High for two CLK2 cycles. The additional clock allows the CPU to completely release $\overline{\text{SMI}}$ and prevents any driver overlap.)

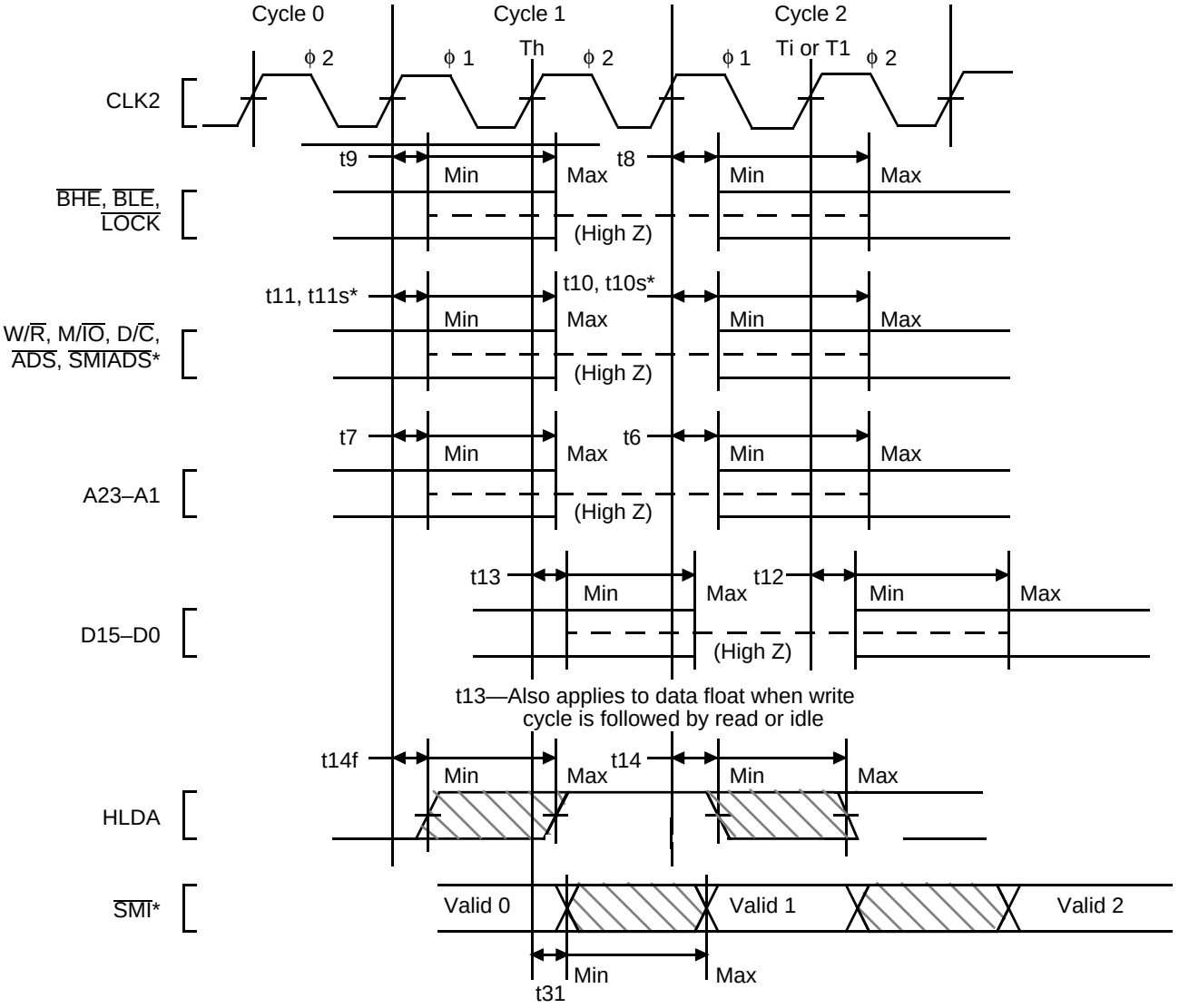
16306B–011

**Figure 13. Initiating and Exiting SMM (Am386SXLV Only)**




16306B–010

**Figure 14. RESET and $\overline{\text{SMI}}$ (Am386SXLV Only)**




** – On Am386SXLV only*

**Figure 15. Output Float Delay and HLDA and SMI* Valid Delay Timing**

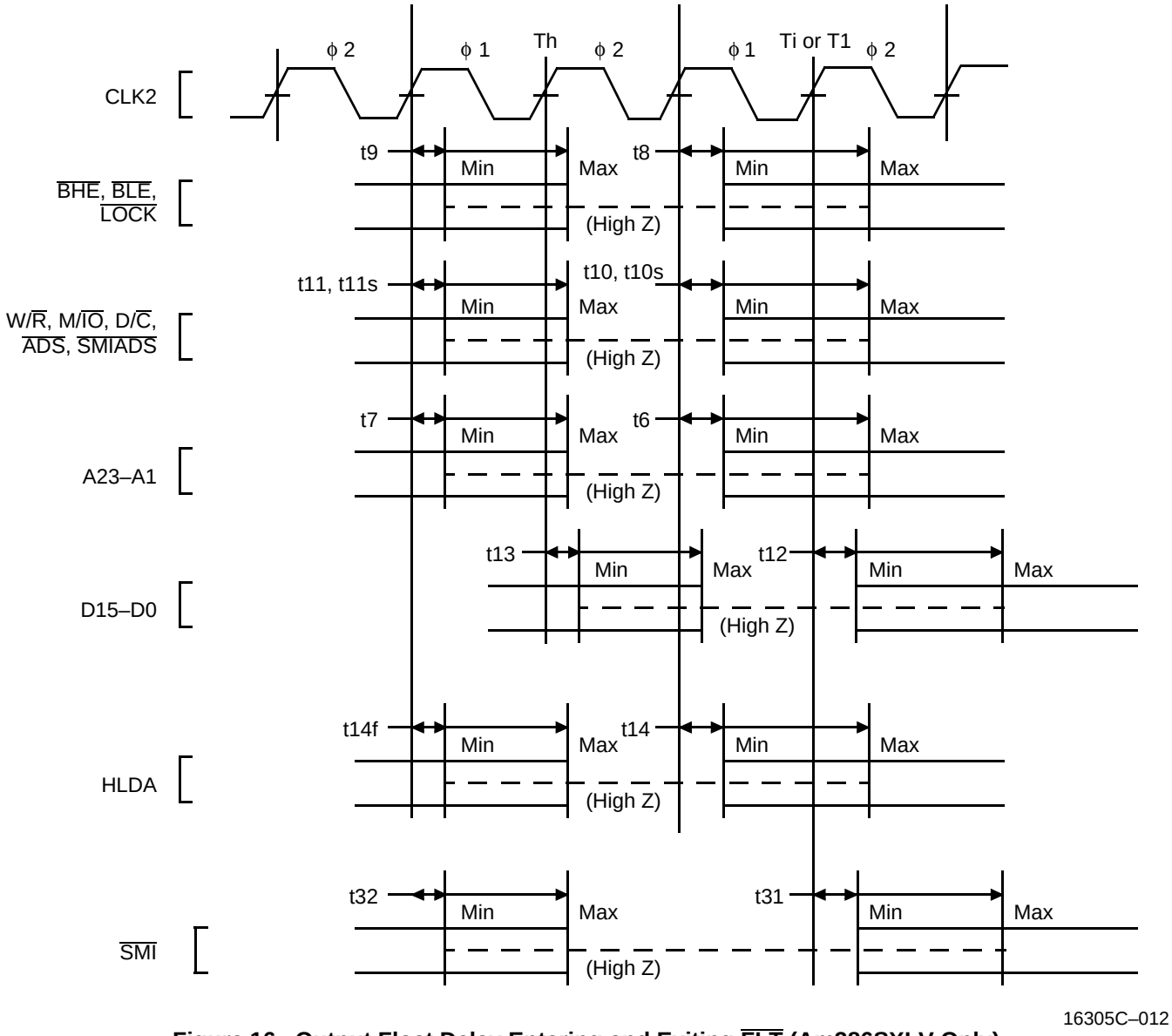
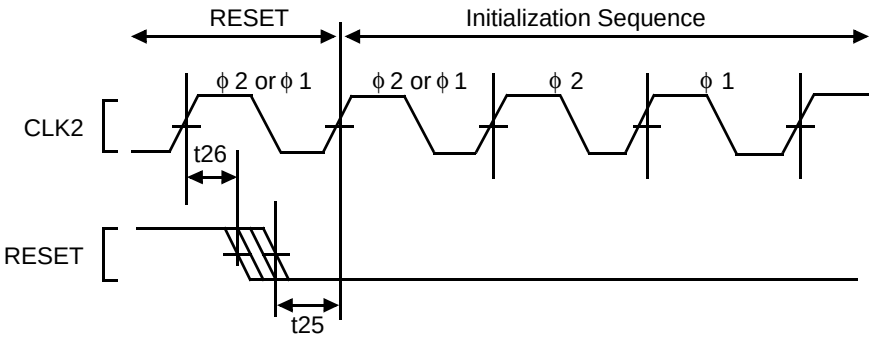


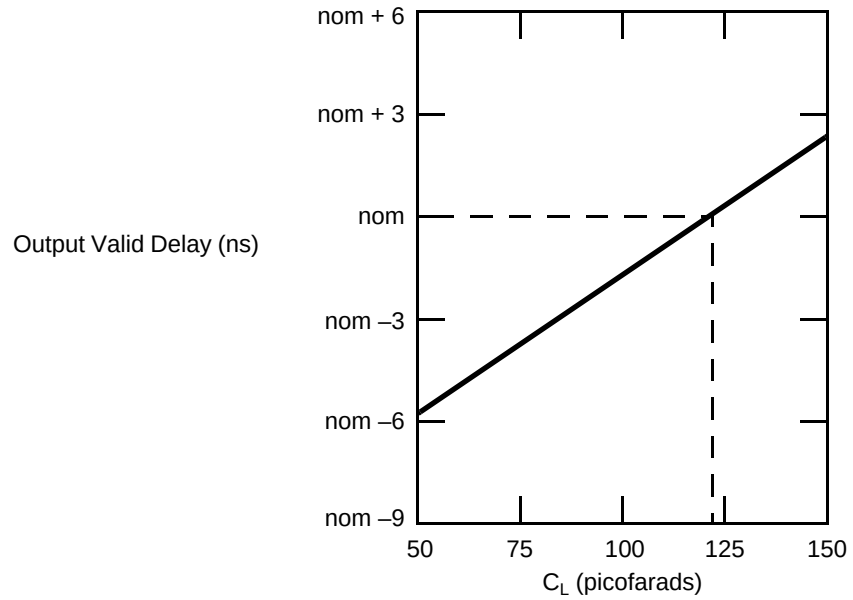

**Figure 16. Output Float Delay Entering and Exiting $\overline{FLT}$ (Am386SXLV Only)**




The second internal processor phase following RESET High-to-Low transition (provided t25 and t26 are met) is ϕ2.

15021B–084

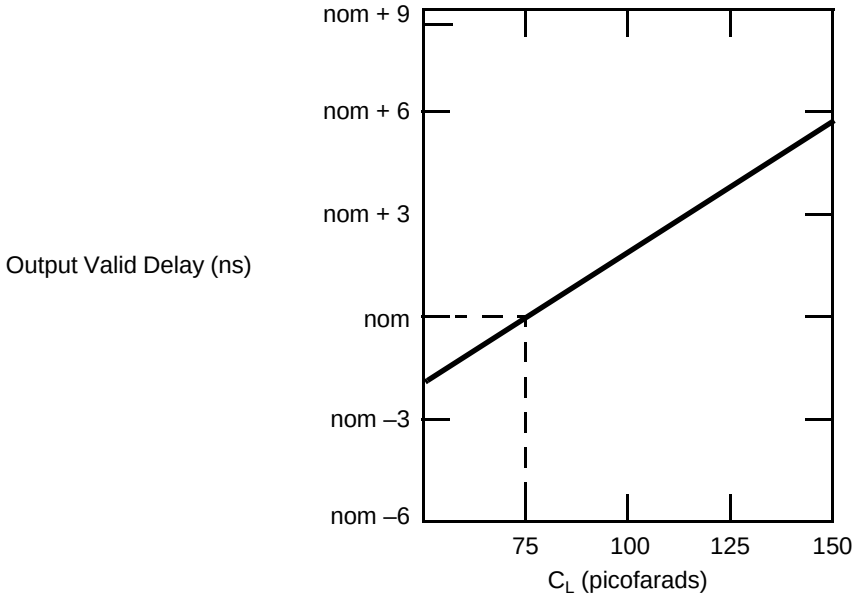
**Figure 17. RESET Setup and Hold Timing and Internal Phase**




***Note:***
*This graph will not be linear outside the $C_L$ range shown.*

15021B–079

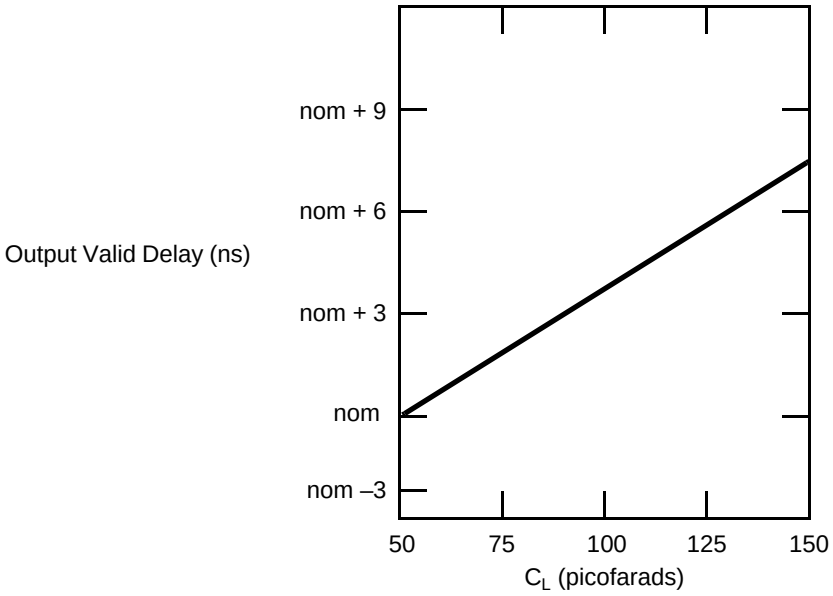
**Figure 18. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ($C_L$=120 pF)**




***Note:***
*This graph will not be linear outside the $C_L$ range shown.*

15021B–080

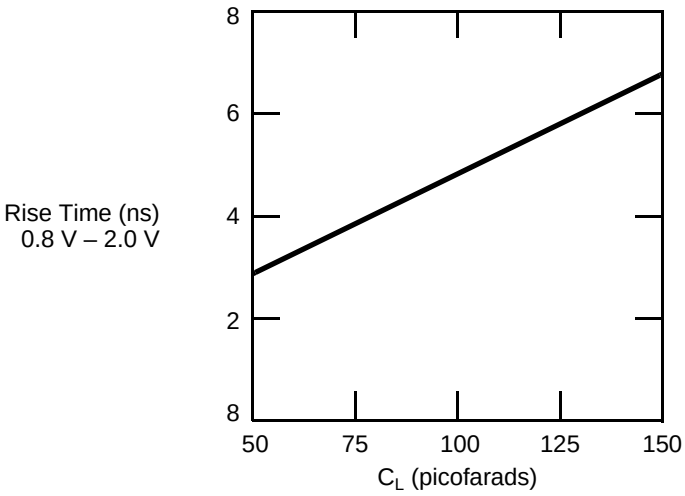
**Figure 19. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ($C_L$=75 pF)**




***Note:***
*This graph will not be linear outside the $C_L$ range shown.*

15021B–081

**Figure 20. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ($C_L$=50 pF)**




***Note:***
*This graph will not be linear outside the $C_L$ range shown.*

15021B–082

**Figure 21. Typical Output Rise Time Versus Load Capacitance at Maximum Operating Temperature**

## DIFFERENCES BETWEEN THE Am386SX/SXL/SXLV AND Am386DX/DXL CPU

The following are the major differences between the Am386SX/SXL/SXLV and the Am386DX/DXL CPU. For brevity, throughout this section the Am386SX/SXL/SXLV CPU is referred to as the SX CPU, and the Am386DX/DXL CPU is referred to as the DX CPU.

- The SX CPU generates byte selects on $\overline{BHE}$ and $\overline{BLE}$ (like the 8086 and 80286) to distinguish the upper and lower bytes on its 16-bit data bus. The DX CPU uses four byte selects, $\overline{BE3}$–$\overline{BE0}$, to distinguish between the different bytes on its 32-bit bus.
- The SX CPU has no bus sizing option. The DX CPU can select between either a 32-bit bus or a 16-bit bus by use of the $\overline{BS16}$ input. The SX CPU has a 16-bit bus size.
- The $\overline{NA}$ pin operation in the SX CPU is identical to that of the $\overline{NA}$ pin on the DX CPU with one exception: the DX CPU $\overline{NA}$ pin cannot be activated on 16-bit bus cycles (where $\overline{BS16}$ is Low in the DX CPU case), whereas $\overline{NA}$ can be activated on any SX CPU bus cycle.
- The contents of all SX CPU registers at reset are identical to the contents of the DX CPU registers at reset, except for the DX register. The DX register contains a component-stepping identifier at reset, that is:
  - In the DX CPU, after reset:
    DH = 3 indicates DX CPU
    DI = revision number
  - In the SX CPU, after reset:
    DH = 23H indicates SX CPU
    DL = revision number
- The DX CPU uses A31 and M/$\overline{IO}$ as selects for the math coprocessor. The SX CPU uses A23 and M/$\overline{IO}$ as selects.
- The DX CPU prefetch unit fetches code in four-byte units. The SX CPU prefetch unit reads two bytes as one unit (like the 80286). In $\overline{BS16}$ mode, the DX CPU takes two consecutive bus cycles to complete a prefetch request. If there is a data read or write request after the prefetch starts, the DX CPU will fetch all four bytes before addressing the new request.
- Both the DX CPU and SX CPU have the same logical address space. The only difference is that the DX CPU has a 32-bit physical address space and the SX CPU has a 24-bit physical address space. The SX CPU has a physical memory address space of up to 16 Mbyte instead of the 4 Gbyte available to the DX CPU. Therefore, in SX CPU systems, the operating system must be aware of this physical memory limit and should allocate memory for applications programs within this limit. If a DX CPU system uses only the lower 16 Mbyte of physical address, then there will be no extra effort required to migrate DX CPU software to the SX CPU. Any application which uses more than 16 Mbyte of memory can run on the SX CPU, if the operating system utilizes the SX CPU's paging mechanism. In spite of this difference in physical address space, the SX CPU and the DX CPU can run the same operating systems and applications within their respective physical memory constraints.
- The SX CPU has an input called $\overline{FLT}$, which three-states all bi-directional and output pins, including HLDA, when asserted. It is used with ON-Circuit Emulation (ONCE).

## PACKAGE THERMAL SPECIFICATIONS

The Am386SX/SXL/SXLV processors are specified for operation when $T_{CASE}$ (the case temperature) is within the range of 0°C to +100°C for commercial parts, and –40°C to +100°C for industrial parts. $T_{CASE}$ can be measured in any environment to determine whether the Am386SX/SXL/SXLV processors are within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

The ambient temperature ($T_A$) is guaranteed as long as $T_{CASE}$ is not violated. The ambient temperature can be calculated from $\theta_{JC}$ and $\theta_{JA}$ and from these equations:

$$T_J = T_{CASE} + P \bullet \theta_{JC}$$
$$T_A = T_J - P \bullet \theta_{JA}$$
$$T_{CASE} = T_A + P \bullet [\theta_{JA} - \theta_{JC}]$$

where:

$T_J$, $T_A$, $T_{CASE}$ = Junction, Ambient, and Case Temperature
$\theta_{JC}$, $\theta_{JA}$ = Junction-to-Case and Junction-to-Ambient Thermal Resistance, respectively
P = Maximum Power Consumption

In the 100-lead PQFP package, $\theta_{JA}$=45.0 and $\theta_{JC}$=11.0.

## ELECTRICAL SPECIFICATIONS

The Am386SX/SXL/SXLV CPU has modest power requirements. However, its high clock frequency and 47 output buffers (address, data, control, and HLDA) can cause power surges as multiple output buffers drive new signal levels simultaneously. For clean on-chip power distribution at high frequency, 14 $V_{CC}$ and 18 $V_{SS}$ pins separately feed functional units of the Am386SX/SXL/SXLV CPU.

Power and ground connections must be made to all external $V_{CC}$ and $V_{SS}$ pins of the Am386SX/SXL/SXLV CPU. On the circuit board, all $V_{CC}$ pins should be connected on a $V_{CC}$ plane, and $V_{SS}$ pins should be connected on a GND plane.

### Power Decoupling Recommendations

Liberal decoupling capacitors should be placed near the Am386SX/SXL/SXLV CPU. The Am386SX/SXL/SXLV CPU driving its 24-bit address bus and 16-bit data bus at high frequencies can cause transient power surges, particularly when driving large capacitive loads. Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the Am386SX/SXL/SXLV CPU and decoupling capacitors as much as possible.

### Resistor Recommendations

The $\overline{\text{ERROR}}$, $\overline{\text{FLT}}$, and $\overline{\text{BUSY}}$ inputs have internal pull-up resistors of approximately 20 Kohms, and the PEREQ input has an internal pull-down resistor of approximately 20 Kohms, built into the Am386SX/SXL/SXLV CPU to keep these signals inactive when a 387SX-compatible math coprocessor is not present in the system (or temporarily removed from its socket).

In typical designs, the external pull-up resistors shown in Table 1 are recommended. However, a particular design may have reason to adjust the resistor values recommended here, or alter the use of pull-up resistors in other ways.

### Other Connection Recommendations

For reliable operation, always connect unused inputs to an appropriate signal level. NC pins should always remain unconnected. Connection of NC pins to $V_{CC}$ or $V_{SS}$ will result in component malfunction or incompatibility with future steppings of the Am386SX/SXL/SXLV CPU.

Particularly when not using the interrupts or bus hold (as when first prototyping), prevent any chance of spurious activity by connecting these associated inputs to GND:

| Pin | Signal |
|---|---|
| 40 | INTR |
| 38 | NMI |
| 4 | HOLD |

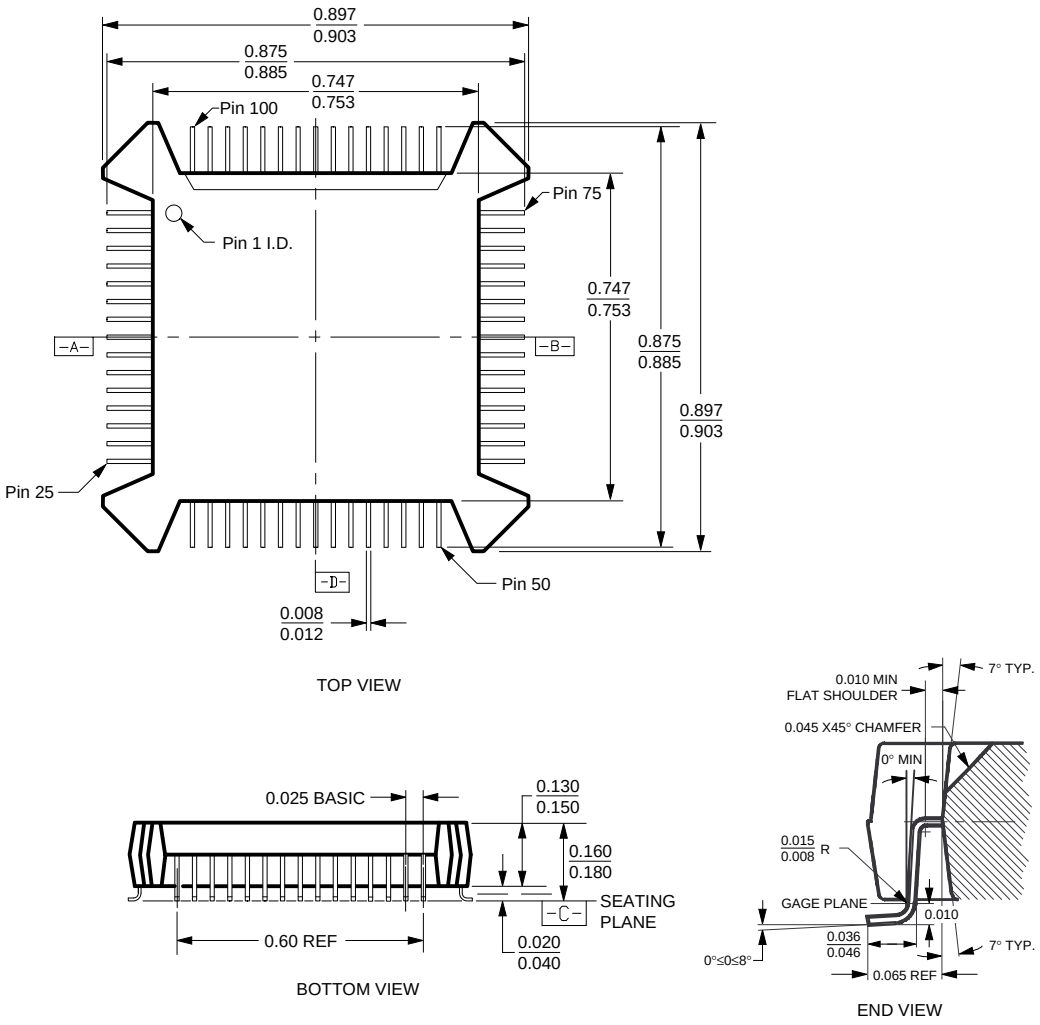
If not using address pipelining, connect pin 6 ($\overline{\text{NA}}$) through a pull-up in the range of 20 Kohms to $V_{CC}$.

**Table 1. Recommended Resistor Pull-Ups to $V_{CC}$**

| Pin | Signal | Pull-Up Value | Purpose |
|---|---|---|---|
| 16 | $\overline{\text{ADS}}$ | 20 Kohms ± 10% | Lightly pull $\overline{\text{ADS}}$ inactive during Am386SX/SXL/SXLV CPU Hold Acknowledge states. |
| 26 | $\overline{\text{LOCK}}$ | 20 Kohms ± 10% | Lightly pull $\overline{\text{LOCK}}$ inactive during Am386SX/SXL/SXLV CPU Hold Acknowledge states. |

## PHYSICAL DIMENSIONS

## PQB 100 (Plastic Quad Flat Pack, Trimmed and Formed)




16-038-PQB
PQB100
DB90
3-6-97 lv

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