

DC CHARACTERISTICS

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Symbol	Personator	ilin .	(Men	Unit	Test Condition		
VILC	Clock Input Low Voltage	-0.3*	+0.45*	v			
VHC	Clock Input High Voltage	Vcc-06*	+8.5*	v			
Ve	Input Low Vollage	-0.3*	+0.8*	۷			
Val	input High Vollage	+2.0*	+5.5*	v			
Va	Output Low Voltage		+0.4*	v	los = 20mA		
VOH I	Output High Voltage	+24*		v	lon = - 250 pt		
	Input/3-State Output Lealage Current	- 10*	+ 10*	م ر	0.4 < Vm < 2.4		
ùn -	Rt Pin Lookage Current	-40*	+ 10*	*	0.4 < V _{IN} < 2.4%		
łoc 🛛	Power Supply Current		. 100°	mA			

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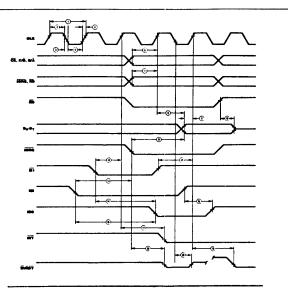
a Tested b Guarantaed by Design c Guarantaed by Characterization

AC CHARACTERISTICS"

Number	Symbol	Parameter	280-4 Min	DART	200-6 Min	DART
1	TeC	Clock Cycle Time	250*	4000 *	165 *	4000*
2	TeCh	Clock Width (High)	105*	2000 °	70*	2000
3	TIC .	Clock Fell Time		30 *		15
4	10	Clock Rise Time		30 °		154
5	TeCl	Clock Width (Low)	105*	2000 °	70*	2000
	TeAD(C)	CE, C/D, B/Ä to Clock † Setup Time	145*		60°	
7	TeCS(C)	ICRO, RD to Clock † Setup Time	115*		60 °	
	TaC(DO)	Clock 1 to Data Out Dalay		220 °		150
	TsDI(C)	Data in to Clock I Setup (Write or M1 Cycle)	50 ·		30*	
10	ToPD(DOz)	RD 1 to Data Out Float Datey		110°		909
11	TalO(DOI)	IORO - to Date Out Datey (INTACK Cycle)		160°		100
12	TsM1(C)	MT to Clock 1 Setup Time	90 *		75 •	
13	TalEI(IC)	IEI to IORO I Setup Time (INTACK Cycle)	140 °		120 °	
14	TdM1(IEO)	MT 4 to IEO 4 Delay (interrupt before M1)		190 °		160 9
15	TallEl(IEOr)	IEI 1 to IEO 1 Delay (alter ED decode)		100 °		70 9
16	TOTEL(IEOI)	EI + to EO + Datey		100 *		70*
17	ToC(INT)	Clock t to INT # Deley		200 °		150
18	TotO(W/RWI)	ICRG I or CE I to W/RDY IDelay (Wat Mode)		210¢		1754
19	Toc(W/RP)	Clock t to W/RDY + Delay (Ready Mode)		120*		100 9
20	ToC(W/RWz)	Clock I to W/RDY Floet Delay (West Mode)		130°		1104

"Units in narroseconds (ns). e Tested b Guerantaed by Design c Gueranteed by Cherecterizetien

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AC CHARACTERISTICS (Commund)

Number	Symbol	Parameter	160-4 Min	DART Mex	280-4	6 DART	Notes*
					ili n	Nex	
1	1wPh	Pulse Width (High)	200 ¢		200 ¢		2
2	TwPt	Pulse Width (Low)	200 ¢		200¢		2
3	TcTrC	TrC Cycle Time	400*		330 ¢	• ¢	2
4	WBCI	TrC Wrath (Low)	180°		100 ¢	t	2
5	Wit/Ch	TiC Width (High)	180 °	÷,	100 °	• c	2
8	TofleC(TxD)	TeC 4 to TeD Datay		300*		220*	2
7	Totac(W/RRI)	SC + to W/RDV + Delay (Ready Mode)	50		5°	8 C	1
8	ToThC(INT)	SiC 4 to INT 4 Datay	50	. gc	50	9¢	1
	TeRxC	Ric Cycle Time	400 °	• °	330¢	C	2
10	TerRaCl	FixC Width (Low)	180 °	-c	100 °	•• C	2
11	TwRxCh	RuC Width (High)	180*	-	100 °	c	2
12	TeRxD(RxC)	RxD to RxC 1 Setup Time (x1 Mode)	0¢		0¢		2
13	ThRxD(RxC)	RxD Hold Time (x1 Mode)	140 ¢		100 °		2
14	ToRxC(W/RRI)	Ric t to W/RDY I Delay (Ready Mode)	10°	13¢	10 °	13¢	1
15	TdRxC(INT)	RuC t to INT + Delay	10 °	13¢	10¢	13¢	1

* In all model, the System Clock rate must be at least twe 1. Une squarts System Clock Percols, 2. Unes nemessioned ing 2. Test.ed 5. Guaranteed by Design c. Guaranteed by Characterization RESET must be active a m

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