PRELIMINARY

CY8C20111, CY8C20121

CapSense Express™ - One Button and Two Button Capacitive Controllers

1. Features

- Capacitive Button Input tied to a Configurable Output
  - Robust sensing algorithm
  - High sensitivity, low noise
  - Immunity to RF and AC noise
  - Low radiated EMC noise
  - Supports wide range of input capacitance, sensor shapes, and sizes
- Target Applications
  - Printers
  - Cellular handsets
  - LCD monitors
  - Portable DVD players
- Industry's Best Configurability
  - Custom sensor tuning
  - Output supports strong 20 mA sink current
  - Output state can be controlled through I^2C or directly from CapSense input state
  - Run time reconfigurable over I^2C
- Advanced Features
  - Plug-and-play with factory defaults – tuned to support up to 1 mm overlay
  - Nonvolatile storage of custom settings
  - Easy integration into existing products – configure output to match system
  - No external components required
  - World class free configuration tool
- Wide Range of Operating Voltages
  - 2.45V to 2.9V
  - 3.10V to 3.6V
  - 4.75V to 5.25V
- I^2C Communication
  - Supported from 1.8V
  - Internal pull up resistor support option
  - Data rate up to 400 kbps.
  - Configurable I^2C addressing
- Industrial Temperature Range: –40°C to +85°C
- Available in 8-Pin SOIC Package

2. Overview

The CapSense Express™ controllers support two capacitive sensing (CapSense) buttons and two general purpose outputs in CY8C20121 and one CapSense button and one general purpose output in CY8C20111. The device functionality is configured through the I^2C port and can be stored in on-board nonvolatile memory for automatic loading at power on. The digital outputs are controlled from CapSense inputs in factory default settings, but are user configurable for direct control through I^2C.

The four key blocks that make up the CY8C20111 and CY8C20121 controllers are: a robust capacitive sensing core with high immunity against radiated and conductive noise, control registers with nonvolatile storage, configurable outputs, and I^2C communications. The user can configure registers with parameters needed to adjust the operation and sensitivity of the CapSense buttons and outputs and permanently store the settings. The standard I^2C serial communication interface allows the host to configure the device and read sensor information in real time. I^2C address is fully configurable without any external hardware strapping.

3. Pinouts

Figure 1. CY8C20111 Pin Diagram - 8 SOIC - 1 Button

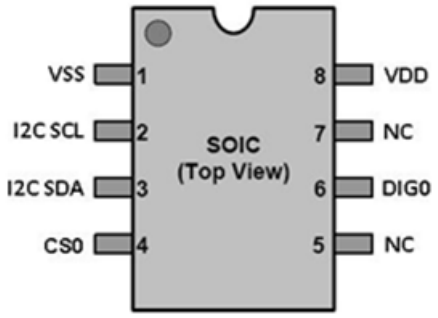


Table 1. Pin Definitions – 8 SOIC- 1 Button

Pin No	Name	Description
1	VSS	Ground
2	I2C SCL	I^2C Clock
3	I2C SDA	I^2C Data
4	CS0	CapSense Input
5	NC	No Connect
6	DIG0	Digital Output
7	NC	No Connect
8	VDD	Supply Voltage

Figure 2. CY8C20121 Pin Diagram – 8 SOIC- 2 Button

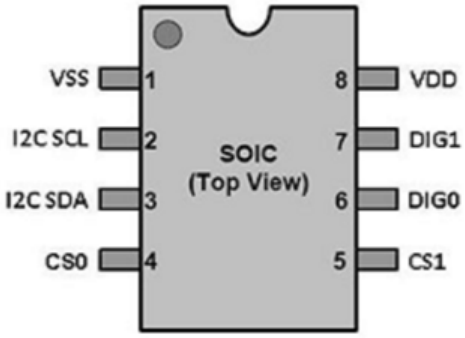
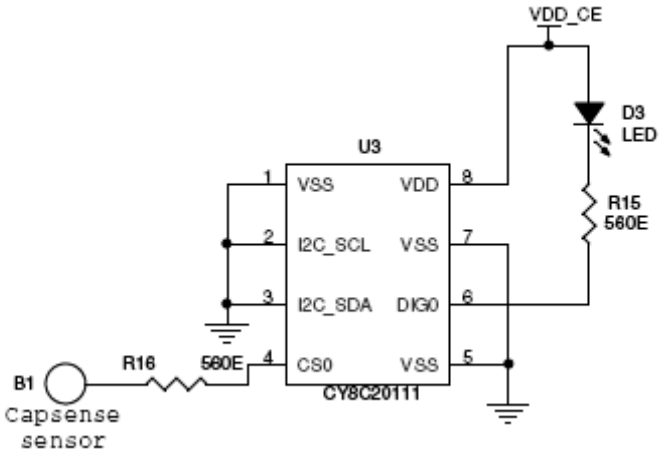


Table 2. Pin Definitions – 8 SOIC- 2 Button

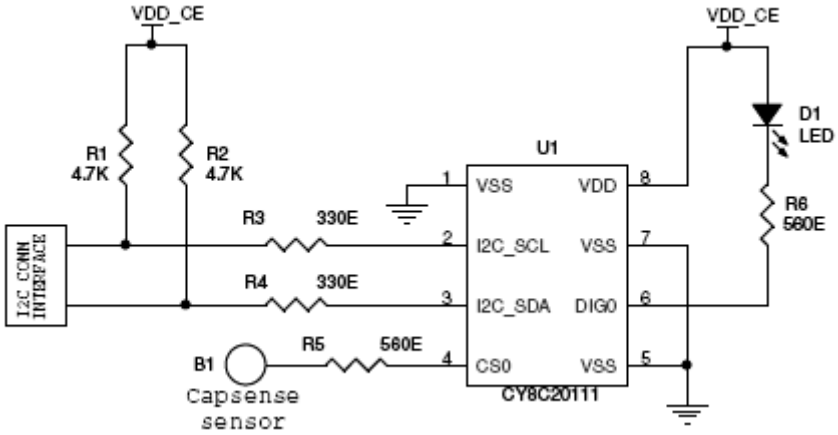
Pin No	Name	Description
1	VSS	Ground
2	I2C SCL	I^2C Clock
3	I2C SDA	I^2C Data
4	CS0	CapSense Input
5	CS1	CapSense Input
6	DIG0	Digital Output
7	DIG1	Digital Output
8	VDD	Supply Voltage

4. Typical Circuits

4.1 Circuit-1: One Button and One LED[1]

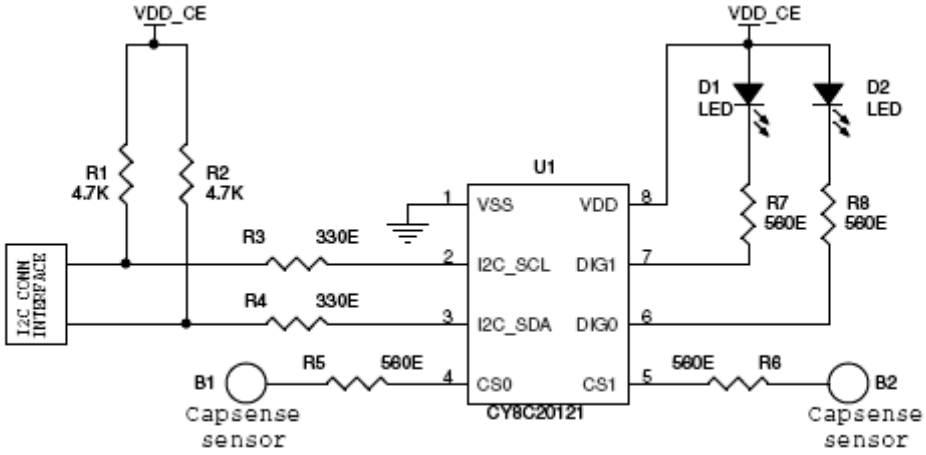


4.2 Circuit-2: One Button and One LED with I²C Interface

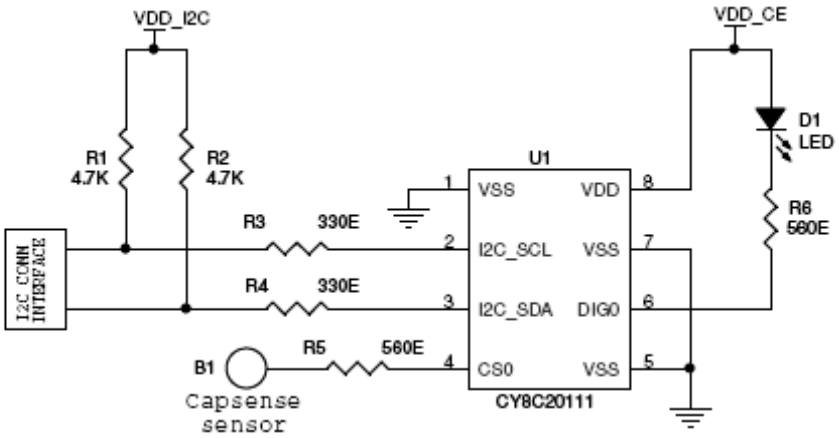


Note
1. The sensors are factory tuned to work with 1 mm plastic or glass overlay.

4.3 Circuit-3: Two Buttons and Two LEDs with I²C Interface

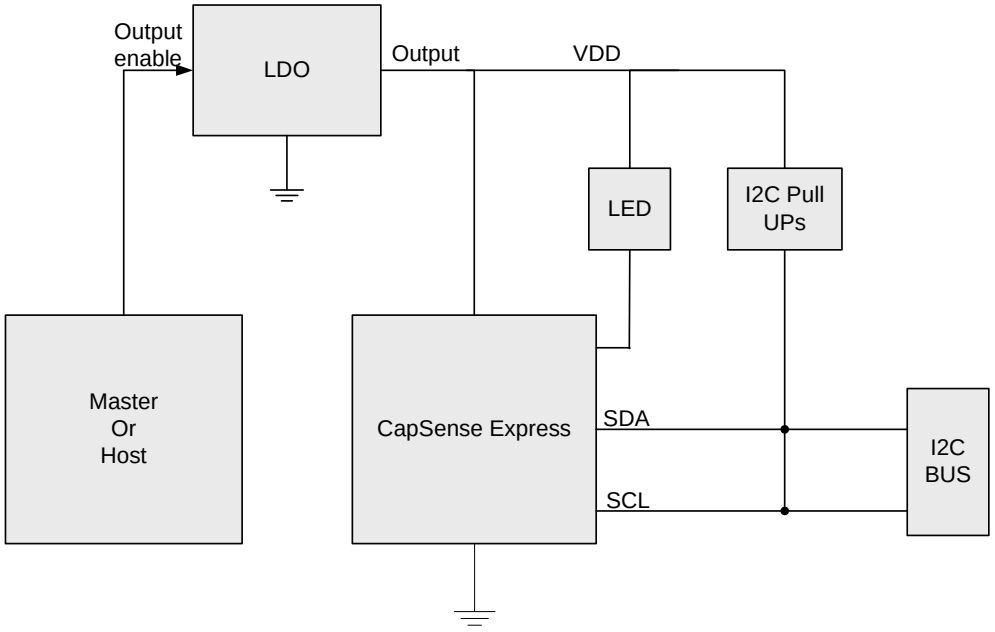


4.4 Circuit-4: Compatibility with 1.8V I²C Signaling[2]



Note
2. 1.8V ≤ VDD_I2C ≤ VDD_CE and 2.4V ≤ VDD_CE ≤ 5.25V.

4.5 Circuit-5: Powering Down CapSense Express Device for Low Power Requirements



For low power requirements, if Vdd is to be turned off, the above concept can be used. The Vdds of CapSense Express, I^2C pull ups, and LEDs must be from the same source. Turning off the Vdd ensures that no signal is applied to the device while it is unpowered. The I^2C signals should not be driven high by the master in this situation. If a port pin or group of port pins can cater to the power supply requirement of the circuit, the LDO can be avoided.

5. Operating Modes

5.1 Normal Mode

In normal mode of operation, the acknowledgment time is optimized. The timings remain approximately the same for different configurations of the slave. To reduce the acknowledgment times in normal mode, the registers 0x07, 0x08, 0x11, 0x50, 0x51, 0x5C, 0x5D are given only read access. Writing to these registers can be done only in setup mode.

5.2 Setup Mode

All registers have read and write access (except those which are read only) in this mode. The acknowledgment times are longer compared to normal mode. When CapSense scanning is disabled (command code 0x0A in command register 0xA0), the acknowledgment times can be improved to values similar to the normal mode of operation.

6. I^2C Interface

The CapSense Express devices support the industry standard I^2C protocol, which can be used to:

- Configure the device
- Read the status and data registers of the device
- Control device operation
- Execute commands

The I^2C address can be modified during configuration.

6.1 I^2C Device Addressing

The device uses a seven bit addressing protocol. The I^2C data transfer is always initiated by the master sending one byte address; first 7-bit contains address and LSb indicates the data transfer direction. Zero in the LSb indicates the write transaction form master and one indicates read transfer by the master. Table 3 shows example for different I^2C addresses.

Table 3. I^2C Addresses

7 Bit Slave Address (in Dec)	D7	D6	D5	D4	D3	D2	D1	D0	8 Bit Slave Address (in Hex)
1	0	0	0	0	0	0	1	0(W)	02
1	0	0	0	0	0	0	1	1(R)	03
75	1	0	0	1	0	1	1	0(W)	96
75	1	0	0	1	0	1	1	1(W)	97

6.2 I²C Clock Stretching

"Clock stretching" or "bus stalling" in I²C communication protocol is a state in which the slave holds the SCL line low to indicate that it is busy. In this condition, the master is expected to wait until the SCL is released by the slave.

When an I²C master communicates with the CapSense Express device, the CapSense Express stalls the I²C bus after the reception of each byte (that is, just before the ACK/NAK bit) until processing of the byte is complete and critical internal functions are executed. Use a fully I²C compliant master to communicate with the CapSense Express device.

An I²C master which does not support clock stretching (a bit banged software I²C Master) must wait for a specific amount of time specified (as shown in the section Format for Register Write and Read) for each register write and read operation before the next bit is transmitted. It is mandatory to check the SCL status (it should be high) before I²C master initiates any data transfer with CapSense Express. If the master fails to do so and continues to communicate, the communication is erroneous.

The following diagrams represent the ACK time delays shown in the Register Map on page 7.

Figure 3. Write ACK Time Representation

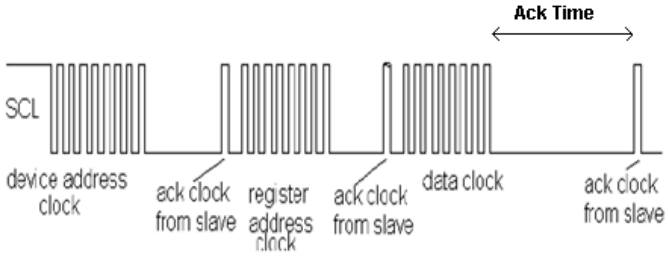
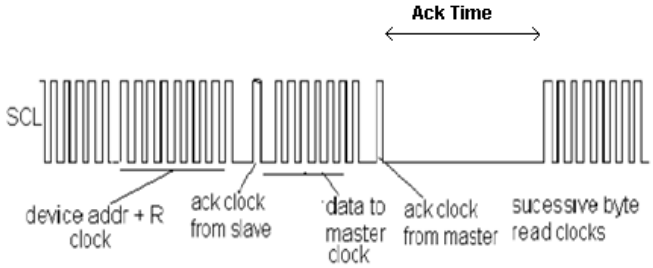


Figure 4. Read ACK Time Representation



6.3 Format for Register Write and Read

Register write format.

Start	Slave Addr + W	A	Reg Addr	A	Data	A	Data	A	. . . . .	Data	A	Stop

Register read format.

Start	Slave Addr + W	A	Reg Addr	A	Stop						
Start	Slave Addr + R	A	Data	A	Data	A	. . . . .	Data	N	Stop	

Legends:

Master	A - ACK
Slave	N- NAK

7. Registers

Table 4. Register Conventions

Convention	Description
RW	Register have both read and write access
R	Register have only read access
WPR	Write register with pass code
FD	Factory defaults

Table 5. Register Map

Name	Register Address (in Hex)	Access	Writable Only in Setup Mode[3]	Factory Default Values of Registers (in Hex)		I²C Max ACK Time in Normal Mode (ms)[5]	I²C Max ACK Time in Setup Mode (ms)[5]	Page No.
				1 Button	2 Button			
OUTPUT_PORT	04	W		01	03	0.10		9
CS_ENABLE	07	RW	Yes	01	03		11	9
DIG_ENABLE	08	RW	Yes	01	03		11	10
SET_STRONG_DM	11	RW	Yes	01	03		11	10
OP_SEL_0	1C	RW		82	82	0.12	11	12
LOGICAL_OPR_INPUT0	1E	RW		01	01	0.12	11	12
OP_SEL_1[4]	21	RW			82	0.12	11	12
LOGICAL_OPR_INPUT1[4]	23	RW			02	0.12	11	12
CS_NOISE_TH	4E	RW		28	28	0.11	11	13
CS_BL_UPD_TH	4F	RW		64	64	0.11	11	13
CS_SETL_TIME	50	RW	Yes	A0	A0		35	13
CS_OTH_SET	51	RW	Yes	00	00		35	14
CS_HYSTERISIS	52	RW		0A	0A	0.11	11	14
CS_DEBOUNCE	53	RW		03	03	0.11	11	15
CS_NEG_NOISE_TH	54	RW		14	14	0.11	11	15
CS_LOW_BL_RST	55	RW		14	14	0.11	11	15
CS_FILTERING	56	RW		20	20	0.11	11	16
CS_SCAN_POS_0	5C	RW	Yes	00	00		11	16
CS_SCAN_POS_1[4]	5D	RW	Yes		01		11	16
CS_FINGER_TH_0	66	RW		64	64	0.14	11	17
CS_FINGER_TH_1[4]	67	RW			64	0.14	11	17
CS_IDAC_0	70	RW		0A	0A	0.14	11	17
CS_IDAC_1[4]	71	RW			0A	0.14	11	17
I2C_ADDR_LOCK	79	RW		00	00	0.11	11	17
DEVICE_ID	7A	R		11	21	0.11	11	18
DEVICE_STATUS	7B	R		03	03	0.11	11	18
I2C_ADDR_DM	7C	RW		00	00	0.11	11	19
CS_READ_BUTTON	81	RW		00	00	0.12	11	19
CS_READ_BLM	82	R		00	00	0.12	11	20
CS_READ_BLL	83	R		00	00	0.12	11	20
CS_READ_DIFFM	84	R		00	00	0.12	11	20
CS_READ_DIFFL	85	R		00	00	0.12	11	20
CS_READ_RAWM	86	R		00	00	0.12	11	20
CS_READ_RAWL	87	R		00	00	0.12	11	20
CS_READ_STATUS	88	R		00	00	0.12	11	21
COMMAND_REG	A0	W		00	00	0.10	11	21

Notes
3. These registers are writable only after entering into setup mode. All other registers are available for read and write in normal and setup mode.
4. These registers are available only in CY8C20121 device.
5. The Ack times specified are 1x I2C Ack times.

Table 6. CapSense Express Commands

Command [5]	Description	Executable Mode	Duration the Device is NOT Accessible after ACK (in ms)[5]
W 00 A0 00	Get firmware revision	Setup/Normal	0
W 00 A0 01	Store current configuration to NVM	Setup/Normal	120
W 00 A0 02	Restore factory configuration	Setup/Normal	120
W 00 A0 03	Write NVM POR defaults	Setup/Normal	120
W 00 A0 04	Read NVM POR defaults	Setup/Normal	5
W 00 A0 05	Read current configurations (RAM)	Setup/Normal	5
W 00 A0 06	Reconfigure device (POR)	Setup	5
W 00 A0 07	Set Normal mode of operation	Setup/Normal	0
W 00 A0 08	Set Setup mode of operation	Setup/Normal	0
W 00 A0 09	Start scan	Setup/Normal	10
W 00 A0 0A	Stop scan	Setup/Normal	5
W 00 A0 0B	Get CapSense scan status	Setup/Normal	0

Note
6. 'W' indicates the write transfer. The next byte of data represents the 7 bit I^2C address.

7.1 OUTPUT_PORT

Output Port Register

OUTPUT_PORT: 04h

1 Button	7	6	5	4	3	2	1	0
Access: FD								W:01
Bit Name								DIG[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							W:03	
Bit Name							DIG[1:0]	

This register is used to write data to DIG output port. Pins defined as output of combinational logic (in OP_SEL_x register) cannot be changed using this register.

Bit	Name	Description
1:0	DIG [1:0]	A bit set in this register sets the logic level of the output. 0 Logic ‘0’ 1 Logic ‘1’

7.2 CS_ENABLE

Select CapSense Input Register

CS_ENABLE: 07h

(Writable only in Setup mode)

1 Button	7	6	5	4	3	2	1	0
Access: FD								RW:01
Bit Name								CS[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:03	
Bit Name							CS[1:0]	

This register is used to enable CapSense inputs. **This register should be set before setting finger threshold (0x66, 0x67) and IDAC setting (0x70, 0x71) registers.**

Bit	Name	Description
1:0	CS [1:0]	These bits are used to enable CapSense inputs. 0 Disable CapSense input 1 Enable CapSense input

7.3 DIG_ENABLE

Select DIG Output Register

GPO_ENABLE: 08h

(Writable only in Setup mode)

1 Button	7	6	5	4	3	2	1	0
Access: FD								RW:01
Bit Name								DIG[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:03	
Bit Name							DIG [1:0]	

This register is used to enable DIG (Digital) outputs. If DIG output is enabled, the strong drive mode register (11h) should also be set. If DIG output is disabled the drive mode of these pins is High Z.

Bit	Name	Description
1:0	DIG [1:0]	These bits are used to enable DIG outputs. 0 Disable DIG output 1 Enable DIG output

7.4 SET_STRONG_DM

Sets Strong Drive Mode for DIG Outputs.

SET_STRONG_DM: 11h

(Writable only in Setup mode)

1 Button	7	6	5	4	3	2	1	0
Access: FD								RW:01
Bit Name								DM [0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:03	
Bit Name							DM [1:0]	

This register sets strong drive mode for DIG (Digital) outputs. To set strong drive mode the pin should be enabled as GP output.

Bit	Name	Description
1:0	DM [1:0]	These bits are used to set the strong drive mode to DIG outputs. 0 Strong drive mode not set 1 Strong drive mode set

Figure 5. CY8C20111 Digital Logic Diagram

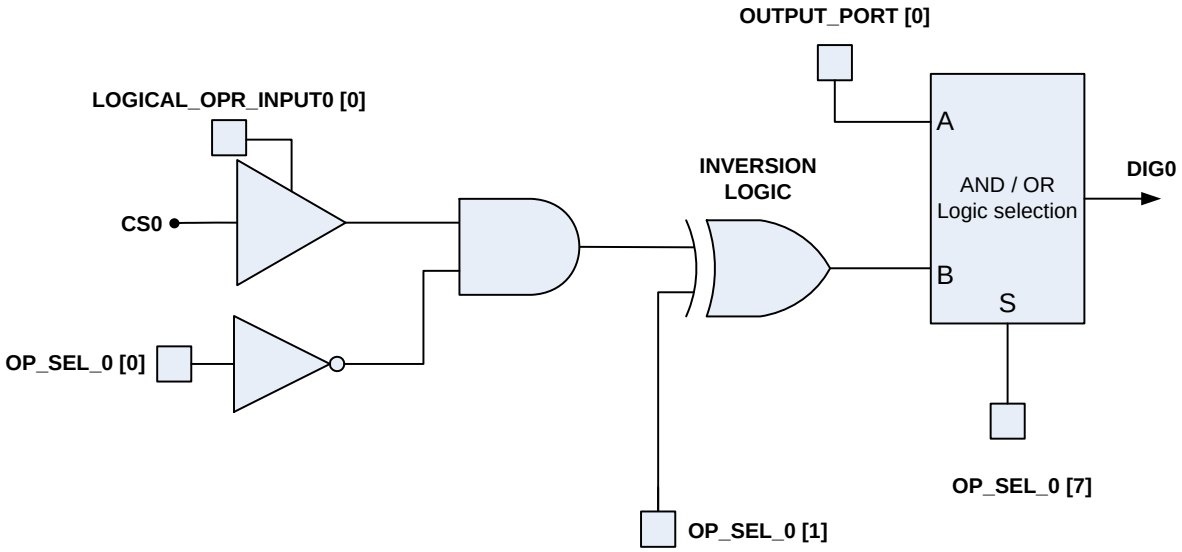
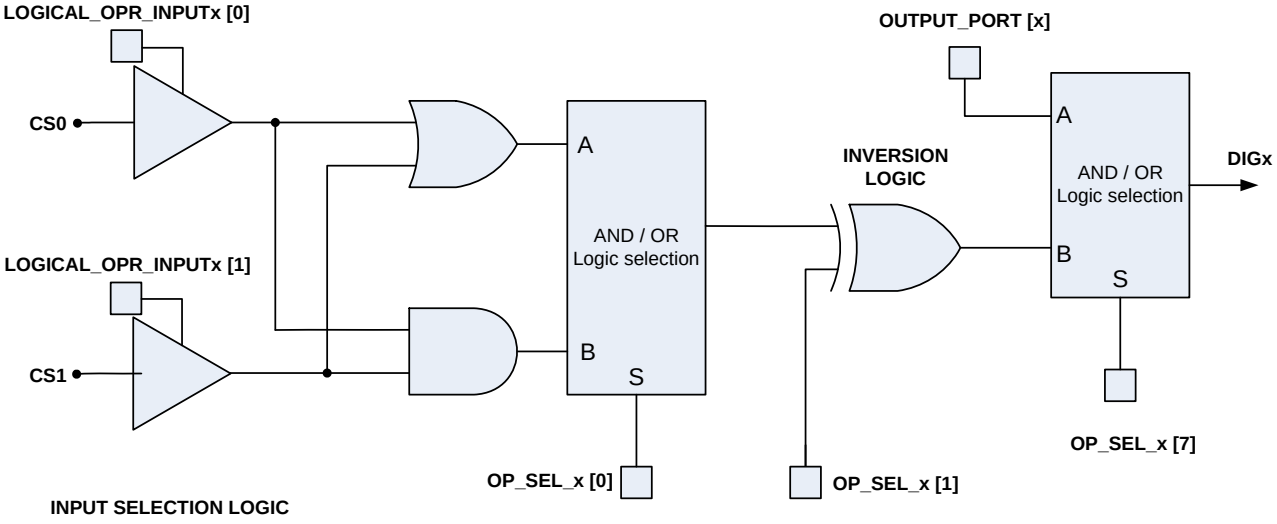


Figure 6. CY8C20121 Digital Logic Diagram



7.5 OP_SEL_x

Logic Operation Selection Registers

OP_SEL_0: 1Ch OP_SEL_1: 21h (Not available for 1 Button)

1/2Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0						RW: 0	RW: 0
Bit Name	Op_En						InvOp	Operator

This register is used to enable logic operation on GP outputs. OP_SEL_0 should be configured to get the logic operation output on DIG0 output and OP_SEL_1 for DIG1 output. Write to these registers during the disable state of respective DIG output pins does not have any effect.

The input to the logic operation can be selected in LOGIC_OPRX registers. The selected inputs can be ORed or ANDed. The output of logic operation can also be inverted.

Bit	Name	Description
7	Op_En	This bit enables or disables logic operation. 0 Disable logic operation 1 Enable logic operation
1	InvOp	This bit enables or disables logic operation output inversion. 0 Logic operation output not inverted 1 Logic operation output inverted
0	Operator	This bit selects which operator should be used to compute logic operation. 0 Logic operator OR is used on inputs 1 Logic operator AND is used on inputs

7.6 LOGICAL_OPR_INPUTx

Selects Input for Logic Operation

LOGICAL_OPR_INPUT0: 1Eh LOGICAL_OPR_INPUT1: 23h (Not available for 1 button)

LOGICAL_OPR_INPUT0

1 Button	7	6	5	4	3	2	1	0
Access: FD								RW:01
Bit Name								CSL[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:01	
Bit Name							CSL [1:0]	

LOGICAL_OPR_INPUT1

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:02	
Bit Name							CSL [1:0]	

These registers are used to give the input to logic operation block. The inputs can be only CapSense input status.

Bit	Name	Description
1:0	CSL [1:0]	These bits selects the input for logic operation block.

7.7 CS_NOISE_TH

Noise Threshold Register

CS_NOISE_TH: 4Eh

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:28							
Bit Name	NT[7:0]							

This register sets the noise threshold value. For individual sensors, count values above this threshold do not update the baseline. This count is relative to baseline. This parameter is common for all sensors.

The range is 3 to 255 and it should satisfy the equation NT < Min (Finger Threshold – Hysteresis – 5). Recommended value is 40% of finger threshold.

Bit	Name	Description
7:0	NT [7:0]	These bits are used to set the noise threshold value.

7.8 CS_BL_UPD_TH

Baseline Update Threshold Register

CS_BL_UPD_TH: 4Fh

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:64							
Bit Name	BLUT[7:0]							

When the new raw count value is above the current baseline and the difference is below the noise threshold, the difference between the current baseline and the raw count is accumulated into a “bucket.” When the bucket fills, the baseline increments and the bucket is emptied. This parameter sets the threshold that the bucket must reach for the baseline to increment. In other words, lower value provides faster baseline update rate and vice versa. This parameter is common for all sensors.

The range is 0 to 255.

Bit	Name	Description
7:0	BLUT [7:0]	These bits set the threshold that the bucket must reach for baseline to increment.

7.9 CS_SETL_TIME

Settling Time Register

CS_SETL_TIME: 50h

(Writable only in Setup mode)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:A0							
Bit Name	STLNG_TM[7:0]							

The settling time parameter controls the duration of the capacitance-to-voltage conversion phase. The parameter setting controls a software delay that allows the voltage on the integrating capacitor to stabilize. This parameter is common for all sensors.

This register should be set before setting finger threshold (0x66, 0x67) and IDAC setting (0x70, 0x71) registers.

The range is 2 to 255.

Bit	Name	Description
7:0	STLNG_TM [7:0]	These bits are used to set the settling time value.

7.10 CS_OTH_SET

CapSense Clock Select, Sensor Auto Reset Register

CS_OTH_SET: 51h

(Writable only in Setup mode)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD		RW: 00			RW: 0			
Bit Name		CS_CLK[1:0]			Sns_Ar			

The registers set the CapSense module frequency of operation and enables or disables the sensor auto reset.

CS_CLK bits provides option to select variable clock input for the CapSense block. A sensor design having higher paratactic requires lower clock for better performance and vice versa.

Sensor Auto Reset determines whether the baseline is updated at all times or only when the signal difference is below the noise threshold. When set to '1' (enabled), the baseline is updated constantly. This setting limits the maximum time duration of the sensor, but it prevents the sensors from permanently turning on when the raw count suddenly rises without anything touching the sensor. This sudden rise can be caused by a large power supply voltage fluctuation, a high energy RF noise source, or a very quick temperature change. When the parameter is set to '0' (disabled), the baseline is updated only when raw count and baseline difference is below the noise threshold parameter. This parameter may be enabled unless there is a demand to keep the sensors in the on state for a long time. This parameter is common for all sensors.

Bit	Name	Description
6:5	CS_CLK[1:0]	These bits selects the CapSense clock.

CS_CLK[1:0]	Frequency of Operation
00	IMO
01	IMO/2
10	IMO/4
11	IMO/8

3	Sns_Ar	This bit is used to enable or disable sensor auto reset. 0 Disable Sensor auto reset 1 Enable Sensor auto reset

7.11 CS_HYSTERISIS

Hysteresis Register

CS_HYSTERISIS: 52h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:0A							
Bit Name	HYS[7:0]							

The Hysteresis parameter adds to or subtracts from the finger threshold depending on whether the sensor is currently active or inactive. If the sensor is off, the difference count must overcome the 'finger threshold + hysteresis'. If the sensor is on, the difference count must go below the 'finger threshold – hysteresis'. It is used to add debouncing and "stickiness" to the finger detection algorithm. This parameter is common for all sensors.

Possible values are 0 to 255. However, the setting must be lower than the finger threshold parameter setting. Recommended value for hysteresis is 15 percent of finger threshold.

Bit	Name	Description
7:0	HYS [7:0]	These bits are used to set the hysteresis value.

7.12 CS_DEBOUNCE

Debounce Register.

CS_DEBOUNCE: 53h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:0A							
Bit Name	DB[7:0]							

The Debounce parameter adds a debounce counter to the 'sensor active transition'. For the sensor to transition from inactive to active, the consecutive samples of difference count value must stay above the 'finger threshold + hysteresis' for the number specified. This parameter is common for all sensors.

Possible values are 1 to 255. A setting of '1' provides no debouncing.

Bit	Name	Description
7:0	DB [7:0]	These bits are used to set the debounce value.

7.13 CS_NEG_NOISE_TH

Negative Noise Threshold Register

CS_NEG_NOISE_TH: 54h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:0A							
Bit Name	NNT[7:0]							

This parameter adds a negative difference count threshold. If the current raw count is below the baseline and the difference between them is greater than this threshold, the baseline is not updated. However, if the current raw count stays in the low state (difference greater than the threshold) for the number of samples specified by the Low Baseline Reset parameter, the baseline is reset. This parameter is common for all sensors.

Bit	Name	Description
7:0	NNT [7:0]	These bits are used to set the negative noise value.

7.14 CS_LOW_BL_RST

Low Baseline Reset Register

CS_LOW_BL_RST: 55h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:0A							
Bit Name	LBR[7:0]							

This parameter works together with the Negative Noise Threshold parameter. If the sample count values are below the baseline minus the negative noise threshold for the specified number of samples, the baseline is set to the new raw count value. It essentially counts the number of abnormally low samples required to reset the baseline. It is generally used to correct the finger-on-at-startup condition. This parameter is common for all sensors.

Bit	Name	Description
7:0	LBR [7:0]	These bits are used to set the Low Baseline Reset value.

7.15 CS_FILTERING

CapSense Filtering Register

CS_FILTERING: 56h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0		RW: 1	RW: 0			RW: 00	
Bit Name	RstBl		I2C_DS	Avg_En			Avg_Order[1:0]	

This register provides an option for forced baseline reset and to enable and configure two different types of software filters.

Bit	Name	Description
7	RstBl	This bit resets all the baselines and it is auto cleared to '0'. 0 All Baselines are not reset 1 All baselines are reset
5	I2C_DS	When this bit is set to '1' the CapSense scan sample is dropped if I^2C communication was active during scanning. 0 Disable the I^2C drop sample filer 1 Enable the I^2C drop sample filter
4	Avg_En	This bit enables average filter on raw counts. 0 Disable the average filter 1 Enable the average filter
[1:0]	Avg_Order[1:0]	These bits are used to select the number of CapSense samples to average:

Avg_Order[1:0] in Hex	Samples to Average
00	2
01	4
10	8
11	16

7.16 CS_SCAN_POS_x

Scan Position Registers

CS_SCAN_POS_0: 5Ch

(Writable only in Setup mode)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD								RW: 0
Bit Name								Scan_Pstn

CS_SCAN_POS_1: 5Dh (Not available for 1 Button)

(Writable only in Setup mode)

2 Button	7	6	5	4	3	2	1	0
Access: FD								RW: 1
Bit Name								Scan_Pstn

This register is used to set the position of the sensors in the switch table for proper scanning sequence because the CapSense sensors are scanned in sequence.

This register should be set after setting 0x07, 0x50, and 0x51 registers.

Bit	Name	Description
0	Scan_Pstn	This bit sets the scan position.

7.17 CS_FINGER_TH_x

Finger Threshold Registers

CS_FINGER_TH_0: 66h CS_FINGER_TH_1: 67h (Not available in 1 Button)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 64							
Bit Name	FT[7:0]							

This register sets the finger threshold value for CapSense inputs. Possible values are 3 to 255. This parameter should be configured individually for each CapSense inputs.

This register should be set after setting 0x07, 0x50, and 0x51 registers.

Bit	Name	Description
[7:0]	FT [7:0]	These bit set the finger threshold for CapSense inputs.

7.18 CS_IDAC_x

IDAC Setting Registers

CS_IDAC_0: 70h CS_IDAC_1: 71h (Not available in 1 Button)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0A							
Bit Name	IDAC[7:0]							

The IDAC register controls the sensitivity of the CapSense algorithm. This register is used to tune the CapSense input for specific design or overlays. Decreasing the value of this register increases the sensitivity of the CapSense buttons and vice versa. Decreasing the value of IDAC increases noise and vice versa.

Possible values are 1 to 255. If the value is set to 0 then the value is reset to default value 10.

The recommended value is greater than 4. Setting value $\leq$ 4 creates excessive amount of noise.

This register should be set after setting 0x07, 0x50, and 0x51 registers.

Bit	Name	Description
[7:0]	IDAC [7:0]	These bit set the IDAC values.

7.19 I2C_ADDR_LOCK

I2C Address Lock Registers

I2C_ADDR_LOCK: 79h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD								WPR: 0
Bit Name								I2CAL

This register is used to unlock and lock the I^2C address register (7Ch) access. The device I^2C address should be modified by writing new address to register 7Ch after unlocking the access using this register. Write to the 7C register during the locked state does not have any effect and the new address take effect only after the access is locked.

To lock or unlock the I^2C AL bit, the following three bytes must be written to register 79h:

- unlock I2CAL: 3Ch A5h 69h
- lock I2CAL: 96h 5Ah C3h

Reading the I2CAL bit from register 79h indicates the current access state.

Bit	Name	Description
0	I2CAL	This bit gives the lock/unlock status of I^2C address. 0 Unlocked 1 Locked

7.20 DEVICE_ID

Device ID Register

DEVICE_ID: 7Ah

1 Button	7	6	5	4	3	2	1	0
Access: FD	R: 11							
Bit Name	DEV_ID[7:0]							

2 Button	7	6	5	4	3	2	1	0
Access: FD	R: 21							
Bit Name	DEV_ID[7:0]							

This register contains the device and product ID. The device and product ID corresponds to “xx” in CY8C201xx.

Bit	Name	Description
7:0	DEV_ID [7:0]	These bits contain the device and product ID.

Part No	Device/Product ID
CY8C20111	11
CY8C20121	21

7.21 DEVICE_STATUS

Device Status Register

DEVICE_STATUS: 7Bh

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	R : 00		R: 0	R : 0	R: 0		R: 0	R: 0
Bit Name	Ip_Volt[1:0]		IRES	Load_FD	No_NVM_Wr		CSE	DIGE

This register contains the device status.

Bit	Name	Description
7:6	Ip_Volt [1:0]	Supply voltage is automatically detected and these bits are set accordingly.

Ip_Volt[1:0]	Supply Voltage
00	5
01	3.3
10	2.7
11	Reserved

5	IRES	When set to ‘1’, this bit indicates that an internal reset occurred. 0 indicates the last system reset was not internal reset 1 indicates the last system reset was internal reset
4	Load_FD	This bit indicates whether factory defaults are loaded during power up. 0 User default configuration is loaded during power up 1 Factory default configuration is loaded during power up
3	No_NVM_Wr	When set to ‘1’, this bit indicates that the supply voltage applied to the device Is too low for a write to nonvolatile memory operation, and no write is performed. This bit must be checked before any Store or Write POR command.
1	CSE	This bit indicates whether CapSense function is enabled or disabled. 0 Functionality of CapSense block is disabled 1 Functionality of CapSense block is enabled
0	DIGE	This bit indicates whether GP Output function is enabled or disabled. 0 Functionality of Digital output block is disabled 1 Functionality of Digital output block is enabled

7.22 I2C_ADDR_DM

Device I²C Address and I²C Pin Drive Mode Register

I2C_ADDR_DM: 7Ch

1 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0	RW: 00						
Bit Name	I2CIP_EN	I2C_ADDR[6:0]						

This register sets the drive mode of I²C pins and I²C slave address. To write to this register, register 79h must first be unlocked. The value written to register 7Ch is applied only after locking register 79h again.

Bit	Name	Description
7	I2CIP_EN	This bit is used to set the I²C pins drive mode. 0 Internal pull up enabled 1 Internal pull up disabled
6:0	I2C_ADDR [6:0]	Used to set the device I²C address.

7.23 CS_READ_BUTTON

Button Select Register

I2C_ADDR_DM: 81h

1 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0							RW: 0
Bit Name	RD_EN							CSBN[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0						RW: 00	
Bit Name	RD_EN						CSBN[1:0]	

The scan result of a CapSense input (raw count, difference count, and baseline) can be read only for one input at a time using 82h-87h registers. This register is used to select a CapSense input to read the raw count, difference count, and baseline. Only the pins defined as CapSense inputs in register 07h can be used with this register. Trying to select other pins not defined as CapSense does not have any change.

Bit	Name	Description
7	RD_EN	This bit enables the CapSense raw data reading. 0 Disable CapSense scan result reading 1 Enable CapSense scan result reading
1:0	CSBN [1:0]	These bits decide which CapSense button scan result are read. When writing to this register, the bitmask must contain only one bit set to '1', otherwise the data is discarded.

CSBN [1:0]	CapSense Button No
01	1
10	2

7.24 CS_READ_BLx

Baseline Value MSB/LSB Registers

CS_READ_BLM: 82h CS_READ_BLL: 83h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	R: 00							
Bit Name	BL [7:0]							

Reading from this register returns the 2-byte current baseline value for the selected CapSense input.

Bit	Name	Description
7:0	BL [7:0]	These bits represent the baseline value.

7.25 CS_READ_DIFFx

Difference Count Value MSB/LSB Registers

CS_READ_DIFFM: 82h CS_READ_DIFFL: 83h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	R: 00							
Bit Name	DIF [7:0]							

Reading from this register returns the 2-byte current difference count for the selected CapSense input.

Bit	Name	Description
7:0	DIF [7:0]	These bits represent the sensor difference count.

7.26 CS_READ_RAWx

Difference Count Value MSB/LSB Registers

CS_READ_RAWM: 82h CS_READ_RAWL: 83h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	R: 00							
Bit Name	RC [7:0]							

Reading from this register returns the 2-byte current raw count value for the selected CapSense input.

Bit	Name	Description
7:0	RC [7:0]	These bits represent the raw count value.

7.27 CS_READ_STATUS

Sensor On Status Register

CS_READ_STATUS: 88h

1 Button	7	6	5	4	3	2	1	0
Access: FD								R: 0
Bit Name								BT_ST[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							R: 00	
Bit Name							BT_ST[1:0]	

This register gives the sensor ON/OFF status. A bit '1' indicates sensor is ON and '0' indicates sensor is OFF.

Bit	Name	Description
1:0	BT_ST [1:0]	These bits used to represent sensor status. 0 Sensor OFF 1 Sensor ON

7.28 COMMAND_REG

Command Register

COMMAND_REG: A0h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	W: 00							
Bit Name	Cmnd [7:0]							

Commands are executed by writing the command code to the command register.

Bit	Name	Description
7:0	Cmnd [7:0]	Refer to the following table for command register opcodes.

Command Code	Name	Description
00h	Get Firmware Revision	The I^2C buffer is loaded with the one byte firmware revision value. Reading one byte after writing this command returns the firmware revision. The upper nibble of the firmware revision byte is the major revision number and the lower nibble is the minor revision number.
01h	Store Current Configuration to NVM	The current register settings are saved in nonvolatile memory (Flash). This setting is automatically loaded after the next device reset/power up or if the Reconfigure Device (06h) command is issued.
02h	Restore Factory Configuration	Replaces the saved user configuration with the factory default configuration. Current settings are unaffected by this command. New settings are loaded after the next device reset/power up or if the 06h command is issued.
03h	Write POR Defaults	Sends new power up defaults to the CapSense controller without changing current settings unless the 06h command is issued afterwards. This command is followed by 123 data bytes according to the POR Default Data Structure table. The CRC is calculated as the XOR of the 122 data bytes (00h-79h). If the CRC check fails or an incomplete block is sent, the slave responds with an ACK and the data is NOT saved to Flash. To define new POR defaults: ■ Write command 03h ■ Write 122 data bytes with new values of registers (use the _flash.iic file generated from s/w tool) ■ Write one CRC byte calculated as XOR of previous 122 data bytes

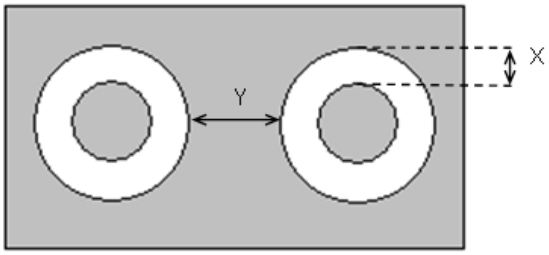
Command Code	Name	Description
04h	Read POR Defaults	Reads the POR settings stored in the nonvolatile memory. To read POR defaults: ■ Write command 04h ■ Read 122 data bytes ■ Read one CRC byte
05h	Read Device Configuration (RAM)	Reads the current device configuration. Gives the user "flat-address-space" access to all device settings. To read device configuration: ■ Write command 05h ■ Read 122 data bytes ■ Read one CRC byte
06h	Reconfigure Device (POR)	Immediately reconfigures the device with actual POR defaults from Flash. Has the same effect on the registers as a POR. This command can only be executed in setup operation mode (command code 08).
07h	Set Normal Operation Mode	Sets the device in normal operation mode. In this mode, CapSense pin assignments cannot be modified; settling time, IDAC setting, external capacitor, and sensor auto-reset also cannot be modified.
08h	Set Setup Operation Mode	Sets the device in setup operation mode. In this mode, CapSense pin assignments can be changed along with other parameters.
09h	Start CapSense Scanning	Allows the user to start CSA scanning after it has been stopped using command 0x0A. Note that at POR, scanning is enabled and started by default if one or more sensors are enabled.
0Ah	Stop CapSense Scanning	Allows the user to stop CSA scanning. A system host controller might initiate this command before powering down the device to make sure that during power down no CapSense touches are detected. When CSA scanning is stopped by the user and the device is still in the valid VCC operating range, the following behavior is supported: ■ Any change to configuration can still be done (as long as VCC is in operating range). ■ Command code 0x06 overrides the status of stop/scan by enabling and starting CSA scanning if one or more sensors are enabled. ■ CapSense read-back values return 0x00.
0Bh	Returns CapSense Scanning Status	The I^2C buffer is loaded with the one-byte CSA scanning status value. After writing the value 0Bh to the A0h register, reading one byte returns the CSA scanning status. It returns the LVD_STOP_SCAN and STOP_SCAN bits. LVD_STOP_SCAN is bit 3 - Set when CSA is stopped because VCC is outside the valid operating range. STOP_SCAN is bit 2 - Set when CSA is stopped by the user by writing command 0x0A.

8. Layout Guidelines and Best Practices

Sl. No.	Category	Min	Max	Recommendations/Remarks
1	Button Shape			Solid round pattern, round with LED hole, rectangle with round corners
2	Button Size	5 mm	15 mm	10 mm
3	Button Button Spacing	= Button Ground Clearance		8 mm
4	Button Ground Clearance	0.5 mm	2 mm	Button ground clearance = Overlay Thickness
5	Ground Flood - Top Layer			Hatched ground 7 mil trace and 45 mil grid (15% filling)
6	Ground Flood - Bottom Layer			Hatched ground 7 mil trace and 70 mil grid (10% filling)
7	Trace Length from Sensor to PSoC - Buttons		200 mm	< 100 mm.
8	Trace Width	0.17 mm	0.20 mm	0.17 mm (7 mil)
9	Trace Routing			Traces should be routed on the non sensor side. If any non CapSense trace crosses CapSense trace, ensure that inter-section is orthogonal.
10	Via Position for the Sensors			Via should be placed near the edge of the button/slider to reduce trace length thereby increasing sensitivity.
11	Via Hole Size for Sensor Traces			10 mil
12	No. of Via on Sensor Trace	1	2	1
13	CapSense Series Resistor Placement		10mm	Place CapSense series resistors close to PSoC for noise suppression.CapSense resistors have highest priority place them first.
14	Distance between any CapSense Trace to Ground Flood	10 mil	20 mil	20 mil
15	Device Placement			Mount the device on the layer opposite to sensor. The CapSense trace length between the device and sensors should be minimum
16	Placement of Components in 2 Layer PCB			Top layer-sensor pads and bottom layer-PSoC, other compo-nents and traces.
17	Placement of Components in 4 Layer PCB			Top layer-sensor pads, second layer – CapSense traces, third layer-hatched ground, bottom layer- PSoC, other components and non CapSense traces
18	Overlay Thickness - Buttons	0 mm	2 mm	1 mm
19	Overlay Material			Should to be non conductive material. Glass, ABS Plastic, Formica
20	Overlay Adhesives			Adhesive should be non conductive and dielectrically homog-enous. 467MP and 468MP adhesives made by 3M are recommended.
21	LED Back Lighting			Cut a hole in the sensor pad and use rear mountable LEDs. Refer Example PCB Layout Design with Two CapSense Buttons and Two LEDs on page 26.
22	Board Thickness			Standard board thickness for CapSense FR4 based designs is 1.6 mm.

Figure 7. Button Shapes

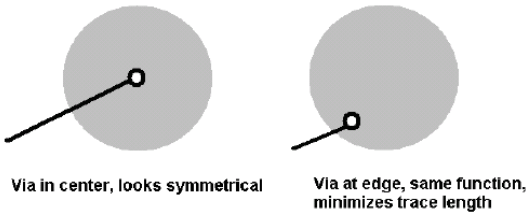
Figure 8. Button Layout Design



X: Button to ground clearance

Y: Button to button clearance

Figure 9. Recommended Via-hole Placement



8.1 Example PCB Layout Design with Two CapSense Buttons and Two LEDs

Figure 10. Top Layer

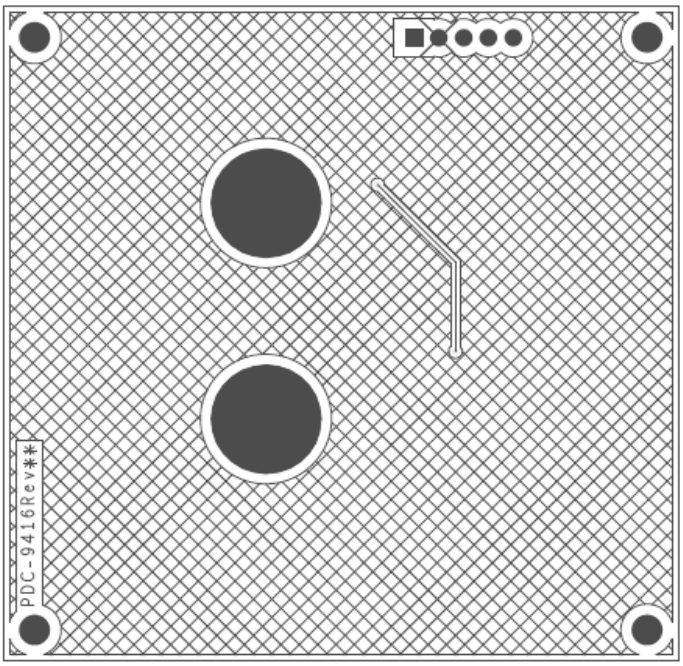
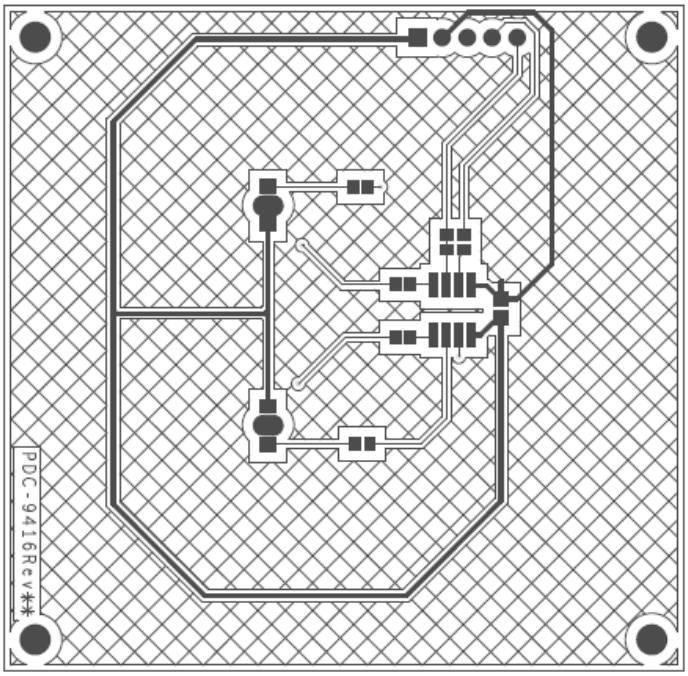
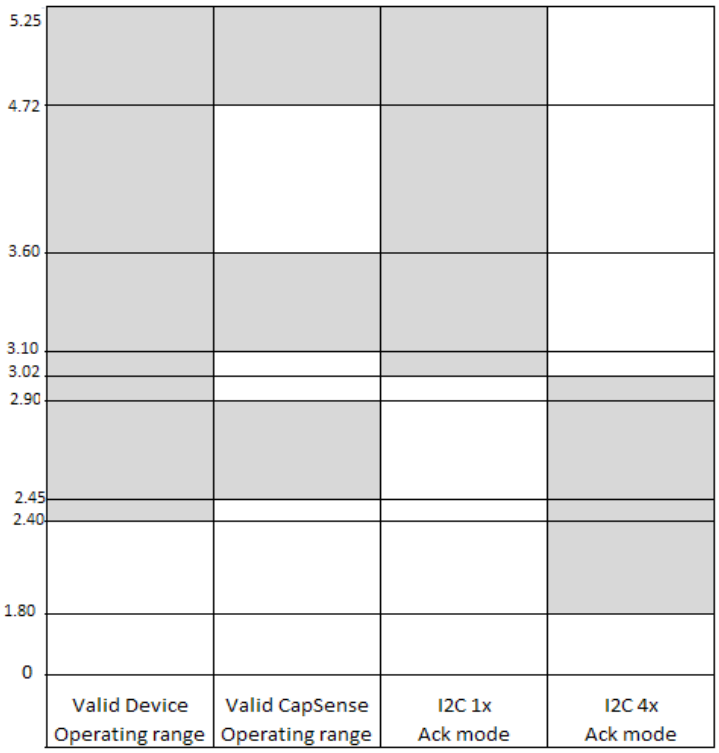


Figure 11. Bottom Layer



9. Operating Voltages



For details on I2C 1x Ack time, refer Register Map on page 7 and CapSense Express Commands on page 8. I2C 4x Ack time is approximately four times the values mentioned in these tables.

10. CapSense Constraints

Parameter	Min	Typ	Max	Units	Notes
Parasitic Capacitance (C_P) of the CapSense Sensor			30	pF	
Overlay Thickness	0	1	2	mm	All layout best practices followed, properly tuned and noise free condition.
Supply Voltage Variation (V_{DD})			± 5%		

11. Electrical Specifications

11.1 Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C (0°C to 50°C). Extended duration storage temperatures above 65°C degrade reliability
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any GPIO pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch up current	–	–	200	mA	

11.2 Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	

11.3 DC Electrical Characteristics

11.3.1 DC Chip Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	
I_{DD}	Supply current	–	1.5	2.5	mA	Conditions are V_{DD} = 3.10V, T_A = 25°C

11.3.2 5V and 3.3V DC General Purpose I/O Specifications

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C≤TA≤85°C, 3.10V to 3.6V -40°C≤TA≤85°C. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage	V_{DD} – 0.2	–	–	V	IOH ≤ 10 µA/pin, VDD ≥ 3.10V
V_{OH2}	High output voltage	V_{DD} – 0.9	–	–	V	IOH = 1 mA/pin, VDD ≥ 3.10V
V_{OL}	Low output voltage	–	–	0.75	V	IOL = 20 mA/pin, VDD > 3.10V, maximum of 40 mA sink current
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C.

11.3.3 2.7 DC General Purpose I/O Specifications

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4V to 2.90V and -40°C<T_A<85°C, respectively. Typical parameters apply to 2.7V at 25°C and are for design guidance only.

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage	V_{DD} – 0.2	–	–	V	IOH ≤ 10 µA/pin
V_{OH2}	High output voltage	V_{DD} – 0.5	–	–	V	IOH = 0.2 mA/pin
V_{OL}	Low output voltage	–	–	0.75	V	IOL = 10 mA/pin, maximum of 20 mA sink current
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C.

11.3.4 2.7V DC Spec for I^2C Line with 1.8V External Pull-Up

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4V to 2.9V and 3.10V to 3.60V, and -40°C≤TA ≤85°C, respectively. Typical parameters apply to 2.7V at 25°C. The I^2C lines drive mode must be set to open drain and pulled up to 1.8V externally.

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OLP}	Low output voltage	–	–	0.4	V	IOL=5 mA/pin, maximum of 10 mA device sink current 2.4≤V_{DD} ≤2.9V and 3.1≤V_{DD} ≤3.6V.
V_{IL}	Input low voltage	–	–	0.75	V	V_{DD} = 2.4 to 2.90V and 3.10V to 3.6V.
V_{IH}	Input high voltage	1.4	–	–	V	V_{DD} = 2.4 to 2.7V.
C_{I2C}	Capacitive load on I^2C pins	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C.
R_{PU}	Pull up resistor	4	5.6	8	kΩ	

11.3.5 DC POR and LVD Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
	V_{DD} Value for PPOR Trip					V_{DD} must be greater than or equal to 2.5V during startup or reset from watchdog.
V_{PPOR0}	V_{DD}= 2.7V	–	2.36	2.40	V	
V_{PPOR1}	V_{DD}= 3.3V, 5V	–	2.60	2.65	V	

11.3.6 DC Flash Write Specifications

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C<TA<85°C, 3.10V to 3.6V and -40°C<TA<85°C or 2.4V to 2.90V and -40°C<TA<85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only. Flash Endurance and Retention specifications are valid only within the range: 25°C±20°C during the Flash Write operation. It is at the user's own risk to operate out of this temperature range. If Flash writing is done out of this temperature range, the endurance and data retention reduces.

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations[6]	2.7	–	–	V	
I_{DDP}	Supply Current for Flash Write Operations	–	5	25	mA	
$Flash_{ENPB}$	Flash Endurance	50,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

11.4 CapSense Electrical Characteristics

Max (V)	Typ (V)	Min (V)	Conditions for Supply Voltage	Result
3.6	3.3	3.1	<2.9	The device automatically reconfigures itself to work in 2.7V mode of operation.
			>2.9 or <3.10	This range is not recommended for CapSense usage.
2.90	2.7	2.45	<2.45V	The scanning for CapSense parameters shuts down until the voltage returns to over 2.45V.
			>3.10	The device automatically reconfigures itself to work in 3.3V mode of operation.
			<2.4V	The device goes into reset.
5.25	5.0	4.75	<4.73V	The scanning for CapSense parameters shuts down until the voltage returns to over 4.73V.

Note
7. Commands involving Flash Writes (0x01, 0x02, 0x03) must be executed only within the same VCC voltage range detected at POR (power on, or command 0x06) and above 2.7V.

11.5 AC Electrical Specifications

11.5.1 5V and 3.3V AC General Purpose I/O Specifications

Parameter	Description	Min	Max	Unit	Notes
TRise	Rise time, strong mode, Cload = 50 pF	15	80	ns	V_{DD} = 3.10V to 3.6V and 4.75V to 5.25V, 10% - 90%
TFall	Fall time, strong mode, Cload = 50 pF	10	50	ns	V_{DD} = 3.10V to 3.6V and 4.75V to 5.25V, 10% - 90%

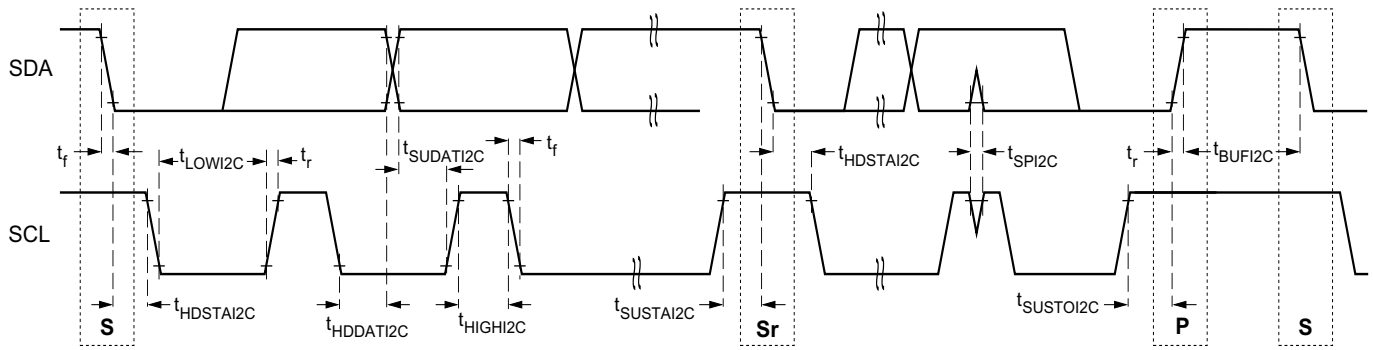
11.5.2 2.7V AC General Purpose I/O Specifications

Parameter	Description	Min	Max	Unit	Notes
TRise	Rise time, strong mode, Cload = 50 pF	15	100	ns	V_{DD} = 2.4V to 2.90V, 10% - 90%
TFall	Fall time, strong mode, Cload = 50 pF	10	70	ns	V_{DD} = 2.4V to 2.90V, 10% - 90%

11.5.3 AC I²C Specifications

Parameter	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
$F_{SCL}I^2C$	SCL clock frequency	0	100	0	400	kbps	Fast mode not supported for V_{DD} < 3.0V
$T_{HDSTA}I^2C$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs	
$T_{LOW}I^2C$	LOW period of the SCL clock	4.7	–	1.3	–	µs	
$T_{HIGH}I^2C$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	
$T_{SUSTA}I^2C$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	
$T_{HDDAT}I^2C$	Data hold time	0	–	0	–	µs	
$T_{SUDAT}I^2C$	Data setup time	250	–	100	–	ns	
$T_{SUSTO}I^2C$	Setup time for STOP condition	4.0	–	0.6	–	µs	
$T_{BUF}I^2C$	BUS free time between a STOP and START condition	4.7	–	1.3	–	µs	
$T_{SP}I^2C$	Pulse width of spikes suppressed by the input filter	–	–	0	50	ns	

Figure 12. Definition of Timing for Fast/Standard Mode on the I²C Bus



12. Examples of Frequently Used I²C Commands

Sl. No.	Requirement	I²C Commands[7]	Comment
1	Enter into setup mode	W 00 A0 08	
2	Enter into normal mode	W 00 A0 07	
3	Load factory defaults to RAM registers	W 00 A0 02	
4	Do a software reset	W 00 A0 08 W 00 A0 06	; Enter into setup mode ; Do software reset
5	Save current configuration to flash	W 00 A0 01	
6	Load factory defaults to RAM registers and save as user configuration	W 00 A0 08 W 00 A0 02 W 00 A0 01 W 00 A0 06	; Enter into setup mode ; Load factory defaults to SRAM ; Save the configuration to Flash. Wait for time specified in Table 6. ; Do software reset
7	Disable combinational logic output to DIG0	W 00 1C 00	
8	Disable combinational logic output to DIG1	W 00 21 00	
9	Clearing (logic 0) the both DIG0 and DIG1 outputs	W 00 04 00	Combinational logic output on DIG0 and DIG1 should be disabled before dong this operation (SL# 7 and 8)
10	Setting (logic 1) the DIG0 and clearing (Logic 0) the DIG1 outputs	W 00 04 01	
11	Clearing (logic 0) the DIG0 and Setting (Logic 1) the DIG1 outputs	W 00 04 02	
12	Setting (logic 1) the both DIG0 and DIG1 outputs	W 00 04 03	
13	Change CapSense clock to IMO/2	W 00 A0 08 W 00 51 20 W 00 A0 07	; Enter into setup mode ; CapSense clock is set as IMO/2 ; Enter into normal mode
14	Change value of IDAC0 to ‘x’h	W 00 70 x	‘x’ represents new value of IDAC register
15	Change value of IDAC1 to ‘y’h	W 00 71 y	‘y’ represents new value of IDAC register
16	Change value of IDAC0 and IDAC1 to ‘x’h and ‘y’h	W 00 70 x y	‘x’ and ‘y’ represents new value of IDAC register
17	Change the value FT0 to ‘x’h	W 00 66 x	‘x’ represents new value of FT register
18	Change the value FT1 to ‘y’h	W 00 67 y	‘y’ represents new value of FT register
19	Change the value FT0 and FT1 to ‘x’h and ‘y’h	W 00 66 x y	‘x’ and ‘y’ represents new value of FT registers
20	Change noise threshold to ‘x’h	W 00 4E x	
21	Read CapSense button CS0 scan results	W 00 81 81 W 00 82 R 00 RD RD RD RD RD RD RD	; Select CapSense button for reading scan result ; Set the read point to 82h ; Consecutive 6 reads gets baseline, difference count and raw count (all two byte each)
22	Read CapSense button status register	W 00 88 R 00 RD	; Set the read pointer to 88 ; Reading a byte gets status CapSense inputs

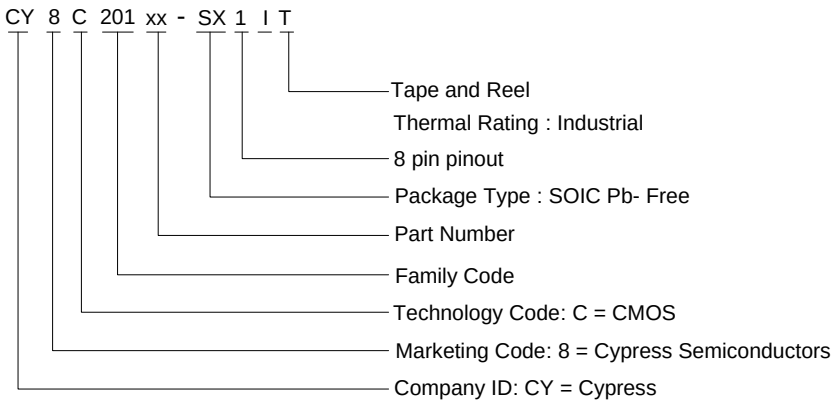
Note
8. The ‘W’ indicates the write transfer and the next byte of data represents the 7-bit I2C address. The I2C address is assumed to be ‘0’ in the above examples. Similarly ‘R’ indicates the read transfer followed by 7-bit address and data byte read operations.

13. Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Temperature	CapSense Blocks	CapSense Inputs	Digital Outputs	XRES Pin
CY8C20111-SX1I	51-85066	8 SOIC	Industrial	Yes	1	1	No
CY8C20111-SX1IT	51-85066	8 SOIC (Tape and Reel)	Industrial	Yes	1	1	No
CY8C20121-SX1I	51-85066	8 SOIC	Industrial	Yes	2	2	No
CY8C20121-SX1IT	51-85066	8 SOIC (Tape and Reel)	Industrial	Yes	2	2	No

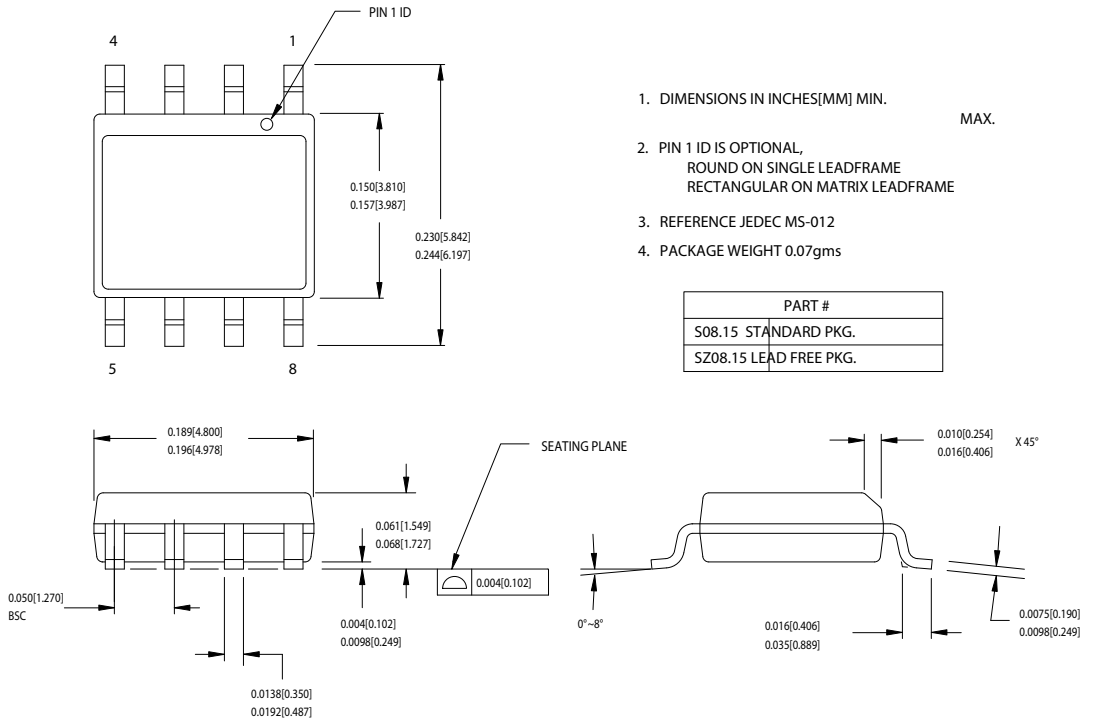
Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

13.1 Ordering Code Information



14. Package Diagram

Figure 13. 8-Pin (150-Mil) SOIC (51-85066)



51-85066-*C

15. Document History Page

Document Title: CY8C20111, CY8C20121 CapSense Express™ - One Button and Two Button Capacitive Controllers Document Number: 001-53516				
Rev.	**ECN.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2709248	SLAN/PYRS	See ECN	New data sheet

16. Sales, Solutions, and Legal Information

16.1 Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

16.2 Products

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