CY8C20110/CY8C20180/CY8C20160 CY8C20140/CY8C20142

CapSense® Express™ Button Capacitive Controllers

Features

- 10/8/6/4 Capacitive Button Input
  - Robust sensing algorithm
  - High sensitivity, low noise
  - Immunity to RF and AC noise
  - Low radiated EMC noise
  - Supports wide range of input capacitance, sensor shapes, and sizes
- Target Applications
  - Printers
  - Cellular handsets
  - LCD monitors
  - Portable DVD players
- Low Operating Current
  - Active current: continuous sensor scan: 1.5 mA
  - Deep sleep current: 4 uA
- Industry's Best Configurability
  - Custom sensor tuning, one optional capacitor
  - Output supports strong drive for LED
  - Output state can be controlled through I^2C or directly from CapSense® input state
  - Run time re-configurable over I^2C
- Advanced Features
  - All GPIOs support LED dimming with configurable delay option in CY8C21110
  - Interrupt outputs
  - User defined Inputs
  - Wake on interrupt input
  - Sleep control pin
  - Nonvolatile storage of custom settings
  - Easy integration into existing products – configure output to match system
  - No external components required
  - World class free configuration tool
- Wide Range of Operating Voltages
  - 2.4V to 2.9V
  - 3.10V to 3.6V
  - 4.75V to 5.25V
- I^2C Communication
  - Supported from 1.8V
  - Internal pull up resistor support option
  - Data rate up to 400 kbps
  - Configurable I^2C addressing
- Industrial temperature range: –40°C to +85°C.
- Available in16-pin COL, 8-pin, and 16-pin SOIC Packages

Overview

These CapSense Express™ controllers support 4 to 10 capacitive sensing (CapSense buttons). The device functionality is configured through an I^2C port and can be stored in onboard nonvolatile memory for automatic loading at power on. The CY8C20110 is optimized for dimming LEDs in 15 selectable duty cycles for back light applications. The device can be configured to have up to 10 GPIOs connected to the PWM output. The PWM duty cycle is programmable for variable LED intensities.

The four key blocks that make up these devices are: a robust capacitive sensing core with high immunity against radiated and conductive noise, control registers with nonvolatile storage, configurable outputs, and I^2C communications. The user can configure registers with parameters needed to adjust the operation and sensitivity of the CapSense buttons and outputs and permanently store the settings. The standard I^2C serial communication interface enables the host to configure the device and read sensor information in real time. The I^2C address is fully configurable without any external hardware strapping.

Pinouts

Figure 1. Pin Diagram - 16 COL- CY8C20110 (10 Buttons)/CY8C20180 (8 Buttons) CY8C20160 (6 Buttons)/CY8C20140 (4 Buttons)

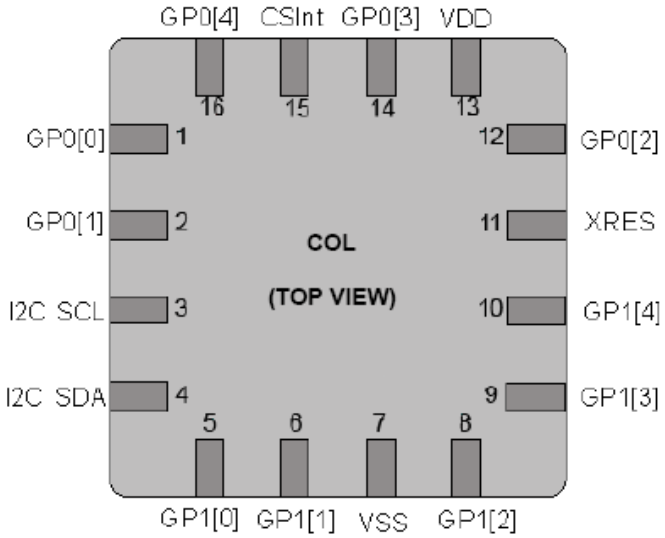


Table 1. Pin Definitions – 16 COL- CY8C20110 (10 Buttons)/CY8C20180 (8 Buttons) CY8C20160 (6 Buttons)/CY8C20140 (4 Buttons)[1]

Pin No.	Pin Name	Description
1	GP0[0]	Configurable as CapSense or GPIO
2	GP0[1]	Configurable as CapSense or GPIO
3	I^2C SCL	I^2C Clock
4	I^2C SDA	I^2C Data
5	GP1[0]	Configurable as CapSense or GPIO
6	GP1[1]	Configurable as CapSense or GPIO
7	VSS	Ground Connection
8	GP1[2]	Configurable as CapSense or GPIO
9	GP1[3]	Configurable as CapSense or GPIO
10	GP1[4]	Configurable as CapSense or GPIO
11	XRES	Active high external reset with internal pull up
12	GP0[2]	Configurable as CapSense or GPIO
13	VDD	Supply voltage
14	GP0[3]	Configurable as CapSense or GPIO
15	CSInt	Integrating Capacitor Input. The external capacitance is required only if 5:1 SNR cannot be achieved. Typical range is 1 nF to 4.7 nF
16	GP0[4]	Configurable as CapSense or GPIO

Note
1. 8/6/4 available configurable IOs can be configured to any of the 10 IOs of the package. After any of the 8/6/4 IOs are chosen, the remaining 2/4/6 IOs of the package are not available for any functionality.

Figure 2. Pin Diagram – 16 SOIC– CY8C20110 (10 Buttons)/CY8C20180 (8 Buttons) CY8C20160 (6 Buttons)/CY8C20140 (4 Buttons)

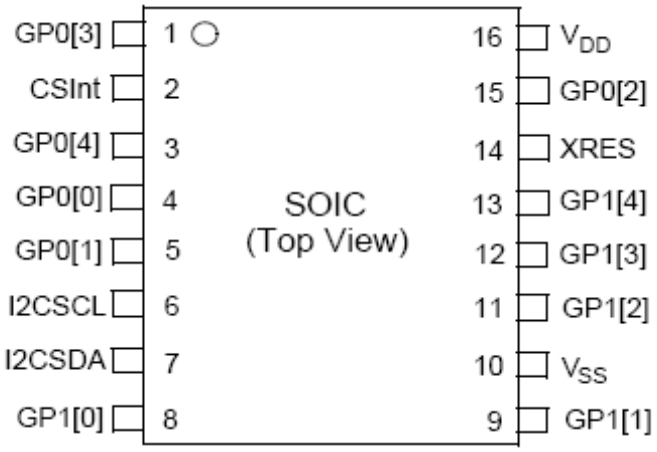


Table 2. Pin Definitions – 16 SOIC– CY8C20110 (10 Buttons)/CY8C20180 (8 Buttons) CY8C20160 (6 Buttons)/CY8C20140 (4 Buttons)[1]

Pin No	Name	Description
1	GP0[3]	Configurable as CapSense or GPIO
2	CSint	Integrating Capacitor Input. The external capacitance is required only if 5:1 SNR cannot be achieved. Typical range is 1 nF to 4.7 nF
3	GP0[4]	Configurable as CapSense or GPIO
4	GP0[0]	Configurable as CapSense or GPIO
5	GP0[1]	Configurable as CapSense or GPIO
6	I^2C SCL	I^2C Clock
7	I^2C SDA	I^2C Data
8	GP1[0]	Configurable as CapSense or GPIO
9	GP1[1]	Configurable as CapSense or GPIO
10	VSS	Ground Connection
11	GP1[2]	Configurable as CapSense or GPIO
12	GP1[3]	Configurable as CapSense or GPIO
13	GP1[4]	Configurable as CapSense or GPIO
14	XRES	Active high external reset with internal pull up
15	GP0[2]	Configurable as CapSense or GPIO
16	VDD	Supply voltage

Figure 3. Pin Diagram - 8-Pin SOIC- CY8C20142 (4 Button)

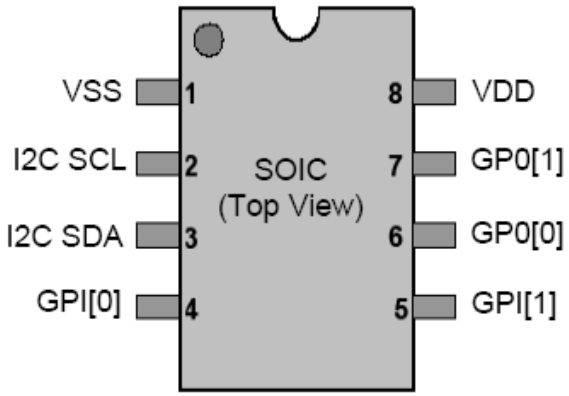
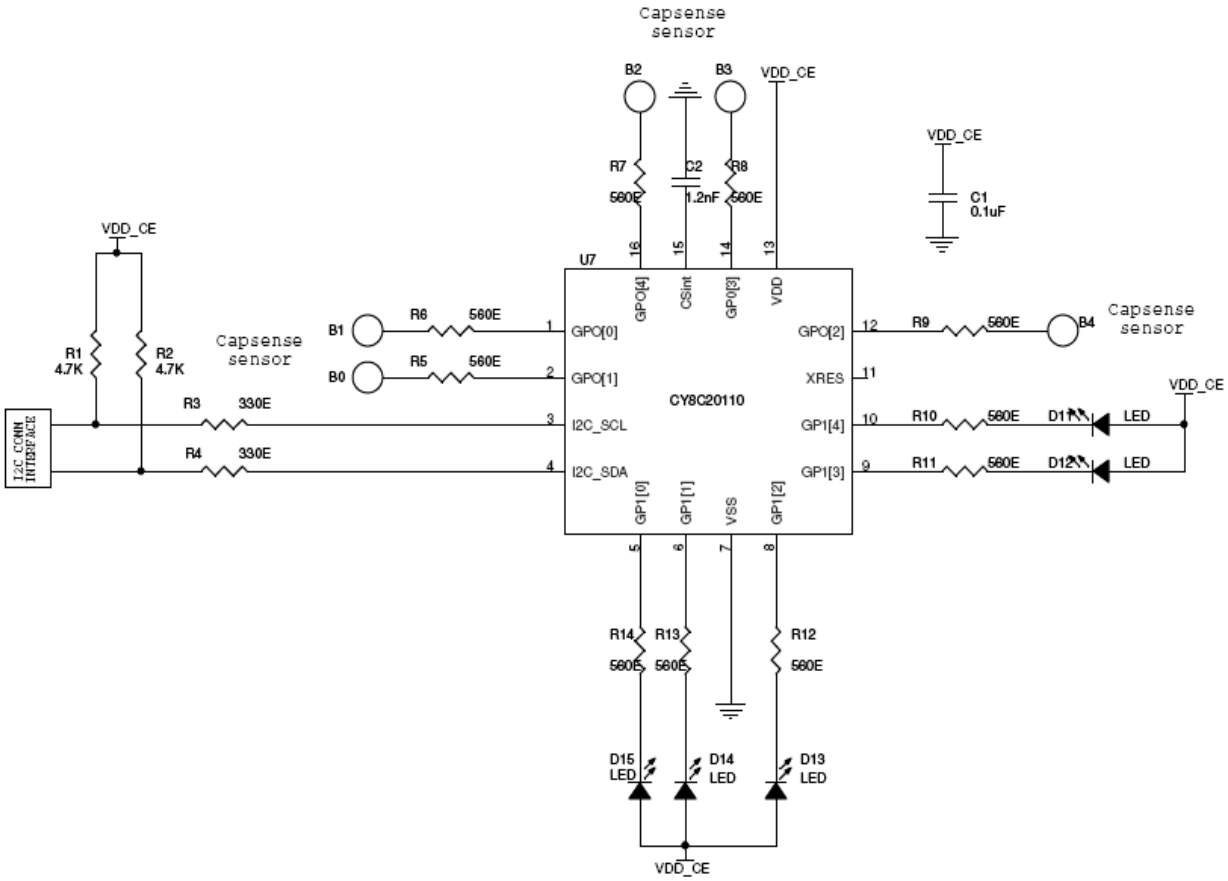


Table 3. Pin Definitions - 8-Pin SOIC - CY8C20142 (4 Button)

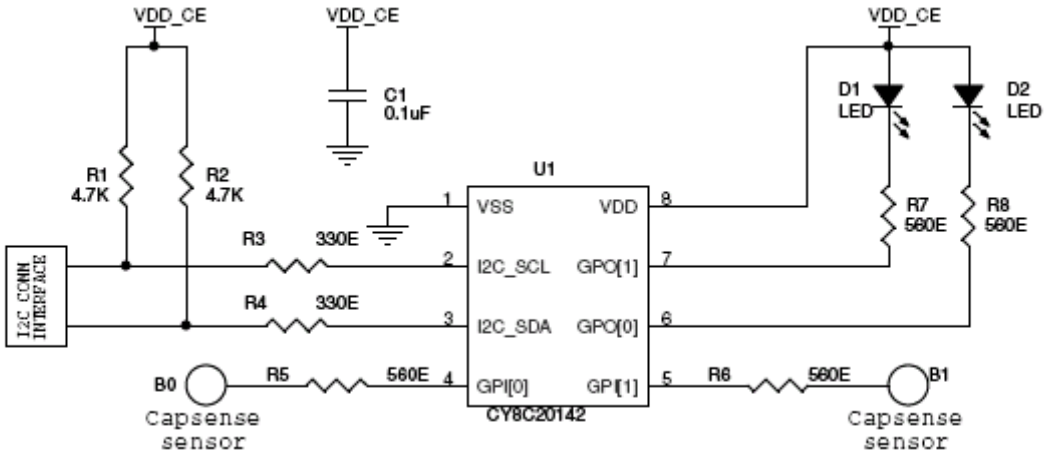
Pin No	Name	Description
1	VSS	Ground
2	I^2C SCL	I^2C Clock
3	I^2C SDA	I^2C Data
4	GP1[0]	Configurable as CapSense or GPIO
5	GP1[1]	Configurable as CapSense or GPIO
6	GP0[0]	Configurable as CapSense or GPIO
7	GP0[1]	Configurable as CapSense or GPIO
8	VDD	Supply voltage

Typical Circuits

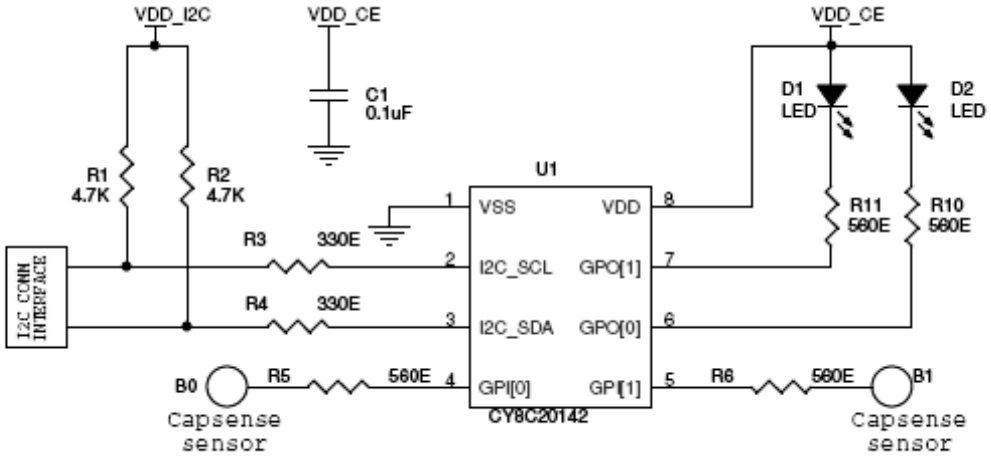
Circuit-1: Five Button and Five LED with I²C Interface



Circuit 2 - Two Buttons and Two LEDs with I²C Interface

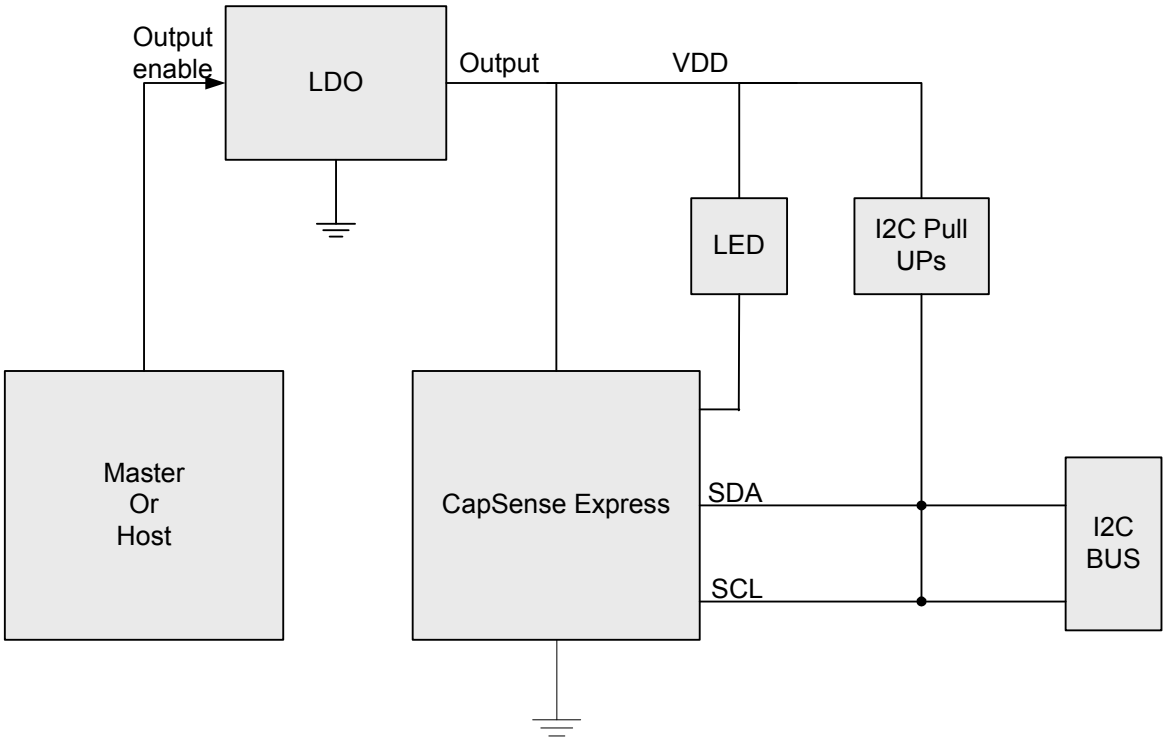


Circuit 3 - Compatibility with 1.8V I²C Signaling



Note 1.8V ≤ VDD_I2C ≤ VDD_CE and 2.4V ≤ VDD_CE ≤ 5.25V

Circuit 4 - Powering Down CapSense Express Device for Low Power Requirements



For low power requirements, if Vdd is to be turned off, this concept can be used. The requirement is that the Vdds of CapSense Express, I²C pull ups, and LEDs should be from the same source such that turning off the Vdd ensures that no signal is applied to the device while it is unpowered. The I²C signals should not be driven high by the master in this situation. If a port pin or group of port pins of the master can cater to the power supply requirements of the circuit, the LDO can be avoided.

I²C Interface

The CapSense Express devices support the industry standard I²C protocol, which can be used for:

- Configuring the device
- Reading the status and data registers of the device
- Controlling device operation
- Executing commands

The I²C address can be modified during configuration.

I²C Device Addressing

The device uses a seven bit addressing protocol. The I²C data transfer is always initiated by the master sending a one byte address: the first 7 bits contain the address and the LSB indicates the data transfer direction. Zero in the LSB bit indicates the write transaction from master and one indicates read transfer by the master. The following table shows examples for different I²C addresses.

Table 4. I²C Address Examples

7 Bit Slave Address	D7	D6	D5	D4	D3	D2	D1	D0	8 Bit Slave Address
1	0	0	0	0	0	0	1	0(W)	02
1	0	0	0	0	0	0	1	1(R)	03
75	1	0	0	1	0	1	1	0(W)	96
75	1	0	0	1	0	1	1	1(W)	97

I²C Clock Stretching

'Clock stretching' or 'bus stalling' in I²C communication protocol is a state in which the slave holds the SCL line low to indicate that it is busy. In this condition, the master is expected to wait till the SCL is released by the slave.

When an I²C master communicates with the CapSense Express device, the CapSense Express stalls the I²C bus after the reception of each byte (that is, just before the ACK/NAK bit) until processing of the byte is complete and critical internal functions are executed. Use a fully I²C compliant master to communicate with the CapSense Express device.

If the I²C master does not support clock stretching (a bit banged software I²C Master), the master must wait for a specific amount of time (as specified in "Format for Register Write and Read" on page 8) for each register write and read operation before the next bit is transmitted. The I²C master must check the SCL status (it should be high) before the I²C master initiates any data transfer with CapSense Express. If the master fails to do so and continues to communicate, the communication is erroneous.

The following diagrams represent the ACK time delays shown in "Format for Register Write and Read" on page 8 for write and read.

Figure 4. Write ACK Time Representation[2]

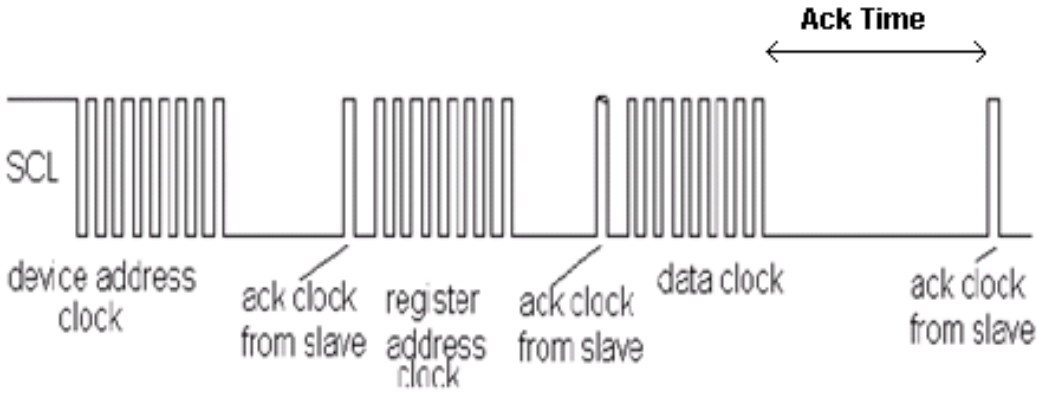
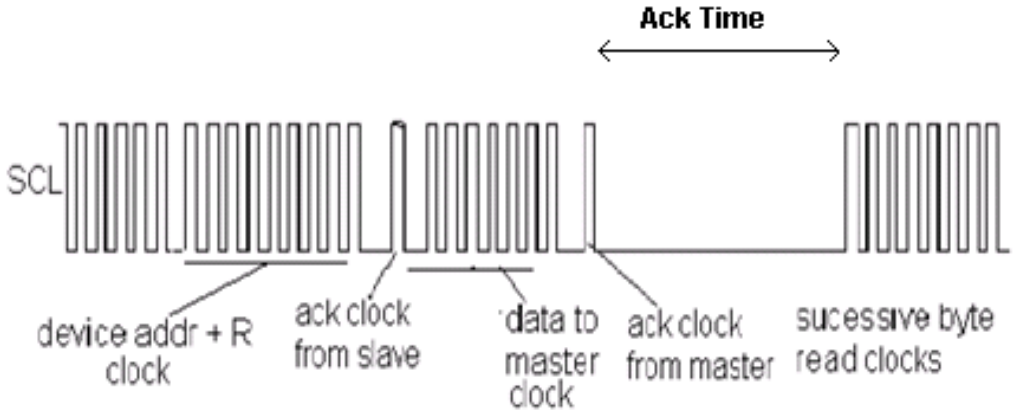


Figure 5. Read ACK Time Representation[3]



Format for Register Write and Read

Register write format

Start	Slave Addr + W	A	Reg Addr	A	Data	A	Data	A	. . . . .	Data	A	Stop

Register read format

Start	Slave Addr + W	A	Reg Addr	A	Stop						
Start	Slave Addr + R	A	Data	A	Data	A	. . . . .	Data	N	Stop	

Legends:

Master	A - ACK
Slave	N- NAK

Notes
2. Time to process the received data
3. Time taken for the device to send next byte

Operating Modes of I²C Commands

Normal Mode

In normal mode of operation, the acknowledgment time is optimized. The timings remain approximately the same for different configurations of the slave. To reduce the acknowledgment times in normal mode, the registers 0x06-0x09, 0x0C, 0x0D, 0x10-0x17, 0x50, 0x51, 0x57-0x60, 0x7E are given only read access. Write to these registers can be done only in setup mode.

Setup Mode

All registers have read and write access (except those which are read only) in this mode. The acknowledgment times are longer compared to normal mode. When CapSense scanning is disabled (command code 0x0A in command register 0xA0), the acknowledgment times can be improved to values similar to the normal mode of operation.

Device Operation Modes

CapSense Express devices are configured to operate in any of the following three modes to meet different power consumption requirements:

- Active Mode
- Periodic Sleep Mode
- Deep Sleep Mode

Active Mode

In the active mode, all the device blocks including the CapSense sub system are powered. Typical active current consumption of the device across the operating voltage range is 1.5 mA.

Periodic Sleep Mode

Sleep mode provides an intermediate power operation mode. It is enabled by configuring the corresponding device registers (0x7E, 0x7F). The device goes into sleep after there is no event for stay awake counter (Reg 0x80) number of sleep intervals. The device wakes up on sleep interval and It scans the capacitive sensors before going back to sleep again. If any sensor is active, then the device wakes up. The device can also wake up from sleep mode with a GPIO interrupt. The following sleep intervals are supported in CapSense Express. The sleep interval is configured through registers.

- 1.95 ms (512 Hz)
- 15.6 ms (64 Hz)
- 125 ms (8 Hz)
- 1s (1 Hz)

Deep Sleep Mode

Deep sleep mode provides the lowest power consumption because there is no operation running. All CapSense scanning is disabled during this mode. In this mode, the device wakes up only using an external GPIO interrupt. A sleep timer interrupt cannot wake up a device from deep sleep mode. This is treated as a continuous sleep mode without periodic wakeups. Refer to the application note CapSense Express Power and Sleep Considerations - AN44209 for details on different sleep modes. To get the lowest power during this mode the sleep timer frequency should be set to 1 Hz.

Sleep Control Pin

The devices require a dedicated sleep control pin to enable reliable I²C communication in case any sleep mode is enabled. This is achieved by pulling the sleep control pin low to wake up the device and start I²C communication. The sleep control pin can be configured on any GPIO.

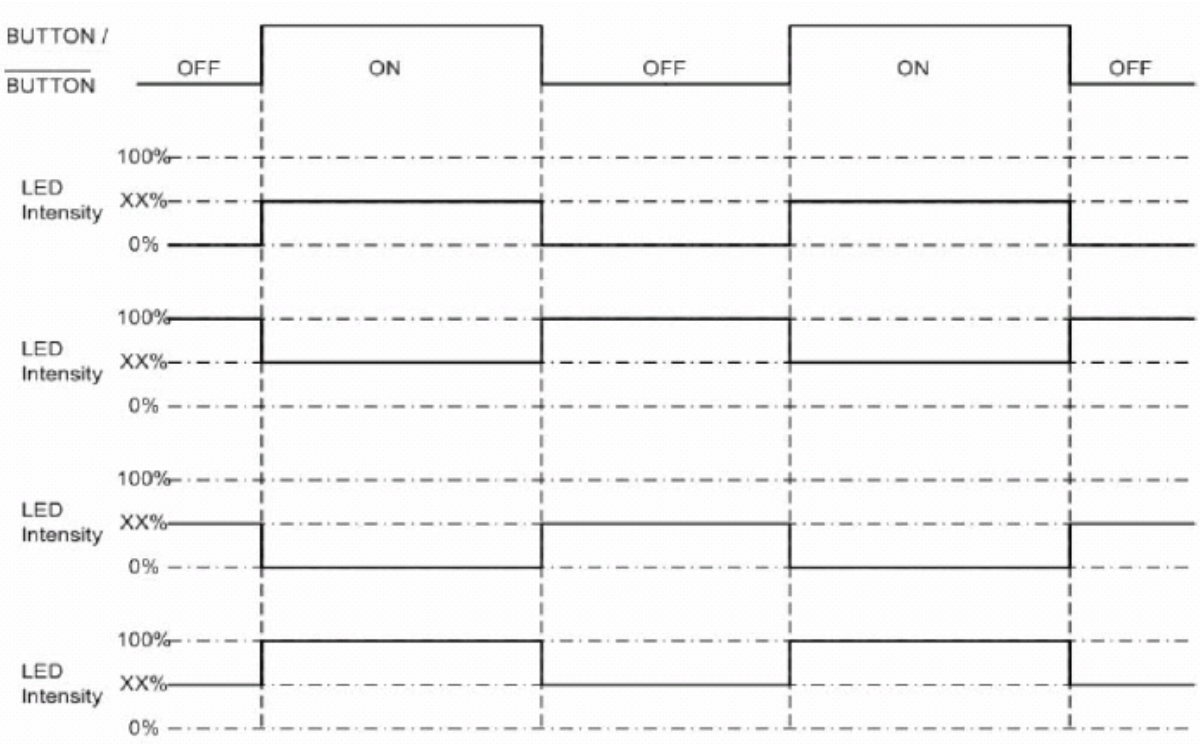
Interrupt Pin to Master

To inform the master of any button press a GPIO can be configured as interrupt output and all CapSense buttons can be connected to this GPIO with an OR logic operator. This can be configured using the software tool.

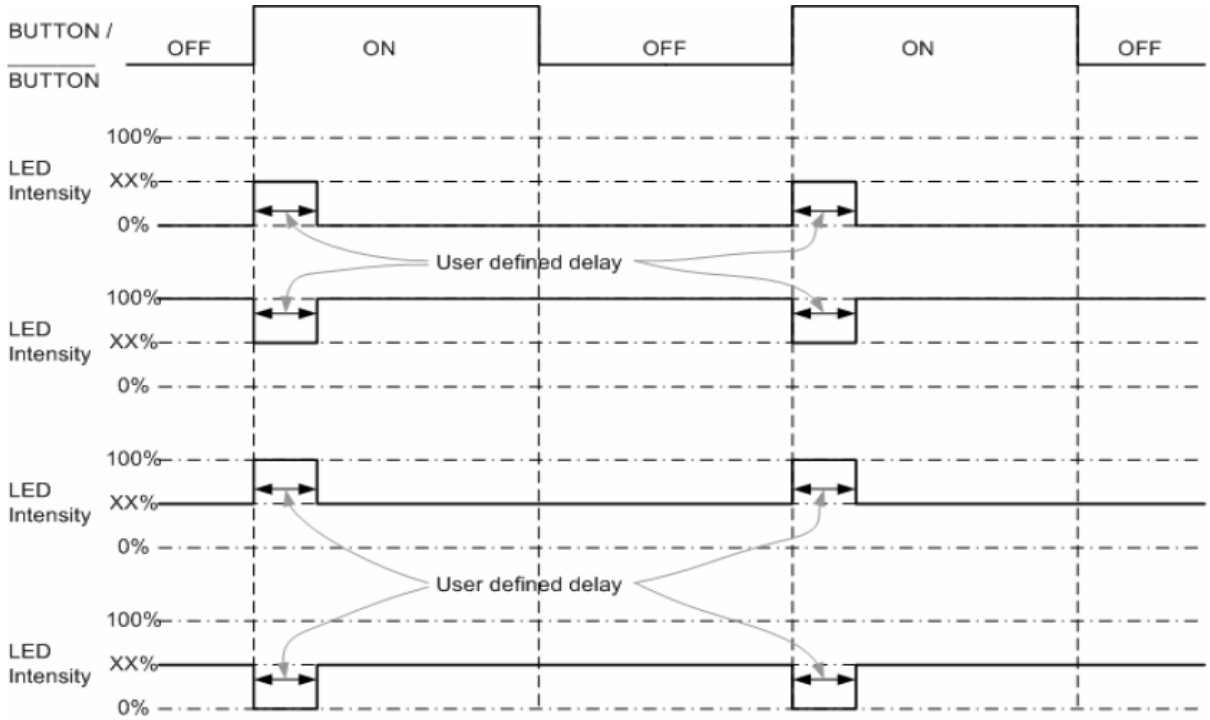
LED Dimming

To change the brightness and intensity of the LEDs, the host master (MCU, MPU, DSP, and so on) must send I²C commands and program the PWM registers to enable output pins, set duty cycle, and mode configuration. The single PWM source is connected to all GPIO pins and has a common user defined duty cycle. Each PWM enabled pin has two possible outputs: PWM and 0/1 (depending on the configuration). Four different modes of LED dimming are possible, as shown in “LED Dimming Mode 1: Change Intensity on ON/OFF Button Status” on page 10 to “LED Dimming Mode 4: Toggle Intensity on ON/OFF or OFF/ON Button Transitions” on page 11. The operation mode and duty cycle of the PWM enabled pins is common. This means that one pin cannot behave as in Mode1 and another pin as in Mode 2.

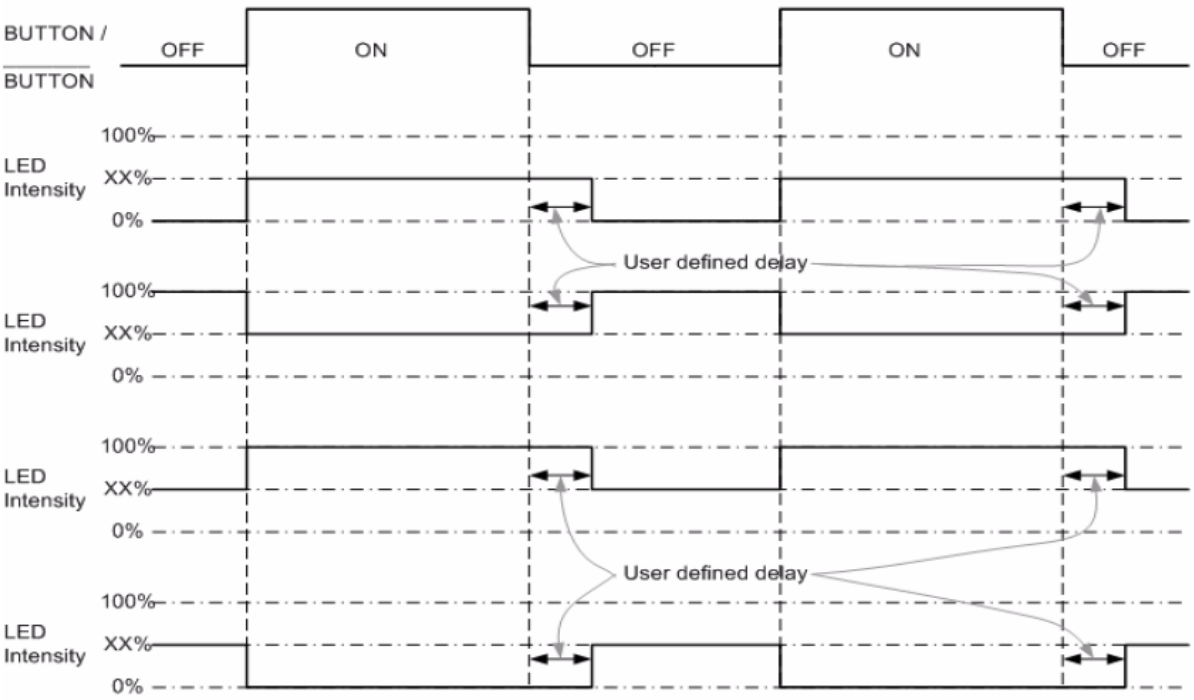
LED Dimming Mode 1: Change Intensity on ON/OFF Button Status



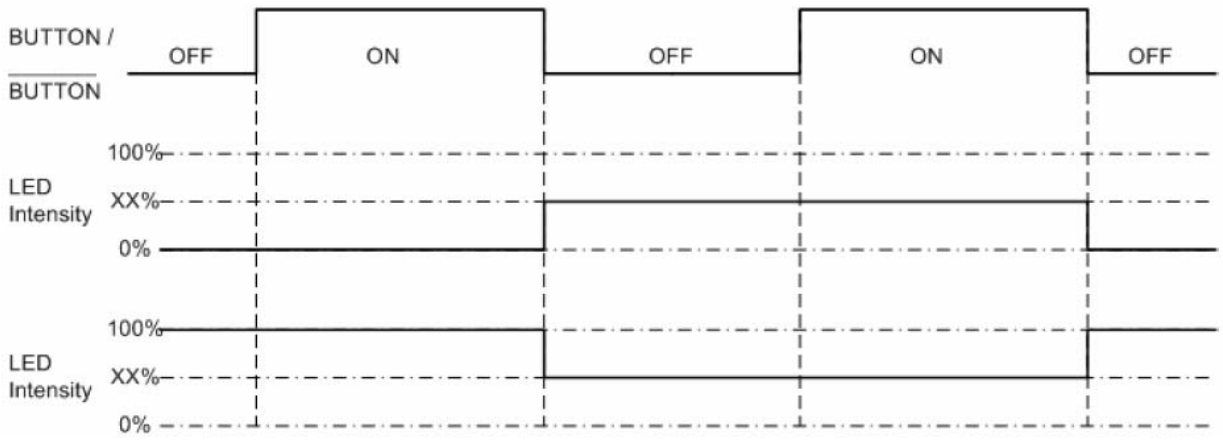
LED Dimming Mode 2: Flash Intensity on ON Button Status



LED Dimming Mode 3: Hold Intensity After ON/OFF Button Transition



LED Dimming Mode 4: Toggle Intensity on ON/OFF or OFF/ON Button Transitions



Note LED DIMMING is available only in CY8C20110.

Register Map

Name	Register Address (in Hex)	Access	Writable Only in SETUP Mode[4]	Factory Default Values of Registers (in Hex)	I2C Max ACK Time in Normal Mode (ms)	I2C Max ACK Time in Setup Mode (ms)
INPUT_PORT0	00	R		00	0.1	
INPUT_PORT1	01	R		00	0.1	
STATUS_POR0	02	R		00	0.1	
STATUS_POR1	03	R		00	0.1	
OUTPUT_PORT0	04	W		00	0.1	
OUTPUT_PORT1	05	W		00	0.1	
CS_ENABL0	06	RW	YES	00		11
CS_ENABLE	07	RW	YES	00		11
GPIO_ENABLE0	08	RW	YES	00		11
GPIO_ENABLE1	09	RW	YES	00		11
INVERSION_MASK0	0A	RW		00	0.11	
INVERSION_MASK1	0B	RW		00	0.11	
INT_MASK0	0C	RW	YES	00		11
INT_MASK1	0D	RW	YES	00		11
STATUS_HOLD_MSK0	0E	RW		03/1F[5]	0.11	
STATUS_HOLD_MSK1	0F	RW		03/1F[5]	0.11	
DM_PULL_UP0	10	RW	YES	00		11
DM_STRONG0	11	RW	YES	00		11
DM_HIGHZ0	12	RW	YES	00		11
DM_OD_LOW0	13	RW	YES	00		11
DM_PULL_UP1	14	RW	YES	00		11
DM_STRONG1	15	RW	YES	00		11
DM_HIGHZ1	16	RW	YES	00		11
DM_OD_LOW1	17	RW	YES	00		11
PWM_ENABLE0[8]	18	RW		00	0.1	
PWM_ENABLE1[8]	19	RW		00	0.1	
PWM_MODE_DC[8]	1A	RW		00	0.1	
PWM_DELAY[8]	1B	RW		00	0.1	
OP_SEL_00	1C	RW		00	0.12	11
OPR1_PRT0_00	1D	RW		00	0.12	11
OPR1_PRT1_00	1E	RW		00	0.12	11
OPR2_PRT0_00	1F	RW		00	0.12	11
OPR2_PRT1_00	20	RW		00	0.12	11
OP_SEL_01	21	RW		00	0.12	11
OPR1_PRT0_01	22	RW		00	0.12	11
OPR1_PRT1_01	23	RW		00	0.12	11
OPR2_PRT0_01	24	RW		00	0.12	11
OPR2_PRT1_01	25	RW		00	0.12	11
OP_SEL_02	26	RW		00	0.12	11
OPR1_PRT0_02	27	RW		00	0.12	11
OPR1_PRT1_02	28	RW		00	0.12	11

Register Map (continued)

Name	Register Address (in Hex)	Access	Writable Only in SETUP Mode[4]	Factory Default Values of Registers (in Hex)	I2C Max ACK Time in Normal Mode (ms)	I2C Max ACK Time in Setup Mode (ms)
OPR2_PRT0_02	29	RW		00	0.12	11
OPR2_PRT1_02	2A	RW		00	0.12	11
OP_SEL_03	2B	RW		00	0.12	11
OPR1_PRT0_03	2C	RW		00	0.12	11
OPR1_PRT1_03	2D	RW		00	0.12	11
OPR2_PRT0_03	2E	RW		00	0.12	11
OPR2_PRT1_03	2F	RW		00	0.12	11
OP_SEL_04	30	RW		00	0.12	11
OPR1_PRT0_04	31	RW		00	0.12	11
OPR1_PRT1_04	32	RW		00	0.12	11
OPR2_PRT0_04	33	RW		00	0.12	11
OPR2_PRT1_04	34	RW		00	0.12	11
OP_SEL_10	35	RW		00	0.12	11
OPR1_PRT0_10	36	RW		00	0.12	11
OPR1_PRT1_10	37	RW		00	0.12	11
OPR2_PRT0_10	38	RW		00	0.12	11
OPR2_PRT1_10	39	RW		00	0.12	11
OP_SEL_11	3A	RW		00	0.12	11
OPR1_PRT0_11	3B	RW		00	0.12	11
OPR1_PRT1_11	3C	RW		00	0.12	11
OPR2_PRT0_11	3D	RW		00	0.12	11
OPR2_PRT1_11	3E	RW		00	0.12	11
OP_SEL_12	3F	RW		00	0.12	11
OPR1_PRT0_12	40	RW		00	0.12	11
OPR1_PRT1_12	41	RW		00	0.12	11
OPR2_PRT0_12	42	RW		00	0.12	11
OPR2_PRT1_12	43	RW		00	0.12	11
OP_SEL_13	44	RW		00	0.12	11
OPR1_PRT0_13	45	RW		00	0.12	11
OPR1_PRT1_13	46	RW		00	0.12	11
OPR2_PRT0_13	47	RW		00	0.12	11
OPR2_PRT1_13	48	RW		00	0.12	11
OP_SEL_14	49	RW		00	0.12	11
OPR1_PRT0_14	4A	RW		00	0.12	11
OPR1_PRT1_14	4B	RW		00	0.12	11
OPR2_PRT0_14	4C	RW		00	0.12	11
OPR2_PRT1_14	4D	RW		00	0.12	11
CS_NOISE_TH	4E	RW		28	0.11	11
CS_BL_UPD_TH	4F	RW		64	0.11	11
CS_SETL_TIME	50	RW	YES	A0		35
CS_OTH_SET	51	RW	YES	00		35
CS_HYSTERISIS	52	RW		0A	0.11	11

Register Map (continued)

Name	Register Address (in Hex)	Access	Writable Only in SETUP Mode[4]	Factory Default Values of Registers (in Hex)	I2C Max ACK Time in Normal Mode (ms)	I2C Max ACK Time in Setup Mode (ms)
CS_DEBOUNCE	53	RW		03	0.11	11
CS_NEG_NOISE_TH	54	RW		14	0.11	11
CS_LOW_BL_RST	55	RW		14	0.11	11
CS_FILTERING	56	RW		20	0.11	11
CS_SCAN_POS_00	57	RW	YES	FF		11
CS_SCAN_POS_01	58	RW	YES	FF		11
CS_SCAN_POS_02	59	RW	YES	FF		11
CS_SCAN_POS_03	5A	RW	YES	FF		11
CS_SCAN_POS_04	5B	RW	YES	FF		11
CS_SCAN_POS_10	5C	RW	YES	FF		11
CS_SCAN_POS_11	5D	RW	YES	FF		11
CS_SCAN_POS_12	5E	RW	YES	FF		11
CS_SCAN_POS_13	5F	RW	YES	FF		11
CS_SCAN_POS_14	60	RW	YES	FF		11
CS_FINGER_TH_00	61	RW		64	0.14	11
CS_FINGER_TH_01	62	RW		64	0.14	11
CS_FINGER_TH_02	63	RW		64	0.14	11
CS_FINGER_TH_03	64	RW		64	0.14	11
CS_FINGER_TH_04	65	RW		64	0.14	11
CS_FINGER_TH_10	66	RW		64	0.14	11
CS_FINGER_TH_11	67	RW		64	0.14	11
CS_FINGER_TH_12	68	RW		64	0.14	11
CS_FINGER_TH_13	69	RW		64	0.14	11
CS_FINGER_TH_14	6A	RW		64	0.14	11
CS_IDAC_00	6B	RW		0A	0.14	11
CS_IDAC_01	6C	RW		0A	0.14	11
CS_IDAC_02	6D	RW		0A	0.14	11
CS_IDAC_03	6E	RW		0A	0.14	11
CS_IDAC_04	6F	RW		0A	0.14	11
CS_IDAC_10	70	RW		0A	0.14	11
CS_IDAC_11	71	RW		0A	0.14	11
CS_IDAC_12	72	RW		0A	0.14	11
CS_IDAC_13	73	RW		0A	0.14	11
CS_IDAC_14	74	RW		0A	0.14	11
	75[6]					
	76[6]					
	77[6]					
	78[6]					
I2C_ADDR_LOCK	79	RW		01	0.11	11
DEVICE_ID	7A	R		42/40/60/80/10[7]	0.11	11
DEVICE_STATUS	7B	R		03	0.11	11
I2C_ADDR_DM	7C	RW		00	0.11	11

Register Map (continued)

Name	Register Address (in Hex)	Access	Writable Only in SETUP Mode[4]	Factory Default Values of Registers (in Hex)	I2C Max ACK Time in Normal Mode (ms)	I2C Max ACK Time in Setup Mode (ms)
	7D[6]					
SLEEP_PIN	7E	RW	YES	00	0.1	11
SLEEP_CTRL	7F	RW		00	0.1	11
SLEEP_SA_CNTR	80	RW		00	0.1	11
CS_READ_BUTTON	81	RW		00	0.12	11
CS_READ_BLM	82	R		00	0.12	11
CS_READ_BLL	83	R		00	0.12	11
CS_READ_DIFFM	84	R		00	0.12	11
CS_READ_DIFFL	85	R		00	0.12	11
CS_READ_RAWM	86	R		00	0.12	11
CS_READ_RAWL	87	R		00	0.12	11
CS_READ_STATUSM	88	R		00	0.12	11
CS_READ_STATUSL	89	R		00	0.12	11
	8A[6]					
	8B[6]					
	8C[6]					
	8D[6]					
COMMAND_REG	A0	W		00	0.1	11

Table 5. Device IDs

Part Number	Device ID
CY8C 20142	42
CY8C 20140	40
CY8C 20160	60
CY8C 20180	80
CY8C 20110	10

Note All the Ack times specified are maximum values with all buttons enabled and filer enabled with maximum order.

Notes
4. These registers are writable only after entering into setup mode. All the other registers available for read and write in Normal as well as in Setup mode.
5. The factory defaults of Reg 0x0E and 0x0F is 0x03 for 20142 device and 0x1F for 20140/60/80/10 devices.
6. The register 0x75- 0x78, 0x7D and 0x8A-0x8D are reserved.
7. The Device ID for different devices are tabulated in Table 5.
8. These registers are available only in CY8C20110.

CapSense Express Commands

Command[9]	Description	Executable Mode	Duration the Device is not accessible after ACK (in ms)
W 00 A0 00	Get firmware revision	Setup/Normal	0
W 00 A0 01	Store current configuration to NVM	Setup/Normal	120
W 00 A0 02	Restore factory configuration	Setup/Normal	120
W 00 A0 03	Write NVM POR defaults	Setup/Normal	120
W 00 A0 04	Read NVM POR defaults	Setup/Normal	5
W 00 A0 05	Read current configurations (RAM)	Setup/Normal	5
W 00 A0 06	Reconfigure device (POR)	Setup	5
W 00 A0 07	Set Normal mode of operation	Setup/Normal	0
W 00 A0 08	Set Setup mode of operation	Setup/Normal	0
W 00 A0 09	Start scan	Setup/Normal	10
W 00 A0 0A	Stop scan	Setup/Normal	5
W 00 A0 0B	Get CapSense scan status	Setup/Normal	0

Register Conventions

This table lists the register conventions that are specific to this section.

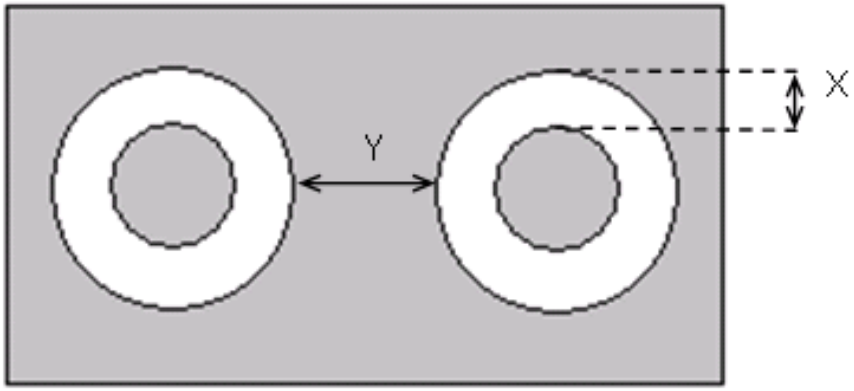
Convention	Description
RW	Register has both read and write access
R	Register has only read access

Note
9. The ‘W’ indicates the write transfer. The next byte of data represents the 7 bit I2C address.

Layout Guidelines and Best Practices

CapSense Button Shapes

Button Layout Design



X: Button to ground clearance (Refer to Table 6 on page 18)
Y: Button to button clearance (Refer to Table 6 on page 18)

Recommended via Hole Placement

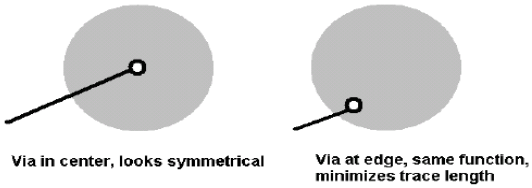


Table 6. Recommended Layout Guidelines and Best Practices

Sl	Category	Min	Max	Recommendations/Remarks
1	Button Shape			Solid round pattern, round with LED hole, rectangle with round corners
2	Button Size	5 mm	15 mm	10 mm
3	Button-Button Spacing	= Button Ground Clearance		8 mm [X]
4	Button Ground Clearance	0.5 mm	2 mm	Button ground clearance = Overlay Thickness [Y]
5	Ground Flood - Top Layer			Hatched ground 7 mil trace and 45 mil grid (15% filling)
6	Ground Flood - Bottom Layer			Hatched ground 7 mil trace and 70 mil grid (10% filling)
7	Trace Length from Sensor to PSoC - Buttons		200 mm	<100 mm.
8	Trace Width	0.17 mm	0.20 mm	0.17 mm (7 mil)
9	Trace Routing			Traces should be routed on the non sensor side. If any non CapSense trace crosses CapSense trace, ensure that inter-section is orthogonal.
10	Via Position for the Sensors			Via should be placed near the edge of the button/slider to reduce trace length thereby increasing sensitivity.
11	Via Hole Size for Sensor Traces			10 mil
12	Number of Vias on Sensor Trace	1	2	1
13	CapSense Series Resistor Placement		10 mm	Place CapSense series resistors close to PSoC for noise suppression.CapSense resistors have highest priority place them first.
14	Distance between any CapSense Trace to Ground Flood	10 mil	20 mil	20 mil
15	Device Placement			Mount the device on the layer opposite to sensor. The CapSense trace length between the device and sensors should be minimum
16	Placement of Components in 2 Layer PCB			Top layer - sensor pads and bottom layer - PSoC, other components, and traces.
17	Placement of Components in 4 Layer PCB			Top layer - sensor pads, second layer - CapSense traces, third layer - hatched ground, bottom layer - PSoC, other components, and non CapSense traces
18	Overlay Thickness - Buttons	0 mm	2 mm	1 mm
19	Overlay Material			Should to be non conductive material. Glass, ABS Plastic, Formica
20	Overlay Adhesives			Adhesive should be non conductive and dielectrically homog-enous. 467MP and 468MP adhesives made by 3M are recommended.
21	LED Back Lighting			Cut a hole in the sensor pad and use rear mountable LEDs. Refer the PCB layout below.
22	Board Thickness			Standard board thickness for CapSense FR4 based designs is 1.6 mm.

Example PCB Layout Design with Two CapSense Buttons and Two LEDs

Figure 6. Top Layer

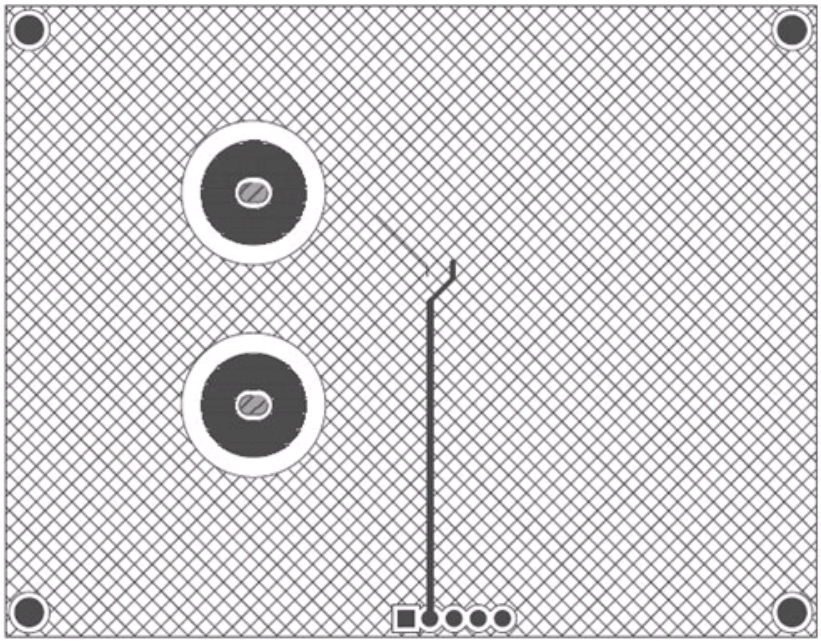
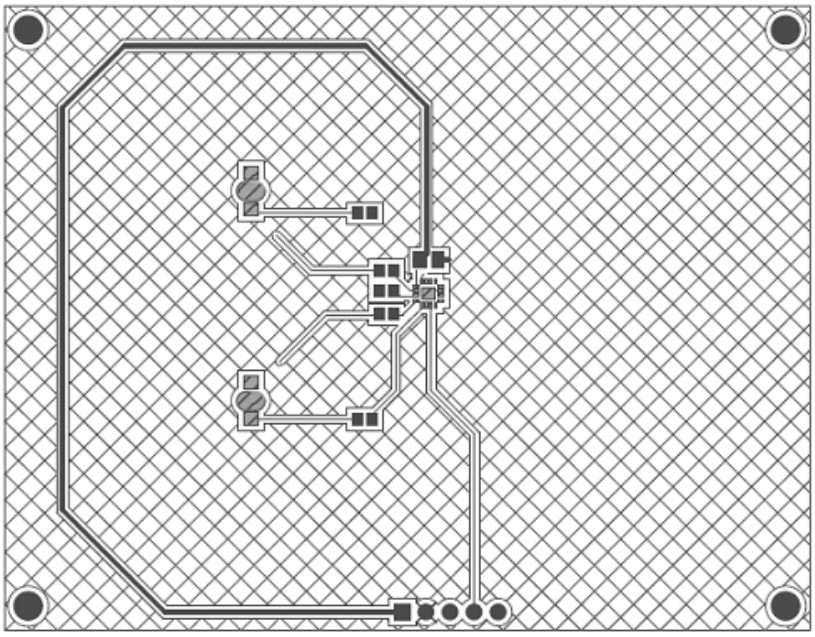
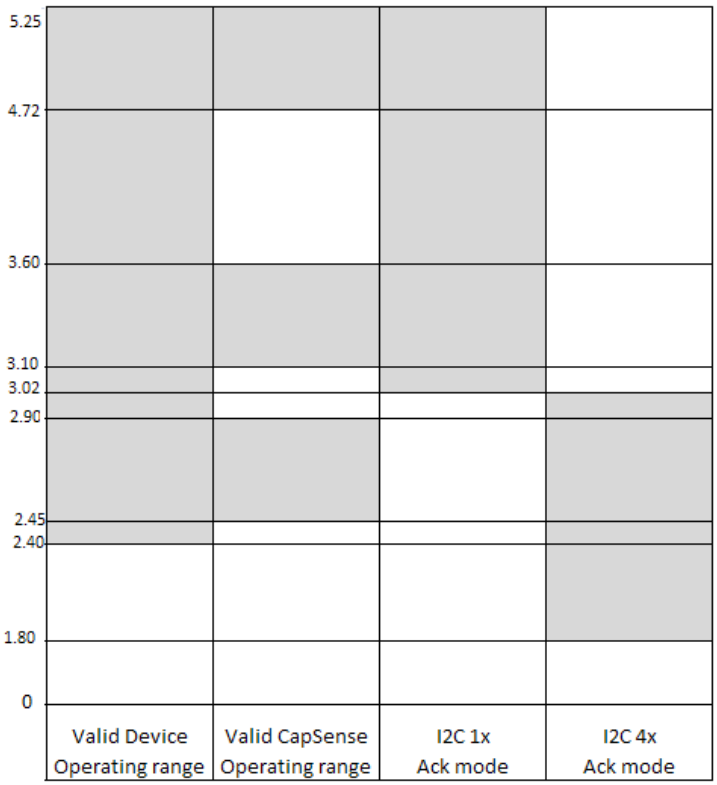


Figure 7. Bottom Layer



Operating Voltages



For details on I^2C 1x ACK time, refer to "Register Map" on page 12 and "CapSense Express Commands" on page 16. I^2C 4x ACK time is approximately four times the values mentioned in these tables.

CapSense Constraints

Parameter	Min	Typ	Max	Units	Notes
Parasitic Capacitance (C_P) of the CapSense Sensor			30	pF	
Overlay Thickness	0	1	2	mm	All layout best practices followed, properly tuned, and noise free condition.
Supply Voltage Variation (V_{DD})			± 5%		

Electrical Specifications

Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C (0°C to 50°C). Extended duration storage temperatures above 65°C degrade reliability
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any GPIO pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch up current	–	–	200	mA	

Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	

DC Electrical Characteristics

DC Chip Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	
I_{DD}	Supply current	–	1.5	2.5	mA	Conditions are V_{DD} = 3.10V, T_A = 25°C
ISB	Deep Sleep mode current with POR and LVD active	–	2.6	4	µA	VDD = 2.55V, 0°C < TA < 40°C
ISB	Deep Sleep mode current with POR and LVD active	–	2.8	5	µA	VDD = 3.3V, –40°C < TA < 85°C
ISB	Deep Sleep mode current with POR and LVD active	–	5.2	6.4	µA	VDD = 5.25V, –40°C < TA < 85°C

5V and 3.3V DC General Purpose I/O Specifications

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C≤TA≤85°C, 3.10V to 3.6V -40°C≤TA≤85°C. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Parameter	Description	Min	Typ	Max	Unit	Notes
VOH1	High output voltage on Port 0 pins	VDD – 0.2	–	–	V	IOH < 10 µA, VDD > 3.10V, maximum of 20 mA source current in all I/Os.
VOH2	High output voltage on Port 0 pins	VDD – 0.9	–	–	V	IOH = 1 mA, VDD > 3.10V, maximum of 20 mA source current in all I/Os.
VOH3	High output voltage on Port 1 pins	VDD – 0.2	–	–	V	IOH < 10 µA, VDD > 3.10V, maximum of 20 mA source current in all I/Os.
VOH4	High output voltage on Port 1 pins	VDD – 0.9	–	–	V	IOH = 5 mA, VDD > 3.10V, maximum of 20 mA source current in all I/Os.

5V and 3.3V DC General Purpose I/O Specifications (continued)

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C≤TA≤85°C, 3.10V to 3.6V -40°C≤TA≤85°C. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Parameter	Description	Min	Typ	Max	Unit	Notes
VOL	Low output voltage	–	–	0.75	V	IOL = 20 mA/pin, VDD > 3.10, maximum of 40/60 mA sink current on even port pins and of 40/60 mA sink current on odd port pins.[10]
VIL	Input low voltage	–	–	0.75	V	VDD = 3.10V to 3.6V.
VIH	Input high voltage	1.6	–	–	V	VDD = 3.10V to 3.6V.
VIL	Input low voltage	–	–	0.8	V	VDD = 4.75V to 5.25V.
VIH	Input high voltage	2.0	–	–	V	VDD = 4.75V to 5.25V.
VH	Input hysteresis voltage	–	140	–	mV	
IIL	Input leakage	–	1	–	nA	Gross tested to 1 µA.
CIN	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C.
COUT	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C.

2.7 DC General Purpose IO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
VOH1	High output voltage on Port 0 pins	VDD – 0.2	–	–	V	IOH <10 µA, maximum of 10 mA source current in all IOs.
VOH2	High output voltage on Port 0 pins	VDD – 0.5	–	–	V	IOH = 0.2 mA, maximum of 10 mA source current in all IOs.
VOH3	High output voltage on Port 1 pins	VDD – 0.2	–	–	V	IOH <10 µA, maximum of 10 mA source current in all IOs.
VOH4	High output voltage on Port 1 pins	VDD – 0.5	–	–	V	IOH = 2 mA, maximum of 10 mA source current in all IOs.
VOL1	Low output voltage	–	–	0.75	V	IOL = 10 mA/pin, VDD > 3.10, maximum of 20/30 mA sink current on even port pins and of 20/30mA sink current on odd port pins.[11]
VIL	Input low voltage	–	–	0.75	V	VDD = 2.4 to 2.90V and 3.10V to 3.6V.
VIH1	Input High voltage	1.4	–	–	V	VDD = 2.4 to 2.7V.
VIH2	Input High voltage	1.6	–	–	V	VDD = 2.7 to 2.90V and 3.10V to 3.6V.
VH	Input hysteresis voltage	–	60	–	mV	
IIL	Input leakage	–	1	–	nA	Gross tested to 1 µA.
CIN	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C.
COUT	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C

Notes
10. The maximum sink current is 40 mA for 20140 and 20142 devices and for all other devices the maximum sink current is 60 mA
11. The maximum sink current per port is 20 mA for 20140 and 20142 devices and for all other devices the maximum sink current is 30 mA.

2.7V DC Spec for I²C Line with 1.8V External Pull Up

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4V to 2.9V and 3.10V to 3.60V, and -40°C≤TA ≤85°C, respectively. Typical parameters apply to 2.7V at 25°C. The I²C lines drive mode must be set to open drain and pulled up to 1.8V externally.

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OLP}	Low output voltage	–	–	0.4	V	IOL=5 mA/pin
V_{IL}	Input low voltage	–	–	0.75	V	V_{DD} = 2.4 to 3.6V.
V_{IH}	Input high voltage	1.4	–	–	V	V_{DD} = 2.4 to 3.6V.
C_{I2C}	Capacitive load on I²C pins	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C.
R_{PU}	Pull up resistor	4	5.6	8	kΩ	

DC POR and LVD Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{PPOR0} V_{PPOR1}	V_{DD} Value for PPOR Trip V_{DD}= 2.7V V_{DD}= 3.3V, 5V	 – –	 2.36 2.60	 2.40 2.65	 V V	V_{DD} must be greater than or equal to 2.5V during startup or internal reset.
VLVD0 VLVD2 VLVD6	VDD Value for LVD Trip VDD= 2.7V VDD= 3.3V VDD= 5V	 2.39 2.75 3.98	 2.45 2.92 4.05	 2.51 2.99 4.12	 V V V	

DC Flash Write Specifications

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C<TA<85°C, 3.10V to 3.6V and -40°C<TA<85°C or 2.4V to 2.90V and -40°C<TA<85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only. Flash Endurance and Retention specifications are valid only within the range: 25°C±20°C during the Flash Write operation. It is at the user's own risk to operate out of this temperature range. If Flash writing is done out of this temperature range, the endurance and data retention reduces.

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations	2.7	–	–	V	
I_{DDP}	Supply Current for Flash Write Operations	–	5	25	mA	
$Flash_{ENPB}$	Flash Endurance	50,000[12]	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

CapSense Electrical Characteristics

Max (V)	Typ (V)	Min (V)	Conditions for Supply Voltage	Result
3.6	3.3	3.1	<2.9	The device automatically reconfigures itself to work in 2.7V mode of operation.
			>2.9 or <3.10	This range is not recommended for CapSense usage.
2.90	2.7	2.45	<2.45V	The scanning for CapSense parameters shuts down until the voltage returns to over 2.45V.
			>3.10	The device automatically reconfigures itself to work in 3.3V mode of operation.
			<2.4V	The device goes into reset.
5.25	5.0	4.75	<4.73V	The scanning for CapSense parameters shuts down until the voltage returns to over 4.73V.

Note
12. Commands involving Flash Writes (0x01, 0x02, 0x03) must be executed only within the same VCC voltage range detected at POR (power on, or command 0x06) and above 2.7V.

AC Electrical Specifications

5V and 3.3V AC General Purpose I/O Specifications

Parameter	Description	Min	Max	Unit	Notes
TRise0	Rise time, strong mode, Cload = 50 pF, Port 0	15	80	ns	V_{DD} = 3.10V to 3.6V and 4.75V to 5.25V, 10% - 90%
TRise1	Rise time, strong mode, Cload = 50 pF, Port 1	15	50	ns	V_{DD} = 3.10V to 3.6V, 10% - 90%
TFall	Fall time, strong mode, Cload = 50 pF, all ports	10	50	ns	V_{DD} = 3.10V to 3.6V and 4.75V to 5.25V, 10% - 90%

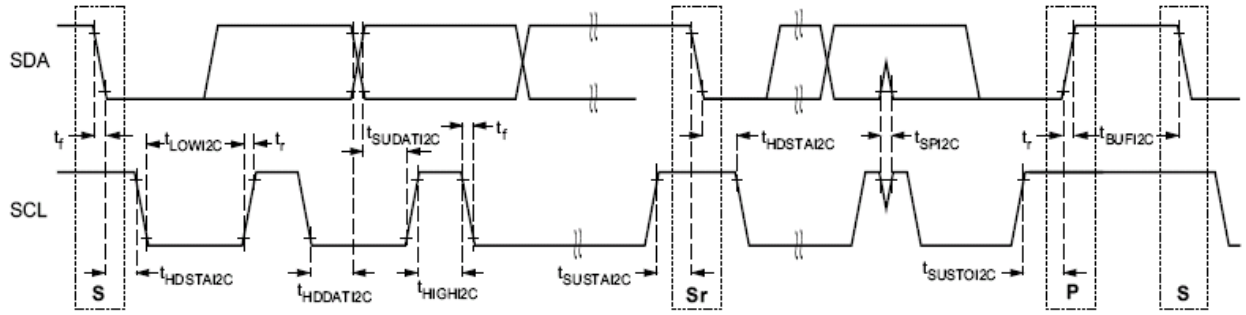
2.7V AC General Purpose I/O Specifications

Parameter	Description	Min	Max	Unit	Notes
TRise0	Rise time, strong mode, Cload = 50 pF, Port 0	15	100	ns	VDD = 2.4V to 2.90V, 10% - 90%
TRise1	Rise time, strong mode, Cload = 50 pF, Port 1	15	70	ns	VDD = 2.4V to 2.90V, 10% - 90%
TFall	Fall time, strong mode, Cload = 50 pF	10	70	ns	VDD = 2.4V to 2.90V, 10% - 90%

AC I^2C Specifications

Parameter	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCL} I^2C	SCL clock frequency	0	100	0	400	kbps	Fast mode not supported for V_{DD} < 3.0V
T_{HDSTA} I^2C	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs	
T_{LOW} I^2C	LOW period of the SCL clock	4.7	–	1.3	–	µs	
T_{HIGH} I^2C	HIGH period of the SCL clock	4.0	–	0.6	–	µs	
T_{SUSTA} I^2C	Setup time for a repeated START condition	4.7	–	0.6	–	µs	
T_{HDDAT} I^2C	Data hold time	0	–	0	–	µs	
T_{SUDAT} I^2C	Data setup time	250	–	100	–	ns	
T_{SUSTO} I^2C	Setup time for STOP condition	4.0	–	0.6	–	µs	
T_{BUF} I^2C	BUS free time between a STOP and START condition	4.7	–	1.3	–	µs	
T_{SP} I^2C	Pulse width of spikes suppressed by the input filter	–	–	0	50	ns	

Figure 8. Definition of Timing for Fast/Standard Mode on the I²C Bus



Appendix- Examples of Frequently Used I²C Commands

Sl No.	Requirement	I²C commands[13]	Comment
1	Enter into setup mode	W 00 A0 08	
2	Enter into normal mode	W 00 A0 07	
3	Load factory defaults to RAM registers	W 00 A0 02	
4	Do a software reset	W 00 A0 08 W 00 A0 06	Enter into setup mode Do software reset
5	Save current configuration to Flash	W 00 A0 01	
6	Load factory defaults to RAM registers and save as user configuration	W 00 A0 08 W 00 A0 02 W 00 A0 01 W 00 A0 06	Enter into setup mode Load factory defaults to SRAM Save the configuration to flash. Wait for time specified in "CapSense Express Commands" on page 16. Do software reset
7	Enable GP00 as CapSense button	W 00 A0 08 W 00 06 01 W 00 A0 01 W 00 A0 06	Enter into setup mode Configuring CapSense buttons Save the configuration to flash. Wait for time specified in "CapSense Express Commands" on page 16. Do software reset
8	Read CapSense button(GP00) scan results	W 00 81 01 W 00 82 R 00 RD. RD. RD.	Select CapSense button for reading scan result Set the read point to 82h Consecutive 6 reads get baseline, difference count and raw count (all two byte each)
9	Read CapSense button status register	W 00 88 R 00 RD	Set the read pointer to 88 Reading a byte gets status CapSense inputs

Note
13. The 'W' indicates the write transfer and the next byte of data represents the 7-bit I2C address. The I2C address is assumed to be '0' in the above examples. Similarly 'R' indicates the read transfer followed by 7-bit address and data byte read operations.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Temperature	CapSense Block	GPIOs	XRES Pin
CY8C20110-LDX2I	001-09116	16 COL[14]	Industrial	Yes	10	Yes
CY8C20110-SX2I	51-85068	16 SOIC	Industrial	Yes	10	Yes
CY8C20180-LDX2I	001-09116	16 COL[14]	Industrial	Yes	08	Yes
CY8C20180-SX2I	51-85068	16 SOIC	Industrial	Yes	08	Yes
CY8C20160-LDX2I	001-09116	16 COL[14]	Industrial	Yes	06	Yes
CY8C20160-SX2I	51-85068	16 SOIC	Industrial	Yes	06	Yes
CY8C20140-LDX2I	001-09116	16 COL[14]	Industrial	Yes	04	Yes
CY8C20140-SX2I	51-85068	16 SOIC	Industrial	Yes	04	Yes
CY8C20142-SX1I	51-85066	8 SOIC	Industrial	Yes	04	No

Note For die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definition

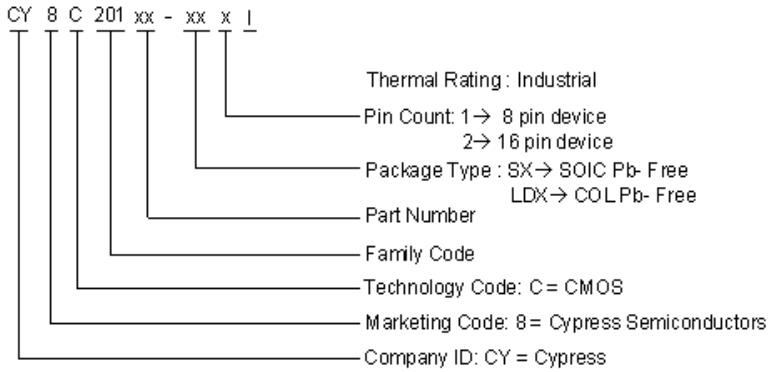


Table 7. Thermal Impedances by Package

Package	Typical θ_{JA}[15]
16 COL[1]	46 °C/W
16 SOIC	79.96 °C/W
8 SOIC	127.22 °C/W

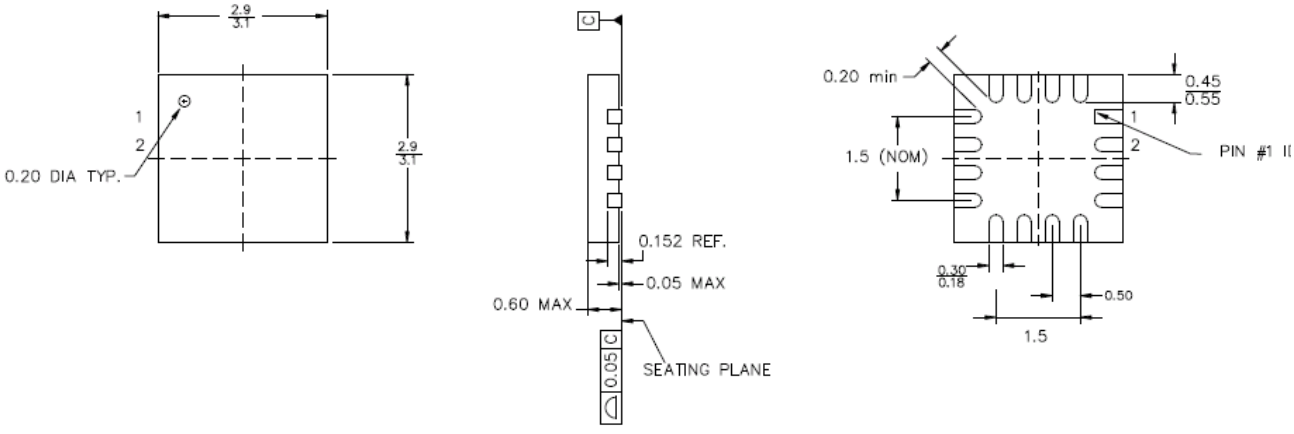
Table 8. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[16]	Maximum Peak Temperature
16 COL[1]	240 °C	260 °C
16 SOIC	240 °C	260 °C
8 SOIC	240 °C	260 °C

Notes
14. Earlier termed as QFN package.
15. $T_J = T_A + \text{Power} \times \theta_{JA}$.
16. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Package Diagrams

Figure 9. 16-Pin Chip On Lead 3 X 3 mm (Sawn) (001-09116)



PART NO.	DESCRIPTION
LG16A	LEAD–FREE
LD16A	STANDARD

NOTES:

1. JEDEC # MO–220
2. Package Weight: 0.014g
3. DIMENSIONS IN MM, MIN / MAX

001-09116 *D

Figure 10. 16-Pin (150-Mil) SOIC (51-85068)

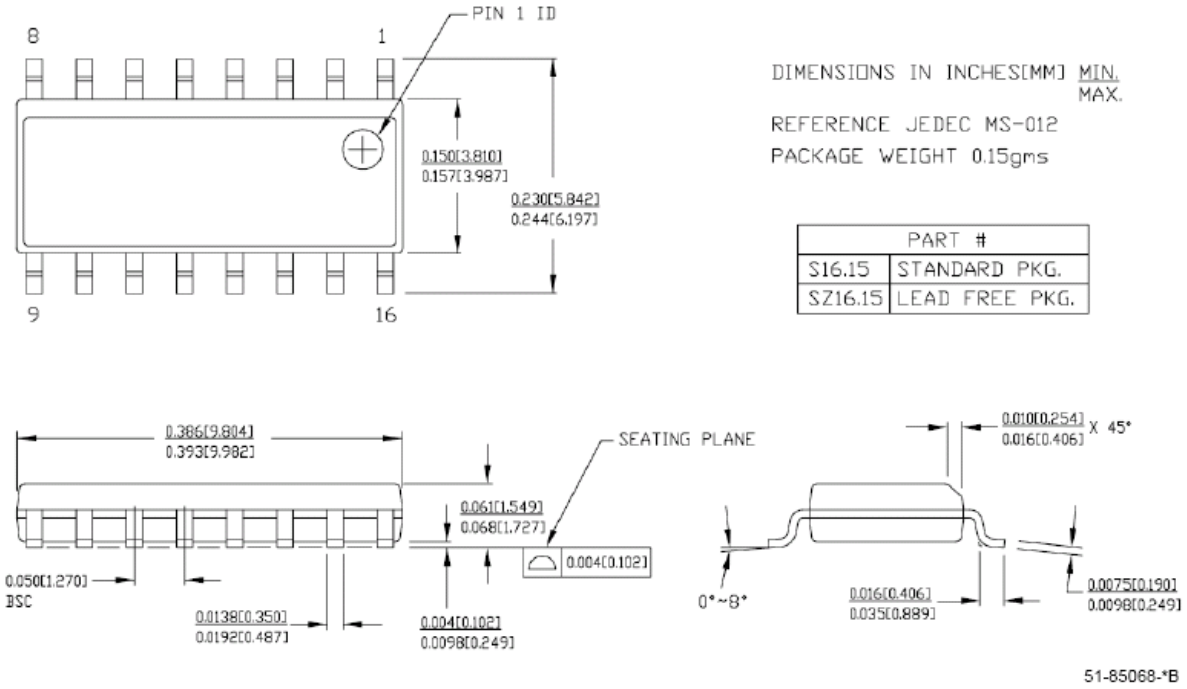
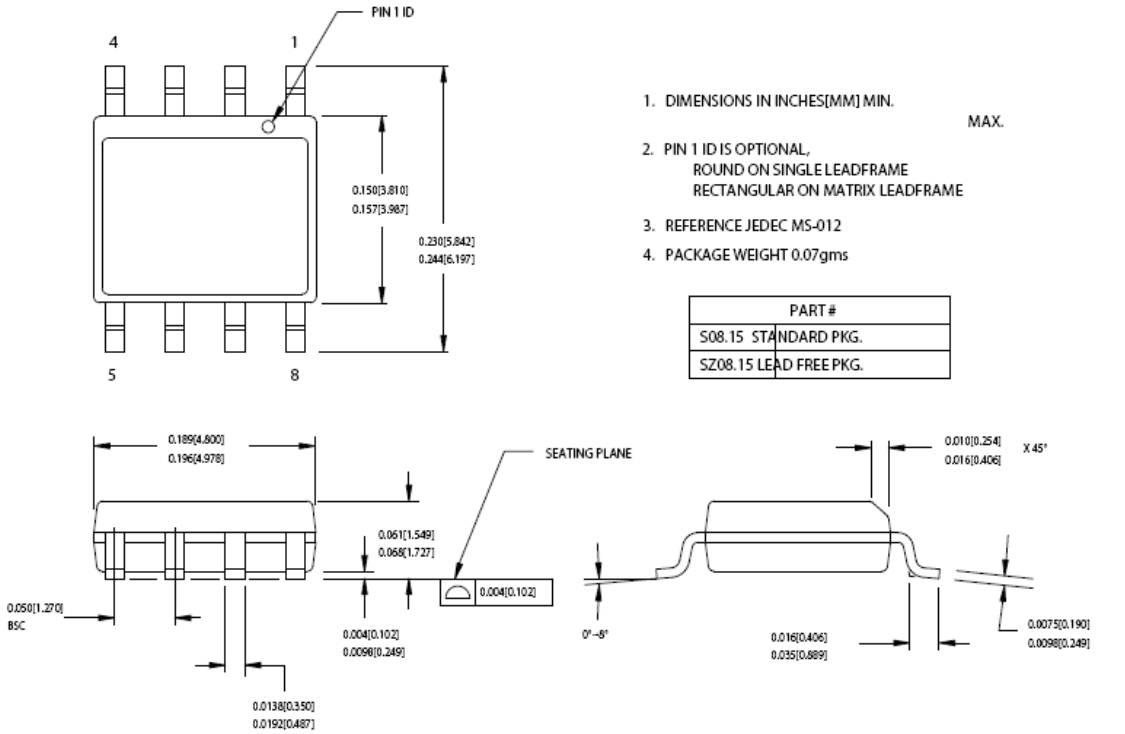


Figure 11. 8-Pin (150-Mil) SOIC (51-85066)



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