SGS-THOMSON MICROELECTRONICS

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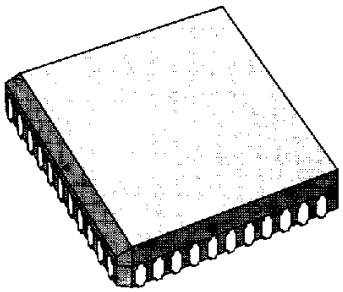
MK62486

VERY FAST CMOS 32K x 9 CACHE BRAM

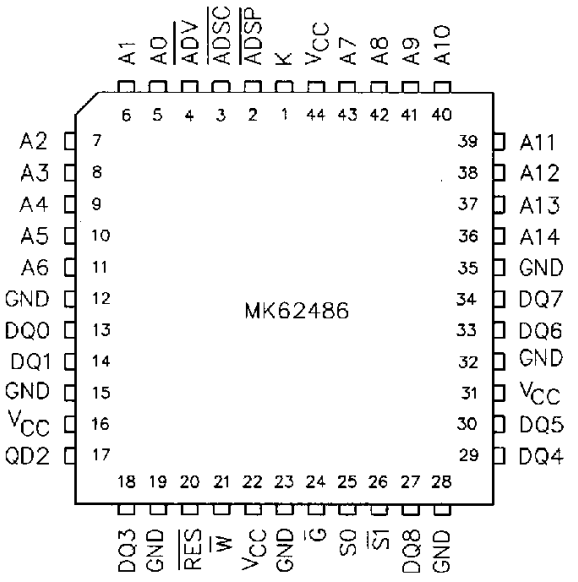
ADVANCE DATA

- 32K x 9 CMOS SYNCHRONOUS BURSTSRAM
- FAST CYCLE TIMES: 25, 30ns
- FAST ACCESS: 19, 24ns Max
- ON-BOARD BURST COUNTER
- INPUT REGISTERS (ADDR.,DATA,CTRL)
- SELF-TIMED WRITE CYCLE
- THREE STATE COMMON I/O
- HIGH OUTPUT DRIVE CAPABILITY
- ASYNCHRONOUS OUTPUT ENABLE ($\overline{G}$)
- BURST CONTROL INPUTS: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$
- DUAL CHIP SELECTS FOR EASY DEPTH EXPANSION



PLCC44 (Q)

Figure 1. Pin Connection

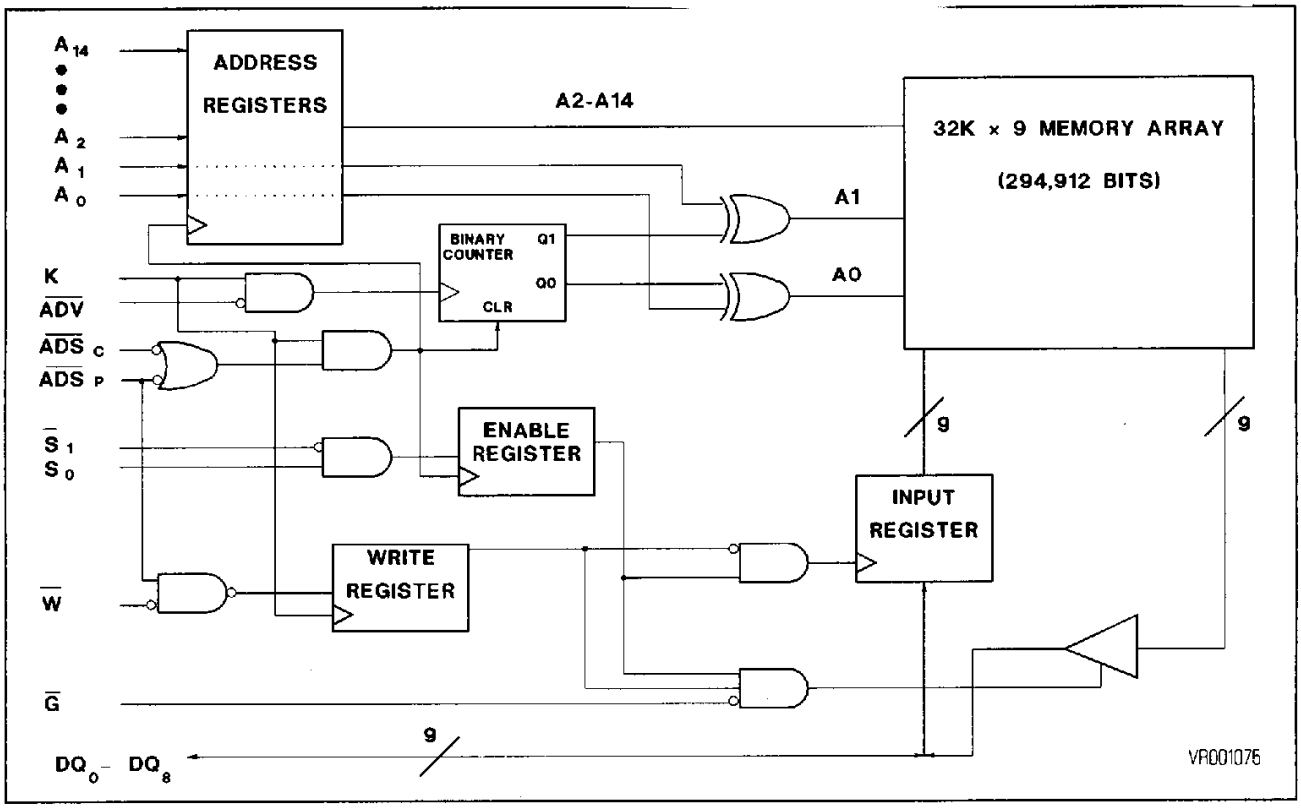


PIN NAMES

A0 - A14	Address Inputs
DQ0 - DQ8	Data Inputs/Outputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0	Chip Select, Active High
$\overline{S1}$	Chip Select, Active Low
$\overline{ADSP}$	Address Status Processor
$\overline{ADSC}$	Address Status Cache Ctrl.
$\overline{ADV}$	Burst Address Advance
$\overline{RES}$	Reserve, Tied Low
V_{CC}, GND	5 Volts, Ground

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Figure 2. Block Diagram S G S-THOMSON T-46-23-13



DESCRIPTION

The MK62486 BRAM™ is a 288K (294,912-bit) CMOS Burst SRAM, organized as 32,768 words x 9 bits. It is fabricated using SGS-Thomson's low power, high performance, CMOS technology. The device integrates a 2-bit burst counter, input registers, high output drive capability, and high speed synchronous SRAM onto a single chip. The syn-chronous design provides precise control using an external clock (K) input. The MK62486 is specifically adapted to provide a burstable, high performance secondary cache for the i486™ microprocessor.

The MK62486 is available in a 44 pin plastic leaded chip-carrier (PLCC). The device provides multiple power and ground pins to reduce effects induced by output noise for high performance applications. Separate power and ground pins (V_{CCQ} and GND_Q) have been employed for DQ_{0-8} to allow output levels referenced to 5 Volts or 3.3 Volts. The main Burst SRAM power requires a single 5V ± 5% supply, and all inputs and outputs are TTL compatible.

DEVICE OPERATIONS

Addresses (A0-A14), data inputs (DQ0-DQ8), and control signals, with exception of Output Enable ($\overline{G}$), are clock controlled inputs through non-inverting, pos-itive edge triggered registers. A cache burst address sequence can be initiated by either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Sta-tus Cache Controller) inputs, with subsequent burst addresses being internally generated by the Burst SRAM. The $\overline{ADV}$ input (burst address advance) provides control of the burst sequence, which imitates the i486 cache burst address sequence. Once a cache burst cycle begins, the subsequent burst address is generated internally each time the $\overline{ADV}$ input is asserted at the rising edge of the clock (K) input. The burst counter operates in the same manner for either cache burst write or read cycles.

The $\overline{ADSP}$ and the $\overline{ADSC}$ inputs control the start and the duration of the burst sequence respectively. Each time either address status input is asserted low, a new external base address is registered on the positive going edge of the clock (K).

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ASYNCHRONOUS TRUTH TABLE

Mode	$\overline{G}$	DQ Status
Read	L	Data Out
Read	H	High-Z
Write[2]	X	Data In (High-Z)
Deselect	X	High-Z

Notes :

1. X = Don't Care.
2. For a cache write cycle following a read operation, $\overline{G}$ must be high before the input data required set-up time, and be held high through the input data hold time.

BURST COUNT SEQUENCE

External Address	A14-A2	A1	A0
1st Burst Address	A14-A2	A1	$\overline{A0}$
2nd Burst Address	A14-A2	$\overline{A1}$	A0
3rd Burst Address	A14-A2	$\overline{A1}$	$\overline{A0}$

Note : The burst count sequence wraps around to the initial address after a full count is completed.

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SYNCHRONOUS TRUTH TABLE

S0	$\overline{S1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K	Address	Operation
L	X	L	X	X	X	↑	N/A	Deselected
X	H	H	L	X	X	↑	N/A	Deselected
H	L	L	X	X	X	↑	External Base Address	Read Cycle - Begin Burst
H	L	H	L	X	L	↑	External Base Address	Write Cycle - Extend Burst
H	L	H	L	X	H	↑	External Base Address	Read Cycle - Extend Burst
X	X	H	H	L	L	↑	Advance Burst Address	Write Cycle - Continue Burst Sequence
X	X	H	H	L	H	↑	Advance Burst Address	Read Cycle - Continue Burst Sequence
X	X	H	H	H	L	↑	Hold Current Burst Address	Write Cycle - Suspend Burst Sequence
X	X	H	H	H	H	↑	Hold Current Burst Address	Read Cycle - Suspend Burst Sequence

Notes :

1. X = Don't Care.
2. All inputs except $\overline{G}$ require set-up and hold times to the rising edge (low to high transition) of the external clock (K).
3. All read and write timings are referenced from $\overline{G}$ or K.
4. A read cycle is defined by $\overline{W}$ high or $\overline{ADSP}$ low for the required set-up and hold times. A write cycle is defined by $\overline{W}$ being asserted low for the set-up and hold times.
5. $\overline{G}$ is a don't care when $\overline{W}$ is registered low from the previous rising clock edge.
6. Chip Selects must be true (S0 = high, $\overline{S1}$ = low) at each rising of the clock while $\overline{ADSP}$ or $\overline{ADSC}$ is asserted for the device to remain enabled; Chip Selects are registered whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted low at the rising edge of the clock.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	–0.5 to 6	V
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
P_D	Power Dissipation	1.2	W
I_{OUT}	Output Current	20	mA

Notes :

1. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.
2. Output current absolute maximum rating is specified for one output at a time, not to exceed a duration of 1 second.

RECOMMENDED DC OPERATING CONDITIONS

(0 °C ≤ T_A ≤ +70 °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
GND	Ground	0	0	0	V
V_{IH}	Logic 1 All Inputs	2.2	3	V_{CC} + 0.3	V
V_{IL}	Logic 0 All Inputs	–0.3	0.2	0.8	V

DC ELECTRICAL CHARACTERISTICS

(0 °C ≤ T_A ≤ +70 °C; V_{CC} = 5V ± 5%)

Symbol	Parameter	Min.	Max.	Unit	Note
I_{CC1}	Average AC Power Supply Current ($\overline{G}$ = S0 = V_{IH}, $\overline{S1}$ = V_{IL}). All inputs = V_{IL} = 0V and V_{IH} ≥ 3V		160	mA	4
I_{SB}	TTL Standby Current (S0 = V_{IL}, $\overline{S1}$ = V_{IH})		40	mA	5
I_{SB1}	CMOS Standby Current (S0 ≤ 0.2V, $\overline{S1}$ ≥ V_{CC} – 0.2V)		30	mA	6
I_{LI}	Input Leakage Current (Any Input)	–1	1	µA	2
I_{LO}	Output Leakage Current	–1	1	µA	2
V_{OH}	Output Logic 1 Voltage (I_{OH} = –4.0mA)	2.4		V	1
V_{OL}	Output Logic 0 Voltage (I_{OL} = 8mA)		0.4	V	1

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CAPACITANCE
(T_A = 25 °C, f = 1MHz)

Symbol	Parameter	Typ.	Max.	Unit	Notes
C_I	Input Capacitance on all pins (except DQ)	4	5	pF	7
C_O	Output Capacitance	8	10	pF	3, 7

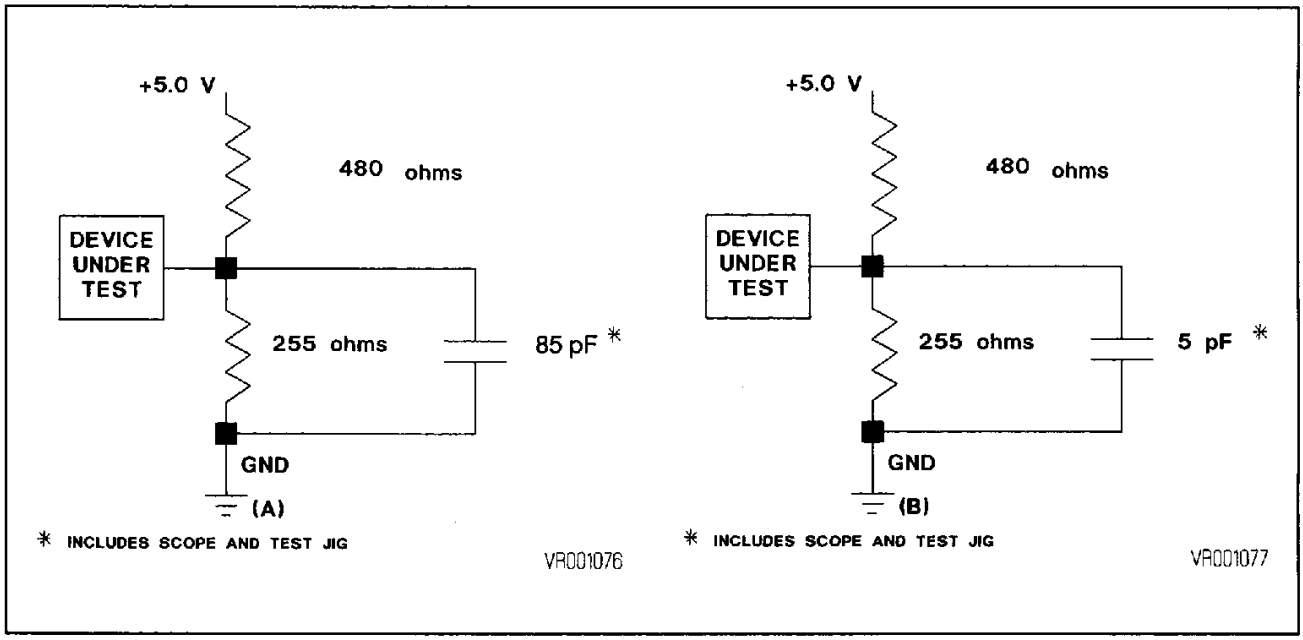
Notes :

1. All voltages referenced to GND.
2. Measured with GND ≤ V ≤ V_{CC} and outputs deselects.
3. Output buffers are deselected.
4. I_{CC1} measured as average AC current, with outputs open, V_{CC} max, t_{KHKH} min duty cycle 100%.
5. All other inputs at V_{IL} or V_{IH}, f = 0, V_{CC} max.
6. All other inputs ≥ V_{CC} – 0.2 or ≤ GND +0.2, f = 0, V_{CC} max.
7. Capacitances are sampled and not 100% tested.
8. For proper operation the $\overline{RES}$ input should be tied to ground.

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	1.5	ns
Input and Output Signal Timing Reference Level	1.5	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ± 15	%

Figure 3. Equivalent Output Load Circuits



READ/WRITE CYCLE TIMING - AC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	-19		-24		Unit	Note
		Min.	Max.	Min.	Max.		
t_{KHKH}	Cycle Time	25		30		ns	
t_{KHQV}	Clock Access Time		19		24	ns	1
t_{KHKL}	Clock High Pulse Width	9.5		11		ns	
t_{KLKH}	Clock Low Pulse Width	9.5		11		ns	
t_{GLQV}	Output Enable Access Time		8		9	ns	1
t_{KHQX}	Clock High to Output Active	3		3		ns	1
t_{GLQX}	Output Enable to Output Active	0		0		ns	2
t_{KHQX2}	Clock High to Q Active (Low-Z)	3		3		ns	2
t_{KHQZ}	Clock High to Q High-Z		12		15	ns	2
t_{GHQZ}	Output Disable to Q High-Z		8		9	ns	2
t_{AVKH}	Address Set-up Time	3		3		ns	3
t_{ADSVKH}	Address Status Set-up Time	3		3		ns	3
t_{DVKH}	Data In Set-up Time	3		3		ns	3
t_{WVKH}	Write/Read Set-up Time	3		3		ns	3
t_{ADVVKH}	Address Advance Set-up Time	3		3		ns	3
t_{S0VKH}	Chip Select 0 (S0) Set-up Time	3		3		ns	3
t_{S1VKH}	Chip Select 1 ($\overline{S1}$) Set-up Time	3		3		ns	3
t_{KHAX}	Address Hold Time	2		2		ns	3
t_{KHADSX}	Address Status Hold Time	2		2		ns	3
t_{KHDX}	Data In Hold Time	2		2		ns	3
t_{KHWX}	Write/Read Hold Time	2		2		ns	3
t_{KHADVX}	Address Advance Hold Time	2		2		ns	3
t_{KHS0X}	Chip Select 0 (S0) Hold Time	2		2		ns	3
t_{KHS1X}	Chip Select 1 ($\overline{S1}$) Hold Time	2		2		ns	3

Notes :

1. Measured with load as shown in Figure 3A.
2. Transition is measured ± 500 mV from steady-stage voltage with load as shown in Figure 3B. This parameter is sampled and not 100 % tested.
3. This is a synchronous device requiring that all inputs must meet the specified set-up and hold times with stable logic levels for all rising edges of the clock input (K).

DEVICE OPERATIONS (Continued)

When $\overline{ADSP}$ is asserted low, any ongoing burst cycle is interrupted, and a read operation (independent of $\overline{W}$ and $\overline{ADSC}$) is performed at the new registered external base address. A new burst cycle is initiated each time $\overline{ADSP}$ is asserted. By asserting $\overline{ADSC}$ low, the present burst cycle (initiated by $\overline{ADSP}$) is interrupted and an extended burst read or write (depending upon the logic state of $\overline{W}$ at the rising edge of K) is performed at the new registered base address. Chip selects (S0 and $\overline{S1}$) are only sampled when a new base address is loaded. Therefore, the chip selects are registered when either address status input is asserted low at the rising edge of the clock (K), and remain latched internally until the next assertion of either $\overline{ADSP}$ or $\overline{ADSC}$. The MK62486 Truth Tables and timing diagrams reference specific device operations.

It should be noted that the MK62486 allows a non-burst mode of operation where $\overline{ADSP}$ is the ADS# of the i486 processor in a 2-2 cycle mode of operation, and $\overline{ADSC}$ is held high during T2 (see Figure 4). However, the non-burst mode obviously negates the advantage of the internal burst counter for fast cache fill operations. In either mode (burst or non-burst), the write cycles are internally self-timed, and are initiated by the rising edge of the clock input. Self-timed write cycles eliminate complex off-chip write pulse generation providing more flexibility for incoming signals.

The $\overline{ADV}$ input controls subsequent burst data accesses after the first data of the burst cycle is processed. Each time $\overline{ADV}$ is asserted low for subsequent bursts at the rising edge of the clock input, the burst counter is advanced to the next burst address sequence. The address is advanced before the operation. Wait states can be inserted during burst cycles by holding the $\overline{ADV}$ pin high during positive clock transitions. Upon completion of the full internal burst count, the address will wrap-around to its initial base address

GENERAL APPLICATION

The MK62486 is organized using the ninth bit as the parity bit to support byte parity. Since the i486 processor provides on-board parity generation and checking, the ninth bit of the cache Burst SRAM can be passed to one of the DP0-DP3 pins of the microprocessor. Thus the MK62486 provides an architecture for building a 32K x 32-bit burstable data cache SRAM array, with byte parity, by using four devices in a 128K byte cache application.

Figure 4. General 128K Byte Cache Block Diagram

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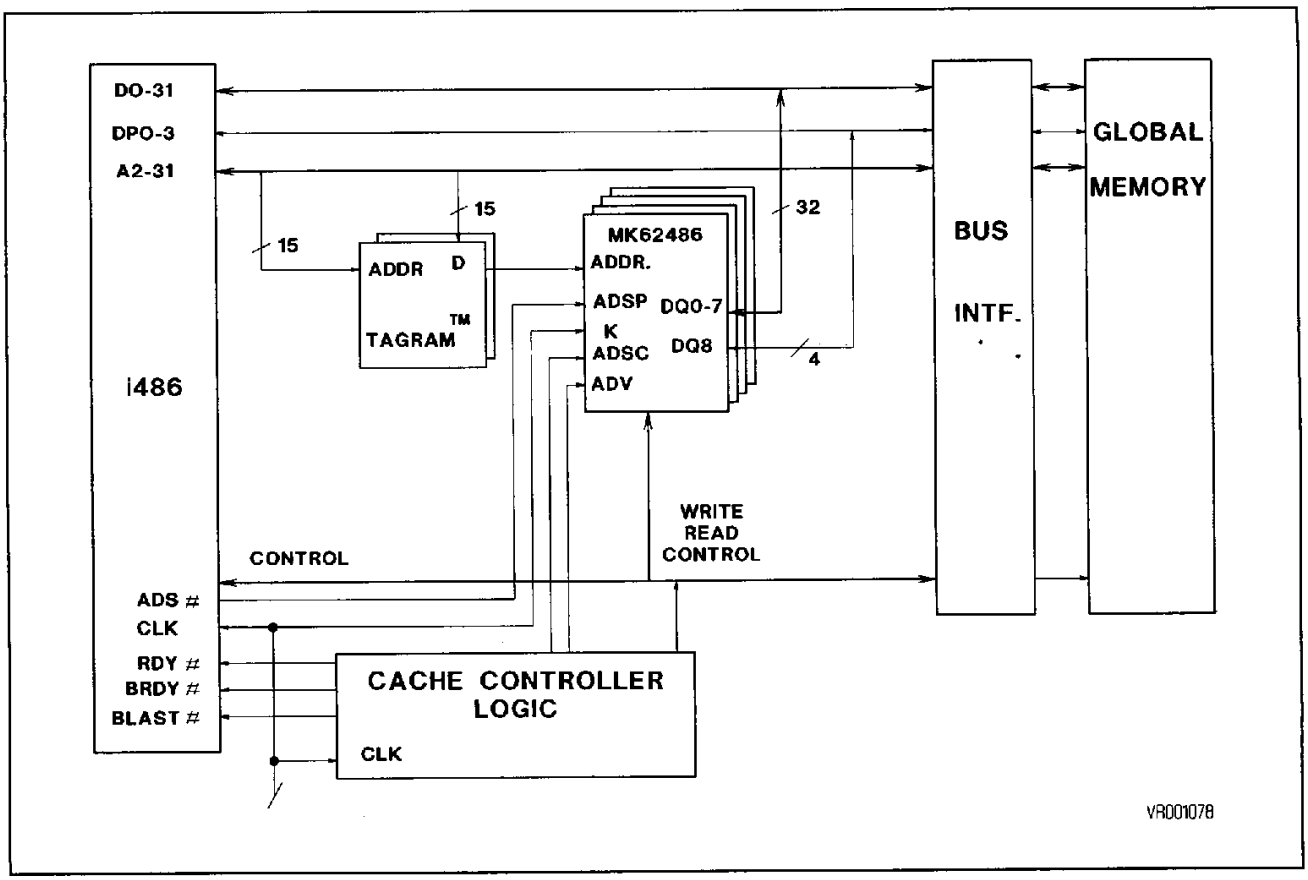

Figure 5. Non-Burst Read/Write 2-2 Cycles S G S-THOMSON T-46-23-13

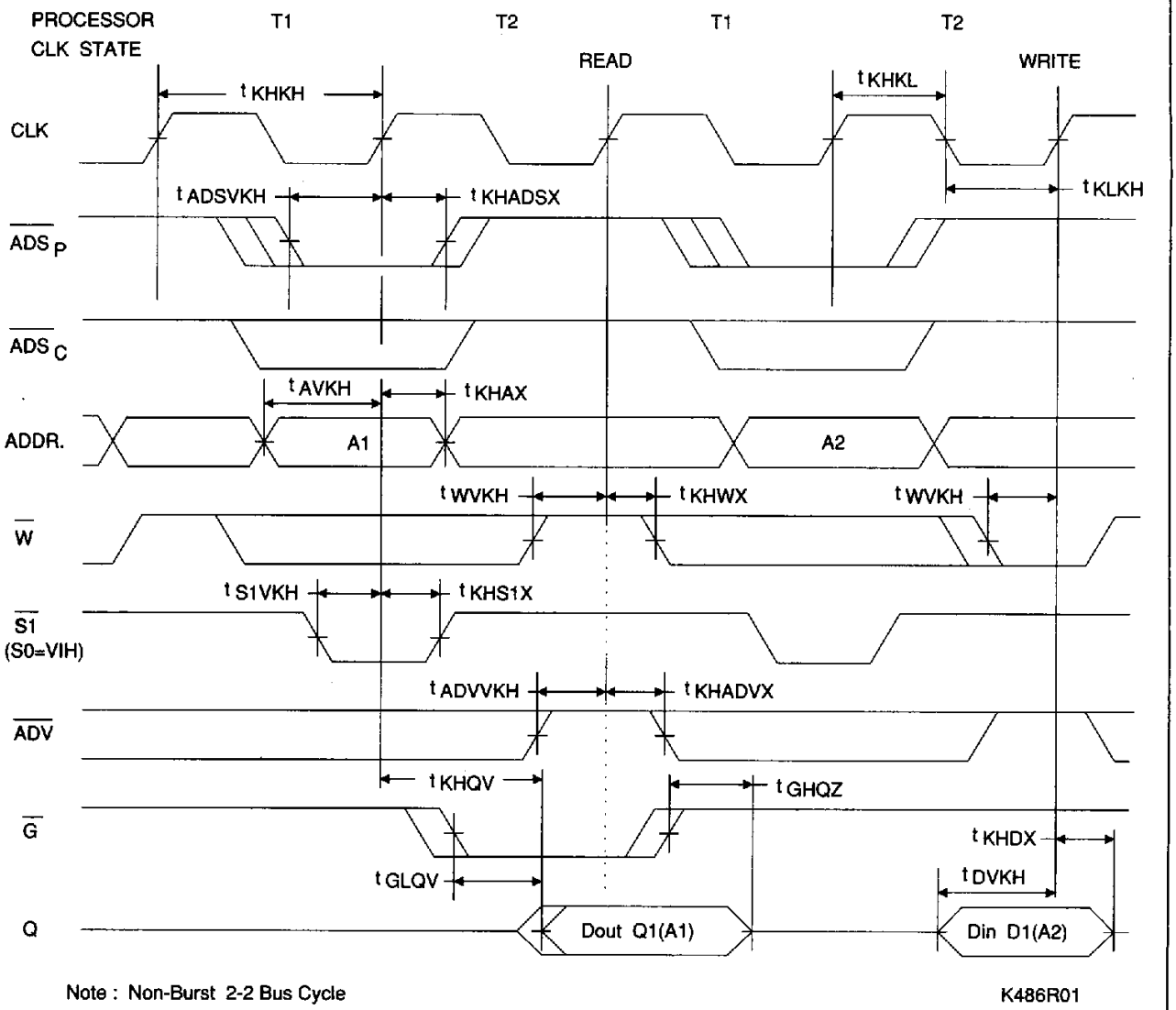

Figure 6. Burst Read Cycle

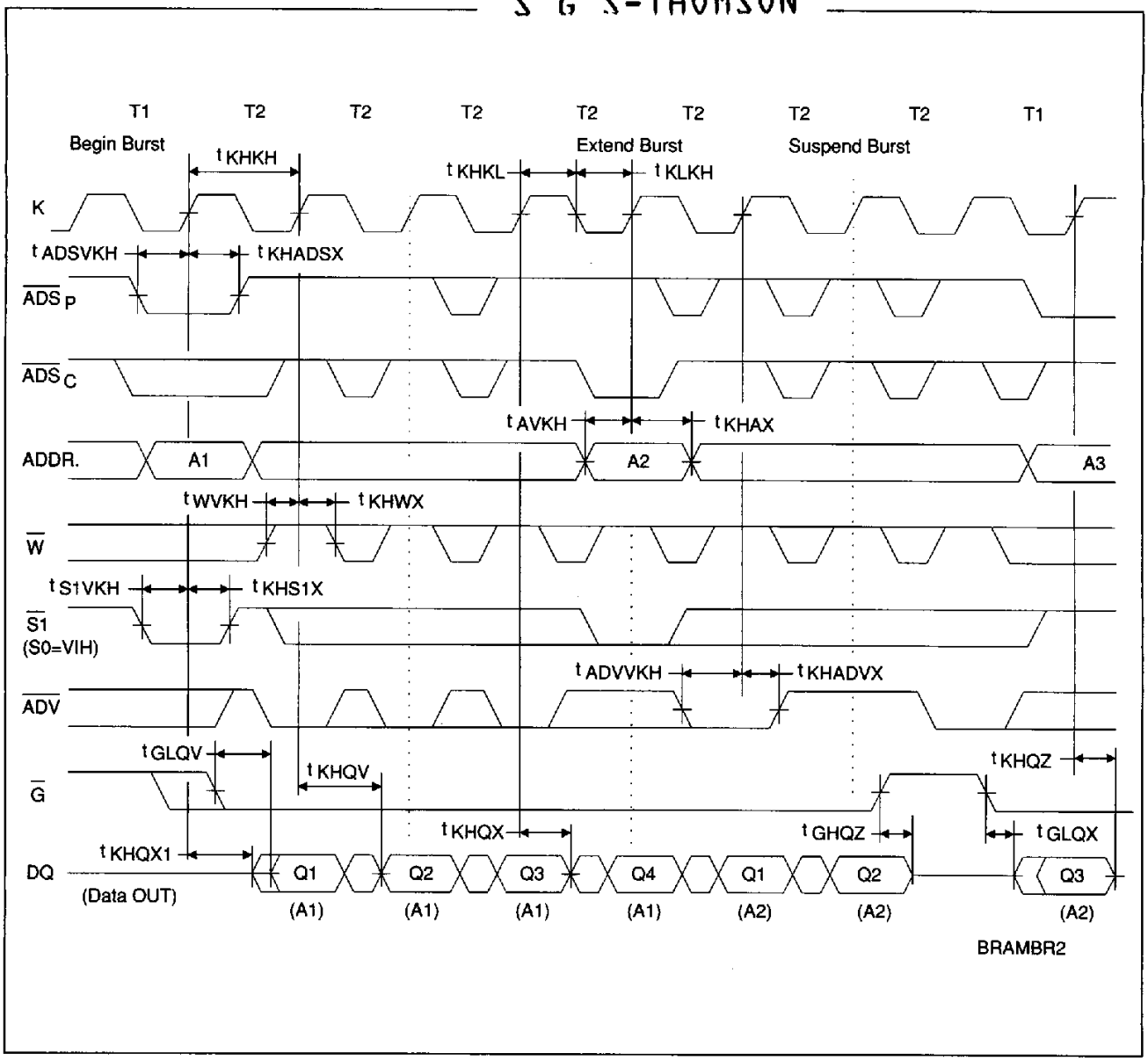

Figure 7. Burst Write Cycle

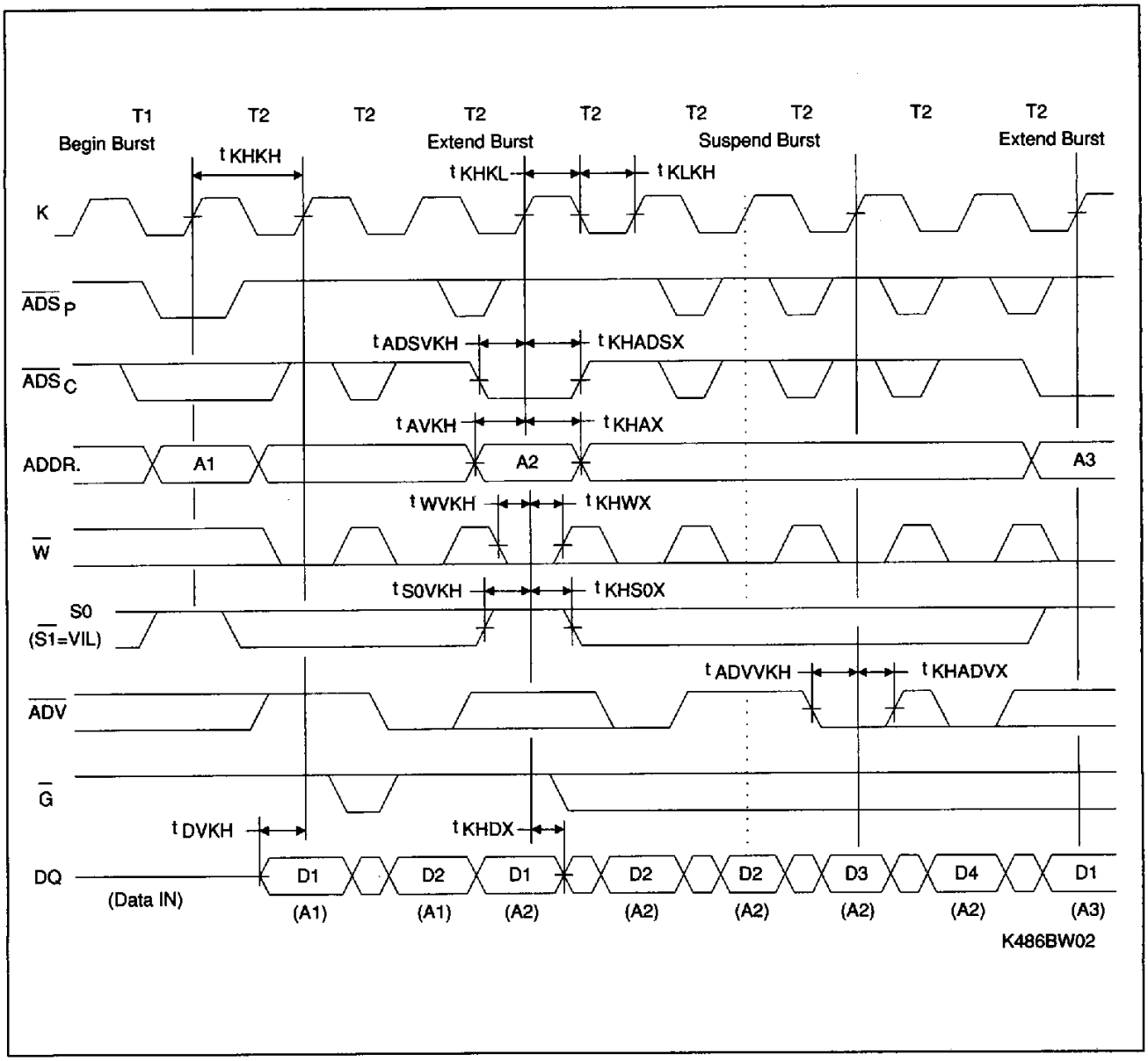

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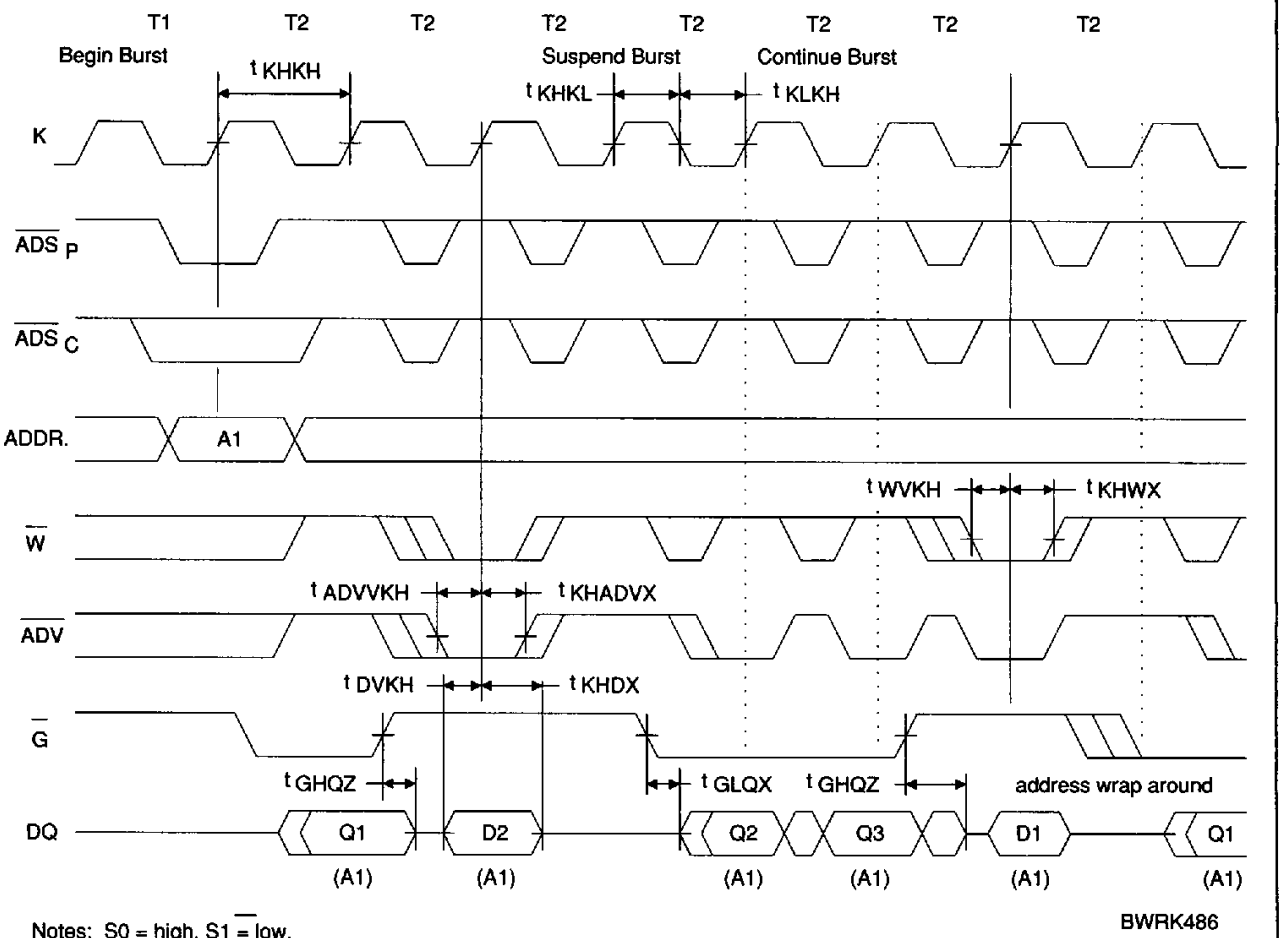
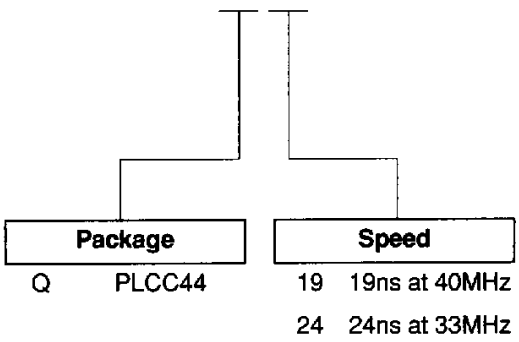
Figure 8. Combined Burst Read/Write Cycle



Notes: S0 = high, S1 = low.

ORDERING INFORMATION

Example: MK62486 Q 19



For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.