Virtex™-E 1.8 V Extended Memory Field Programmable Gate Arrays

DS025-1 (v1.4) April 2, 2001

Preliminary Product Specification

Features

- Fast, Extended Block RAM, 1.8 V FPGA Family
  - 560 Kb and 1,120 Kb embedded block RAM
  - 130 MHz internal performance (four LUT levels)
  - PCI compliant 3.3 V, 32/64-bit, 33/66-MHz
- Sophisticated SelectRAM+™ Memory Hierarchy
  - 294 Kb of internal configurable distributed RAM
  - Up to 1,120 Kb of synchronous internal block RAM
  - True Dual-Port™ block RAM
  - Memory bandwidth up to 2.24 Tb/s (equivalent bandwidth of over 100 RAMBUS channels)
  - Designed for high-performance Interfaces to external memories
    - 200 MHz ZBT* SRAMs
    - 200 Mb/s DDR SDRAMs
- Highly Flexible SelectIO+™ Technology
  - Supports 20 high-performance interface standards
  - Up to 556 singled-ended I/Os or up to 201 differential I/O pairs for an aggregate bandwidth of >100 Gb/s
- Complete Industry-Standard Differential Signalling Support
  - LVDS (622 Mb/s), BLVDS (Bus LVDS), LVPECL
  - Al I/O signals can be input, output, or bi-directional
  - LVPECL and LVDS clock inputs for 300+ MHz clocks
- Proprietary High-Performance SelectLink™ Technology
  - 80 Gb/s chip-to-chip communication link
  - Support for Double Data Rate (DDR) interface
  - Web-based HDL generation methodology
- Eight Fully Digital Delay-Locked Loops (DLLs)
- IEEE 1149.1 boundary-scan logic
- Supported by Xilinx Foundation Series™ and Alliance Series™ Development Systems
  - Internet Team Design (Xilinx iTD™) tool ideal for million-plus gate density designs
  - Wide selection of PC or workstation platforms
- SRAM-based In-System Configuration
  - Unlimited re-programmability
- Advanced Packaging Options
  - 1.0 mm FG676 and FG900
  - 1.27 mm BG560
- 0.18 µm 6-layer Metal Process with Copper Interconnect
- 100% Factory Tested

* ZBT is a trademark of Integrated Device Technology, Inc.

Introduction

The Virtex™-E Extended Memory (Virtex-EM) family of FPGAs is an extension of the highly successful Virtex-E family architecture. The Virtex-EM family (devices shown in Table 1) includes all of the features of Virtex-E, plus additional block RAM, useful for applications such as network switches and high-performance video graphic systems.

Xilinx developed the Virtex-EM product family to enable customers to design systems requiring high memory bandwidth, such as 160 Gb/s network switches. Unlike traditional ASIC devices, this family also supports fast time-to-market delivery, because the development engineering is already completed. Just complete the design and program the device. There is no NRE, no silicon production cycles, and no additional delays for design re-work. In addition, designers can update the design over a network at any time, providing product upgrades or updates to customers even sooner.

The Virtex-EM family is the result of more than fifteen years of FPGA design experience. Xilinx has a history of supporting customer applications by providing the highest level of logic, RAM, and features available in the industry. The Virtex-EM family, first FPGAs to deploy copper interconnect, offers the performance and high memory bandwidth for advanced system integration without the initial investment, long development cycles, and inventory risk expected in traditional ASIC development.

Table 1: **Virtex-E Extended Memory Field-Programmable Gate Array Family Members**

Device	Logic Gates	CLB Array	Logic Cells	Differential I/O Pairs	User I/O	BlockRAM Bits	Distributed RAM Bits
XCV405E	129,600	40 x 60	10,800	183	404	573,440	153,600
XCV812E	254,016	56 x 84	21,168	201	556	1,146,880	301,056

Virtex-E Compared to Virtex Devices

The Virtex-E family offers up to 43,200 logic cells in devices up to 30% faster than the Virtex family.

I/O performance is increased to 622 Mb/s using Source Synchronous data transmission architectures and synchronous system performance up to 240 MHz using singled-ended SelectI/O technology. Additional I/O standards are supported, notably LVPECL, LVDS, and BLVDS, which use two pins per signal. Almost all signal pins can be used for these new standards.

Virtex-E devices have up to 640 Kb of faster (250MHz) block SelectRAM, but the individual RAMs are the same size and structure as in the Virtex family. They also have eight DLLs instead of the four in Virtex devices. Each individual DLL is slightly improved with easier clock mirroring and 4x frequency multiplication.

V_{CCINT}, the supply voltage for the internal logic and memory, is 1.8 V, instead of 2.5 V for Virtex devices. Advanced processing and 0.18 µm design rules have resulted in smaller dice, faster speed, and lower power consumption.

I/O pins are 3 V tolerant, and can be 5 V tolerant with an external 100 Ω resistor. PCI 5 V is not supported. With the addition of appropriate external resistors, any pin can tolerate any voltage desired.

Banking rules are different. With Virtex devices, all input buffers are powered by V_{CCINT}. With Virtex-E devices, the LVTTL, LVCMOS2, and PCI input buffers are powered by the I/O supply voltage V_{CCO}.

The Virtex-E family is not bitstream-compatible with the Virtex family, but Virtex designs can be compiled into equivalent Virtex-E devices.

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions. See the data sheet pinout section for details.

General Description

The Virtex-E FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 6-layer metal 0.18 µm CMOS process. These advances make Virtex-E FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex-E family includes the nine members in Table 1.

Building on experience gained from Virtex FPGAs, the Virtex-E family is an evolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex-E family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Virtex-E Architecture

Virtex-E devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. The abundance of routing resources permits the Virtex-E family to accommodate even the largest and most complex designs.

Virtex-E FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. Configuration data can be read from an external SPROM (master serial mode), or can be written into the FPGA (SelectMAP™, slave serial, and JTAG modes).

The standard Xilinx Foundation Series™ and Alliance Series™ Development systems deliver complete design support for Virtex-E, covering every aspect from behavioral and schematic entry, through simulation, automatic design translation and implementation, to the creation and downloading of a configuration bit stream.

Higher Performance

Virtex-E devices provide better performance than previous generations of FPGAs. Designs can achieve synchronous system clock rates up to 240 MHz including I/O or 622 Mb/s using Source Synchronous data transmission architechtures. Virtex-E I/Os comply fully with 3.3 V PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz.

While performance is design-dependent, many designs operate internally at speeds in excess of 133 MHz and can achieve over 311 MHz. Table 2, page 3, shows performance data for representative circuits, using worst-case timing parameters.

Table 2: **Performance for Common Circuit Functions**

Function	Bits	Virtex-E -7
Register-to-Register		
Adder	16 64	4.3 ns 6.3 ns
Pipelined Multiplier	8 x 8 16 x 16	4.4 ns 5.1 ns
Address Decoder	16 64	3.8 ns 5.5 ns
16:1 Multiplexer		4.6 ns
Parity Tree	9 18 36	3.5 ns 4.3 ns 5.9 ns
Chip-to-Chip		
HSTL Class IV		
LVTTL,16mA, fast slew		
LVDS		
LVPECL		

Virtex-E Extended Memory Device/Package Combinations and Maximum I/O

Table 3: **Virtex-EM Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)**

Package	XCV405E	XCV812E
BG560	404	404
FG676	404	
FG900		556

Virtex-E Extended Memory Ordering Information

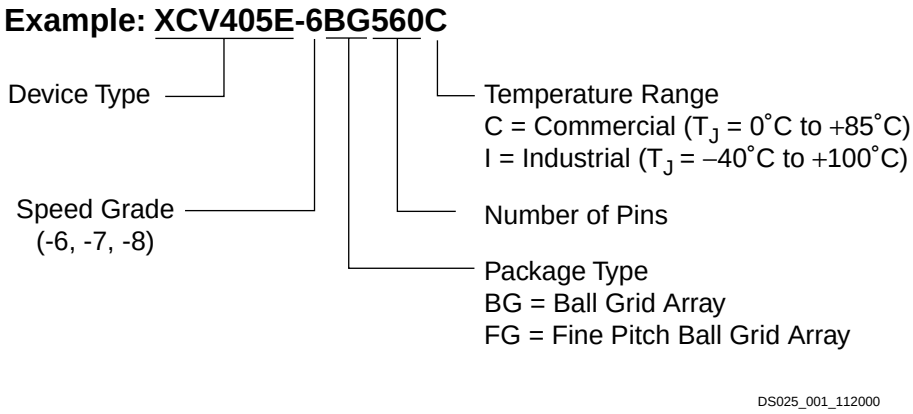

Figure 1: **Virtex Ordering Information**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/23/00	1.0	Initial Xilinx release.
08/01/00	1.1	Accumulated edits and fixes. Upgrade to Preliminary. Preview -8 numbers added. Reformatted to adhere to corporate documentation style guidelines. Minor changes in BG560 pin-out table.
09/19/00	1.2	• In Table 3 (Module 4), **FG676 Fine-Pitch BGA — XCV405E**, the following pins are no longer labeled as VREF: B7, G16, G26, W26, AF20, AF8, Y1, H1. • Min values added to **Virtex-E Electrical Characteristics** tables.
11/20/00	1.3	• Updated speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables (Module 3). • Updated minimums in Table 11 (Module 2), and added notes to Table 12 (Module 2). • Added to note 2 of **Absolute Maximum Ratings** (Module 3). • Changed all minimum hold times to –0.4 for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL** (Module 3). • Revised maximum T_{DLLPW} in -6 speed grade for **DLL Timing Parameters** (Module 3).
04/02/01	1.4	• In Table 4, **FG676 Fine-Pitch BGA — XCV405E**, pin B19 is no longer labeled as VREF, and pin G16 is now labeled as VREF. • Updated values in **Virtex-E Switching Characteristics** tables. • Converted data sheet to modularized format. See **Virtex-E Extended Memory Data Sheet**, below.

Virtex-E Extended Memory Data Sheet

The Virtex-E Extended Memory Data Sheet contains the following modules:

- DS025-1, Virtex-E 1.8V Extended Memory FPGAs: **Introduction and Ordering Information (Module 1)**
- DS025-2, Virtex-E 1.8V Extended Memory FPGAs: **Functional Description (Module 2)**
- DS025-3, Virtex-E 1.8V Extended Memory FPGAs: **DC and Switching Characteristics (Module 3)**
- DS025-4, Virtex-E 1.8V Extended Memory FPGAs: **Pinout Tables (Module 4)**