DSP56F826

Preliminary Technical Data

DSP56F826 16-bit Digital Signal Processor

- Up to 40 MIPS at 80MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- Hardware DO and REP loops
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 31.5K × 16-bit words Program Flash
- 512 × 16-bit words Program RAM
- 2K × 16-bit words Data Flash
- 4K × 16-bit words Data RAM
- 2K × 16-bit words BootFLASH
- Up to 64K × 16-bit words each of external memory expansion for Program and Data memory
- One Serial Port Interface (SPI)
- One additional SPI or two optional Serial Communication Interfaces (SCI)
- One Synchronous Serial Interface (SSI)
- One General Purpose Quad Timer
- JTAG/OnCE™ for debugging
- 100-pin LQFP Package
- 16 dedicated and 30 shared GPIO
- One Time-of-Day module

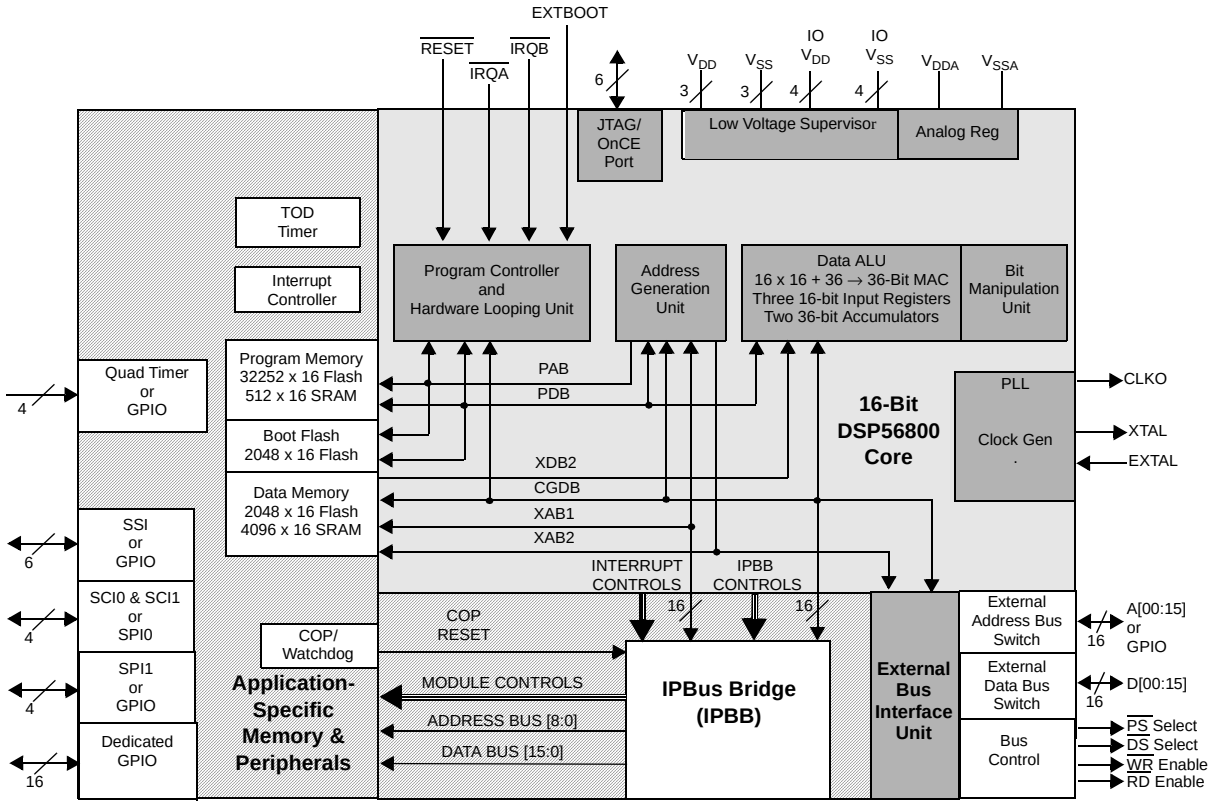

Figure 1. DSP56F826 Block Diagram

Digital DNA™ From Motorola

Part 1 Overview

1.1 DSP56F826 Features

1.1.1 Digital Signal Processing Core

- Efficient 16-bit DSP56800 Family DSP engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators, including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE Debug Programming Interface

1.1.2 Memory

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory including a low cost, high volume flash solution
  - 31.5K × 16-bit words of Program Flash
  - 512 × 16-bit words of Program RAM
  - 2K × 16-bit words of Data Flash
  - 4K × 16-bit words of Data RAM
  - 2K × 16-bit words of BootFLASH
- Off-chip memory expansion capabilities programmable for 0, 4, 8, or 12 wait states
  - As much as 64 K × 16-bit data memory
  - As much as 64 K × 16-bit program memory

1.1.3 Peripheral Circuits for DSP56F826

- One General Purpose Quad Timer totalling 7pins
- One Serial Peripheral Interface with 4 pins (or four additional GPIO lines)
- One Serial Peripheral Interface, or multiplexed with two Serial Communications Interfaces totalling 4 pins
- Synchronous Serial Interface (SSI) with configurable six-pin port (or six additional GPIO lines)

- Sixteen (16) dedicated general purpose I/O (GPIO) pins
- Thirty (30) shared general purpose I/O (GPIO) pins
- Computer-Operating Properly (COP) Watchdog timer
- Two external interrupt pins
- External reset pin for hardware reset
- JTAG/On-Chip Emulation (OnCE™) for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based frequency synthesizer for the DSP core clock
- Fabricated in high-density EMOS with 5V tolerant, TTL-compatible digital inputs
- One Time of Day module

Energy Information

- Dual power supply, 3.3V and 2.5V
- Wait and Multiple Stop modes available

1.2 DSP56F826 Description

The DSP56F826 is a member of the DSP56800 core-based family of Digital Signal Processors (DSPs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution for general purpose applications. Because of its low cost, configuration flexibility, and compact program code, the DSP56F826 is well-suited for many applications. The DSP56F826 includes many peripherals that are especially useful for applications such as: noise suppression, ID tag readers, sonic/subsonic detectors, security access devices, remote metering, sonic alarms, POS terminals, feature phones.

The DSP56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C/C++ Compilers to enable rapid development of optimized control applications.

The DSP56F826 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The DSP56F826 also provides two external dedicated interrupt lines, and up to 46 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The DSP56F826 DSP controller includes 31.5K words (16-bit) of Program Flash and 2K words of Data Flash (each programmable through the JTAG port) with 512 words of Program RAM, and 4K words of Data RAM. It also supports program execution from external memory.

The DSP56F826 incorporates a total of 2K words of BootFLASH for easy customer-inclusion of field-programmable software routines that can be used to program the main Program and Data Flash memory areas. Both Program and Data Flash memories can be independently bulk-erased or erased in page sizes of 256 words. The BootFLASH memory can also be either bulk- or page-erased.

This DSP controller also provides a full set of standard programmable peripherals including one Synchronous Serial Interface (SSI), one Serial Peripheral Interface (SPI), the option to select a second SPI or two Serial Communications Interfaces (SCIs), and one Quad Timer. The SSI, SPI, and quad timer can be used as General Purpose Input/Outputs (GPIOs) if a timer function is not required.

1.3 *Best in Class* Development Environment

The SDK (Software Development Kit) provides fully debugged peripheral drivers, libraries and interfaces that allow programmers to create their unique C application code independent of component architecture. The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, the SDK, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in **Table 1** are required for a complete description and proper design with the DSP56F826. Documentation is available from local Motorola distributors, Motorola semiconductor sales offices, Motorola Literature Distribution Centers, or online at www.motorola.com/semiconductors/.

Table 1. DSP56F826 Chip Documentation

Topic	Description	Order Number
DSP56800 Family Manual	Detailed description of the DSP56800 family architecture, and 16-bit DSP core processor and the instruction set	DSP56800FM/D
DSP56824/F826/F827 User's Manual	Detailed description of memory, peripherals, and interfaces of the DSP56824, DSP56F826, DSP56F827	TBD
DSP56F826 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56F826/D
DSP56F826 Product Brief	Summary description and block diagram of the DSP56F826 core, memory, peripherals and interfaces	DSP56F826PB/D

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for VIL, VOL, VIH, and VOH are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the DSP56F826 are organized into functional groups, as shown in **Table 2** and as illustrated in **Figure 2.** In **Table 3** describes the signal or signals present on a pin.

Table 2. Functional Group Pin Allocations

Functional Group	Number of Pins
Power (V_{DD} , V_{DDIO} or V_{DDA})	(3,4,1)
Ground (V_{SS} , V_{SSIO} or V_{SSA})	(3,4,1)
PLL and Clock	3
Address Bus[1]	16
Data Bus	16
Bus Control	4
Interrupt and Program Control	5
Dedicated General Purpose Input/Output	16
Synchronous Serial Interface (SSI) Port	6
Serial Peripheral Interface (SPI) Port[1]	4
Serial Communications Interface (SCI) Ports	4
Quad Timer Module Ports	4
JTAG/On-Chip Emulation (OnCE)	6

1. Alternately, GPIO pins

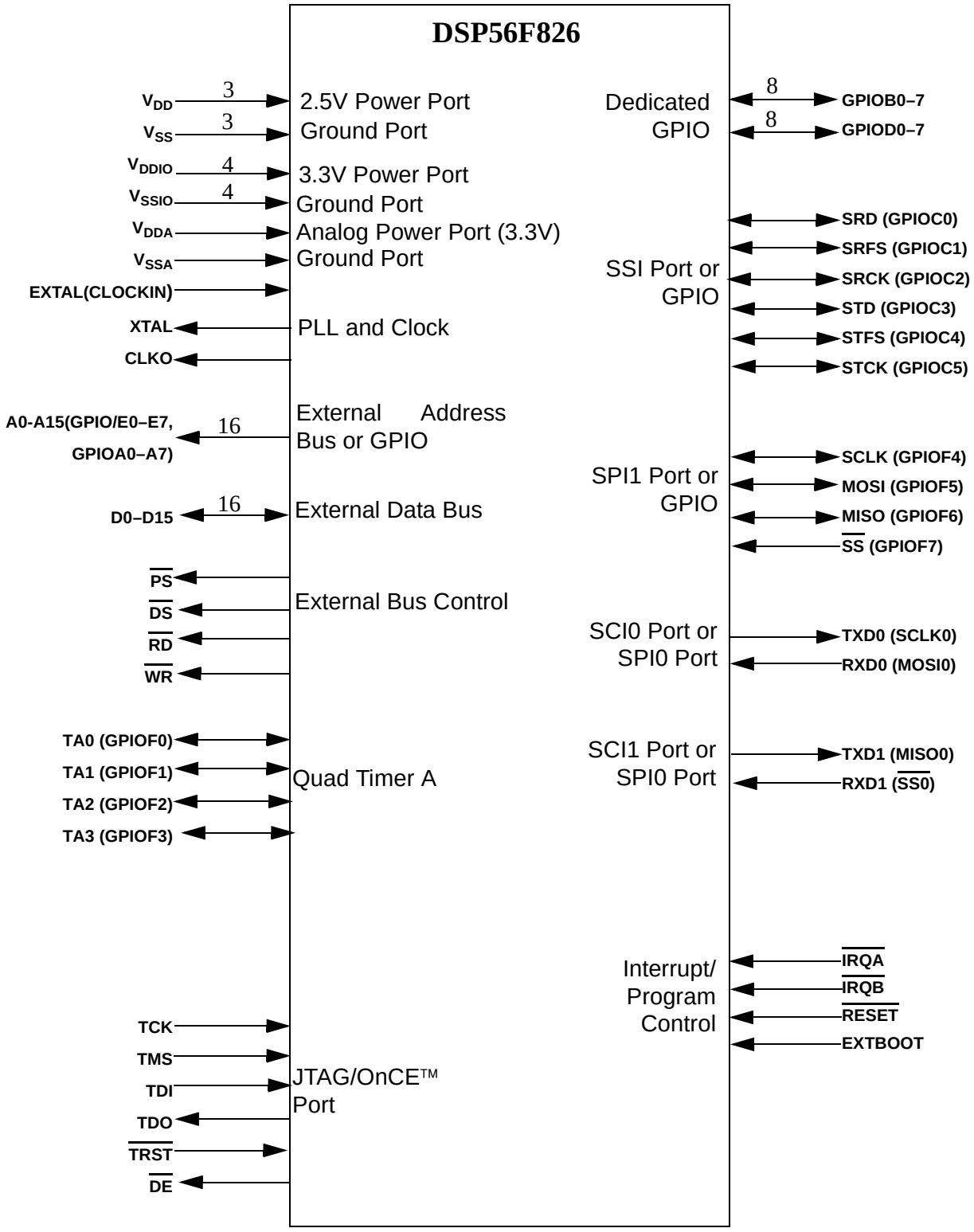

Figure 2. DSP56F826 Signals Identified by Functional Group[1]

1. Alternate pin functionality is shown in parenthesis.

Table 3. DSP56F826 Signal and Package Information for the 100 Pin LQFP

All inputs have a weak internal pull-up circuit associated with them. These pull-up circuits are **always enabled**. Exceptions:

1. When a pn is owned by GPIO, then the pull-up may be disabled under software control.
2. TCK has a weak pull-down circuit always active.

Signal Name	Pin No.	Type	Description
A0	24	Output	**Address Bus**—A0–A7 specify the address for external program or data memory accesses.
A1	23	Output	
A2	22	Output	
A3	21	Output	
A4	18	Output	
A5	17	Output	
A6	16	Output	
A7 GPIOE0–GPIOE7	15	Output Input/Output	**Port E GPIO**—These eight General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is Address Bus.
A8	14	Output	**Address Bus**—A8–A15 specify the address for external program or data memory accesses.
A9	13	Output	
A10	12	Output	
A11	11	Output	
A12	10	Output	
A13	9	Output	
A14	8	Output	
A15 GPIOA0–GPIOA7	7	Output Input/Output	**Port A GPIO**—These eight General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is Address Bus.

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Signal Name	Pin No.	Type	Description
CLKO	65	Output	**Clock Output**—This pin outputs a buffered clock signal. By programming the CLKO Select Register (SLKOSR), the user can select between outputting a version of the signal applied to XTAL and a version of the DSP master clock at the output of the PLL. The clock frequency on this pin can be disabled by programming the CLKO Select Register (CLKOSR).
D0	34	Input/Output	**Data Bus**— D0–D15 specify the data for external program or data memory accesses. D0–D15 are tri-stated when the external bus is inactive.
D1	35		
D2	36		
D3	37		
D4	38		
D5	39		
D6	40		
D7	41		
D8	42		
D9	43		
D10	44		
D11	46		
D12	47		
D13	48		
D14	49		
D15	50		
$\overline{DE}$	98	Output	**Debug Event**—$\overline{DE}$ provides a low pulse on recognized debug events.
$\overline{DS}$	28	Output	**Data Memory Select**—$\overline{DS}$ is asserted low for external data memory access.

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Signal Name	Pin No.	Type	Description
EXTAL	61	Input	**External Crystal Oscillator Input**—This input can be connected to an 4MHz external crystal. If a 4MHz or less external clock source is used, EXTAL can be used as the input and XTAL must not be connected. For more information, please refer to **Section 3.5.2.**
CLOCKIN		Input	**External Clock Input**—This input can be connected to an external 8MHz clock. For more information, please refer to **Section 3.5.** The input clock can be selected to provide the clock directly to the DSP core. This input clock can also be selected as input clock for the on-chip PLL.
EXTBOOT	25	Input	**External Boot**—This input is tied to V_{DD} to force device to boot from off-chip memory. Otherwise, it is tied to ground.
GPIOB0	66	Input or Output	**Port B GPIO**—These eight dedicated General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is GPIO input.
GPIOB1	67		
GPIOB2	68		
GPIOB3	69		
GPIOB4	70		
GPIOB5	71		
GPIOB6	72		
GPIOB7	73		
GPIOD0	74	Input or Output	**Port D GPIO**—These eight dedicated GPIO pins can be individually programmed as an input or output pins. After reset, the default state is GPIO input.
GPIOD1	75		
GPIOD2	76		
GPIOD3	77		
GPIOD4	78		
GPIOD5	79		
GPIOD6	82		
GPIOD7	83		

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Signal Name	Pin No.	Type	Description
$\overline{\text{IRQA}}$	32	Input	**External Interrupt Request A**—The $\overline{\text{IRQA}}$ input is a synchronized external interrupt request that indicates that an external device is requesting service. It can be programmed to be level-sensitive or negative-edge- triggered. If level-sensitive triggering is selected, an external pull up resistor is required for wired-OR operation. If the processor is in the Stop state and $\overline{\text{IRQA}}$ is asserted, the processor will exit the Stop state.
$\overline{\text{IRQB}}$	33	Input	**External Interrupt Request B**—The $\overline{\text{IRQB}}$ input is an external interrupt request that indicates that an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered. If level-sensitive triggering is selected, an external pull up resistor is required for wired-OR operation.
MISO	86	Input/Output	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
GPIOF6		Input/Output	**Port F GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as input or output. After reset, the default state is MISO.
MOSI	85	Input/Output	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.
GPIOF5		Input/Output	**Port F GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as input or output.
$\overline{\text{PS}}$	29	Output	**Program Memory Select**—$\overline{\text{PS}}$ is asserted low for external program memory access.
$\overline{\text{RD}}$	26	Output	**Read Enable**—$\overline{\text{RD}}$ is asserted during external memory read cycles. When $\overline{\text{RD}}$ is asserted low, pins D0–D15 become inputs and an external device is enabled onto the DSP data bus. When $\overline{\text{RD}}$ is deasserted high, the external data is latched inside the DSP. When $\overline{\text{RD}}$ is asserted, it qualifies the A0–A15, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ pins. $\overline{\text{RD}}$ can be connected directly to the $\overline{\text{OE}}$ pin of a Static RAM or ROM.

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All inputs have a weak internal pull-up circuit associated with them. These pull-up circuits are **always enabled**. Exceptions:

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Signal Name	Pin No.	Type	Description
$\overline{\text{RESET}}$	45	Input	**Reset**—This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the DSP is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the external boot pin. The internal reset signal will be deasserted synchronous with the internal clocks, after a fixed number of internal clocks. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware DSP reset is required and it is necessary not to reset the OnCE/ JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.
RXD0 MOSI0	96	Input Input/ Output	**Receive Data (RXD0)**— receive data input **SPI Master Out/Slave In**—This serial data pin is an output from a master device, and an input to a slave device. The master device places data on the MOSI line one half-cycle before the clock edge the slave device uses to latch the data. After reset, the default state is SCI input.
RXD1 $\overline{\text{SS0}}$	92	Input Input	**Receive Data (RXD1)**— receive data input **SPI Slave Select**—In maste mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave. After reset, the default state is SCI input.
SCLK GPIOF4	84	Input/Output Input/Output	**SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. **Port F GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as input or output. After reset, the default state is SCLK.
SRCK GPIOC2	53	Input/Output Input/Output	**SSI Serial Receive Clock (STCK)—**This bidirectional pin provides the serial bit rate clock for the Receive section of the SSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode. **Port C GPIO—**This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.

Table 3. DSP56F826 Signal and Package Information for the 100 Pin LQFP

All inputs have a weak internal pull-up circuit associated with them. These pull-up circuits are **always enabled**. Exceptions:

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Signal Name	Pin No.	Type	Description
SRD	51	Input/Output	**SSI Receive Data (SRD)—**This input pin receives serial data and transfers the data to the SSI Receive Shift Receiver.
GPIOC0		Input/Output	**Port C GPIO**—This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.
SRFS	52	Input/ Output	**SSI Serial Receive Frame Sync (SRFS)—**This bidirectional pin is used by the receive section of the SSI as frame sync I/O or flag I/O. The STFS can be used only by the receiver. It is used to synchronize data transfer and can be an input or an output.
GPIOC1		Input/Output	**Port C GPIO**—This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.
$\overline{SS}$	87	Input	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave.
GPIOF7		Input/Output	**Port F GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as input or output. After reset, the default state is $\overline{SS}$.
STCK	56	Input/ Output	**SSI Serial Transmit Clock (STCK)—**This bidirectional pin provides the serial bit rate clock for the transmit section of the SSI. The clock signal can be continuous or gated. It can be used by both the transmitter and receiver in synchronous mode.
GPIOC5		Input/Output	**Port C GPIO—**This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.
STD	54	Output	**SSI Transmit Data (STD)—**This output pin transmits serial data from the SSI Transmitter Shift Register.
GPIOC3		Input/Output	**Port C GPIO—**This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.

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All inputs have a weak internal pull-up circuit associated with them. These pull-up circuits are **always enabled**. Exceptions:

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2. TCK has a weak pull-down circuit always active.

Signal Name	Pin No.	Type	Description
STFS	55	Input	**SSI Serial Transmit Frame Sync (STFS)—**This bidirectional pin is used by the Transmit section of the SSI as frame sync I/O or flag I/O. The STFS can be used by both the transmitter and receiver in synchronous mode. It is used to synchronize data transfer and can be an input or output pin.
GPIOC4		Input/Output	**Port C GPIO—**This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.
$\overline{\text{TA0-3}}$	91	Input/Output	**TA0–3**—Timer F Channels 0, 1, 2, and 3
GPIOF0-GPIOF3	90 89 88	Input/Output	**Port F GPIO**—These four General Purpose I/O (GPIO) pins can be individually programmed as input or output. After reset, the default state is Quad Timer.
TCS	99		**TCS**—This pin is reserved for factory use. It must be tied to V_{SS} for normal use. In block diagrams, this pin is considered an additional V_{SS}.
TCK	100	Input	**Test Clock Input**—This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
TDI	2	Input	**Test Data Input**—This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
TDO	3	Output	**Test Data Output**—This tri-statable output pin provides a serial output data stream from the JTAG/OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
TMS	1	Input	**Test Mode Select Input**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
$\overline{\text{TRST}}$	4	Input	**Test Reset**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment when a hardware DSP reset is required and it is necessary not to reset the JTAG/OnCE module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.

Table 3. DSP56F826 Signal and Package Information for the 100 Pin LQFP

All inputs have a weak internal pull-up circuit associated with them. These pull-up circuits are **always enabled**. Exceptions:

1. When a pn is owned by GPIO, then the pull-up may be disabled under software control.
2. TCK has a weak pull-down circuit always active.

Signal Name	Pin No.	Type	Description
TXD0 SCLK0	97	Output Input/Output	**Transmit Data (TXD0)**—transmit data output **SPI Serial Clock—**In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. After reset, the default state is SCI output.
TXD1 MISO0	93	Output Input/Output	**Transmit Data (TXD1)**—transmit data output **SPI Master In/Slave Out—**This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if hte slave device is not selected. After reset, the default state is SCI output.
V_{DD}	20	V_{DD}	**Power**—These pins provide power to the internal structures of the chip, and are generally connected to a 2.5V supply.
V_{DD}	64	V_{DD}	
V_{DD}	94	V_{DD}	
V_{DDA}	59	V_{DDA}	**Analog Power**—This pin supplies an analog power source (generally 2.5V).
V_{DDIO}	5	V_{DDIO}	**Power**—These pins provide power to the I/O structures of the chip, and are generally connected to a 3.3V supply.
V_{DDIO}	30	V_{DDIO}	
V_{DDIO}	57	V_{DDIO}	
V_{DDIO}	80	V_{DDIO}	
V_{SS}	19	V_{SS}	**GND**—These pins provide grounding for the internal structures of the chip. All should be attached to V_{SS}.
V_{SS}	63	V_{SS}	
V_{SS}	95	V_{SS}	
V_{SSA}	60	V_{SSA}	**Analog Ground**—This pin supplies an analog ground.
V_{SSIO}	6	V_{SSIO}	**GND In/Out**—These pins provide grounding for the I/O ring on the chip. All should be attached to V_{SS}.
V_{SSIO}	31	V_{SSIO}	
V_{SSIO}	58	V_{SSIO}	
V_{SSIO}	81	V_{SSIO}	

Table 3. DSP56F826 Signal and Package Information for the 100 Pin LQFP

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2. TCK has a weak pull-down circuit always active.

Signal Name	Pin No.	Type	Description
$\overline{WR}$	27	Output	**Write Enable**—$\overline{WR}$ is asserted during external memory write cycles. When $\overline{WR}$ is asserted low, pins D0–D15 become outputs and the DSP puts data on the bus. When $\overline{WR}$ is deasserted high, the external data is latched inside the external device. When $\overline{WR}$ is asserted, it qualifies the A0–A15, $\overline{PS}$, and $\overline{DS}$ pins. $\overline{WR}$ can be connected directly to the $\overline{WE}$ pin of a Static RAM.
XTAL	62	Output	**Crystal Oscillator Output**—This output connects the internal crystal oscillator output to an external crystal. If an external clock source over 4MHz is used, XTAL must be used as the input and EXTAL connected to V_{SS}. For more information, please refer to **Section 3.5.2.**

Part 3 Specifications

3.1 General Characteristics

The DSP56F826 is fabricated in high-density CMOS with 5-volt tolerant TTL-compatible digital inputs. The term *5-volt tolerant* refers to the capability of an I/O pin, built on a 3.3V compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V- compatible I/O voltage levels. A standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage. This 5V tolerant capability, therefore, offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 4** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The DSP56F826 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either or V_{DD} or V_{SS}).

Table 4. Absolute Maximum Ratings (V_{SS} = 0 V)

Characteristic	Symbol	Min	Max	Unit
Supply voltage, core	V_{DD}	V_{SS} – 0.3	3.0	V
Supply voltage, IO and analog	V_{DDIO}	V_{SS} – 0.3	4.0	V
All other input voltages	V_{IN}	V_{SS} – 0.3	V_{DDIO} + 0.3	V
Current drain per pin excluding V_{DD}, V_{SS}	I	—	10	mA
Junction temperature	T_J	—	150	°C
Storage temperature range	T_{STG}	–55	150	°C

Table 5. Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Supply voltage, core	V_{DD}	2.25	2.75	V
Supply Voltage, IO and analog	V_{DDIO}, V_{DDA}	3.0	3.6	V
Ambient operating temperature	T_A	–40	85	°C
Flash program/erase temperature	T_F	0	85	°C

Table 6. Thermal Characteristics[1]

Characteristic	100-pin LQFP		
	Symbol	Value	Unit
Thermal resistance junction-to-ambient (estimated)	θ_{JA}	39.7	°C/W
I/O pin power dissipation	$P_{I/O}$	User Determined	W
Power dissipation	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O}$	W
Maximum allowed P_D	P_{DMAX}	$(T_J - T_A) / \theta_{JA}$	°C

1. See **Section 5.1** for more detail.

3.2 DC Electrical Characteristics

Table 7. DC Electrical Characteristics

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0 V, V_{DDIO}=3.0 to 3.6V, V_{DD} = V_{DDA} = 2.25–2.75 V, T_A = –40° to +85°C, $C_L \leq 50$ pF, f_{op} = 80 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	2.25	2.5	2.75	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	-0.3	—	0.5	V
Input high voltage	V_{IH}	2.0	—	5.5	V
Input low voltage	V_{IL}	-0.3	—	0.8	V
Input current low (pullups disabled)	I_{IL}	-1	—	1	µA
Input current high (pullups disabled)	I_{IH}	-1	—	1	µA
Output tri-state current low	I_{OZL}	-10	—	10	µA

Table 7. DC Electrical Characteristics (Continued)

Operating Conditions: $V_{SSIO}=V_{SS} = V_{SSA} = 0$ V, V_{DDIO}=3.0 to 3.6V, $V_{DD} = V_{DDA}$ = 2.25–2.75 V, T_A = –40° to +85°C, $C_L \leq 50$ pF, f_{op} = 80 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Output tri-state current high	I_{OZH}	-10	—	10	µA
Output High Voltage with IOH load	V_{OH}	V_{DD} – 0.7	—	—	V
Output Low Voltage with IOL load	V_{OL}	—	—	0.4	V
Output High Current	I_{OH}	-300	—	—	µA
Output Low Current	I_{OL}	—	—	2	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current Run [1] Wait[2] Stop	I_{DD}	 — — —	 50 20 2	 TBD TBD TBD	 mA mA mA
Low Voltage Interrupt[3]	V_{EI}	—	2.7	TBD	V
Low Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power on Reset[4]	POR	—	1.5	2.0	V

1. Run (operating) I_{DD} measured using external square external square clock source (f_{osc} = 4MHz) into XTAL. All inputs 0.2V from rail; no DC loads; outputs unloaded. All ports configured as inputs; measured with all modules enabled. PLL set to 80MHz out.

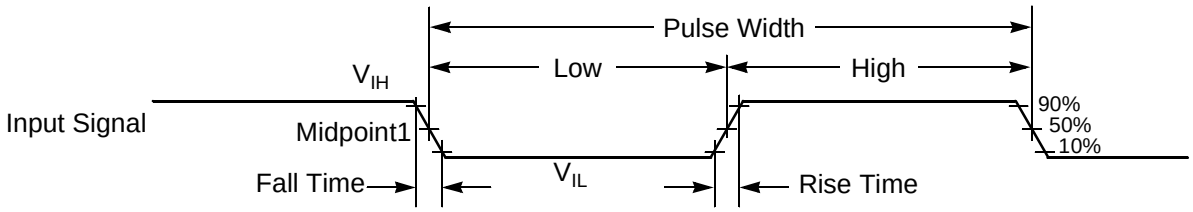
2. Wait I_{DD} measured using external square wave clock source (f_{osc} = 8MHz); all inpuyts 0.2V from rail; no DC loads; less than 50 pF on all outputs. C_L= 20 pF on OSC2; all ports configured as inputs; OSC2 capacitance linearly affects wait I_{DD}; measured with PLL and LVI enabled

3. When V_{DD} drops below V_{EI} max value, an interrupt is generated.

4. Power–on reset occurs whenever the internally regulated 2.5V digital supply drops below 1.5V typical. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 1.5V typical no matter how long the ramp up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp up until 2.5V is reached, at which time it self regulates.

3.3 AC Electrical Characteristics

Timing waveforms in **Section 3.3** are tested with a V_{IL} maximum of 0.8V and a V_{IH} minimum of 2.0V for all pins except XTAL, which is tested using the input levels in **Section 3.2**. In **Figure 3** the levels of V_{IH} and V_{IL} for an input signal are shown.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 3. Input Signal Measurement References

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state.
- Tri-stated, when a bus or signal is placed in a high impedance state.
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}.
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}.

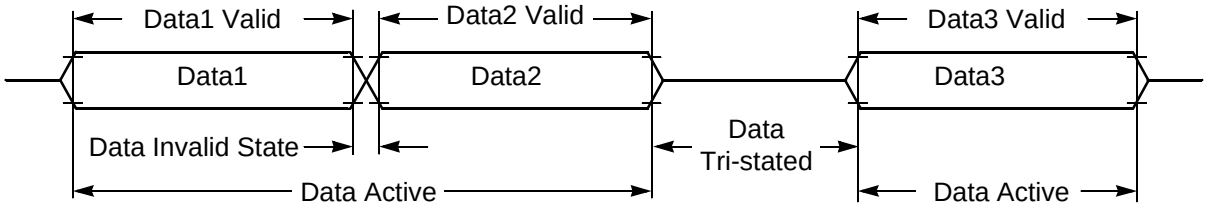


Figure 4. Signal States

3.4 Flash Memory Characteristics

Table 8. Flash Memory Truth Table

Mode	XE[1]	YE[2]	SE[3]	OE[4]	PROG[5]	ERASE[6]	MAS1[7]	NVSTR[8]
Standby	L	L	L	L	L	L	L	L
Read	H	H	H	H	L	L	L	L
Word Program	H	H	L	L	H	L	L	H
Page Erase	H	L	L	L	L	H	L	H
Mass Erase	H	L	L	L	L	H	H	H

1. X address enable, all rows are disabled when XE = 0
2. Y address enable, YMUX is disabled when YE = 0
3. Sense amplifier enable
4. Output enable, tri-state flash data out bus when OE = 0
5. Defines program cycle
6. Defines erase cycle
7. Defines mass erase cycle, erase whole block
8. Defines non-volatile store cycle

Table 9. IFREN Truth Table

Mode	IFREN = 1	IFREN = 0
Read	Read information block	Read main memory block
Word program	Program information block	Program main memory block
Page erase	Erase information block	Erase main memory block
Mass erase	Erase both block	Erase main memory block

Table 10. Timing Symbols

Characteristic	Symbol	See Figure(s)
X address access time	T_{xa}	-
Y address access time	T_{ya}	-
OE access time	T_{oa}	-
PROG/ERASE to NVSTR set up time	T_{nvs*}	Figure 5, Figure 6, Figure 7
NVSTR hold time	T_{nvh*}	Figure 5, Figure 6
NVSTR hold time(mass erase)	T_{nvh1*}	Figure 7
NVSTR to program set up time	T_{pgs*}	Figure 5
Program hold time	T_{pgh}	Figure 5
Address/data set up time	T_{ads}	Figure 5
Address/data hold time	T_{adh}	Figure 5
Recovery time	T_{rcv*}	Figure 5, Figure 6, Figure 7
Cumulative program HV period	T_{hv}	Figure 5
Program time	T_{prog*}	Figure 5
Erase time	T_{erase*}	Figure 6
Mass erase time	T_{me*}	Figure 7

* The Flash interface unit provides registers for the control of these parameters.

Table 11. Flash Timing Parameters

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0 V, V_{DDIO}=3.0 to 3.6V, V_{DD} = V_{DDA} = 2.25–2.75 V, T_A = –40° to +85°C, $C_L \leq 50$ pF, f_{op} = 80 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Program time[1]	T_{prog}	20	—	—	us
Erase time[2]	T_{erase}	20	—	—	ms
Mass erase time[3]	T_{me}	100	—	—	ms
Endurance[4]	E_{CYC}	10,000	—	—	cycles
Data Retention	D_{RET}	10	—	—	years
The following parameters should only be used in the Manual Word Programming mode.					
PROG/ERASE to NVSTR set up time	T_{nvs}	—	5	—	us
NVSTR hold time	T_{nvh}	—	5	—	us
NVSTR hold time(mass erase)	T_{nvh1}	—	100	—	us
NVSTR to program set up time	T_{pgs}	—	10	—	us
Recovery time	T_{rcv}	—	1	—	us
Cumulative program HV period[5]	T_{hv}	—	3	—	ms

1. Program specification guaranteed from T_A = 0° C to 85° C.
2. Erase specification guaranteed from T_A = 0° C to 85° C.
3. Mass erase specification guaranteed from T_A = 0° C to 85° C.
4. One cycle is equal to an erase, program, and read.
5. Thv is the cumulative high voltage programming time to the same row before next erase. The same address cannot be programmed twice before next erase.

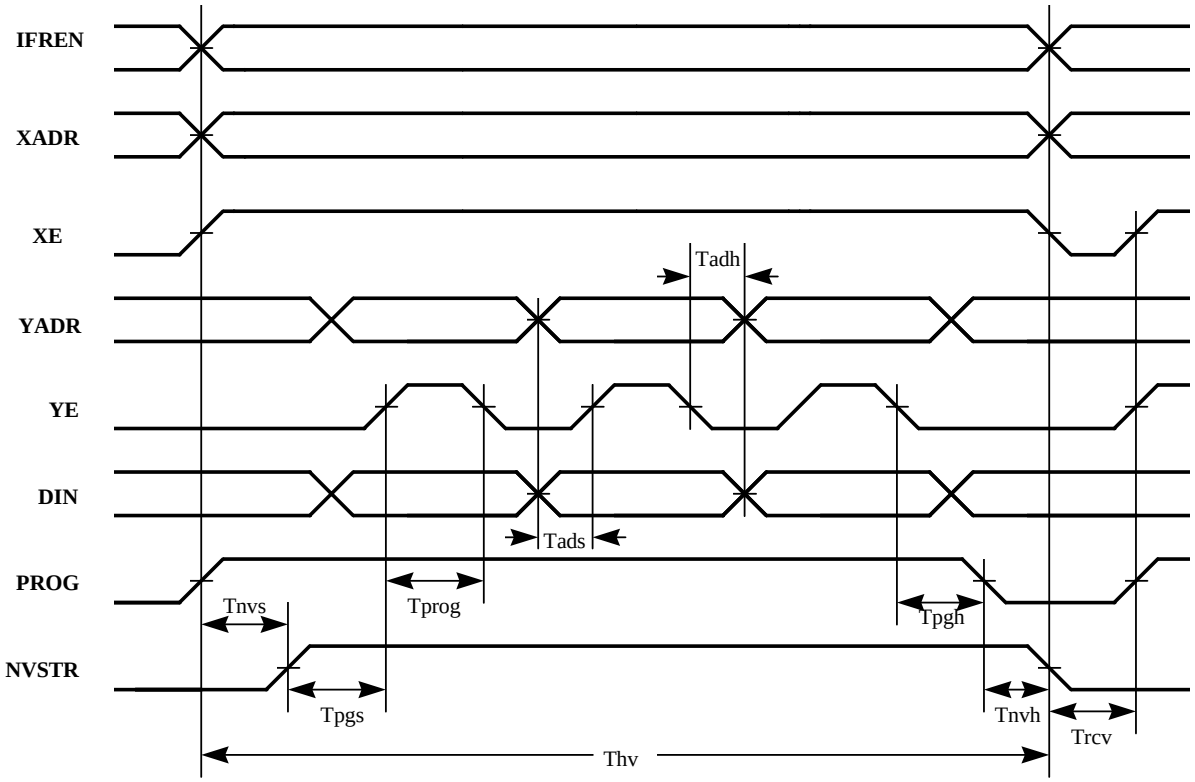


Figure 5. Flash Program Cycle

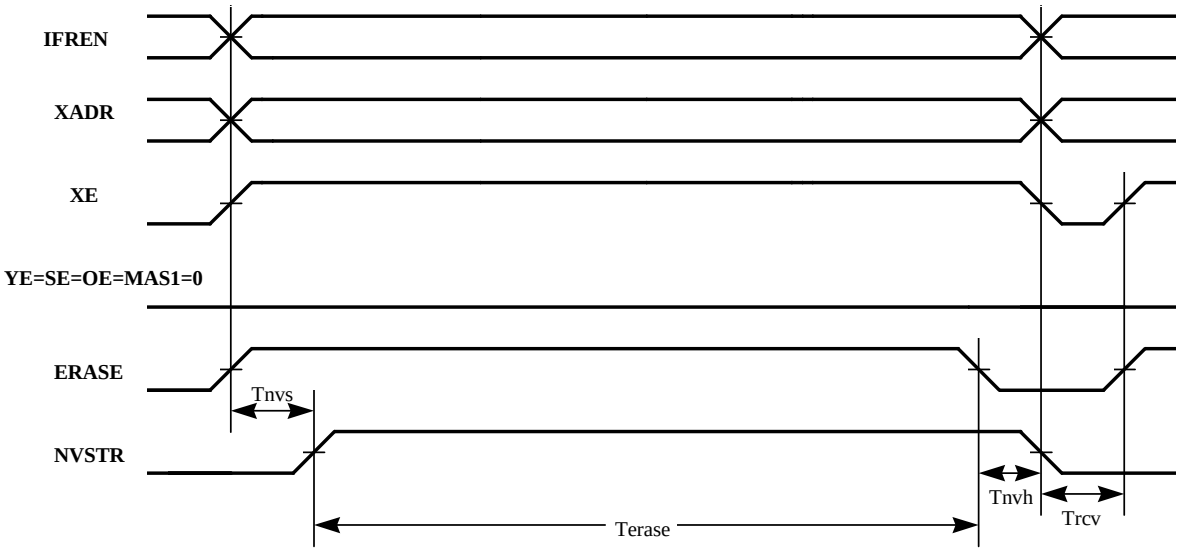


Figure 6. Flash Erase Cycle

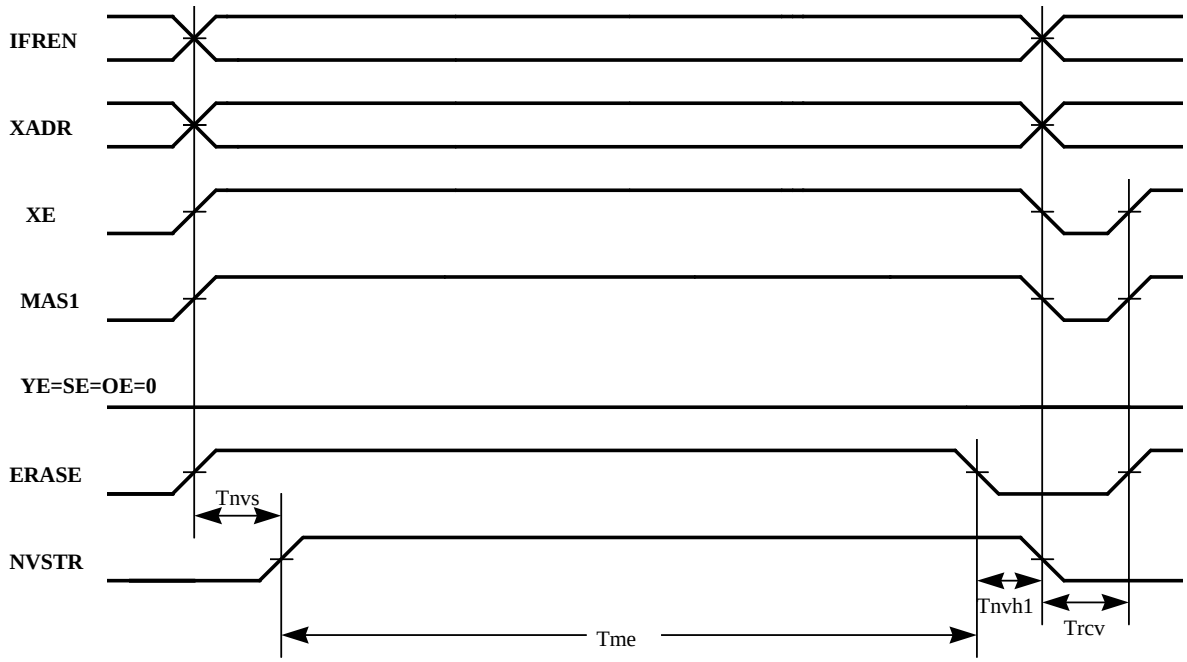


Figure 7. Flash Mass Erase Cycle

3.5 External Clock Operation

The DSP56F826 system clock can be derived from a crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins.

3.5.1 Crystal Oscillator

The internal oscillator is also designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 13.** In **Figure 8** a typical crystal oscillator circuit is shown. Follow the crystal supplier's recommendations when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

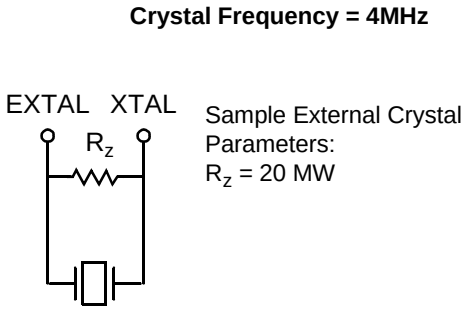


Figure 8. External Crystal Oscillator Circuit

3.5.2 External Clock Source

The recommended method of connecting an external clock is given in **Figure 9**. The external clock source is connected to XTAL and the EXTAL pin is grounded.

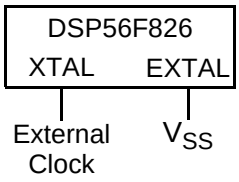


Figure 9. Connecting an External Clock Signal using XTAL

It is possible to instead drive EXTAL with an external clock, though this is not the recommended method. If you elect to drive EXTAL with an external clock source the following conditions must be met:

1. XTAL must be completely un-loaded,
2. the maximum frequency of the applied clock must be less than 6MHz.

Figure 10 illustrates how to connect an external clock circuit with a external clock source using EXTAL as the input.

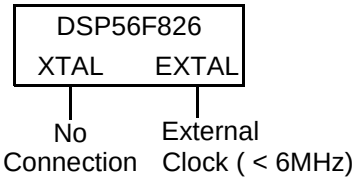


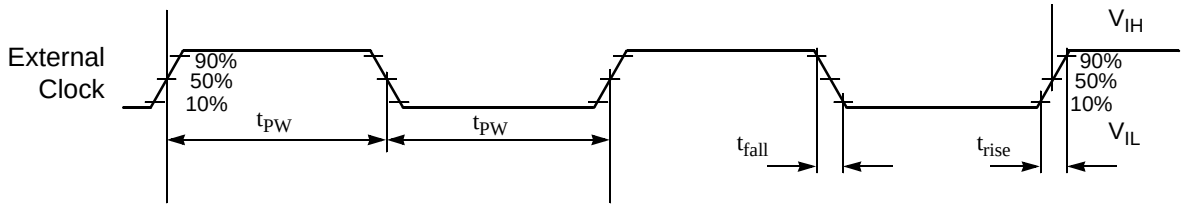
Figure 10. Connecting an External Clock Signal using EXTAL

Table 12. External Clock Operation Timing Requirements

Operating Conditions: $V_{SSIO}=V_{SS} = V_{SSA} = 0$ V, V_{DDIO}=3.0 to 3.6V, $V_{DD} = V_{DDA}$ = 2.25–2.75 V, T_A = –40° to +85°C, $C_L \le 50$ pF, f_{op} = 80 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	0	—	80	MHz
Clock Pulse Width[2, 5]	t_{PW}	6.25	—	—	ns
External clock input rise time[3, 5]	t_{rise}	—	—	3	ns
External clock input fall time[4, 5]	t_{fall}	—	—	3	ns

1. See **Figure 9** for details on using the recommended connection of an external clock driver.
2. The high or low pulse width must be no smaller than 6.25 ns or the chip will not function.
3. External clock input rise time is measured from 10% to 90%.
4. External clock input fall time is measured from 90% to 10%.
5. Parameters shown are guaranteed by design.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 11. External Clock Timing

Table 13. PLL Timing

Operating Conditions: $V_{SSIO}=V_{SS} = V_{SSA} = 0$ V, V_{DDIO}=3.0 to 3.6V, $V_{DD} = V_{DDA}$ = 2.25–2.75 V, T_A = –40° to +85°C, $C_L \le 50$ pF, f_{op} = 80 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	2	4	6	MHz
PLL output frequency	f_{op}	40	—	80	MHz
PLL stabilization time [2]	t_{plls}	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8MHz input crystal.
2. This is the minimum time required after the PLL setup is changed to ensure reliable operation

3.6 External Bus Asynchronous Timing

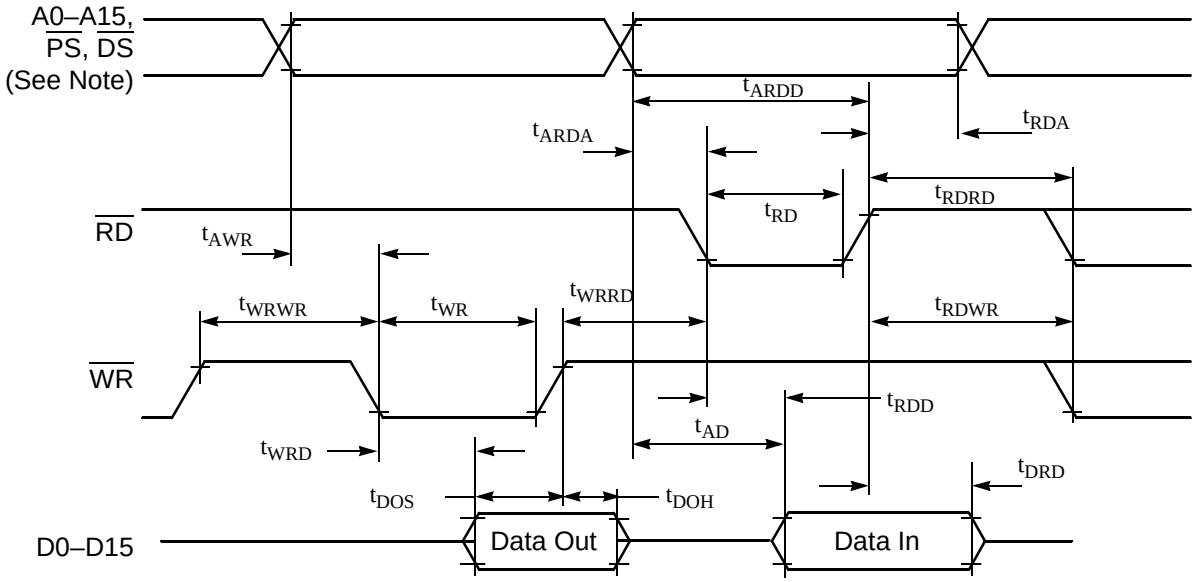
Table 14. External Bus Asynchronous Timing[1, 2]

Operating Conditions: $V_{SSIO}=V_{SS}=V_{SSA}=0$ V, V_{DDIO}=3.0 to 3.6V, $V_{DD}=V_{DDA}$ = 2.25–2.75 V, T_A = –40° to +85°C, $C_L \le 50$ pF, f_{op} = 80 MHz

Characteristic	Symbol	Min	Max	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	6.5	—	ns
$\overline{WR}$ Width Asserted Wait states = 0 Wait states > 0	t_{WR}	 7.5 (T*WS) + 7.5	 — —	 ns ns
$\overline{WR}$ Asserted to D0–D15 Out Valid	t_{WRD}	—	T + 4.2	ns
Data Out Hold Time from $\overline{WR}$ Deasserted	t_{DOH}	4.8	—	ns
Data Out Set Up Time to $\overline{WR}$ Deasserted Wait states = 0 Wait states > 0	t_{DOS}	 6.4 (T*WS) + 6.4	 — —	 ns ns
$\overline{RD}$ Deasserted to Address Not Valid	t_{RDA}	0	—	ns
Address Valid to $\overline{RD}$ Deasserted Wait states = 0 Wait states > 0	t_{ARDD}	 18.7 (T*WS) + 18.7	— 	 ns ns
Input Data Hold to $\overline{RD}$ Deasserted	t_{DRD}	0	—	ns
$\overline{RD}$ Assertion Width Wait states = 0 Wait states > 0	t_{RD}	 19 (T*WS) + 19	 — —	 ns ns
Address Valid to Input Data Valid Wait states = 0 Wait states > 0	t_{AD}	 — —	 1 (T*WS) + 1	 ns ns
Address Valid to $\overline{RD}$ Asserted	t_{ARDA}	-4.4	—	ns
$\overline{RD}$ Asserted to Input Data Valid Wait states = 0 Wait states > 0	t_{RDD}	 — —	 2.4 (T*WS) + 2.4	 ns ns
$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	t_{WRRD}	6.8	—	ns
$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	t_{RDRD}	0	—	ns
$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	t_{WRWR}	14.1	—	ns
$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	t_{RDWR}	12.8	—	ns

1. Timing is both wait state and frequency dependent. In the formulas listed, WS = the number of wait states and T = Clock Period. For 80MHz operation, T = 12.5ns.
2. Parameters listed are guaranteed by design.

To calculate the required access time for an external memory for any frequency < 80Mhz, use this formula:
Top = Clock period @ desired operating frequency
WS = Number of wait states
Memory Access Time = (Top*WS) + (Top- 11.5)



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 12. External Bus Asynchronous Timing

3.7 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 15. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1, 5]

Operating Conditions: $V_{SSIO}=V_{SS}=V_{SSA}=0$ V, V_{DDIO}=3.0 to 3.6V, $V_{DD}=V_{DDA}$ = 2.25–2.75 V, T_A = –40° to +85°C, $C_L \le 50$ pF, f_{op} = 80 MHz

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	21	ns	Figure 13
Minimum $\overline{\text{RESET}}$ Assertion Duration[2] OMR Bit 6 = 0 OMR Bit 6 = 1	t_{RA}	 275,000T 128T	 — —	 ns ns	Figure 13
$\overline{\text{RESET}}$ De-assertion to First External Address Output	t_{RDA}	33T	34T	ns	Figure 13
Edge-sensitive Interrupt Request Width	t_{IRW}	1.5T	—	ns	Figure 14
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	—	15T	ns	Figure 15
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	—	16T	ns	Figure 15
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State[3]	t_{IRI}	—	13T	ns	Figure 16
$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State[4]	t_{IW}	—	2T	ns	Figure 17
Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of first instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IF}	 — —	 275,000T 12T	 ns ns	Figure 17
Duration for Level Sensitive $\overline{\text{IRQA}}$ Assertion to Cause the Fetch of First $\overline{\text{IRQA}}$ Interrupt Instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IRQ}	 — —	 275,000T 12T	 ns ns	Figure 18
Delay from Level Sensitive $\overline{\text{IRQA}}$ Assertion to First Interrupt Vector Address Out Valid (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{II}	 — —	 275,000T 12T	 ns ns	Figure 18

1. In the formulas, T = clock cycle. For an operating frequency of 80MHz, T = 12.5 ns.
2. Circuit stabilization delay is required during reset when using an external clock or crystal oscillator in two cases:
   - After power-on reset
   - When recovering from Stop state
3. The minimum is specified for the duration of an edge-sensitive IRQA interrupt required to recover from the Stop state. This is not the minimum required so that the IRQA interrupt is accepted.
4. The interrupt instruction fetch is visible on the pins only in Mode 3.
5. Parameters listed are guaranteed by design.

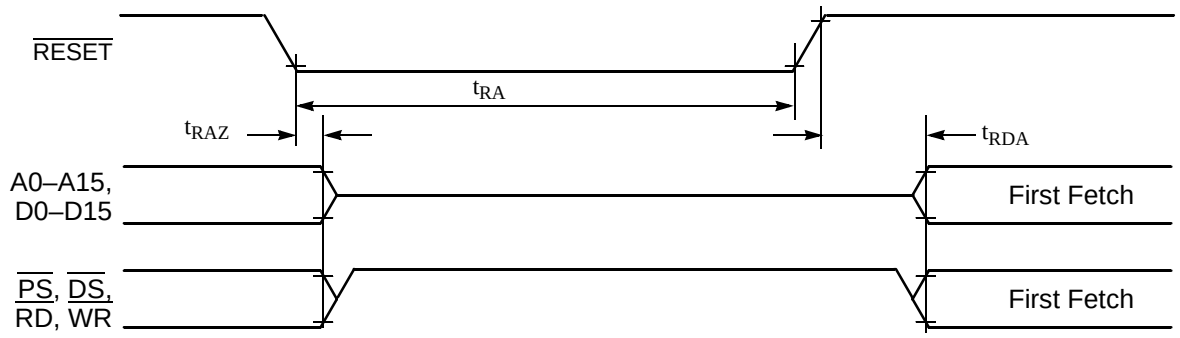


Figure 13. Asynchronous Reset Timing

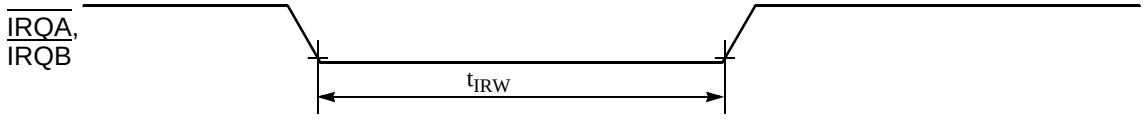


Figure 14. External Interrupt Timing (Negative-Edge-Sensitive)

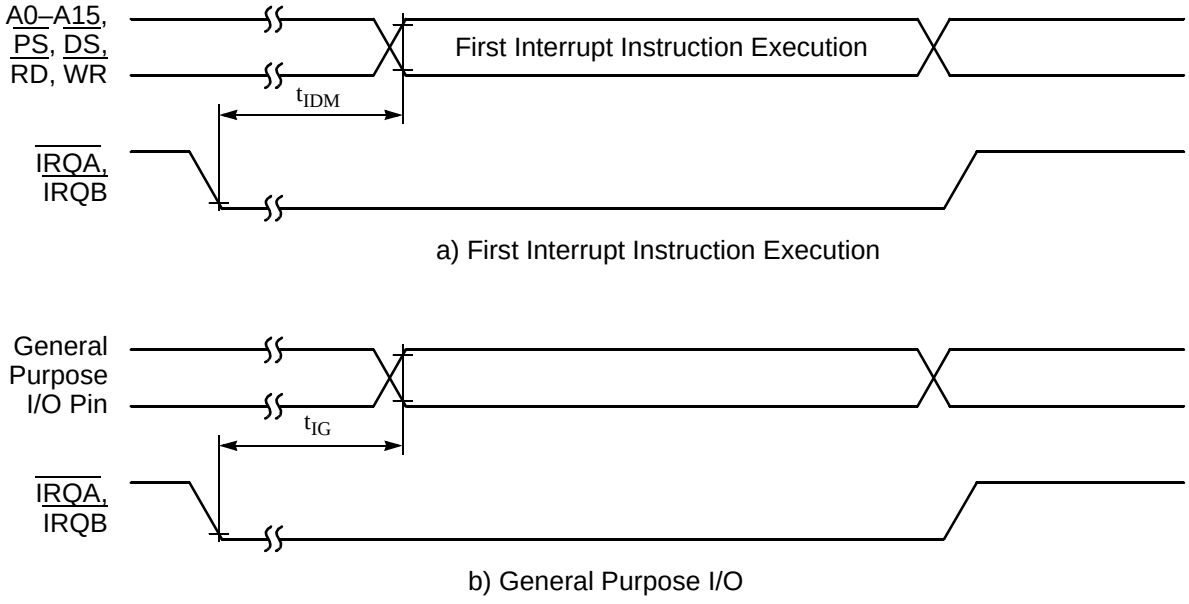


Figure 15. External Level-Sensitive Interrupt Timing

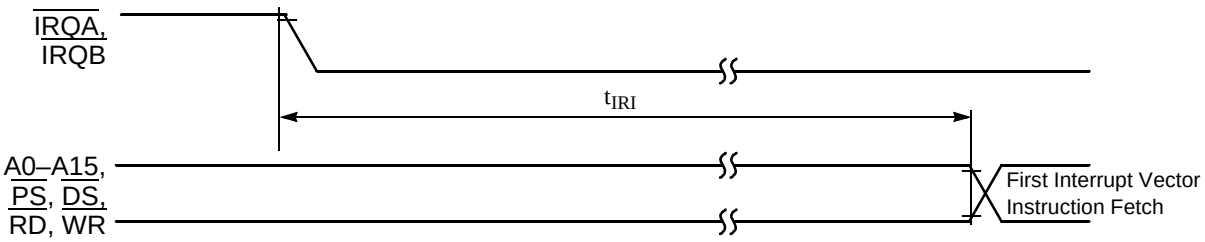


Figure 16. Interrupt from Wait State Timing

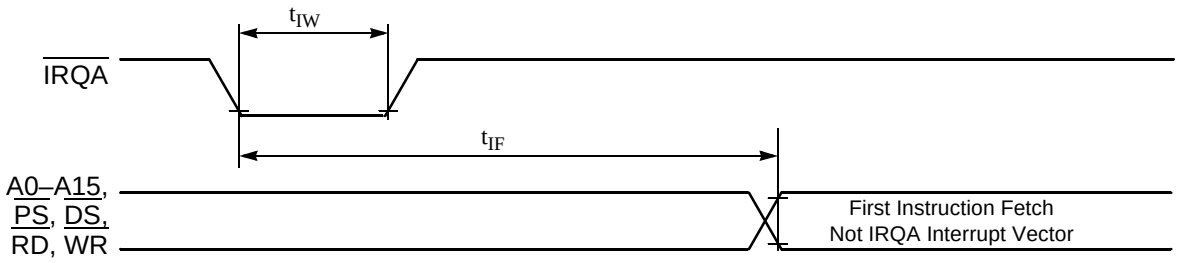


Figure 17. Recovery from Stop State Using Asynchronous Interrupt Timing

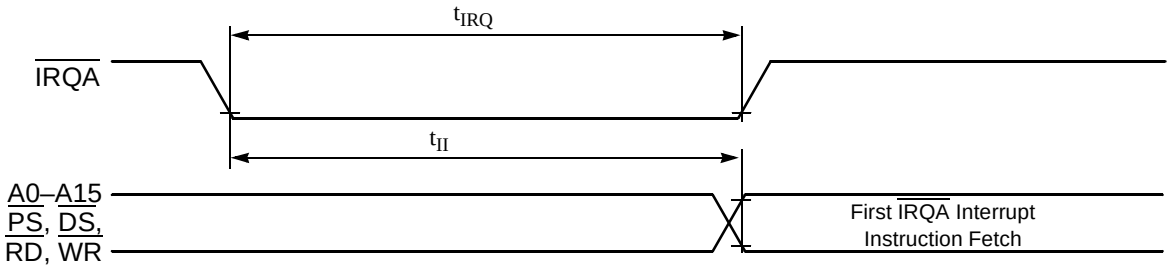


Figure 18. Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

3.8 Serial Peripheral Interface (SPI) Timing

Table 16. SPI Timing[1]

Operating Conditions: $V_{SSIO}=V_{SS} = V_{SSA} = 0$ V, V_{DDIO}=3.0 to 3.6V, $V_{DD} = V_{DDA} = 2.25–2.75$ V, $T_A = –40°$ to +85°C, $C_L \leq 50$ pF, $f_{op} = 80$ MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 50	 — —	 ns ns	Figures 19, 20, 21, 22
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	Figure 22
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	Figure 22
Clock (SCLK) high time Master Slave	t_{CH}	 17.6 25	 — —	ns ns	Figures 19, 20, 21, 22
Clock (SCLK) low time Master Slave	t_{CL}	 24.1 25	 — —	 ns ns	Figures 19, 20, 21, 22
Data setup time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figures 19, 20, 21, 22
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figures 19, 20, 21, 22
Access time (time to data active from high-impedance state) Slave	t_A	 4.8	 15	 ns	Figure 22
Disable time (hold time to high-impedance state) Slave	t_D	 3.7	 15.2	 ns	Figure 22
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figures 19, 20, 21, 22
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figures 19, 20, 21, 22
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figures 19, 20, 21, 22
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figures 19, 20, 21, 22

1.Parameters listed are guaranteed by design.

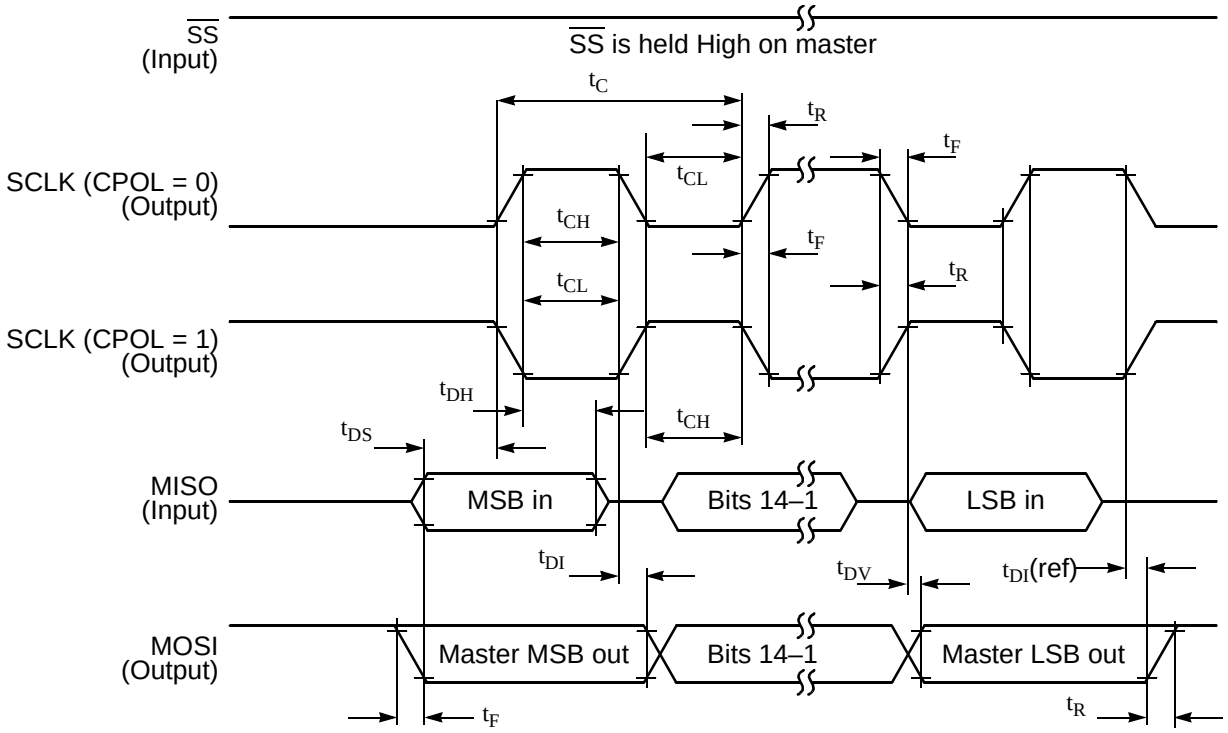


Figure 19. SPI Master Timing (CPHA = 0)

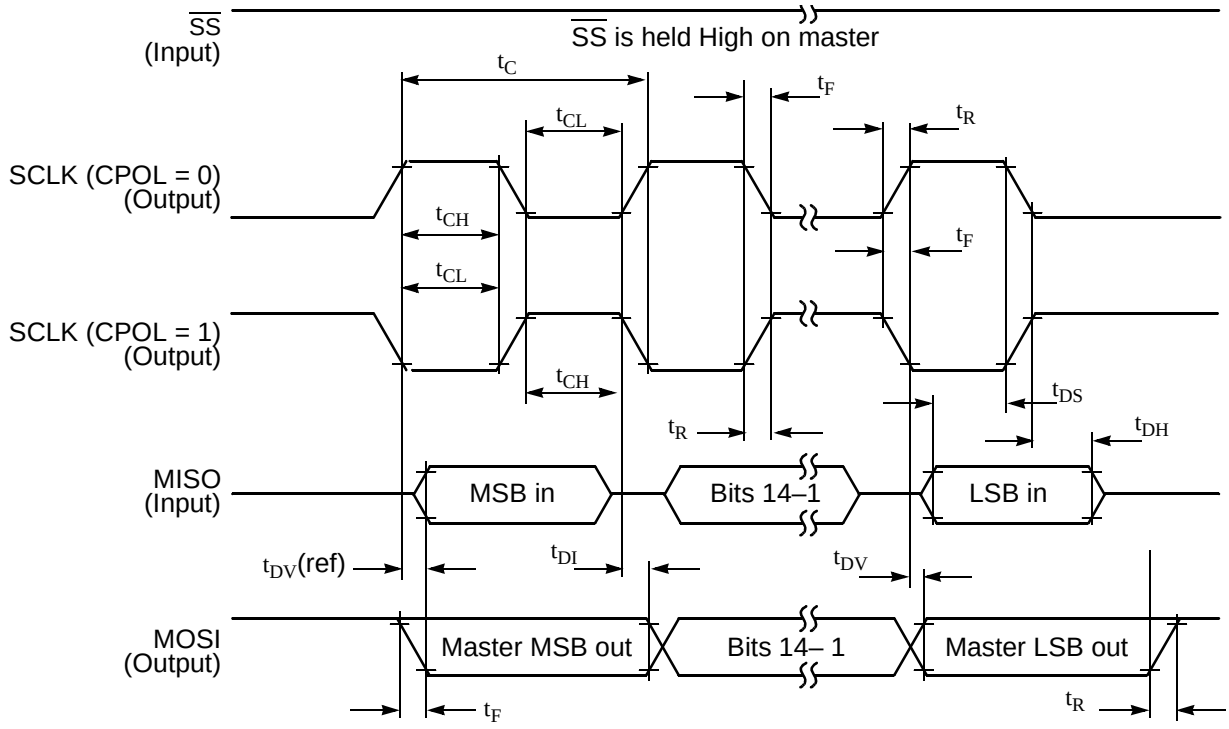


Figure 20. SPI Master Timing (CPHA = 1)

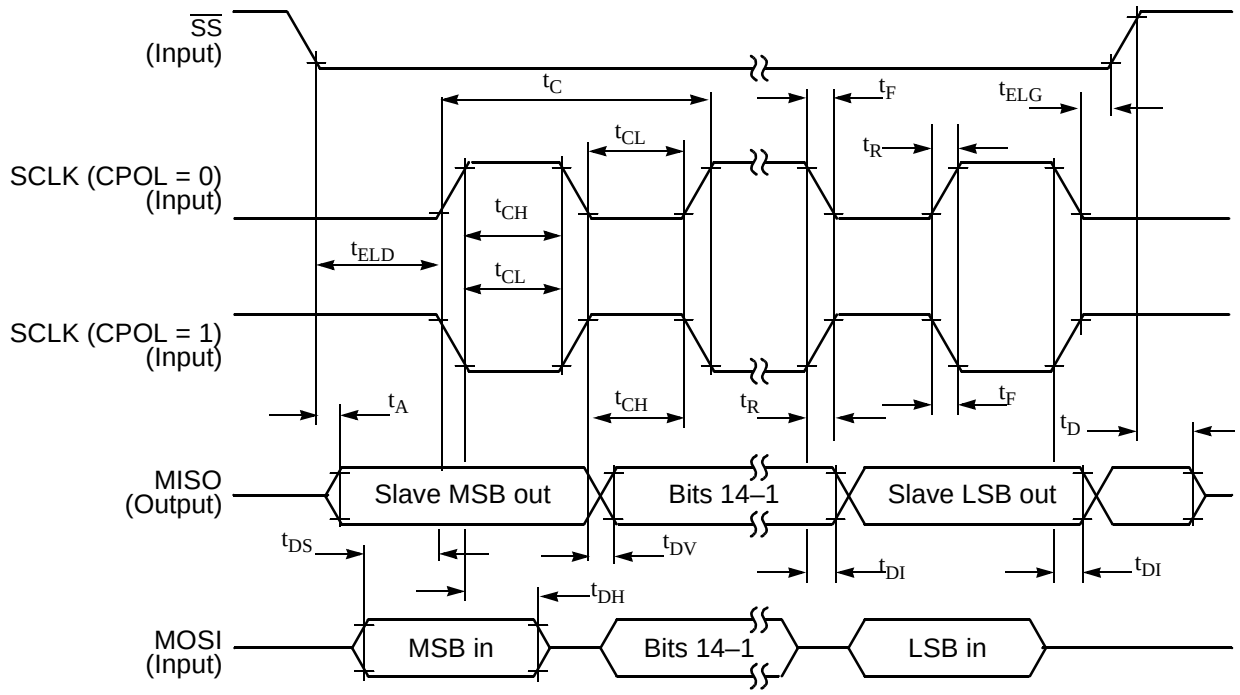


Figure 21. SPI Slave Timing (CPHA = 0)

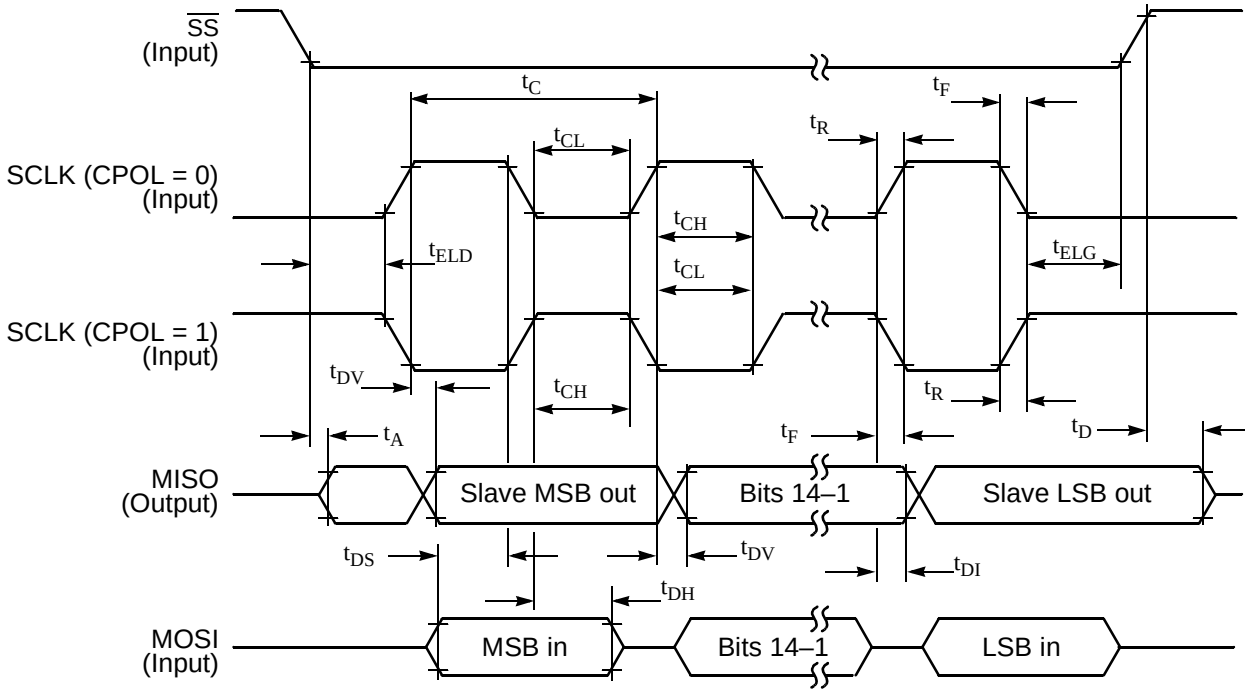


Figure 22. SPI Slave Timing (CPHA = 1)

3.9 Quad Timer Timing

Table 17. Timer Timing[1, 2]

Operating Conditions: $V_{SSIO}=V_{SS} = V_{SSA} = 0$ V, V_{DDIO}=3.0 to 3.6V, $V_{DD} = V_{DDA} = 2.25–2.75$ V, $T_A = –40°$ to +85°C, $C_L \le 50$ pF, $f_{op} = 80$ MHz

Characteristic	Symbol	Min	Max	Unit
Timer input period	P_{IN}	4T+6	—	ns
Timer input high/low period	P_{INHL}	2T+3	—	ns
Timer output period	P_{OUT}	2T-3	—	ns
Timer output high/low period	P_{OUTHL}	1T-3	—	ns

1. In the formulas listed, T = clock cycle. For 80MHz operation, T = 12.5 ns.
2. Parameters listed are guaranteed by design.

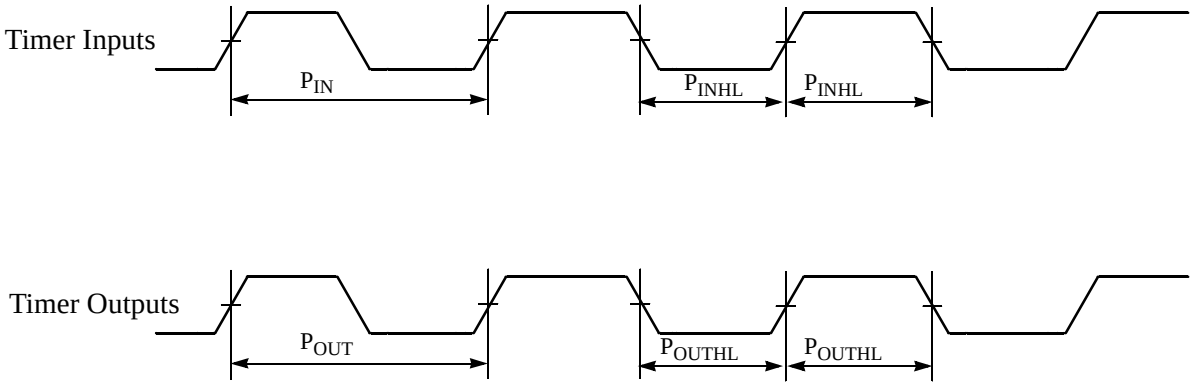


Figure 23. Quad Timer Timing

3.10 Serial Communication Interface (SCI) Timing

Table 18. SCI Timing[4]

Operating Conditions: $V_{SSIO}=V_{SS} = V_{SSA} = 0$ V, V_{DDIO}=3.0 to 3.6V, $V_{DD} = V_{DDA} = 2.25–2.75$ V, $T_A = –40°$ to +85°C, $C_L \le 50$ pF, $f_{op} = 80$ MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate[1]	BR	—	$(f_{MAX}*2.5)/(80)$	Mbps
RXD[2] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns
TXD[3] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns

1. f_{MAX} is the frequency of operation of the system clock in MHz.
2. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
3. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
4. Parameters listed are guaranteed by design.

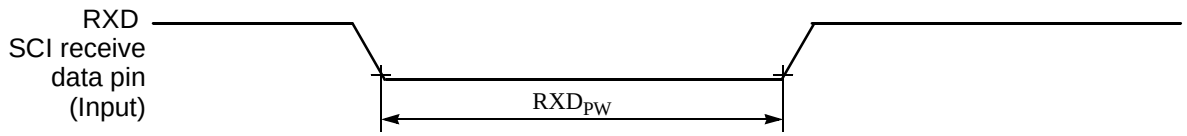


Figure 24. RXD Pulse Width

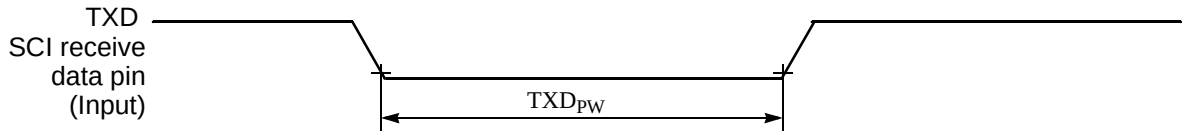


Figure 25. TXD Pulse Width

3.11 JTAG Timing

Table 19. JTAG Timing[1, 3]

Operating Conditions: $V_{SSIO}=V_{SS}=V_{SSA}=0$ V, V_{DDIO}=3.0 to 3.6V, $V_{DD}=V_{DDA}$ = 2.25–2.75 V, T_A = –40° to +85°C, $C_L \le 50$ pF, f_{op} = 80MHz

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation[2]	f_{OP}	DC	10	MHz
TCK cycle time	t_{CY}	100	—	ns
TCK clock pulse width	t_{PW}	50	—	ns
TMS, TDI data setup time	t_{DS}	0.4	—	ns
TMS, TDI data hold time	t_{DH}	1.2	—	ns
TCK low to TDO data valid	t_{DV}	—	26.6	ns
TCK low to TDO tri-state	t_{TS}	—	23.5	ns
$\overline{\text{TRST}}$ assertion time	t_{TRST}	50	—	ns
$\overline{\text{DE}}$ assertion time	t_{DE}	4T	—	ns

1. Timing is both wait state and frequency dependent. For the values listed, T = clock cycle. For 80MHz operation, T = 12.5 ns.
2. TCK frequency of operation must be less than 1/8 the processor rate.
3. Parameters listed are guaranteed by design.

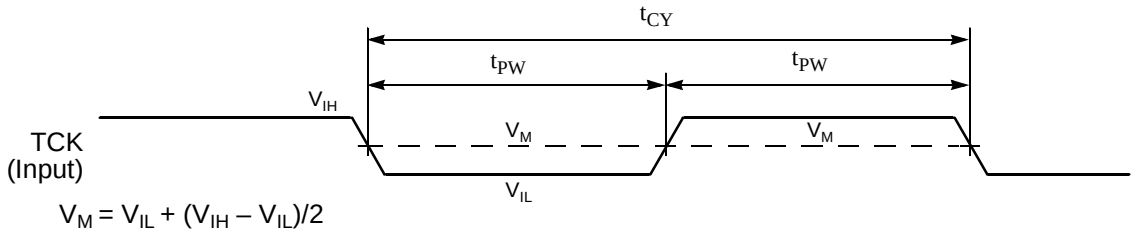


Figure 26. Test Clock Input Timing Diagram

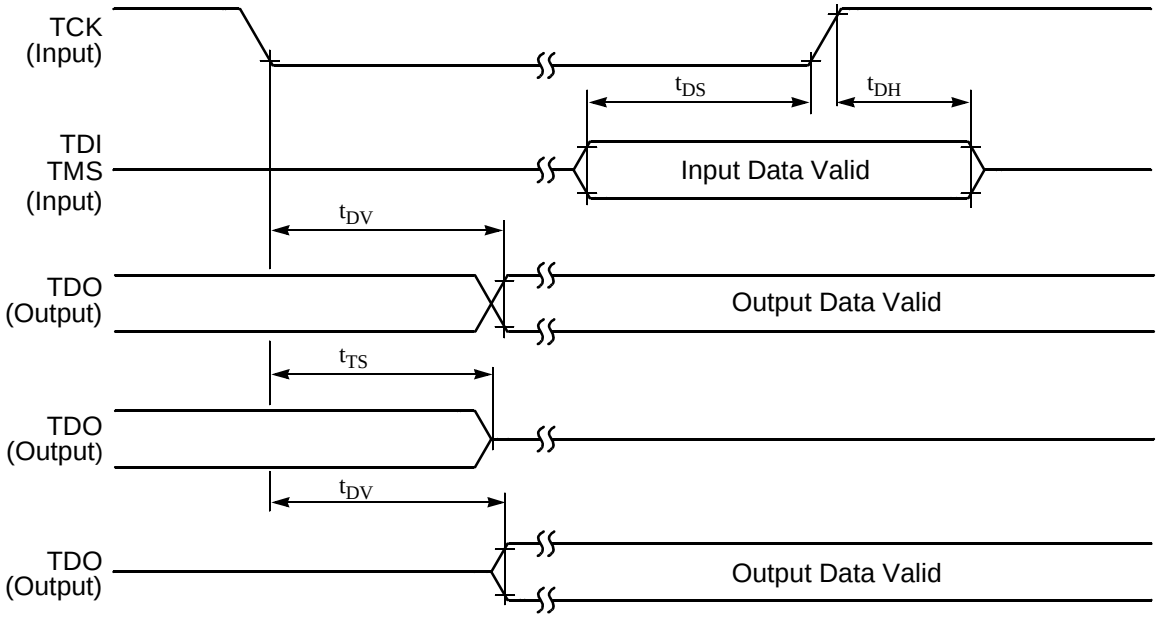


Figure 27. Test Access Port Timing Diagram

Figure 28. $\overline{\text{TRST}}$ Timing Diagram

Figure 29. OnCE—Debug Event

Part 4 Packaging

4.1 Package and Pin-Out Information DSP56F826

This section contains package and pin-out information for the 100-pin LQFP configuration of the DSP56F826.

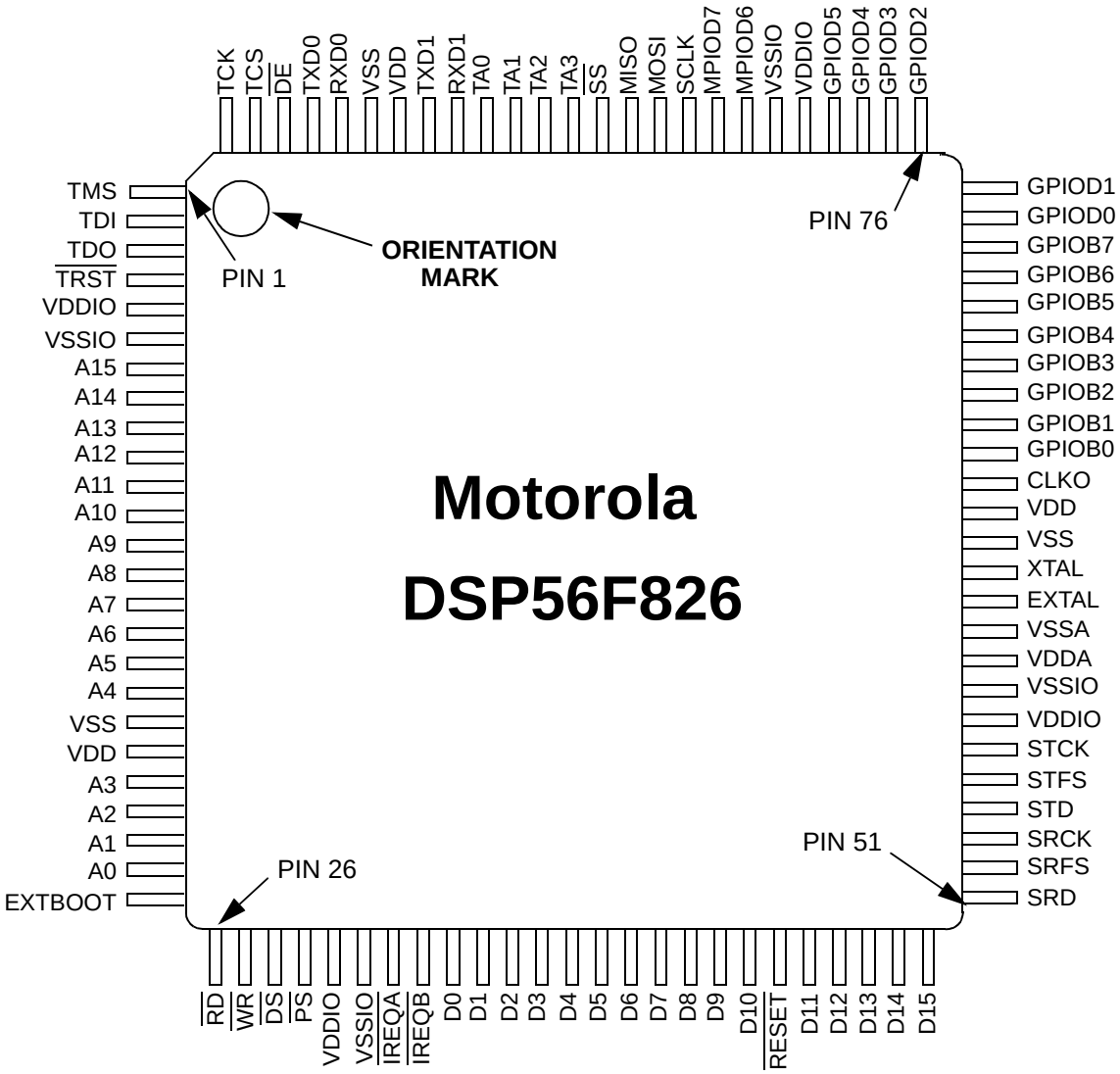
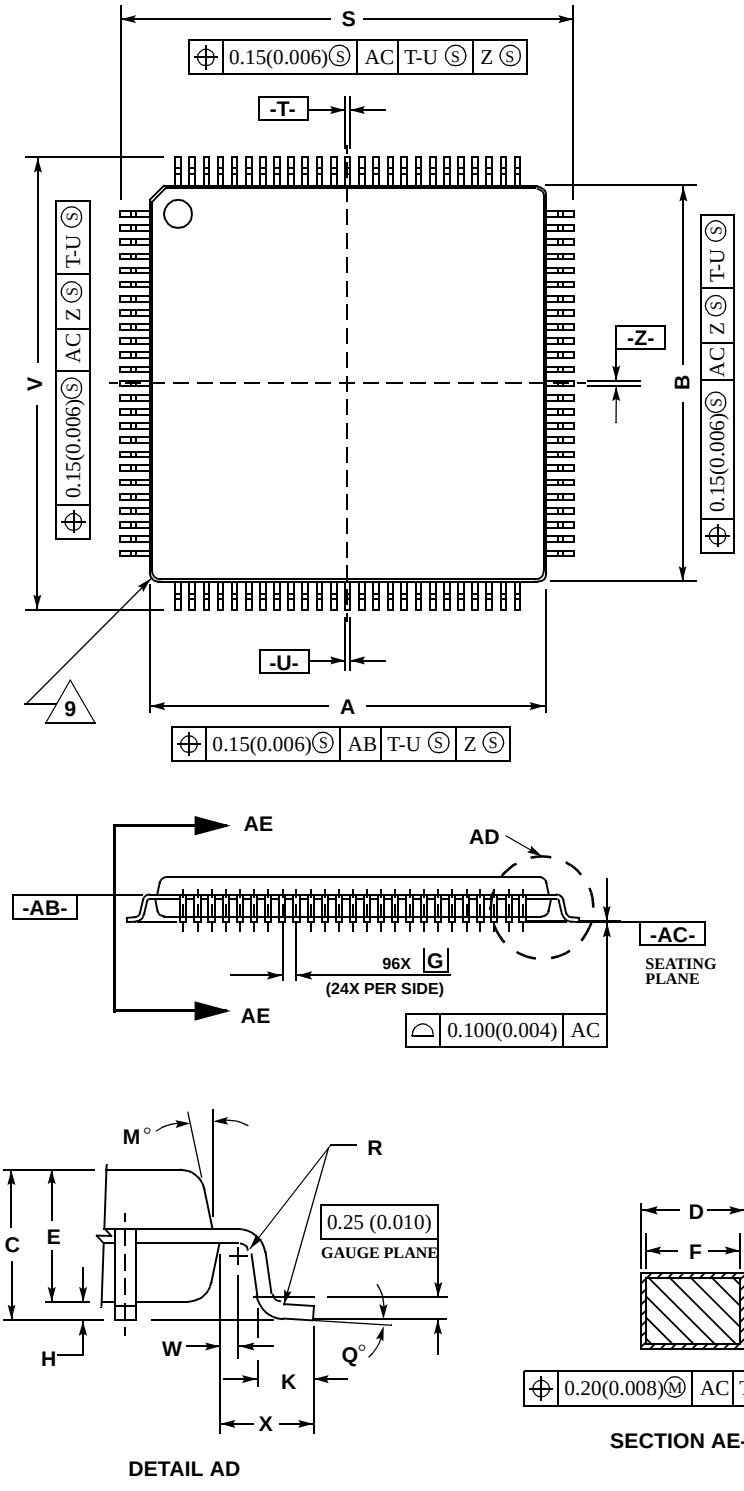


Figure 30. Top View, DSP56F826 100-pin LQFP Package

Table 20. DSP56F826 Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	TMS	26	$\overline{RD}$	51	SRD	76	GPIOD2
2	TDI	27	$\overline{WR}$	52	SRFS	77	GPIOD3
3	TDO	28	$\overline{DS}$	53	SRCK	78	GPIOD4
4	$\overline{TRST}$	29	$\overline{PS}$	54	STD	79	GPIOD5
5	VDDIO	30	VDDIO	55	STFS	80	VDDIO
6	VSSIO	31	VSSIO	56	STCK	81	VSSIO
7	A15	32	$\overline{IRQA}$	57	VDDIO	82	GPIOD6
8	A14	33	$\overline{IRQB}$	58	VSSIO	83	GPIOD7
9	A13	34	D0	59	VDDA	84	SCLK
10	A12	35	D1	60	VSSA	85	MOSI
11	A11	36	D2	61	EXTAL	86	MISO
12	A10	37	D3	62	XTAL	87	$\overline{SS}$
13	A9	38	D4	63	VSS	88	TA3
14	A8	39	D5	64	VDD	89	TA2
15	A7	40	D6	65	CLKO	90	TA1
16	A6	41	D7	66	GPIOB0	91	TA0
17	A5	42	D8	67	GPIOB1	92	RXD1
18	A4	43	D9	68	GPIOB2	93	TXD1
19	VSS	44	D10	69	GPIOB3	94	VDD
20	VDD	45	$\overline{RESET}$	70	GPIOB4	95	VSS
21	A3	46	D11	71	GPIOB5	96	RXD0
22	A2	47	D12	72	GPIOB6	97	TXD0
23	A1	48	D13	73	GPIOB7	98	$\overline{DE}$
24	A0	49	D14	74	GPIOD0	99	TCS
25	EXTBOOT	50	D15	75	GPIOD1	100	TCK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014). DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.070 (0.003).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.950	14.050	0.549	0.553
B	13.950	14.050	0.549	0.553
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	15.950	16.050	0.628	0.632
V	15.950	16.050	0.628	0.632
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

CASE 842F-01

Figure 31. 100-pin LQPF Mechanical Information

Part 5 Design Considerations

5.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

Definitions:

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.

- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

The junction-to-case thermal resistances quoted in this data sheet are determined using the first definition on page 41. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual. Hence, the new thermal metric, Thermal Characterization Parameter, or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

5.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Use the following list of considerations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the DSP, and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place six 0.01–0.1 µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the eight V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and V_{SS}.
- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100 µF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal.

- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.
- Take special care to minimize noise levels on the VREF, V_{DDA} and V_{SSA} pins.
- When using Wired-OR mode on the SPI or the $\overline{\text{IRQx}}$ pins, the user must provide an external pull-up device.
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. Designs that do not require debugging functionality, such as consumer products, should tie these pins together.
- Because the Flash memory is programmed through the JTAG/OnCE port, designers should provide an interface to this port to allow in-circuit Flash programming.

Part 6 Ordering Information

Table 21 lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 21. DSP56F803 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56F826	3.0–3.6 V 2.25-2.75 V	Plastic Quad Flat Pack (LQFP)	100	80	DSP56F803BU80

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ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tao Po, N.T., Hong Kong. 852-26668334

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