

Features

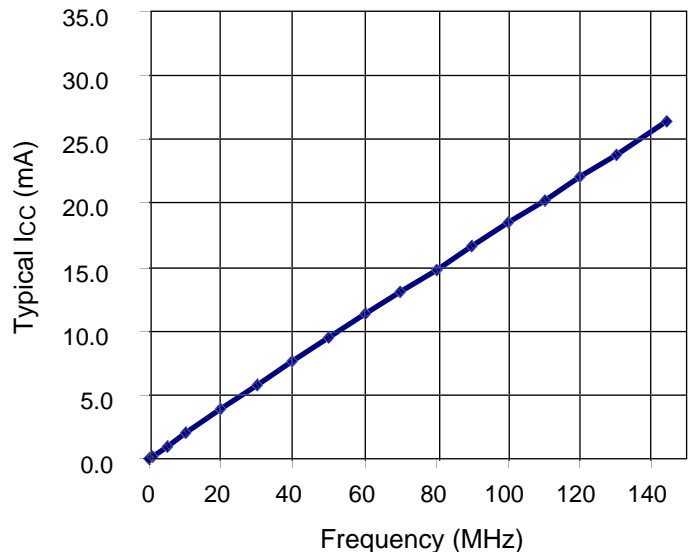
- Lowest power 64 macrocell CPLD
- 6.0 ns pin-to-pin logic delays
- System frequencies up to 145 MHz
- 64 macrocells with 1,500 usable gates
- Available in small footprint packages
 - 44-pin PLCC (36 user I/O pins)
 - 44-pin VQFP (36 user I/O pins)
 - 48-ball CS BGA (40 user I/O pins)
 - 56-ball CP BGA (48 user I/O pins)
 - 100-pin VQFP (68 user I/O pins)
- Optimized for 3.3V systems
 - Ultra-low power operation
 - 5V tolerant I/O pins with 3.3V core supply
 - Advanced 0.35 micron five layer metal EEPROM process
 - Fast Zero Power™ (FZP) CMOS design technology
- Advanced system features
 - In-system programming
 - Input registers
 - Predictable timing model
 - Up to 23 available clocks per function block
 - Excellent pin retention during design changes
 - Full IEEE Standard 1149.1 boundary-scan (JTAG)
 - Four global clocks
 - Eight product term control terms per function block
- Fast ISP programming times
- Port Enable pin for dual function of JTAG ISP pins
- 2.7V to 3.6V supply voltage at industrial temperature range
- Programmable slew rate control per macrocell
- Security bit prevents unauthorized access
- Refer to XPLA3 family data sheet ([DS012](#)) for architecture description

Description

The XCR3064XL is a 3.3V, 64-macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of four function blocks provide 1,500 usable gates. Pin-to-pin propagation delays are 6.0 ns with a maximum system frequency of 145 MHz.

TotalCMOS Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its sum of products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to [Figure 1](#) and [Table 1](#) showing the I_{CC} vs. Frequency of our XCR3064XL TotalCMOS CPLD (data taken with four resettable up/down, 16-bit counters at 3.3V, 25°C).



DS017_01_102401

Figure 1: I_{CC} vs. Frequency at $V_{CC} = 3.3V$, 25°C

Table 1: I_{CC} vs. Frequency ($V_{CC} = 3.3V$, 25°C)

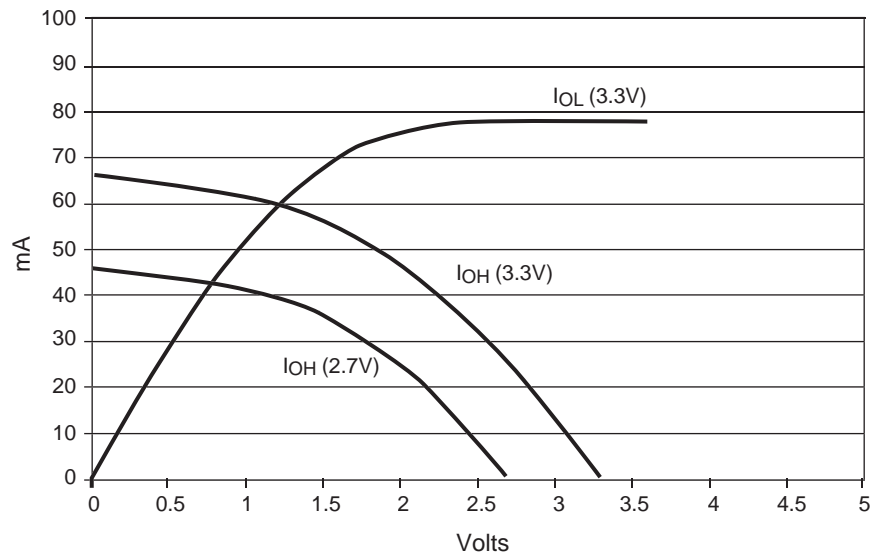
Frequency (MHz)	0	1	5	10	20	40	60	80	100	120	140
Typical I_{CC} (mA)	0	0.2	1.0	2.0	3.9	7.6	11.3	14.8	18.5	22.1	25.6

DC Electrical Characteristics Over Recommended Operating Conditions⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$V_{OH}^{(2)}$	Output High voltage	$I_{OH} = -8 \text{ mA}$	2.4	-	V
V_{OL}	Output Low voltage for 3.3V outputs	$I_{OL} = 8 \text{ mA}$	-	0.4	V
I_{IL}	Input leakage current	$V_{IN} = \text{GND or } V_{CC}$	-10	10	μA
I_{IH}	I/O High-Z leakage current	$V_{IN} = \text{GND or } V_{CC}$	-10	10	μA
I_{CCSB}	Standby current	$V_{CC} = 3.6\text{V}$	-	100	μA
I_{CC}	Dynamic current ^(3,4)	$f = 1 \text{ MHz}$	-	0.5	mA
		$f = 50 \text{ MHz}$	-	15	mA
C_{IN}	Input pin capacitance ⁽⁵⁾	$f = 1 \text{ MHz}$	-	8	pF
C_{CLK}	Clock input capacitance ⁽⁵⁾	$f = 1 \text{ MHz}$	-	12	pF
$C_{I/O}$	I/O pin capacitance ⁽⁵⁾	$f = 1 \text{ MHz}$	-	10	pF

Notes:

1. See XPLA3 family data sheet ([DS012](#)) for recommended operating conditions.
2. See [Figure 2](#) for output drive characteristics of the XPLA3 family.
3. See [Table 1](#), [Figure 1](#) for typical values.
4. This parameter measured with a 16-bit, resettable up/down counter loaded into every function block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
5. Typical values, not tested.



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Figure 2: Typical I/V Curve for the XPLA3 Family

AC Electrical Characteristics Over Recommended Operating Conditions^(1,2)

Symbol	Parameter	-6		-7		-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
T _{PD1}	Propagation delay time (single p-term)	-	5.5	-	7.0	-	9.1	ns
T _{PD2}	Propagation delay time (OR array) ⁽³⁾	-	6.0	-	7.5	-	10.0	ns
T _{CO}	Clock to output (global synchronous pin clock)	-	4.0	-	5.0	-	6.5	ns
T _{SUF}	Setup time (fast input register)	2.5	-	2.5	-	3.0	-	ns
T _{SU1} ⁽⁴⁾	Setup time (single p-term)	3.5	-	4.3	-	5.4	-	ns
T _{SU2}	Setup time (OR array)	4.0	-	4.8	-	6.3	-	ns
T _H ⁽⁴⁾	Hold time	0	-	0	-	0	-	ns
T _{WLH} ⁽⁴⁾	Global Clock pulse width (High or Low)	2.5	-	3.0	-	4.0	-	ns
T _{tPLH} ⁽⁴⁾	P-term clock pulse width	4.0	-	5.0	-	6.0	-	ns
T _R ⁽⁴⁾	Input rise time	-	20	-	20	-	20	ns
T _L ⁽⁴⁾	Input fall time	-	20	-	20	-	20	ns
f _{SYSTEM} ⁽⁴⁾	Maximum system frequency	-	145	-	119	-	95	MHz
T _{CONFIG} ⁽⁴⁾	Configuration time ⁽⁵⁾	-	60	-	60	-	60	μs
T _{INIT} ⁽⁴⁾	ISP initialization time	-	60	-	60	-	60	μs
T _{POE} ⁽⁴⁾	P-term OE to output enabled	-	7.5	-	9.3	-	11.2	ns
T _{POD} ⁽⁴⁾	P-term OE to output disabled ⁽⁶⁾	-	7.5	-	9.3	-	11.2	ns
T _{PCO} ⁽⁴⁾	P-term clock to output	-	6.5	-	8.3	-	10.7	ns
T _{PAO} ⁽⁴⁾	P-term set/reset to output valid	-	8.0	-	9.3	-	11.2	ns

Notes:

1. Specifications measured with one output switching.
2. See XPLA3 family data sheet ([DS012](#)) for recommended operating conditions.
3. See [Figure 4](#) for derating.
4. These parameters guaranteed by design and/or characterization, not testing.
5. Typical current draw during configuration is 6 mA at 3.6V.
6. Output C_L = 5 pF.

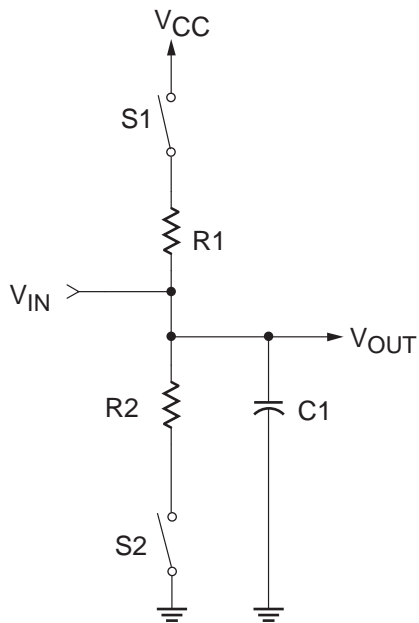
Internal Timing Parameters⁽²⁾

Symbol	Parameter	-6		-7		-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Buffer Delays								
T _{IN}	Input buffer delay	-	1.3	-	1.6	-	2.2	ns
T _{FIN}	Fast Input buffer delay	-	2.3	-	3.0	-	3.1	ns
T _{GCK}	Global Clock buffer delay	-	0.8	-	1.0	-	1.3	ns
T _{OUT}	Output buffer delay	-	2.2	-	2.7	-	3.6	ns
T _{EN}	Output buffer enable/disable delay	-	4.2	-	5.0	-	5.7	ns
Internal Register and Combinatorial Delays								
T _{LDI}	Latch transparent delay	-	1.3	-	1.6	-	2.0	
T _{SUI}	Register setup time	1.0	-	1.0	-	1.2	-	ns
T _{HI}	Register hold time	0.3	-	0.5	-	0.7	-	ns
T _{ECSU}	Register clock enable setup time	2.0	-	2.5	-	3.0	-	ns
T _{ECHO}	Register clock enable hold time	3.0	-	4.5	-	5.5	-	ns
T _{COI}	Register clock to output delay	-	1.0	-	1.3	-	1.6	ns
T _{AOI}	Register async. S/R to output delay	-	2.5	-	2.3	-	2.1	ns
T _{RAI}	Register async. recovery	-	4.0	-	5.0	-	6.0	ns
T _{LOGI1}	Internal logic delay (single p-term)	-	2.0	-	2.7	-	3.3	ns
T _{LOGI2}	Internal logic delay (PLA OR term)	-	2.5	-	3.2	-	4.2	ns
Feedback Delays								
T _F	ZIA delay	-	2.4	-	2.9	-	3.5	ns
Time Adders								
T _{LOGI3}	Fold-back NAND delay	-	6.0	-	7.5	-	9.5	ns
T _{UDA}	Universal delay	-	1.5	-	2.0	-	2.5	ns
T _{SLEW}	Slew rate limited delay	-	4.0	-	5.0	-	6.0	ns

Notes:

1. These parameters guaranteed by design and/or characterization, not testing.
2. See XPLA3 family data sheet ([DS012](#)) for timing model.

Switching Characteristics



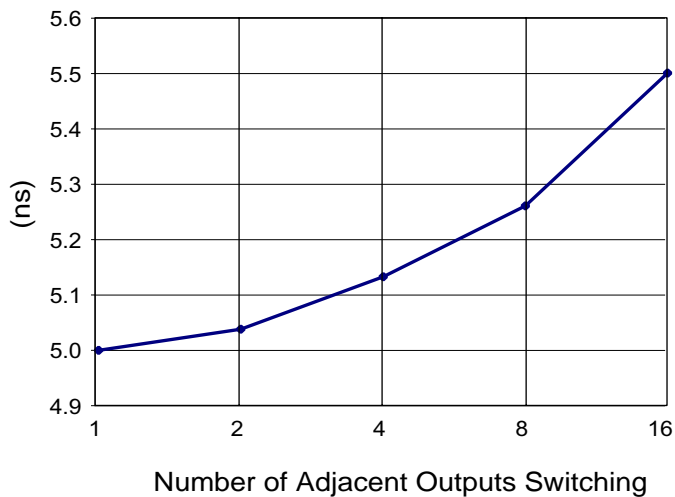
Component	Values
R1	390Ω
R2	390Ω
C1	35 pF

Measurement	S1	S2
T _{POE} (High)	Open	Closed
T _{POE} (Low)	Closed	Open
T _P	Closed	Closed

Note: For T_{POD}, C1 = 5 pF. Delay measured at output level of V_{OL} + 300 mV, V_{OH} - 300 mV.

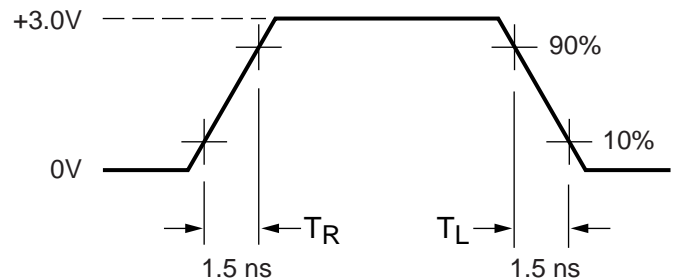
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Figure 3: AC Load Circuit



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Figure 4: Derating Curve for T_{PD2}



Measurements:

All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

DS017_05_042800

Figure 5: Voltage Waveform

Pin Descriptions

Table 2: XCR3064XL User I/O Pins

	PC44	VQ44	CS48	CP56	VQ100
Total User I/O Pins	36	36	40	48	68

Table 3: XCR3064XL I/O Pins

Function Block	Macro-cell	PC44	VQ44	CS48	CP56	VQ100
1	1	41	35	C5	C8	85
1	2	40	34	A6	A8	84
1	3	-	-	-	-	83
1	4	-	-	-	A9	81
1	5	-	-	-	A5	80
1	6	-	-	A7	A10	79
1	7	-	-	-	-	76
1	8	39	33	B6	B10	75
1	9	38 ⁽¹⁾	32 ⁽¹⁾	B7 ⁽¹⁾	C10 ⁽¹⁾	73 ⁽¹⁾
1	10	37	31	D4	D8	71
1	11	36	30	C6	E8	69
1	12	-	-	-	-	68
1	13	-	-	-	-	67
1	14	34	28	D6	F8	65
1	15	33	27	D7	E10	64
1	16	-	-	-	-	63
2	1	4	42	A2	C4	92
2	2	5	43	A1	C3	93
2	3	6	44	C4	A1	94
2	4	-	-	-	-	96
2	5	-	-	-	B1	97
2	6	-	-	-	-	98
2	7	-	-	-	A2	99
2	8	-	-	B2	A3	100
2	9	7 ⁽¹⁾	1 ⁽¹⁾	B1 ⁽¹⁾	C1 ⁽¹⁾	4 ⁽¹⁾
2	10	8	2	C2	D1	6
2	11	9	3	C1	D3	8
2	12	-	-	-	-	9
2	13	-	-	-	-	10
2	14	11	5	D3	E3	12

Table 3: XCR3064XL I/O Pins

Function Block	Macro-cell	PC44	VQ44	CS48	CP56	VQ100
2	15	12	6	D1	F1	13
2	16	-	-	-	-	14
3	1	32 ⁽¹⁾	26 ⁽¹⁾	E5 ⁽¹⁾	F10 ⁽¹⁾	62 ⁽¹⁾
3	2	31	25	E7	G8	61
3	3	-	-	-	-	60
3	4	29	23	F7	H10	58
3	5	-	-	-	-	57
3	6	-	-	-	-	56
3	7	-	-	F6	K8	54
3	8	-	-	-	K10	52
3	9	28	22	G7	K9	48
3	10	27	21	G6	J10	47
3	11	26	20	F5	H8	46
3	12	25	19	G5	H7	45
3	13	24	18	F4	H6	44
3	14	-	-	-	-	42
3	15	-	-	-	K7	41
3	16	-	-	-	-	40
4	1	13 ⁽¹⁾	7 ⁽¹⁾	D2 ⁽¹⁾	G1 ⁽¹⁾	15 ⁽¹⁾
4	2	14	8	E1	F3	16
4	3	-	-	-	-	17
4	4	16	10	F1	G3	19
4	5	17	11	G1	J1	20
4	6	-	-	-	-	21
4	7	-	-	-	-	23
4	8	-	-	-	K1	25
4	9	18	12	E4	K4	29
4	10	19	13	F2	K2	30
4	11	20	14	G2	K3	31
4	12	21	15	F3	H3	32
4	13	-	-	G3	H4	33
4	14	-	-	-	-	35
4	15	-	-	-	K5	36
4	16	-	-	-	-	37

Notes:

- JTAG pins

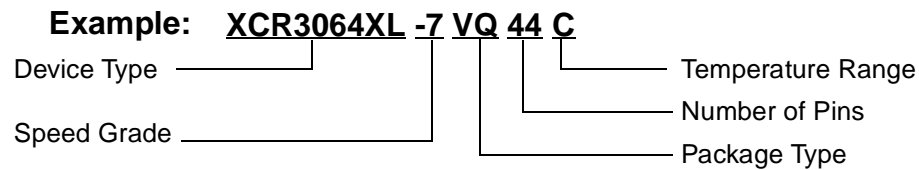
Table 4: XCR3064XL Global, JTAG, Port Enable, Power, and No connect Pins

Pin Type	PC44	VQ44	CS48	CP56	VQ100
IN0 / CLK0	2	40	A3	C5	90
IN1 / CLK1	1	39	B4	C6	89
IN2 / CLK2	44	38	A4	C7	88
IN3 / CLK3	43	37	B5	A6	87
TCK	32	26	E5	F10	62
TDI	7	1	B1	C1	4
TDO	38	32	B7	C10	73
TMS	13	7	D2	G1	15
PORT_EN	10 ⁽¹⁾	4 ⁽¹⁾	C3 ⁽¹⁾	E1 ⁽¹⁾	11 ⁽¹⁾
V _{CC}	3, 15, 23, 35	9, 17, 29, 41	B3, C7, E2, G4	A4, D10, H1, H5	3, 18, 34, 39, 51, 66, 82, 91
GND	22, 30, 42	16, 24, 36	A5, E3, E6	A7, G10, K6	26, 38, 43, 59, 74, 86, 95
No Connects	-	-	-	-	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78

Notes:

1. Port Enable is brought High to enable JTAG pins when JTAG pins are used as I/O. See family data sheet ([DS012](#)) for more information.

Ordering Information



Device Ordering Options

Speed	
-10	10 ns pin-to-pin delay
-7	7.5 ns pin-to-pin delay
-6	6 ns pin-to-pin delay

Package	
PC44	44-pin Plastic Leaded Chip Carrier
VQ44	44-pin Very Thin Quad Flat Pack
CS48	48-ball Chip Scale Package
CP56	56-ball Chip Scale Package
VQ100	100-pin Very Thin Quad Flat Package

Temperature	
C = Commercial	$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ $V_{CC} = 3.0\text{V}$ to 3.6V
I = Industrial	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 2.7\text{V}$ to 3.6V

Component Availability

Pins		100	56	48	44	44
Type		Plastic VQFP	Plastic BGA	Plastic BGA	Plastic VQFP	Plastic PLCC
Code		VQ100	CP56	CS48	VQ44	PC44
XCR3064XL	-6	C	C	C	C	C
	-7, -10	C,I	C,I	C,I	C,I	C,I

Revision History

The following table shows the revision history for this document..

Date	Version	Revision
06/01/00	1.0	Initial Xilinx release.
08/30/00	1.1	Added 48-ball CS BGA package.
11/18/00	1.2	Updated to full production data sheet; corrected note in Table 4 to read: "port enable pin is brought High".
12/08/00	1.3	Added PC44 package.
04/11/01	1.4	Added Typical I/V curve, Figure 2 ; added Table 2 : Total User I/O; changed V_{OH} spec.
04/19/01	1.5	Updated Typical I/V curve, Figure 2 : added voltage levels.
01/08/02	1.6	Moved I_{CC} vs. Freq Figure 1 and Table 1 to page 1. Added single p-term setup time (T_{SU1}) to AC Table, renamed T_{SU} to T_{SU2} for setup time through the OR array. Updated T_{SUF} and T_{FIN} spec to match software timing. Added T_{INIT} spec. Updated T_{CONFIG} spec. Updated T_{HI} spec to correct a typo. Updated AC Load Circuit diagram to more closely resemble true test conditions, added note for T_{POD} delay measurement. Updated note 5 in AC Characteristics table lowering typical current draw during configuration.