

Features

- Industries best 0.18 micron CMOS CPLD
 - 4.0 ns pin-to-pin logic delays
 - less than 100 μ A standby current consumption
 - 64 macrocells with up to 1,600 logic gates
 - Fast input registers
 - Slew rate control on individual outputs
 - LVCMOS 1.8V through 3.3V
 - LVTTTL 3.3V
- Available in multiple package styles
 - 44-pin PLCC with 33 user I/O
 - 44-pin VQFP with 33 user I/O
 - 56-ball CP (0.05mm) BGA with 45 user I/O
 - 100-pin VQFP with 64 user I/O
- Optimized for high performance 1.8V systems
 - Ultra low power operation
 - Advanced 0.18 micron 4-metal layer Non-volatile process
- Advanced system features
 - Quadruple enhanced security
 - Multi-voltage system interface
 - Hot pluggable
 - IEEE1532 In-system programmable
 - Superior pin locking through PLA array
 - Input hysteresis (Schmitt trigger) on all pins
 - Bus hold circuitry on all user pins
 - IEEE standard 1149.1 boundary scan (JTAG)
 - Fast programming times
 - Excellent pin retention during design changes
 - High quality and reliability
 - Guaranteed 10,000 program/erase cycles
 - 20 year data retention

Refer to the CoolRunner™-II family data sheet for architecture description.

Description

The CoolRunner-II 64-macrocell device is designed for both high performance and low power applications. This lends power savings to high-end communication equipment and speed to battery operated devices.

This device consists of four Function Blocks inter-connected by a low power Advanced Interconnect Matrix (AIM). The AIM feeds 40 inputs to each Function Block. The Function Blocks consist of a 40 by 56 p-term PLA and 16 macrocells which contain numerous configuration bits that allow for combinational or registered modes of operation. Additionally, these registers can be globally reset or preset and configured as a D or T flip-flop or as a D latch. There are also multiple clock signals, both global and local product term based, on a per macrocell basis. Output control signals include slew rate control, bus hold and open drain. An additional Schmitt-trigger input is available on a per input pin basis.

In addition to combinatorial and registered outputs, the registers may be configured as fast inputs.

Clocking is available on a global or Function Block basis. Three global clocks are available for all Function Blocks as a synchronous clock source. Global clocks are additionally used to set or preset individual macrocell registers on power up. Local clocks are generated in specific Function Blocks and only available to macrocell registers in that Function Block.

A DualEDGE flip-flop feature is also available on a per macrocell basis. This feature allows performance where it is needed without raising the total power consumption of the entire device.

The CoolRunner-II 64-macrocell CPLD is I/O compatible with standard LVTTTL33 and LVCMOS18, 25, and 33 volts (see Table 1).

Fast Zero Power Design Technology

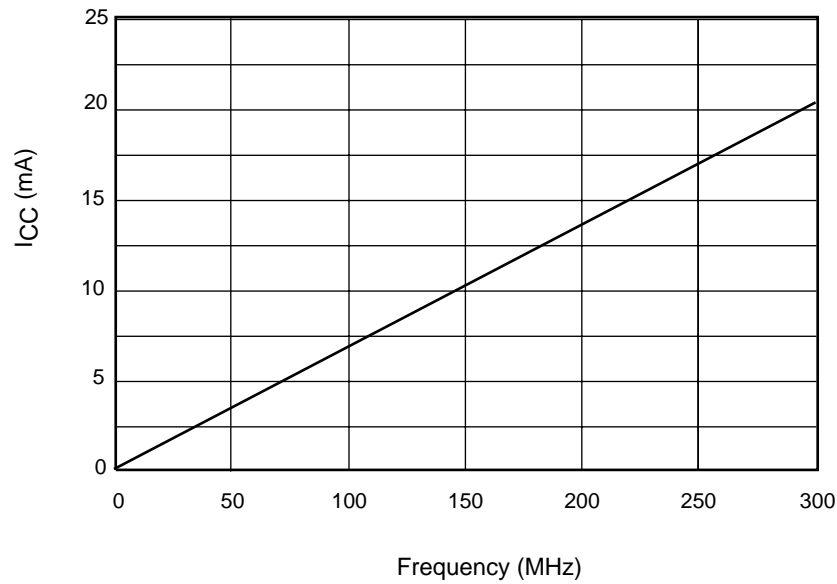
All CoolRunner-II CPLDs employ Fast Zero Power™ (FZP), a design technique that employs CMOS technology in both the fabrication and design methodology. Xilinx CoolRunner-II is fabricated on a 0.18 micron process technology which is derived from leading edge FPGA product development. CoolRunner-II design technology employs a cascade of CMOS gates to implement sum of products instead of traditional sense amplifier methodology. Due to this FZP technology, Xilinx CoolRunner-II CPLDs achieve both high performance and low power operation.

Supported I/O Standards

The CoolRunner-II 64 macrocell features both LVCMOS and LVTTTL I/O implementations. See [Table 1](#) for I/O standard voltages. The LVTTTL I/O standard is a general purpose EIA/JESDSA standard for 3.3V applications that use an LVTTTL input buffer and Push-Pull output buffer. The LVCMOS standard is used in 3.3V, 2.5V, 1.8V, and 1.5V applications. It does not require the use of a reference voltage or termination voltage.

Table 1: I/O Standards for XC2C64

I/O Standard	Output V_{CCIO}	Input V_{CCIO}	Input V_{REF}	Board Termination Voltage V_T
LVTTTL	3.3V	3.3V	N/A	N/A
LVCMOS33	3.3	3.3	N/A	N/A
LVCMOS25	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A



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Figure 1: I_{CC} vs Frequency

Table 2: I_{CC} vs Frequency (LVCMOS 1.8V T_A = 25°C)

	Frequency (MHz)										
	50	75	100	125	150	175	200	225	250	275	300
Typical I _{CC} (mA)	3.6	5.5	7.3	9.1	10.8	12.5	14.2	15.9	17.5	19.2	20.8

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to ground	-0.5 to 2.0	V
V_{CCIO}	Supply voltage for output drivers	-0.5 to 4.0	V
V_{IN}	Input voltage relative to ground ⁽¹⁾	-0.5 to 4.0	V
V_{TS}	Voltage applied to 3-state output ⁽¹⁾	-0.5 to 4.0	V
V_{STG}	Storage Temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum Soldering temperature (10s @ 1/16in. = 1.5mm)	+ 60	°C
T_J	Junction Temperature	+ 50	°C

Notes:

- Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easiest to achieve. During transitions, the device pins may undershoot to -2.0v or overshoot to +3.9V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units	
V_{CC}	Supply voltage for internal logic and input buffers	Commercial $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	1.7	1.9	V
		Industrial $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.7	1.9	V
V_{CCIO}	Supply voltage for output drivers @ 3.3V operation	3.0	3.6	V	
	Supply voltage for output drivers @ 2.5V operation	2.3	2.7	V	
	Supply voltage for output drivers @ 1.8V operation	1.7	1.9	V	
	Supply voltage for output drivers @ 1.5V operation ⁽¹⁾	1.4	1.6	V	

Notes:

- Use input hysteresis for 1.5V LVCMOS.

DC Electrical Characteristics (Over Recommended Operating Conditions)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		3.0	3.6	V
V_{IH}	High level input voltage		2.0	$V_{CCIO} + 0.3V$	V
V_{IL}	Low level input voltage		-0.3	0.8	V
V_{OH}	High level output voltage	$I_{OH} = -8\text{ mA}$, $V_{CCIO} = 3V$	2.4	-	V
V_{OL}	Low level input voltage	$I_{OL} = 8\text{ mA}$, $V_{CCIO} = 3V$	-	0.4	V
I_{IL}	Input leakage current	$V_{IN} = 0$ or V_{CCIO}	-10	10	μA
I_{IH}	I/O High-Z leakage	$V_{IN} = 0$ or V_{CCIO}	-10	10	μA
I_{CCSB}	Standby current	$V_{CC} = 1.9V$, $V_{CCIO} = 3.6V$		100	μA
I_{CC}	Dynamic current	$f = 1\text{ MHz}$			mA
		$f = 50\text{ MHz}$			mA
C_{JTAG}	JTAG input capacitance	$f = 1\text{ MHz}$			pF
C_{CLK}	Global clock input capacitance	$f = 1\text{ MHz}$			pF
C_{IO}	I/O capacitance	$f = 1\text{ MHz}$			pF

LVC MOS 3.3V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		3.0	3.6	V
V_{IH}	High level input voltage		2	$V_{CCIO} + 0.3V$	V
V_{IL}	Low level input voltage		-0.3	0.8	V
V_{OH}	High level output voltage	$I_{OH} = -8 \text{ mA}, V_{CCIO} = 3V$	$V_{CCIO} - 0.4V$	-	V
		$I_{OH} = -0.1 \text{ mA}, V_{CCIO} = 3V$	$V_{CCIO} - 0.2V$	-	V
V_{OL}	Low level output voltage	$I_{OL} = 8 \text{ mA}, V_{CCIO} = 3V$	-	0.4	V
		$I_{OL} = 0.1 \text{ mA}, V_{CCIO} = 3V$	-	0.2	V
I_{IL}	Input leakage current	$V_{IN} = 0V \text{ or } V_{CCIO}$	-10	10	μA
I_{IH}	I/O High-Z leakage	$V_{IN} = 0V \text{ or } V_{CCIO}$	-10	10	μA
C_{JTAG}	JTAG input capacitance	$f = 1 \text{ MHz}$			pF
C_{CLK}	Global clock input capacitance	$f = 1 \text{ MHz}$			pF
C_{IO}	I/O capacitance	$f = 1 \text{ MHz}$			pF

LVC MOS 2.5V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		2.3	2.7	V
V_{IH}	High level input voltage		1.7	3.9	V
V_{IL}	Low level input voltage		-0.3	0.7	V
V_{OH}	High level output voltage	$I_{OH} = -8 \text{ mA}, V_{CCIO} = 3V$	$V_{CCIO} - 0.4V$	-	V
		$I_{OH} = -0.1 \text{ mA}, V_{CCIO} = 3V$	$V_{CCIO} - 0.2V$	-	V
V_{OL}	Low level output voltage	$I_{OL} = 8 \text{ mA}, V_{CCIO} = 3V$	-	0.4	V
		$I_{OL} = 0.1 \text{ mA}, V_{CCIO} = 3V$	-	0.2	V
I_{IL}	Input leakage current	$V_{IN} = 0V \text{ or } V_{CCIO}$	-10	10	V
I_{IH}	I/O High-Z leakage	$V_{IN} = 0V \text{ or } V_{CCIO} \text{ to } 3.9V$	-10	10	V
C_{JTAG}	JTAG input capacitance	$f = 1 \text{ MHz}$			pF
C_{CLK}	Global clock input capacitance	$f = 1 \text{ MHz}$			pF
C_{IO}	I/O capacitance	$f = 1 \text{ MHz}$			pF

LVCMOS 1.8V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		1.7	1.9	V
V_{IH}	High level input voltage		$0.7 \times V_{CCIO}$	3.9	V
V_{IL}	Low level input voltage		-0.3	$0.2 \times V_{CCIO}$	V
V_{OH}	High level output voltage	$I_{OH} = -8 \text{ mA}, V_{CCIO} = 3V$	$V_{CCIO} - 0.45$	-	V
		$I_{OH} = -0.1 \text{ mA}, V_{CCIO} = 3V$	$V_{CCIO} - 0.2$	-	V
V_{OL}	Low level input voltage	$I_{OL} = 8 \text{ mA}, V_{CCIO} = 3V$	-	0.45?	V
		$I_{OL} = 0.1 \text{ mA}, V_{CCIO} = 3V$	-	0.2	V
I_{IL}	Input leakage current	$V_{IN} = 0 \text{ or } V_{CCIO} \text{ to } 3.9V$	-10	10	μA
I_{IH}	I/O High-Z leakage	$V_{IN} = 0 \text{ or } V_{CCIO} \text{ to } 3.9V$	-10	10	μA
C_{JTAG}	JTAG input capacitance	$f = 1 \text{ MHz}$			pF
C_{CLK}	Global clock input capacitance	$f = 1 \text{ MHz}$			pF
C_{IO}	I/O capacitance	$f = 1 \text{ MHz}$			pF

1.5V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		1.4	1.6	V
V_{IH}	High level input voltage		$0.7 \times V_{CCIO}$	3.9	V
V_{IL}	Low level input voltage		-0.3	0.3	V
V_{OH}	High level output voltage	$I_{OH} = -8 \text{ mA}, V_{CCIO} = 3V$	$V_{CCIO} - 0.45$		V
		$I_{OH} = -0.1 \text{ mA}, V_{CCIO} = 3V$	$V_{CCIO} - 0.2$		V
V_{OL}	Low level input voltage	$I_{OL} = 8 \text{ mA}, V_{CCIO} = 3V$		0.4	V
		$I_{OL} = 0.1 \text{ mA}, V_{CCIO} = 3V$		0.2	V
I_{IL}	Input leakage current	$V_{IN} = 0 \text{ or } V_{CCIO} \text{ to } 3.9V$	-10	10	μA
I_{IH}	I/O High-Z leakage	$V_{IN} = 0 \text{ or } V_{CCIO} \text{ to } 3.9V$	-10	10	μA
C_{JTAG}	JTAG input capacitance	$f = 1 \text{ MHz}$			pF
C_{CLK}	Global clock input capacitance	$f = 1 \text{ MHz}$			pF
C_{IO}	I/O capacitance	$f = 1 \text{ MHz}$			pF

AC Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	-4		-5		-7		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
T _{PD1}	Propagation delay single p-term	-	3.7	-	4.6	-	6.7	ns
T _{PD2}	Propagation delay OR array	-	4.0	-	5.0	-	7.5	ns
T _{SU1}	Setup time fast	1.6	-	1.9	-	2.3	-	ns
T _{SU2}	Setup time	2.0	-	2.4	-	3.3	-	ns
T _{H1}	Fast input register hold time	0	-	0	-	0	-	ns
T _{H2}	P-term hold time	0	-	0	-	0	-	ns
T _{CO}	Clock to output	-	3.0	-	3.9	-	6.0	ns
T _{TOGGLE}	Internal toggle rate	-	416	-	250	-	168	MHz
F _{SYSTEM}	Maximum system frequency	-	270	-	213	-	141	MHz
F _{EXT}	Maximum external frequency	-	200	-	159	-	108	MHz
T _{PSU1}	Fast input register p-term clock setup time	1.0	-	1.2	-	1.5	-	ns
T _{PSU2}	P-term clock setup time	1.4	-	1.7	-	2.5	-	ns
T _{PH1}	Fast input register p-term clock hold time	0.4	-	0.6	-	0.7	-	ns
T _{PH2}	P-term clock hold	0.3	-	0.5	-	0.5	-	ns
T _{PCO}	P-term clock to output	-	3.6	-	4.6	-	6.8	ns
T _{OE/TOD}	Global OE to output enable/disable	-	3.9	-	4.9	-	7.0	ns
T _{POE/TPOD}	P-term OE to output enable/disable	-	4.3	-	5.3	-	7.3	ns
T _{MOE/TMOD}	Macrocell driven OE to output enable/disable	-	4.9	-	6.3	-	9.2	ns
T _{PAO}	P-term set/reset to output valid	-	5.4	-	6.4	-	9.1	ns
T _{AO}	Global set/reset to output valid	-	5.5	-	6.5	-	9.3	ns
T _{SUEC1}	Fast input register clock enable setup time	1.6	-	1.9	-	2.3	-	ns
T _{SUEC2}	Register clock enable setup time	2.0	-	2.4	-	3.3	-	ns
T _{HEC1}	Fast input register clock enable hold time	0	-	0	-	0	-	ns
T _{HEC2}	Register clock enable hold time	0	-	0	-	0	-	ns
T _{CW}	Global clock pulse width High or Low	1.2	-	2.0	-	3.0	-	ns
T _{PCW}	P-term pulse width High or Low	4.0	-	5.0	-	7.5	-	ns
T _{CONFIG}	Configuration time							us

Internal Timing Parameters

Symbol	Parameter ⁽¹⁾	-4		-5		-7		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Buffer Delays								
T _{IN}	Input buffer delay	-	1.3	-	1.7	-	2.4	ns
T _{FIN}	Fast data register input delay	-	1.6	-	2.1	-	3.0	ns
T _{GCK}	Global Clock buffer delay	-	1.2	-	1.6	-	2.5	ns
T _{GSR}	Global set/reset buffer delay	-	1.9	-	2.4	-	3.5	ns
T _{GTS}	Global 3-state buffer delay	-	1.4	-	1.9	-	3.0	ns
T _{OUT}	Output buffer delay	-	1.6	-	1.9	-	2.8	ns
T _{EN}	Output buffer enable/disable delay	-	2.5	-	3.0	-	4.0	ns
P-term Delays								
T _{CT}	Control term delay	-	0.5	-	0.6	-	0.9	ns
T _{LOGI1}	Single P-term delay adder	-	0.4	-	0.5	-	0.8	ns
T _{LOGI2}	Multiple P-term delay adder	-	0.3	-	0.4	-	0.8	ns
Macrocell Delay								
T _{PDI}	Input to output valid	-	0.4	-	0.5	-	0.7	ns
T _{SUI}	Setup before clock	1.2	-	1.4	-	1.8	-	ns
T _{HI}	Hold after clock	0	-	0	-	0	-	ns
T _{ECSU}	Enable clock setup time	1.2	-	1.4	-	1.8	-	ns
T _{ECHO}	Enable clock hold time	0	-	0	-	0	-	ns
T _{COI}	Clock to output valid	-	0.2	-	0.4	-	0.7	ns
T _{AOI}	Set/reset to output valid	-	2.0	-	2.2	-	3.0	ns
T _{CDBL}	Clock doubler delay	-	0	-	0	-	0	ns
Feedback Delays								
T _F	Feedback delay	-	1.6	-	2.0	-	3.0	ns
T _{OEM}	Macrocell to global OE delay	-	1.0	-	1.3	-	2.0	ns
I/O Standard Time Adder Delays 1.5V CMOS								
T _{IN15}	Standard input adder							ns
T _{HYS15}	Hysteresis input adder							ns
T _{OUT15}	Output adder							ns
T _{SLEW15}	Output slew rate adder							ns
I/O Standard Time Adder Delays 1.8V CMOS								
T _{IN18}	Standard input adder	-	0	-	0	-	0	ns
T _{HYS18}	Hysteresis input adder	-	2.0	-	3.0	-	4.0	ns
T _{OUT18}	Output adder	-	0	-	0	-	0	ns
T _{SLEW}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays 2.5V CMOS								

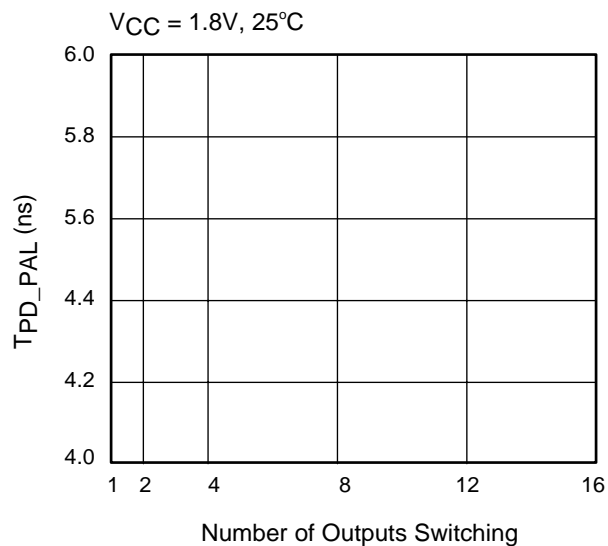
Internal Timing Parameters (Continued)

Symbol	Parameter ⁽¹⁾	-4		-5		-7		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
T _{IN25}	Standard input adder	-	0.5	-	0.8	-	1.0	ns
T _{HYS25}	Hysteresis input adder	-	1.5	-	2.5	-	3.0	ns
T _{OUT25}	Output adder	-	1.5	-	2.5	-	3.0	ns
T _{SLEW25}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays 3.3V CMOS/TTL								
T _{IN33}	Standard input adder	-	0.7	-	1.0	-	2.0	ns
T _{HYS33}	Hysteresis input adder	-	1.0	-	2.0	-	3.0	ns
T _{OUT33}	Output adder	-	1.0	-	2.0	-	3.0	ns
T _{SLEW33}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns

Notes:

1. 1.5 ns input pin signal rise/fall.

Switching Characteristics



DS092_09_121501

Pin Descriptions

Function Block	Macro-cell	PC44	VQ44	CP56	VQ100
1	1	44	38	F1	13
1	2	43	37	E3	12
1	3	42	36	E1	11
1	4	-	-	-	10
1	5	-	-	-	9
1	6	-	-	-	8
1	7	-	-	D3	7
1	8	-	-	-	6
1(GTS1)	9	40	34	D1	4
1(GTS0)	10	39	33	C1	3
1(GTS3)	11	38	32	A3	2
1(GTS2)	12	37	31	A2	1
1(GRS)	13	36	30	B1	99
1	14	-	-	A1	97
1	15	-	-	C3	94
1	16	-	-	A4	92
2	1	1	39	G1	14
2	2	2	40	F3	15
2	3	-	-	-	16
2	4	-	-	-	17
2	5	3	41	H1	18
2	6	4	42	G3	19
2(GCK0)	7	5	43	J1	22
2(GCK1)	8	6	44	K1	23
2	9	-	-	K4	24
2(GCK2)	10	7	1	K2	27
2	11	-	-	-	28
2	12	8	2	K3	29
2	13	9	3	H3	30
2	14	-	-	K5	32
2	15	-	-	-	33
2	16	-	-	-	34

Pin Descriptions (Continued)

Function Block	Macro-cell	PC44	VQ44	CP56	VQ100
3	1	35	29	C4	91
3	2	34	28	A4	90
3	3	33	27	C5	89
3	4	-	-	A7	81
3	5	-	-	C8	79
3	6	29	23	A8	78
3	7	-	-	A9	77
3	8	-	-	-	76
3	9	-	-	A5	74
3	10	28	22	A10	72
3	11	27	21	B10	71
3	12	26	20	C10	70
3	13	-	-	D8	68
3	14	25	19	E8	67
3	15	24	18	D10	64
3	16	-	-	-	61
4	1	11	5	K6	35
4	2	12	6	H5	36
4	3	-	-	-	37
4	4	-	-	-	39
4	5	-	-	H7	40
4	6	-	-	-	41
4	7	14	8	H8	42
4	8	-	-	-	43
4	9	-	-	-	49
4	10	-	-	K8	50
4	11	18	12	H10	52
4	12	-	-	-	53
4	13	19	13	G10	55
4	14	20	14	-	56
4	15	22	16	F10	58
4	16	-	-	E10	60

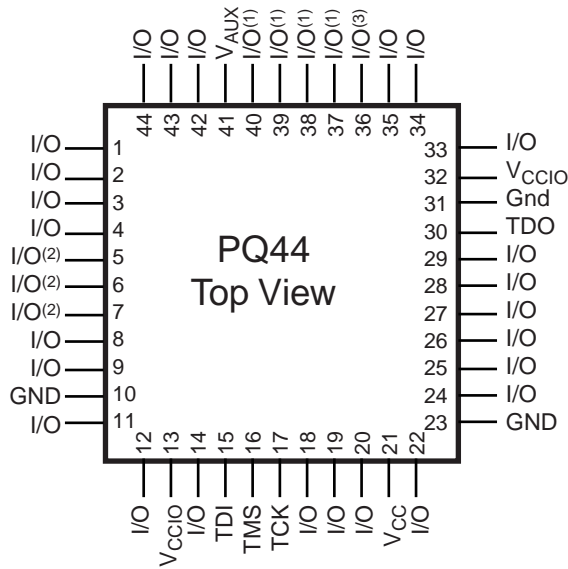
Note: GTS = global output enable, GRS = global reset/set, GCK = global clock x

XC2C64 Global, JTAG, Power/Ground and No Connect Pins

Pin Type	PC44	VQ44	CP56	VQ100
TCK	17	11	K10	48
TDI	15	9	J10	45
TDO	30	24	A6	83
TMS	16	10	K9	47
V _{AUX} (JTAG supply voltage)	41	35	D3	5
Power internal (V _{CC})	21	15	G8	26,57
Power external I/O (V _{CCIO})	13, 32	7,26	H6, C6	38, 51,88, 98
Ground	10,23,31	4,17,25	H4, F8, C7	21,31,62,69,84,100
No connects				20,25,44,46,54,59,63,65,66,73,75, 80,82,85,86,87,93,95,96
Total user I/O	33	33	45	64

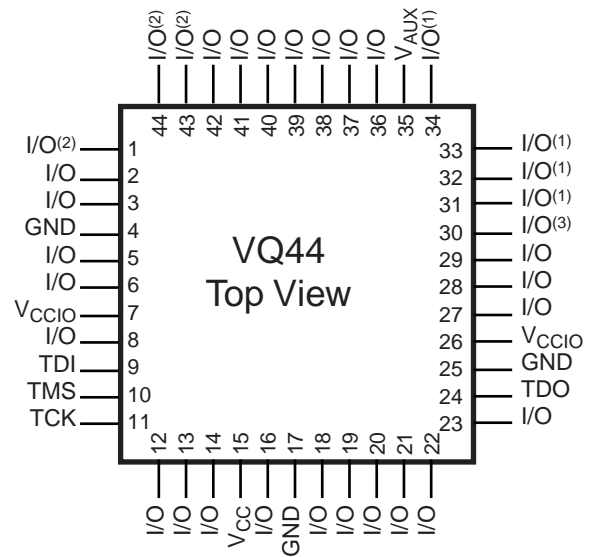
Ordering Information

Part Number	Pin/Ball Spacing	θ_{JA} (C/Watt)	θ_{JC} (C/Watt)	Package Type	I/O	Commercial (C) Industrial (I)
XC2C64-4PC44C	1.27mm	53.1	28.7	Plastic Leaded Chip Carrier	33	C
XC2C64-5PC44C	1.27mm	53.1	28.7	Plastic Leaded Chip Carrier	33	C
XC2C64-7PC44C	1.27mm	53.1	28.7	Plastic Leaded Chip Carrier	33	C
XC2C64-4VQ44C	0.8mm	46.6	8.2	Very Thin Quad Flat Pack	33	C
XC2C64-5VQ44C	0.8mm	46.6	8.2	Very Thin Quad Flat Pack	33	C
XC2C64-7VQ44C	0.8mm	46.6	8.2	Very Thin Quad Flat Pack	33	C
XC2C64-4CP56C	0.5mm	65.0	15.0	Chip Scale Package	45	C
XC2C64-5CP56C	0.5mm	65.0	15.0	Chip Scale Package	45	C
XC2C64-7CP56C	0.5mm	65.0	15.0	Chip Scale Package	45	C
XC2C64-4VQ100C	0.5mm	53.2	14.6	Very Thin Quad Flat Pack	64	C
XC2C64-5VQ100C	0.5mm	53.2	14.6	Very Thin Quad Flat Pack	64	C
XC2C64-7VQ100C	0.8mm	53.2	14.6	Very Thin Quad Flat Pack	64	C
XC2C64-5PC44I	1.27mm	53.1	28.7	Plastic Leaded Chip Carrier	33	I
XC2C64-7PC44I	1.27mm	53.1	28.7	Plastic Leaded Chip Carrier	33	I
XC2C64-5VQ44I	0.8mm	46.6	8.2	Very Thin Quad Flat Pack	33	I
XC2C64-7VQ44I	0.8mm	46.6	8.2	Very Thin Quad Flat Pack	33	I
XC2C64-5CP56I	0.5mm	65.0	15.0	Chip Scale Package	45	I
XC2C64-7CP56I	0.5mm	65.0	15.0	Chip Scale Package	45	I
XC2C64-5VQ100I	0.5mm	53.2	14.6	Very Thin Quad Flat Pack	64	I
XC2C64-7VQ100I	0.5mm	53.2	14.6	Very Thin Quad Flat Pack	64	I



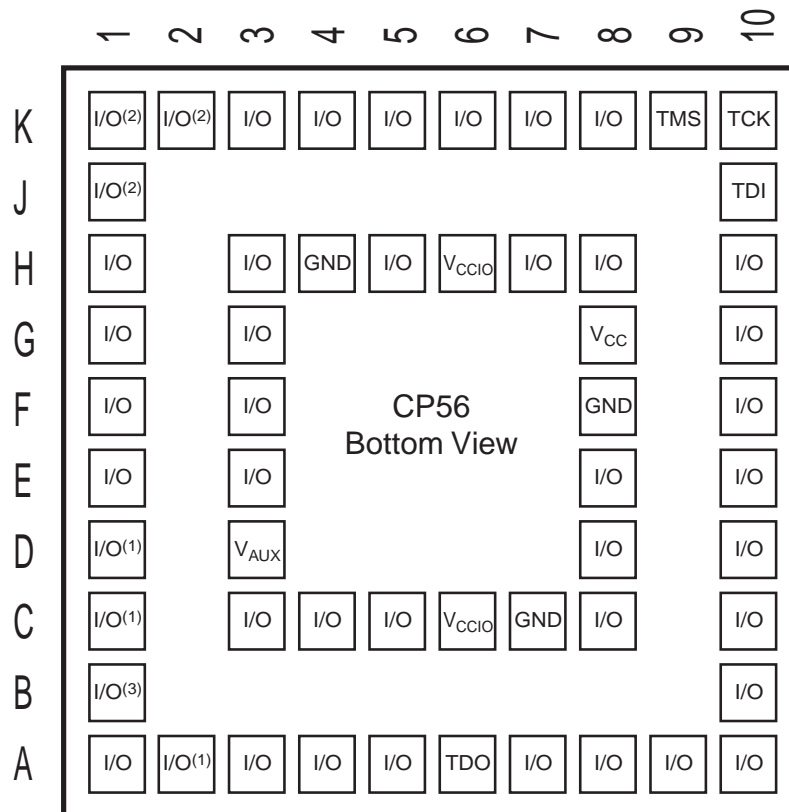
- (1) - Global Output Enable
- (2) - Global Clock
- (3) - Global Set/Reset

Figure 2: PQ44 Package



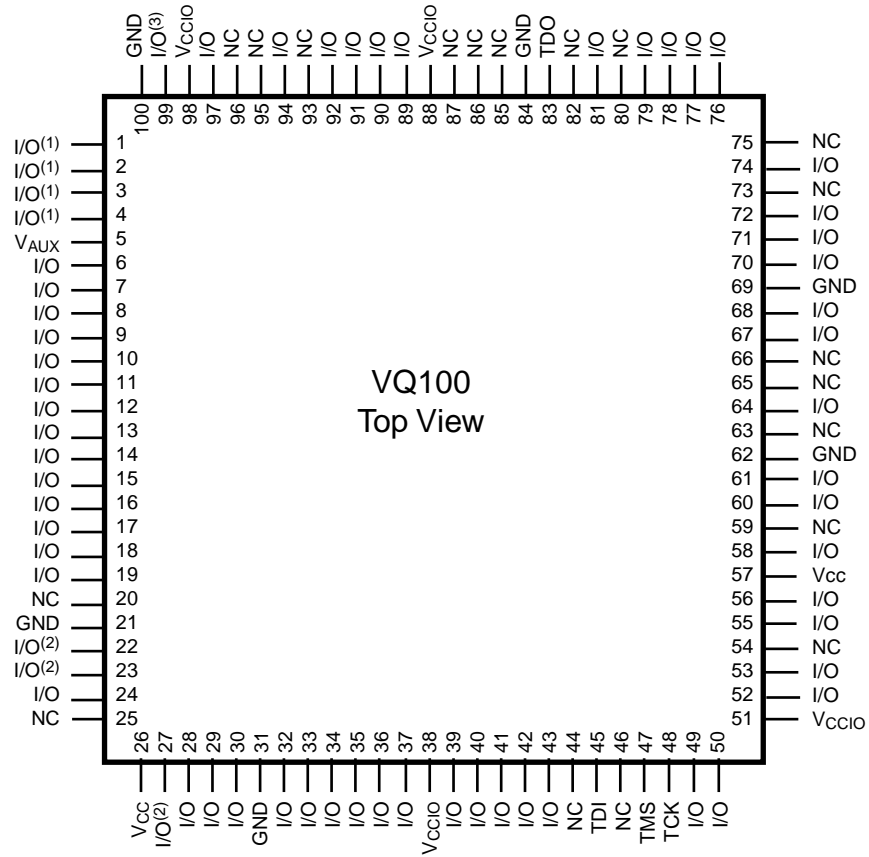
- (1) - Global Output Enable
- (2) - Global Clock
- (3) - Global Set/Reset

Figure 3: VQ44 Package



- (1) - Global Output Enable
- (2) - Global Clock
- (3) - Global Set/Reset

Figure 4: CP56 Package



- (1) - Global Output Enable
- (2) - Global Clock
- (3) - Global Set/Reset

Figure 5: VQ100 Package

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/19/01	0.1	Initial final draft.