Features

- High Density, High Performance Electrically Erasable Complex Programmable Logic Device
  - 256 Macrocells
  - 5 Product Terms per Macrocell, Expandable up to 40 per Macrocell
  - 160, 192, 208-pins
  - 10 ns Maximum Pin-to-Pin Delay
  - Registered Operation Up To 100 MHz
  - Enhanced Routing Resources
- Flexible Logic Macrocell
  - D/T/Latch Configurable Flip Flops
  - Global and Individual Register Control Signals
  - Global and Individual Output Enable
  - Programmable Output Slew Rate
  - Programmable Output Open Collector Option
  - Maximum Logic utilization by burying a register within a COM output
- Advanced Power Management Features
  - Automatic 3 mA Stand-By for “L” Version (Max.)
  - Pin-Controlled 4 mA Stand-By Mode (Typical)
  - Programmable Pin-Keeper Inputs and I/Os
  - Reduced-Power Feature Per Macrocell
- Available in Commercial and Industrial Temperature Ranges
- Available in 160-pin PQFP, 192 PGA and 208-pin RQFP Packages
- Advanced EE Technology
  - 100% Tested
  - Completely Reprogrammable
  - 100 Program/Erase Cycles
  - 20 Year Data Retention
  - 2000V ESD Protection
  - 200 mA Latch-Up Immunity
- JTAG Boundary-Scan Testing to IEEE Std. 1149.1-1990 and 1149.1a-1993 Supported
- Fast In-System Programmability (ISP) via JTAG
- PCI-compliant
- 3.3 or 5.0V I/O pins
- Security Fuse Feature

Enhanced Features

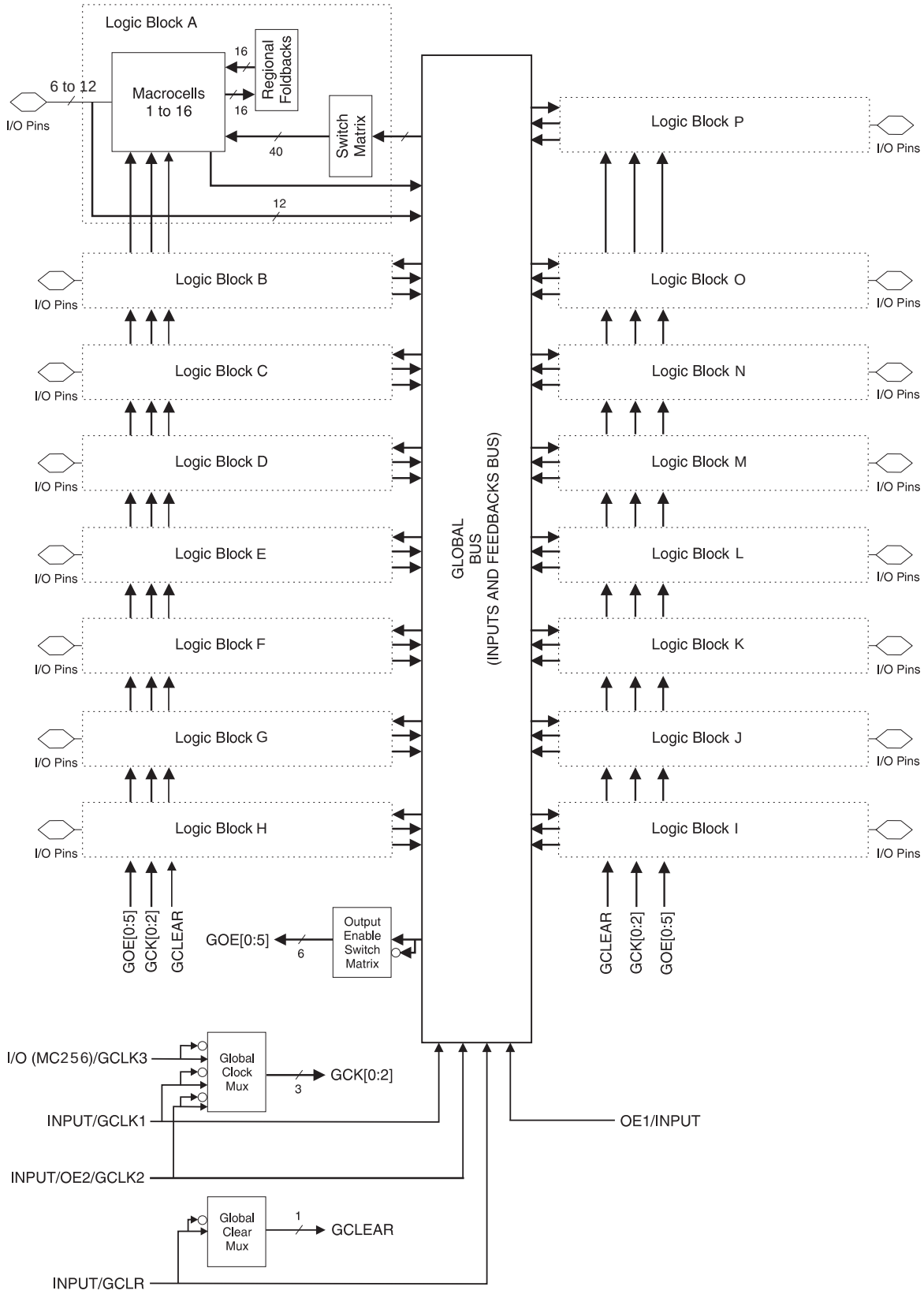
- Improved Connectivity (Additional Feedback Routing, Alternate Input Routing)
- Output Enable Product Terms
- D - Latch Mode
- Combinatorial Output with Registered Feedback within any Macrocell
- Three Global Clock Pins
- ITD (Input Transition Detection) Circuits on Global Clocks, Inputs and I/O
- Fast Registered Input from Product Term
- Programmable “Pin-Keeper” Option
- V_{CC} Power-Up Reset Option
- Pull-Up Option on JTAG Pins TMS and TDI
- Advanced Power Management Features
  - Edge Controlled Power Down “L”
  - Individual Macrocell Power Option
  - Disable ITD on Global Clocks, Inputs and I/O

High Performance EE-Based CPLD

ATF1516AS/L Preliminary

Rev. 0994A-A–01/98

Block Diagram



Description

The ATF1516AS is a high performance, high density Complex Programmable Logic Device (CPLD) which utilizes Atmel's proven electrically erasable technology. With 256 logic macrocells and up to 164 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1516AS's enhanced routing switch matrices increase usable gate count, and increase odds of successful pin-locked design modifications.

The ATF1516AS has up to 160 bi-directional I/O pins and 4 dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal; register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

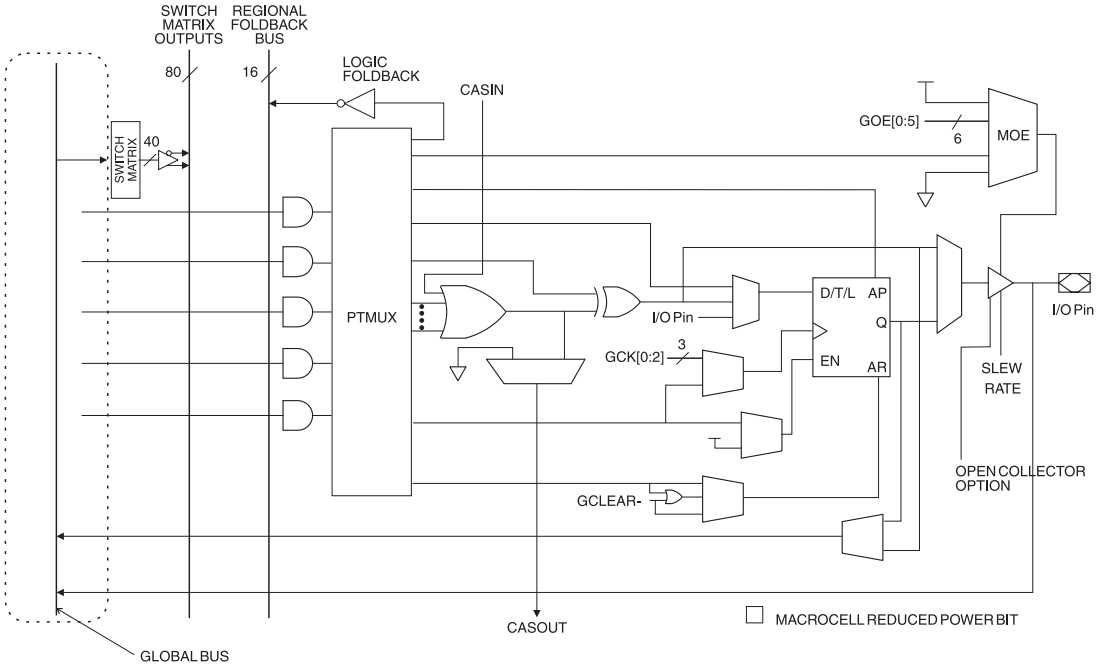
Each of the 256 macrocells generates a buried feedback, which goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term, which goes to a regional bus. Cascade logic between macrocells in the ATF1516AS allows fast, efficient generation of complex logic functions. The ATF1516AS contains eight such logic chains, each capable of creating sum term logic with a fan in of up to 40 product terms

The ATF1516AS macrocell, shown in Figure 1, is flexible enough to support highly complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer; OR/XOR/CASCADE logic; a flip-flop; output select and enable; and logic array inputs.

Unused Macrocells are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the contents of the ATF1516AS. Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

The ATF1516AS device is an In-System Programmable (ISP) device. It uses the industry standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully compliant with JTAG's Boundary Scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Figure 1. ATF1516AS Macrocell



Product Terms and Select MUX

Each ATF1516AS macrocell has five product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

OR/XOR/CASCADE Logic

The ATF1516AS's logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with a very small additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high or low level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms. The XOR gate is also used to emulate T- and JK-type flip-flops.

Flip Flop

The ATF1516AS's flip flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can either be the Global CLK Signal (GCK) or an individual product term. The flip flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

Output Select and Enable

The ATF1516AS macrocell output can be selected as registered or combinatorial. The buried feedback signal can be either combinatorial or registered signal regardless of whether the output is combinatorial or registered.

The output enable multiplexer (MOE) controls the output enable signals. Any buffer can be permanently enabled for simple output operation. Buffers can also be permanently disabled to allow use of the pin as an input. In this configuration all the macrocell resources are still available, including the buried feedback, expander and CASCADE logic. The output enable for each macrocell can be selected as either of the two dedicated OE input pins as an I/O pin configured as an input, or as an individual product term.

Global Bus/Switch Matrix

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 256 macrocells. The Switch Matrix in each Logic Block receives as its inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the Logic Block.

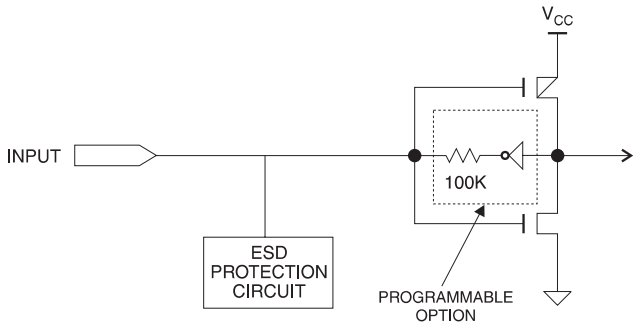
Foldback Bus

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to 16 macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The 16 foldback terms in each region allows generation of high fan-in sum terms (up to 21 product terms) with a small additional delay.

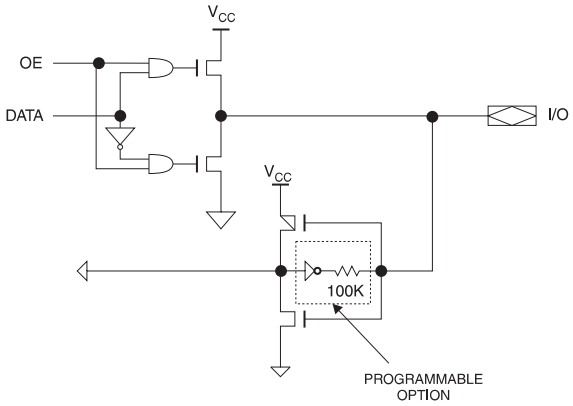
Programmable Pin-Keeper Option for Inputs and I/Os

The ATF1516AS offers the option of programming all input and I/O pins so that “pin keeper” circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which cause unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Input Diagram



I/O Diagram



Speed/Power Management

The ATF1516AS has several built-in speed and power management features. The ATF1516AS contains circuitry that automatically puts the device into a low power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides a proportional power savings for most applications running at system speeds below 50 MHz.

To further reduce power, each ATF1516AS macrocell has a Reduced Power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

All ATF1516ASs also have an optional power down mode. In this mode, current drops to below 10 mA. When the power down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. The power down option is selected in the design source file. When enabled, the device goes into power down when either PD1 or PD2 is high. In the power down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin’s macrocell may still be used to generate buried foldback and cascade logic signals.

All Power-Down AC Characteristic parameters are computed from external input or I/O pins, with Reduced Power Bit turned on. For macrocells in reduced-power mode (Reduced power bit turned on), the reduced power adder, tRPA, must be added to the AC parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH} and t_{SEXP}.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

Design Software Support

ATF1516AS designs are supported by several third party tools. Automated fitters allow logic synthesis using a variety of high level description languages and formats.

Power Up Reset

The ATF1516AS has a power-up reset option at two different voltage trip levels when the device is being powered down. Within the fitter, or during a conversion, if the “power-reset” option is turned “on” (which is the default option), the trip levels during power up or power down is at 2.8V. The user can change this default option from “on” to “off” (within the fitter or specify it as a switch during conversion). When this is done, the voltage trip level during power-down changes from 2.8V to 0.7V. This is to ensure a robust operating environment.

The registers in the ATF1516AS are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. The output state will depend on the polarity of the buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and,
3. The clock must remain stable during T_{PR}.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF1516AS fuse patterns. Once programmed, fuse verify is inhibited. However, User Signature and device ID remains accessible.

Programming

ATF1516AS devices are In-System Programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for program and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the ATF1516AS via the PC. ISP is perfomed by using either a download cable, or a comparable board tester or a simple microprocessor interface.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors. Serial Vector Format (SVF) files can be created by Atmel provided Software utilities.

ATF1516AS devices can also be programmed using standard 3rd party programmers. With 3rd party programmer the JTAG ISP port can be disabled thereby allowing 4 additional I/O pins to be used for logic.

Contact your local Atmel representatives or Atmel PLD applications for details.

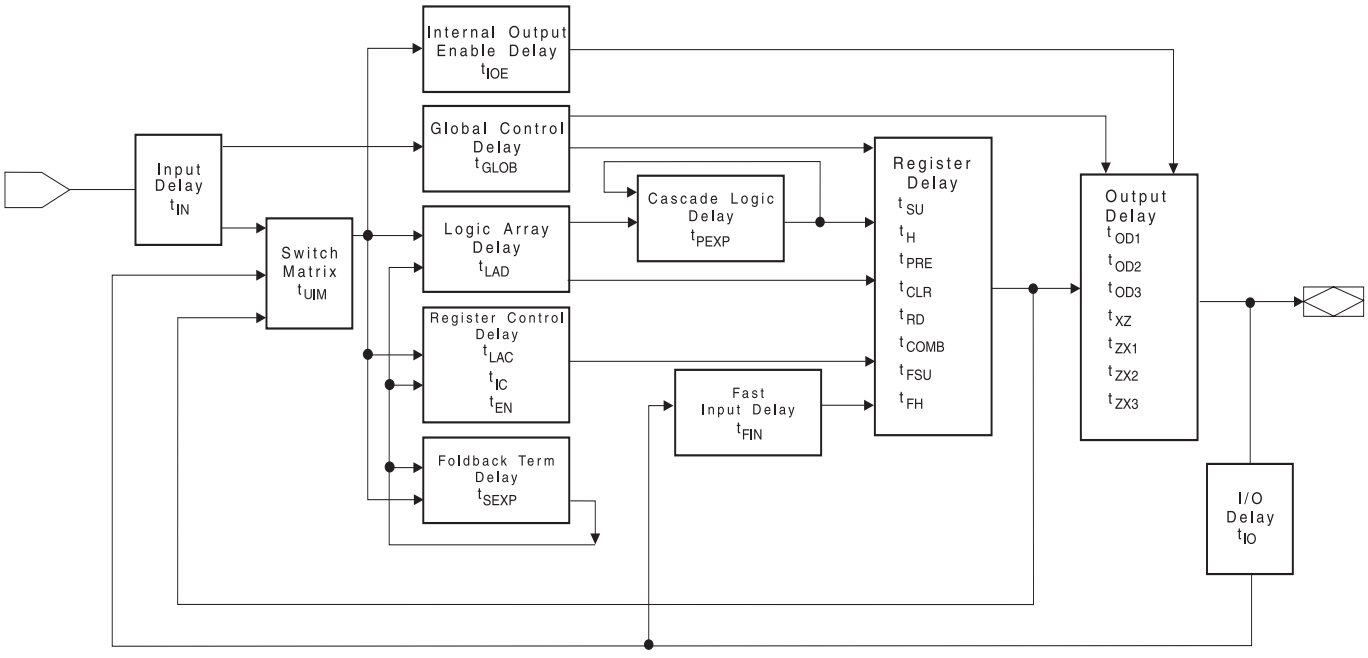
ISP Programming Protection

The ATF1516AS has a special feature which locks the device and prevents the inputs and I/O from driving if the programming process is interrupted due to any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin keeper option preserves the former state during device programming.

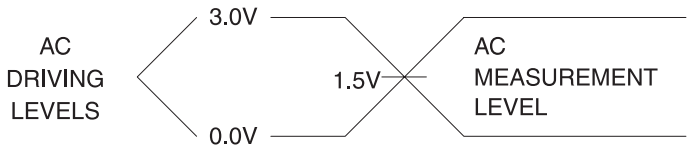
All ATF1516AS devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the “Desigining for In-System Programmability with Atmel CPLDs” application note.

Timing Model

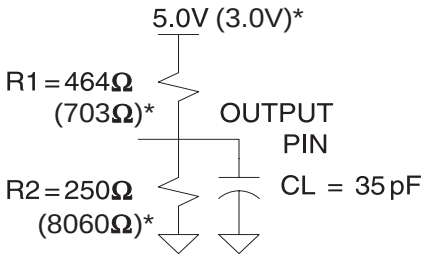


Input Test Waveforms and Measurement Levels



r_R, t_F = 1.5 ns typical

Output AC Test Loads:



Note: *Numbers in parenthesis refer to 3.0V operating conditions (preliminary).

Power Down Mode

The ATF1516AS includes two pins for optional pin controlled power down feature. When this mode is enabled, the PD pin acts as the power down pin. When the PD1 and PD2 pin is high, the device supply current is reduced to less than 3 mA. During power down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs which were in a Hi-Z state at the onset will remain at Hi-Z. During power down, all input signals except the power down pin are blocked. Input and I/O hold latches remain active to insure that pins do not float to indeterminate levels, further reducing system power. The power down pin feature is enabled in the logic design file. Designs using either power down pin may not use the PD pin logic array input. However, all other PD pin as macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

JTAG-BST Overview

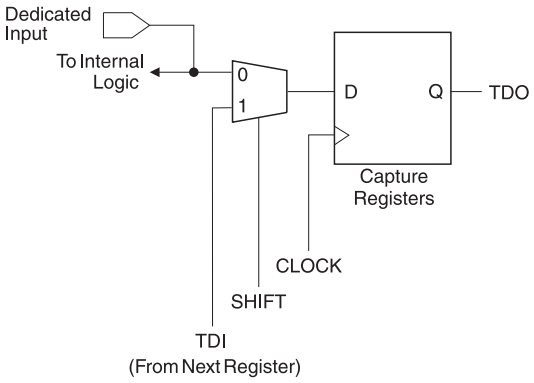
The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1516AS. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own boundary scan cell (BSC) in order to support boundary scan testing. The ATF1516AS does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power up. The six JTAG BST modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE. BST on the ATF1516AS is implemented using the Boundary Scan Definition Language (BSDL) described in the JTAG specification (IEEE Standard 1149.1). Any third party tool that supports the BSDL format can be used to perform BST on the ATF1516AS.

The ATF1516AS also has the option of using four JTAG-standard I/O pins for in-system programming (ISP). The ATF1516AS is programmable through the four JTAG pins using programming compatible with the IEEE JTAG Standard 1149.1. Programming is performed by using 5V TTL-level programming signals from the JTAG ISP interface. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

JTAG Boundary Scan Cell (BSC) Testing

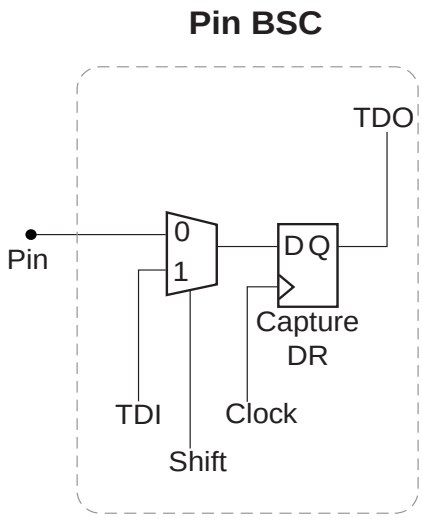
The ATF1516AS contains up to 160 I/O pins and 4 input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own boundary scan cell (BSC) in order to support boundary scan testing as described in detail by IEEE Standard 1149.1. Typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells are shown below.

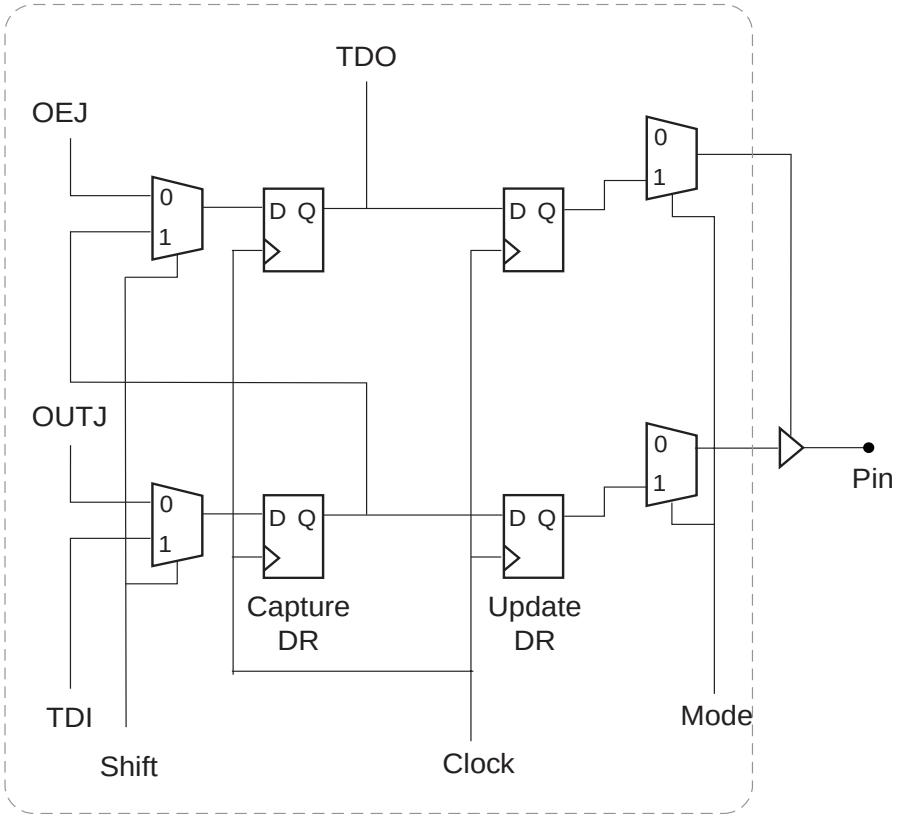
BSC Configuration Pins and Macrocells (except JTAG TAP Pins)



Note: The ATF1516AS has pull-up option on TMS and TDI pins. This feature is selected as a design option.

BSC Configuration for Macrocell



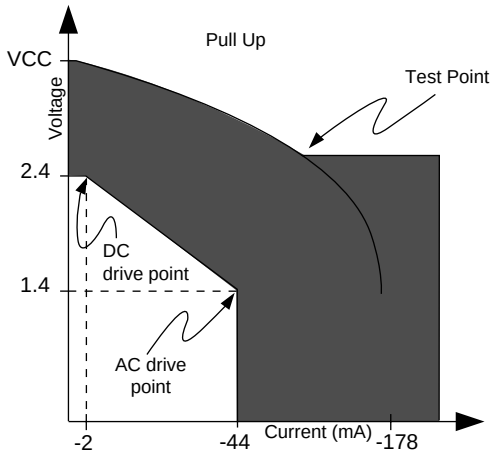


Macrocell BSC

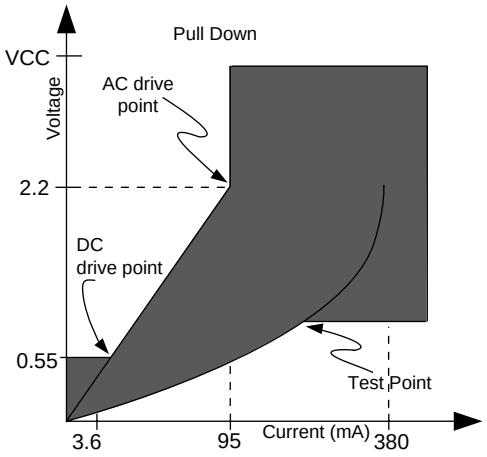
PCI Compliance

The ATF1516AS also supports the growing need in the industry to support the new Peripheral Component Interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers which are much larger than the traditional TTL drivers.

PCI Voltage-to-Current Curves for +5V Signaling in Pull-Up Mode



PCI Voltage-to-Current Curves for +5V Signaling in Pull-Down Mode



Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
10	5	125	ATF1516AS-10QC160 ATF1516AS-10UC192 ATF1516AS-10QHC208	160Q 192U 208QH	Commercial (0°C to 70°C)
15	8	100	ATF1516AS-15QC160 ATF1516AS-15UC192 ATF1516AS-15QHC208	160Q 192U 208QH	Commercial (0°C to 70°C)
15	8	100	ATF1516AS-15Q160 ATF1516AS-15UI192 ATF1516AS-15QHI208	160Q 192U 208QH	Industrial (-40°C to +85°C)
20	12	83.3	ATF1516ASL-20QC160 ATF1516ASL-20UC192 ATF1516ASL-20QHC208	160Q 192U 208QH	Commercial (0°C to 70°C)
20	12	83.3	ATF1516ASL-20QI160 ATF1516ASL-20UI192 ATF1516ASL-20QHI208	160Q 192U 208QH	Industrial (-40°C to +85°C)
25	15	70	ATF1516ASL-25QC160 ATF1516ASL-25UC192 ATF1516ASL-25QHC208	160Q 192U 208QH	Commercial (0°C to 70°C)
25	15	70	ATF1516ASL-25QI60 ATF1516ASL-25UI192 ATF1516ASL-25QHI208	160Q 192U 208QH	Industrial (-40°C to +85°C)

Package Type	
160Q	160-Lead, Plastic Quad FlatPack (PQFP)
192U	192-Lead, Plastic Grid Array (PGA)
208QH	208-Lead, Plastic Quad Flatpack with Heat Spreader (RQFP)