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Tx 270318 ANSUSE I -**FAST SWITCHING THYRISTOR****ATF1040**

Repetitive voltage up to	2000 V
Mean on-state current	1075 A
Surge current	14 kA
Turn-off time	50 µs

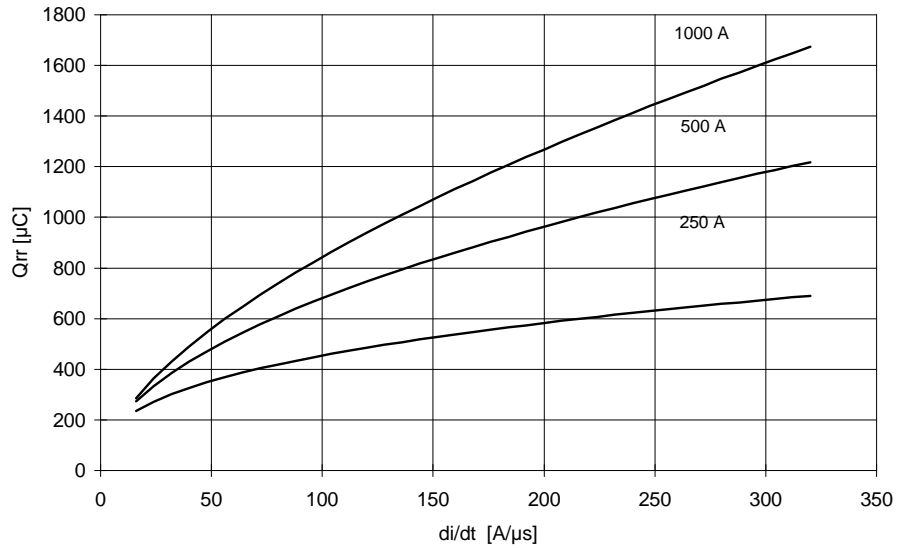
FINAL SPECIFICATION

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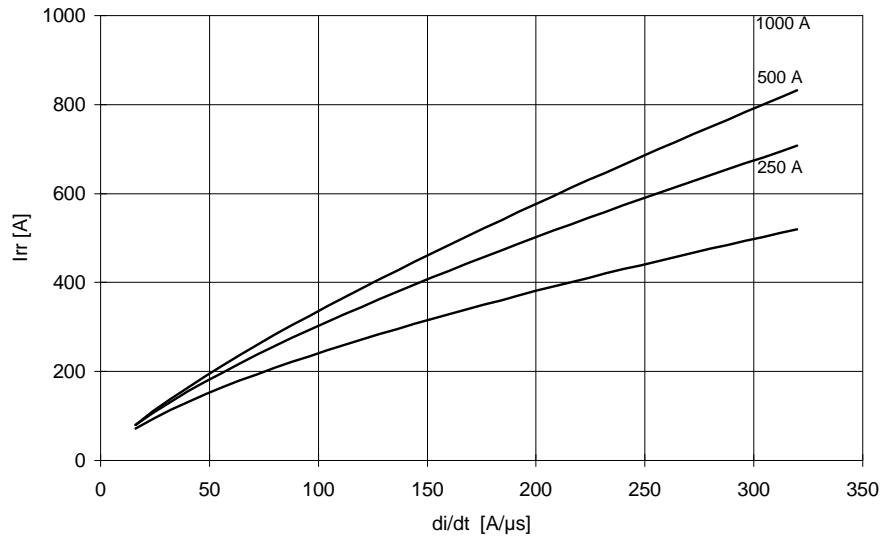
Symbol	Characteristic	Conditions	T _j [°C]	Value	Unit																					
BLOCKING																										
V _{RRM}	Repetitive peak reverse voltage		125	2000	V																					
V _{RSM}	Non-repetitive peak reverse voltage		125	2100	V																					
V _{DRM}	Repetitive peak off-state voltage		125	2000	V																					
I _{RRM}	Repetitive peak reverse current	V=V _{RRM}	125	150	mA																					
I _{DRM}	Repetitive peak off-state current	V=V _{DRM}	125	150	mA																					
CONDUCTING																										
I _{T(AV)}	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		1075	A																					
I _{T(AV)}	Mean on-state current	180° sin, 1 kHz, Th=55°C, double side cooled		1000	A																					
I _{TSM}	Surge on-state current, non repetitive	sine wave, 10 ms	125	14	kA																					
I ² t	I ² t	without reverse voltage		980 x1E3	A ² s																					
V _T	On-state voltage	On-state current = 2000 A	25	2.6	V																					
V _{T(TO)}	Threshold voltage		125	1.40	V																					
r _T	On-state slope resistance		125	0.414	mohm																					
SWITCHING																										
di/dt	Critical rate of rise of on-state current, min	From 75% V _{DRM} up to 1200 A, gate 10V 5 ohm	125	500	A/µs																					
dv/dt	Critical rate of rise of off-state voltage, min	Linear ramp up to 70% of V _{DRM}	125	500	V/µs																					
t _d	Gate controlled delay time, typical	V _D =100V, gate source 20V, 10 ohm, tr=1 µs	25	0.6	µs																					
t _q	Circuit commutated turn-off time	di/dt = 20 A/µs, I = 800 A dV/dt = 200 V/µs, up to 75% V _{DRM}	125	50	µs																					
Q _{rr}	Reverse recovery charge	di/dt = 60 A/µs, I = 1000 A	125	620	µC																					
I _{rr}	Peak reverse recovery current	V _R = 50 V		227	A																					
I _H	Holding current, typical	V _D =5V, gate open circuit	25	500	mA																					
I _L	Latching current, typical	V _D =5V, tp=30µs	25	850	mA																					
GATE																										
V _{GT}	Gate trigger voltage	V _D =5V	25	3.5	V																					
I _{GT}	Gate trigger current	V _D =5V	25	350	mA																					
V _{GD}	Non-trigger gate voltage, min.	V _D =V _{DRM}	125	0.25	V																					
V _{FGM}	Peak gate voltage (forward)		25	30	V																					
I _{FGM}	Peak gate current		25	10	A																					
V _{RGM}	Peak gate voltage (reverse)		25	5	V																					
P _{GM}	Peak gate power dissipation	Pulse width 100 µs	25	150	W																					
P _{G(AV)}	Average gate power dissipation		25	3	W																					
MOUNTING																										
R _{th(j-h)}	Thermal impedance, DC	Junction to heatsink, double side cooled		26	°C/kW																					
T _j	Operating junction temperature			-30 / 125	°C																					
F	Mounting force			14.0 / 17.0	kN																					
	Mass			500	g																					
ORDERING INFORMATION : ATF1040 S 20 S _____ tq code																										
standard specification _____ V _{DRM} &V _{RRM} /100																										
<table border="1"> <tr> <td colspan="2">tq code</td> <td>D 10 µs</td> <td>C 12 µs</td> <td>B 15 µs</td> <td>A 20 µs</td> <td>L 25 µs</td> </tr> <tr> <td></td> <td></td> <td>M 30 µs</td> <td>N 35 µs</td> <td>P 40 µs</td> <td>R 45 µs</td> <td>S 50 µs</td> </tr> <tr> <td></td> <td></td> <td>T 60 µs</td> <td>U 70 µs</td> <td>W 80 µs</td> <td>X 100µs</td> <td>Y 150µs</td> </tr> </table>						tq code		D 10 µs	C 12 µs	B 15 µs	A 20 µs	L 25 µs			M 30 µs	N 35 µs	P 40 µs	R 45 µs	S 50 µs			T 60 µs	U 70 µs	W 80 µs	X 100µs	Y 150µs
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SWITCHING CHARACTERISTICS

REVERSE RECOVERY CHARGE
T_j = 125 °C



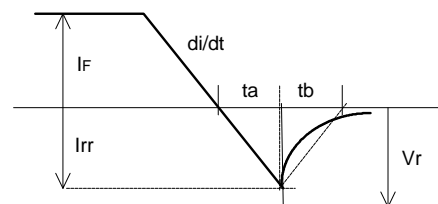
REVERSE RECOVERY CURRENT
T_j = 125 °C



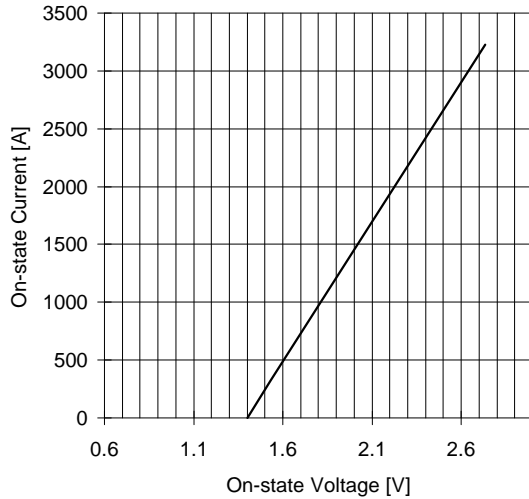
$t_a = I_{rr} / (di/dt) \quad t_b = t_{rr} - t_a$

Softness (s factor) $s = t_b / t_a$

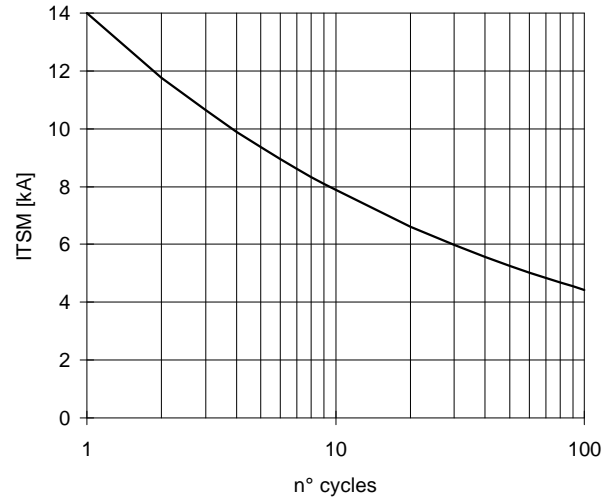
Energy dissipation during recovery $E_r = V_r \cdot (Q_{rr} - I_{rr} \cdot t_a / 2)$



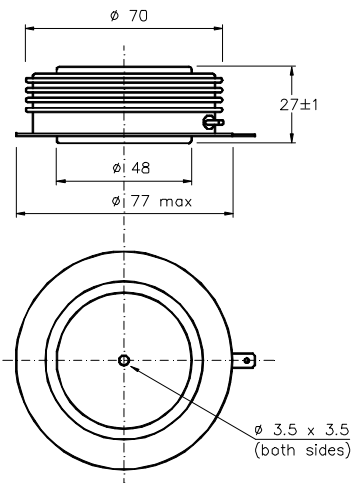
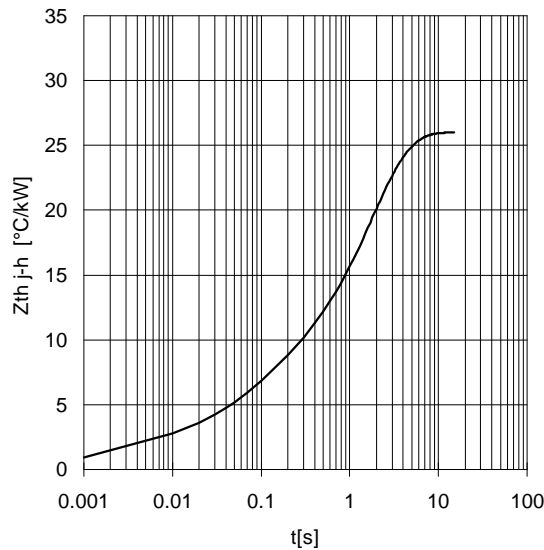
ON-STATE CHARACTERISTIC
T_j = 125 °C



SURGE CHARACTERISTIC
T_j = 125 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED



Dimensions
in mm



Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < 0.03 mm and roughness < 2 μm .

In the interest of product improvement ANSALDO reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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