

Low Power, <100 Lux Optimized, Analog Output Ambient Light Sensor

ISL76671

The ISL76671 is a low cost, light-to-voltage silicon optical sensor combining a photodiode array, a non-linear current amplifier and a micro-power op amp on a single monolithic IC. Similar to the human eye, the photodiode array has peak sensitivity at 550nm and spans the wavelength range 400nm to 600nm, rejecting UV and IR light. The input luminance range is from 0.01 lux to 100 lux.

The integrated non-linear current amplifier boosts and converts the photodiode signal into a square root output format, extending dynamic range while maintaining excellent sensitivity in dimly lit conditions. As such, the part is ideal for measuring incident daylight when mounted behind heavily smoked bezels used around displays or behind mirrors.

The device consumes minimum power. A dark current compensation circuit minimizes the effect of temperature dependent leakage currents in the absence of light, improving the light sensitivity at low lux levels. The output gain has been optimized to require a relatively low value external bias resistor that falls within recommended automotive EMI limits. The built-in 1µA op amp gives the ISL76671 an output voltage driving advantage for heavier loads that can drive an ADC directly.

The ISL76671 is housed in an ultra compact 2mmx2.1mm ODFN plastic surface mount package. Operation is rated from -40°C to +105°C, Grade 2 per AECQ100.

Features

- Square Root Voltage Output
- 0.01 lux to 100 lux Range
- 1.8V to 3V Supply Range
- Close to Human Eye Spectral Response
- Fast Response Time
- Internal Temperature Compensation
- Good IR Rejection
- Low Supply Current
- Operating Temperature Range -40°C to +105°C
- 6 Lead ODFN: 2mmx2.1mmx0.7mm
- Pb-Free (RoHS Compliant)
- AECQ100 Qualified

Applications

- Display Backlight Control - Central Info Display & Instrumentation
- Anti-glare Mirror Systems - Specified to Operate Behind Bezel Mounting

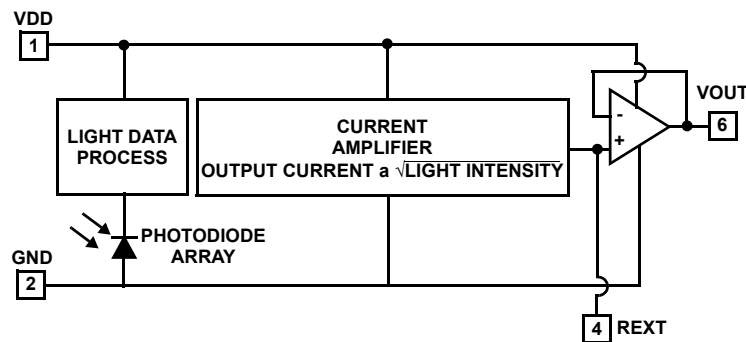
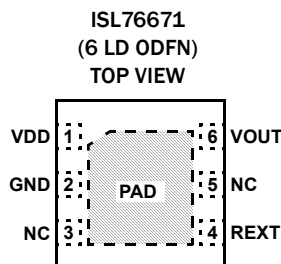


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM

ISL76671

Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VDD	Voltage Supply (1.8V to 3V).
2	GND	Ground
3, 5	NC	No connect
4	REXT	Connected to an external resistor to GND, setting the light-to-voltage scaling constant. A R_{EXT} value of 100k Ω is recommended.
6	VOUT	Voltage Output.
-	PAD	Thermal Pad. The thermal pad can be connected to GND or electrically isolated.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL76671AR0Z-T7	6 Ld ODFN (Tape and Reel)	L6.2X2.1

NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL76671](#). For more information on MSL please see techbrief [TB477](#).

ISL76671

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage Between V _{DD} and GND	3.6V
R _{EXT}	(-0.5V + GND) to (0.5V + V _{DD})
V _{OUT}	(-0.5V + GND) to (0.5V + V _{DD})
V _{OUT} Short Circuit Current	<10mA
ESD Rating	
Human Body Model (Tested per JESD22-A114E)	3kV
Machine Model (Tested per JESD22-A115C)	300V
Charged Device Model (Tested per JESD22-C101E)	1kV
Latch Up (Tested per JESD78C)	100mA

Thermal Information

Thermal Resistance (Typical)	θ _{JA} (°C/W)	θ _{JC} (°C/W)
6 Ld ODFN (Notes 4, 5)	88	7.94
Maximum Die Temperature	+105°C	
Storage Temperature	-40°C to +105°C	
Operating Temperature	-40°C to +105°C	
Pb-Free Reflow Profile (*)	see TB477	
*Peak temperature during solder reflow +260°C max		

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief [TB379](#).
- For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications Unless otherwise noted, all parameter limits are established over the recommended operating conditions: V_{DD} = 3V, T_A = -40°C to +105°C, R_{EXT} = 100kΩ, no load at V_{OUT}, and green LED light. (Typical values are at T_A = +25°C). **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
E	Range of Input Light Intensity for Square Root Relationship to be Held			0.01 - 100		Lux
V _{DD}	Operating Supply Voltage		1.8		3	V
I _{DD}	Supply Current	E = 0 lux, -40°C to 60°C		0.7	2	μA
		E = 0 lux, -40°C to 105°C			5	μA
		E = 100 lux		23	35	μA
V _{OUT}	Light-to-Voltage Accuracy	E = 10 lux		0.65		V
		E = 50 lux		1.35		V
		E = 100 lux	1.4	1.85	2.3	V
V _{DARK}	Voltage Output in the Absence of Light	E = 0 lux, -40°C to 60°C		0.95	20	mV
		E = 0 lux, -40°C to 105°C			120	mV
ΔV _{OUT}	Output Voltage Variation Over Three Light Sources: Fluorescent, Incandescent and Halogen			10		%
PSRR	Power Supply Rejection Ratio	E = 100 lux		0.12		mV/V
V _{O-CMPL}	Maximum Output Compliance Voltage at 95% of Nominal Output			V _{DD} - 0.7V		V
V _{O-MAX}	Maximum Output Voltage Swing				V _{DD}	V
t _R	Rise Time	E = 0 lux to 100 lux		95		μs
t _F	Fall Time	E = 100 lux to 0 lux		155		μs
t _D	Delay Time for Rising Edge	E = 0 lux to 100 lux		350		μs
t _S	Delay Time for Falling Edge	E = 100 lux to 0 lux		250		μs
ISC	Short Circuit Current of Op Amp			±12		mA
SR	Slew Rate of Op Amp			13		V/ms
V _{OS}	Offset Voltage of Op Amp			±0.9		mV

NOTE:

- Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

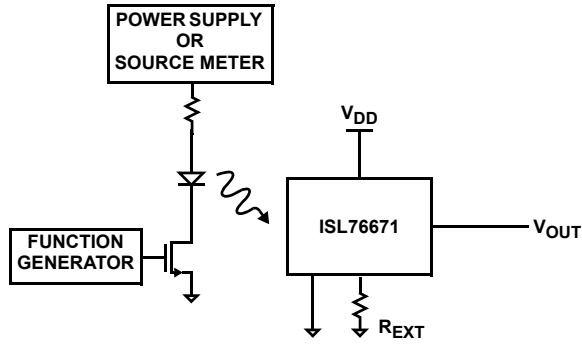


FIGURE 2. TEST CIRCUIT FOR RISE/FALL TIME MEASUREMENT

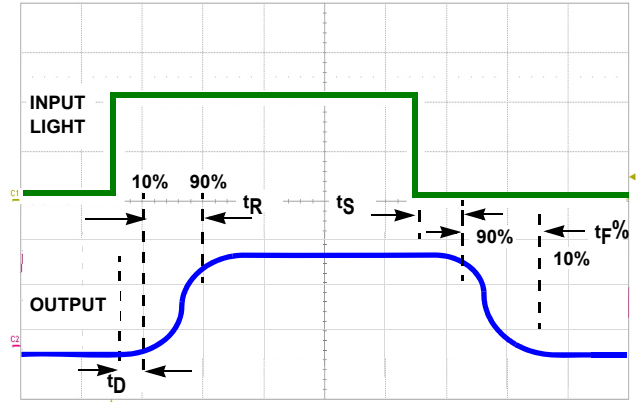


FIGURE 3. TIMING DIAGRAM

Typical Performance Curves $V_{DD} = 3V$, $T_A = +25^\circ C$, $R_{EXT} = 100k\Omega$, no load at V_{OUT} , green LED light, unless otherwise specified.

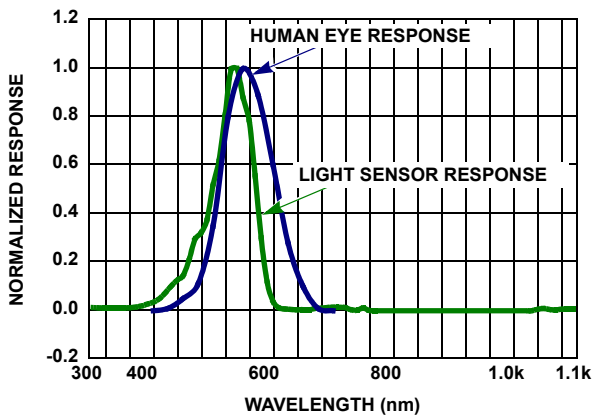


FIGURE 4. SPECTRAL RESPONSE

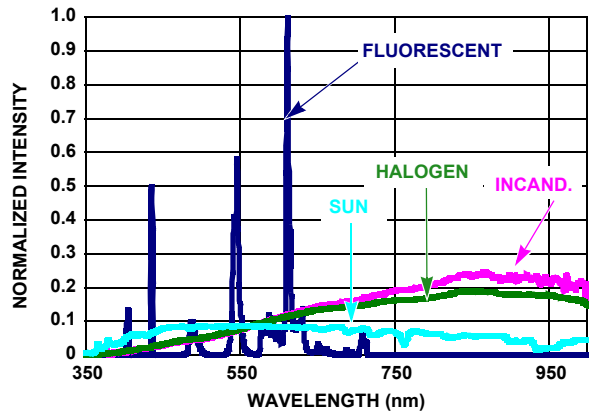


FIGURE 5. SPECTRUM OF FOUR LIGHT SOURCES NORMALIZED BY LUMINOUS INTENSITY (LUX)

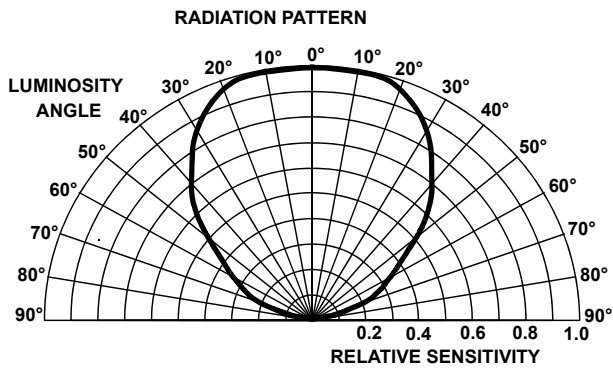


FIGURE 6. RADIATION PATTERN

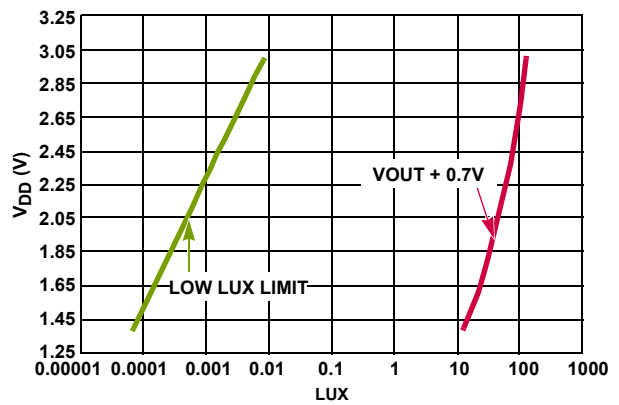


FIGURE 7. V_{DD} OPERATING RANGE (WHITE LED)

Typical Performance Curves $V_{DD} = 3V$, $T_A = +25^\circ C$, $R_{EXT} = 100k\Omega$, no load at V_{OUT} , green LED light, unless otherwise specified.

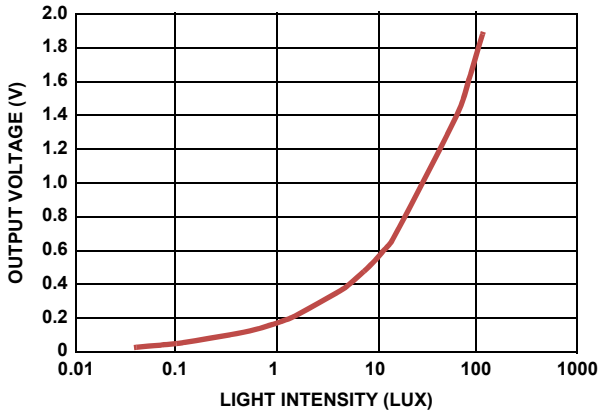


FIGURE 8. OUTPUT VOLTAGE vs LIGHT INTENSITY 0.1 LUX TO 100 LUX

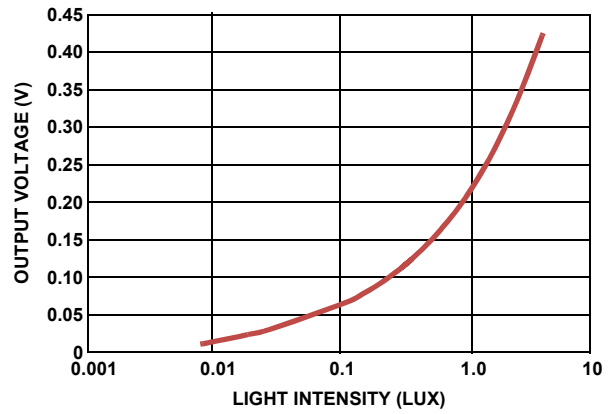


FIGURE 9. OUTPUT VOLTAGE vs LIGHT INTENSITY 0.01 LUX TO 5 LUX

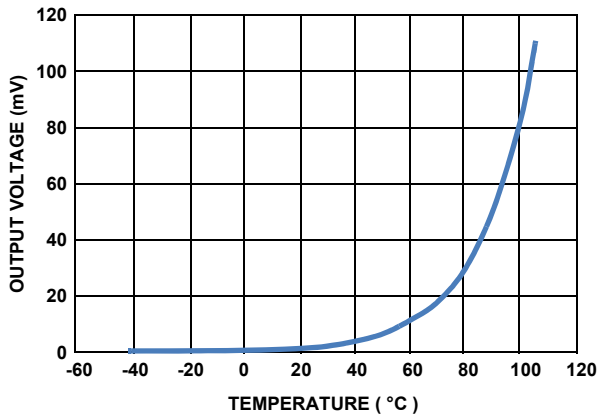


FIGURE 10. OUTPUT VOLTAGE vs TEMPERATURE AT 0 LUX

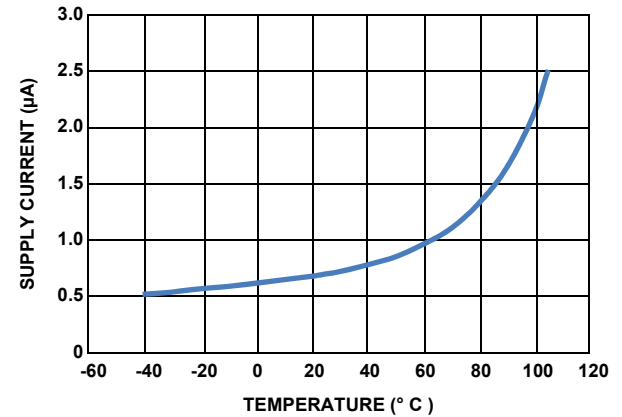


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE AT 0 LUX

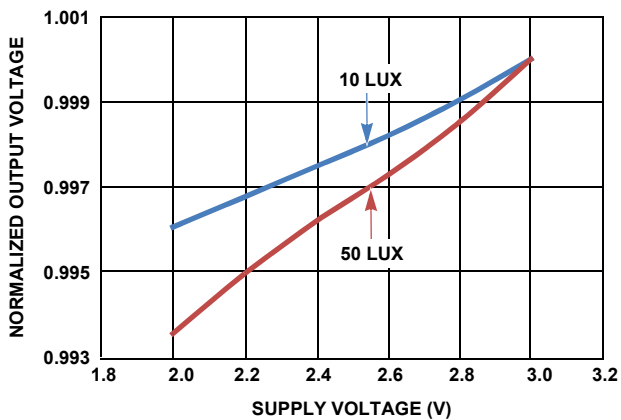


FIGURE 12. NORMALIZED OUTPUT VOLTAGE vs SUPPLY VOLTAGE

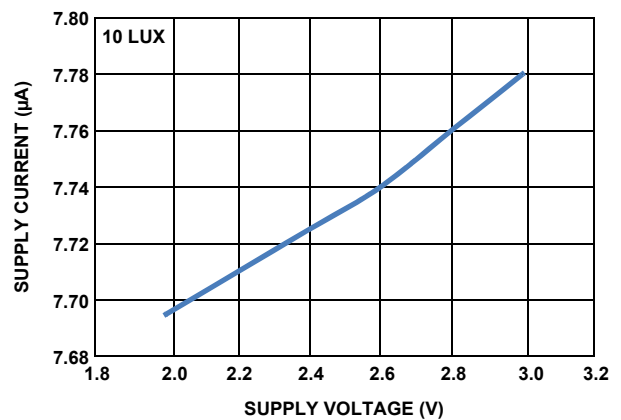


FIGURE 13. SUPPLY CURRENT vs SUPPLY VOLTAGE

ISL76671

Typical Performance Curves $V_{DD} = 3V$, $T_A = +25^\circ C$, $R_{EXT} = 100k\Omega$, no load at V_{OUT} , green LED light, unless otherwise specified.

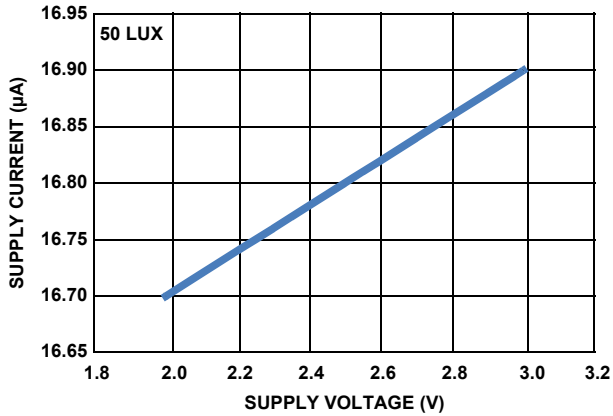


FIGURE 14. SUPPLY CURRENT vs SUPPLY VOLTAGE

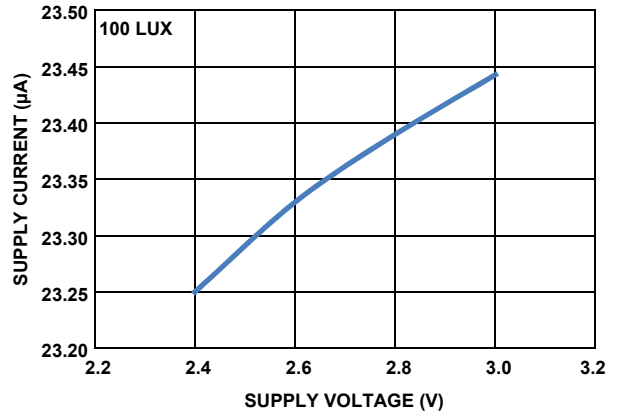


FIGURE 15. SUPPLY CURRENT vs SUPPLY VOLTAGE

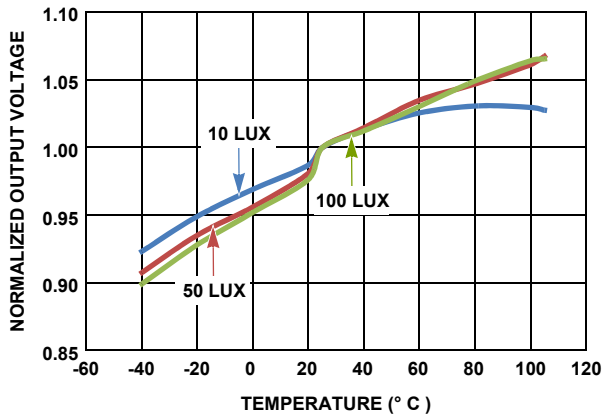


FIGURE 16. NORMALIZED OUTPUT VOLTAGE vs TEMPERATURE

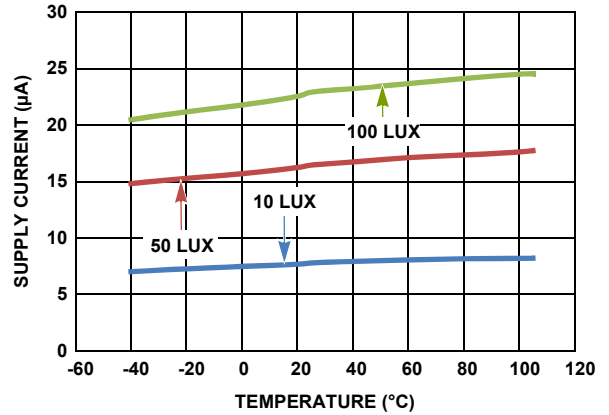


FIGURE 17. SUPPLY CURRENT vs TEMPERATURE

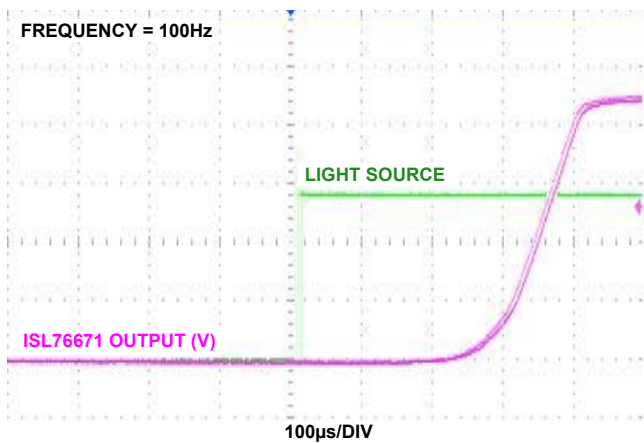


FIGURE 18. DELAY TIME vs LUX CHANGE FROM 0 LUX

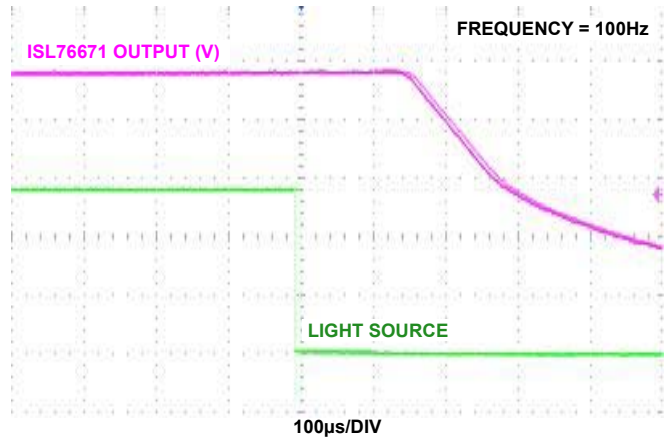


FIGURE 19. DELAY TIME vs LUX CHANGE TO 0 LUX

Application Information

Light-to-Voltage Conversion

The ISL76671 has responsiveness that is a square-root function of the light intensity intercepted by the photodiode in lux.

Because the photodiode has a responsivity that resembles the human eye, conversion rate is independent of the light source (fluorescent light, incandescent light or direct sunlight).

$$V_{OUT} = \frac{18\mu A}{\sqrt{100\text{lux}}} \sqrt{E} \times R_{EXT} \quad (\text{EQ. 1})$$

In Equation 1, V_{OUT} is the output voltage, E is the light intensity and R_{EXT} is the value of the external resistor. The R_{EXT} is used to set the light-to-voltage scaling constant. The compliance of the ISL76671's output circuit may result in premature saturation when an excessively large R_{EXT} is used. A R_{EXT} value of 100k Ω is recommended for automotive applications. The output compliance voltage is 700mV below the supply voltage as listed in V_{O-MAX} of the "Electrical Specifications" table on page 3.

Optical Sensor Location Outline

The green area in Figure 20 shows the optical sensor location outline of ISL76671. Along the pinout direction, the center line (CL) of the sensor coincides with that of the packaging. The sensor width in this direction is 0.39mm. Perpendicular to the pinout direction, the CL of the sensor has an 0.19mm offset from the CL of packaging away from pin 1. The sensor width in this direction is 0.46mm.

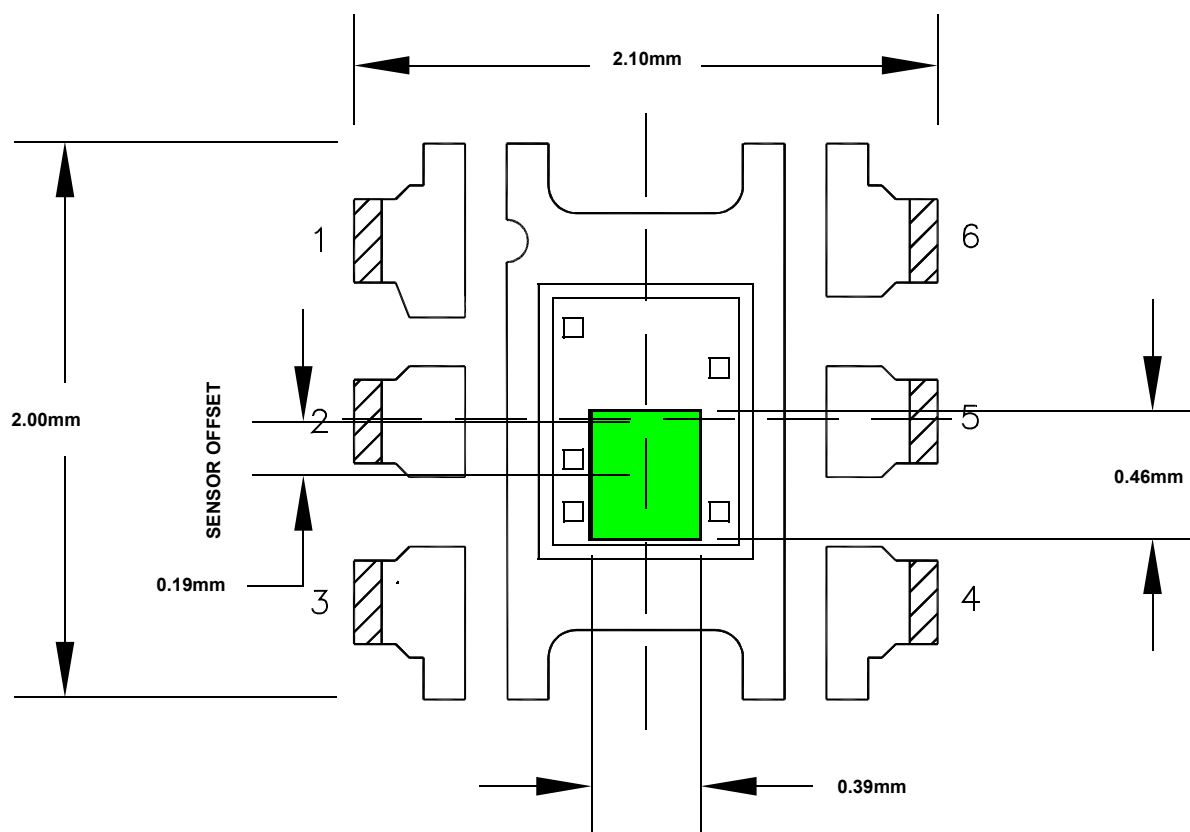


FIGURE 20. 6 LD ODFN SENSOR LOCATION OUTLINE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 12, 2011	FN7716.1	“Thermal Information” on page 3, changed from: Pb-Free Reflow Profile (*) see TB487 *Peak temperature during solder reflow +235 °C max To Pb-Free Reflow Profile (*) see TB477 *Peak temperature during solder reflow +260 °C max “Electrical Specifications” on page 3: Added Min value of 1.4V and Max value of 2.3V for V_{OUT} where $e = 100$ lux
October 19, 2011	FN7716.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL76671](http://intersil.com/ISL76671)

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: <http://rel.intersil.com/reports/sear>

For additional products, see www.intersil.com/product_tree

Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems as noted in the quality certifications found at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

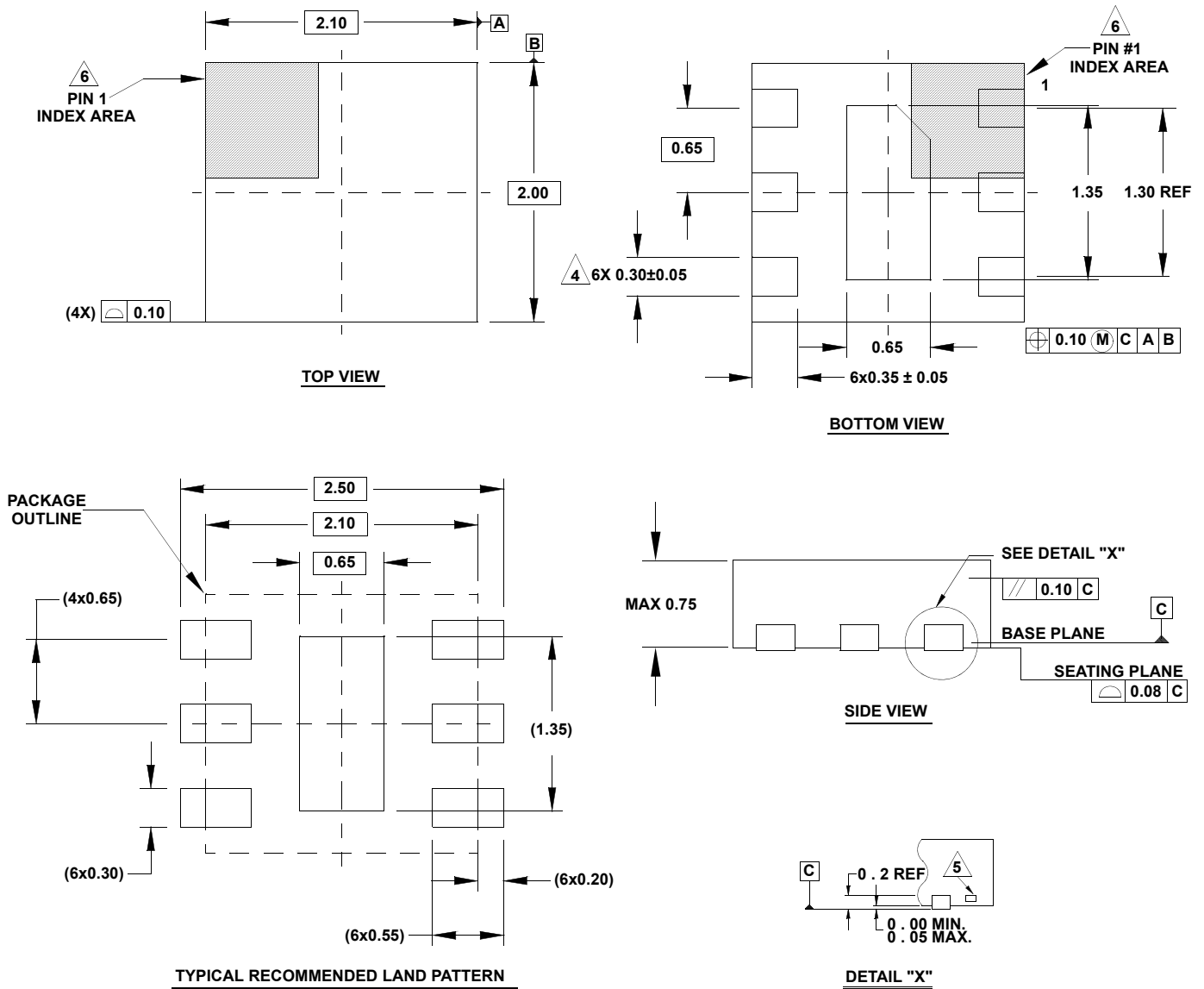
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

L6.2x2.1

6 LEAD OPTICAL DUAL FLAT NO-LEAD PLASTIC PACKAGE (ODFN)

Rev 3, 5/11



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.