Rad Hard and SEE Hard 12A Synchronous Buck Regulator with Multi-Phase Current Sharing

ISL70002SEH

The ISL70002SEH is a radiation hardened and SEE hardened high efficiency monolithic synchronous buck regulator with integrated MOSFETs. This single chip power solution operates over an input voltage range of 3V to 5.5V and provides a tightly regulated output voltage that is externally adjustable from 0.8V to ~85% of the input voltage. Output load current capacity is 12A for $T_J \leq +150°C$. Two ISL70002SEH devices configured to current share can provide 19A total output current, assuming ±27% worst-case current share accuracy.

The ISL70002SEH utilizes peak current-mode control with integrated error amp compensation and pin selectable slope compensation. Switching frequency is also pin selectable to either 1MHz or 500kHz. Two ISL70002SEH devices can be synchronized 180° out-of-phase to reduce input RMS ripple current.

High integration makes the ISL70002SEH an ideal choice to power small form factor applications. Two devices can be synchronized to provide a complete power solution for large scale digital ICs, like field programmable gate arrays (FPGAs), that require separate core and I/O voltages.

Applications

- FPGA, CPLD, DSP, CPU Core and I/O Voltages
- Low-Voltage, High-Density Distributed Power Systems

Features

- DLA SMD#5962-12202
- 12A Output Current for a Single Device (at $T_J = +150°C$)
- 19A Output Current for Two Paralleled Devices
- 1MHz or 500kHz Switching Frequency
- 3V to 5.5V Supply Voltage Range
- ±1% Ref. Voltage (Line, Load, Temp. & Rad.)
- Pre-Biased Load Compatible
- Redundancy/Junction Isolation: Exceptional SET Performance
- Excellent Transient Response
- High Efficiency > 90%
- Two ISL70002SEH Synchronization, Inverted-Phase
- Comparator Input for Enable and Power-Good
- Adjustable Analog Soft-Start
- Input Undervoltage, Output Undervoltage and Adjustable Output Overcurrent Protection
- QML Qualified per MIL-PRF-38535
- Full Mil-Temp Range Operation (-55°C to +125°C)
- Radiation Environment
  - High Dose . . . . . 100 krad(Si)
  - ELDRS . . . . . .100 krad(Si)* *Level guaranteed by characterization; “EH” version is production tested to 50 krad(Si).
- SEE Hardness
  - SEL and SEB LET_{TH} . . . . . 86.4MeV/mg/cm^2
  - SEFI LET_{TH}. . . . . 43MeV/mg/cm^2
  - SET LET_{TH} . . . . . 86.4MeV/mg/cm^2

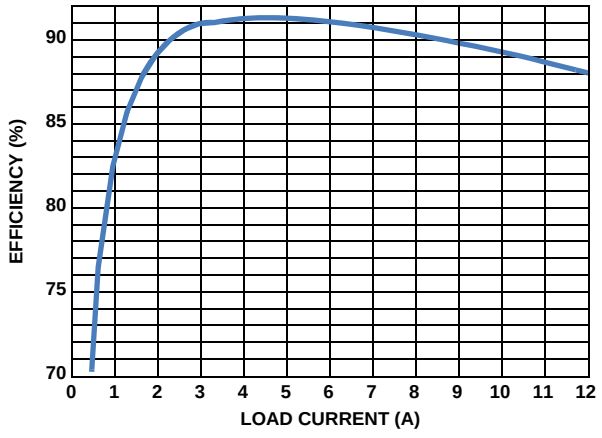


FIGURE 1. EFFICIENCY 5V INPUT TO 2.5V OUTPUT, $T_A = +25°C$

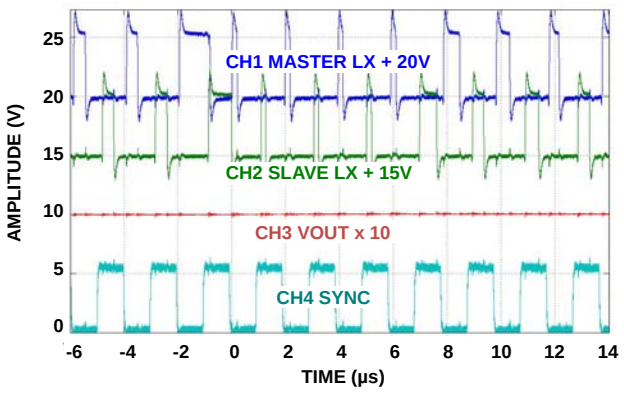
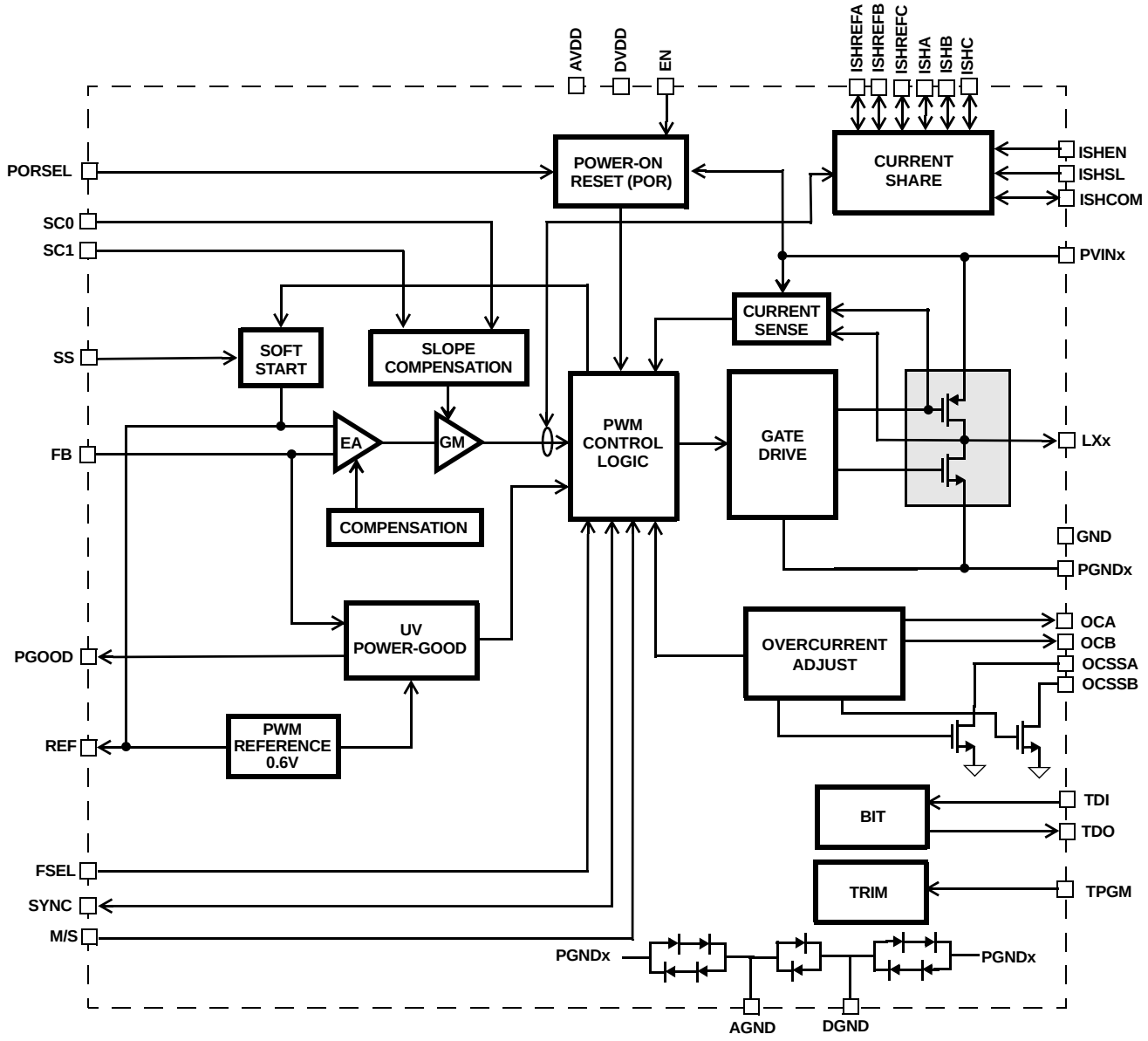


FIGURE 2. 2-PHASE SET PERFORMANCE at 86.4MeV/mg/cm^2

Functional Block Diagram



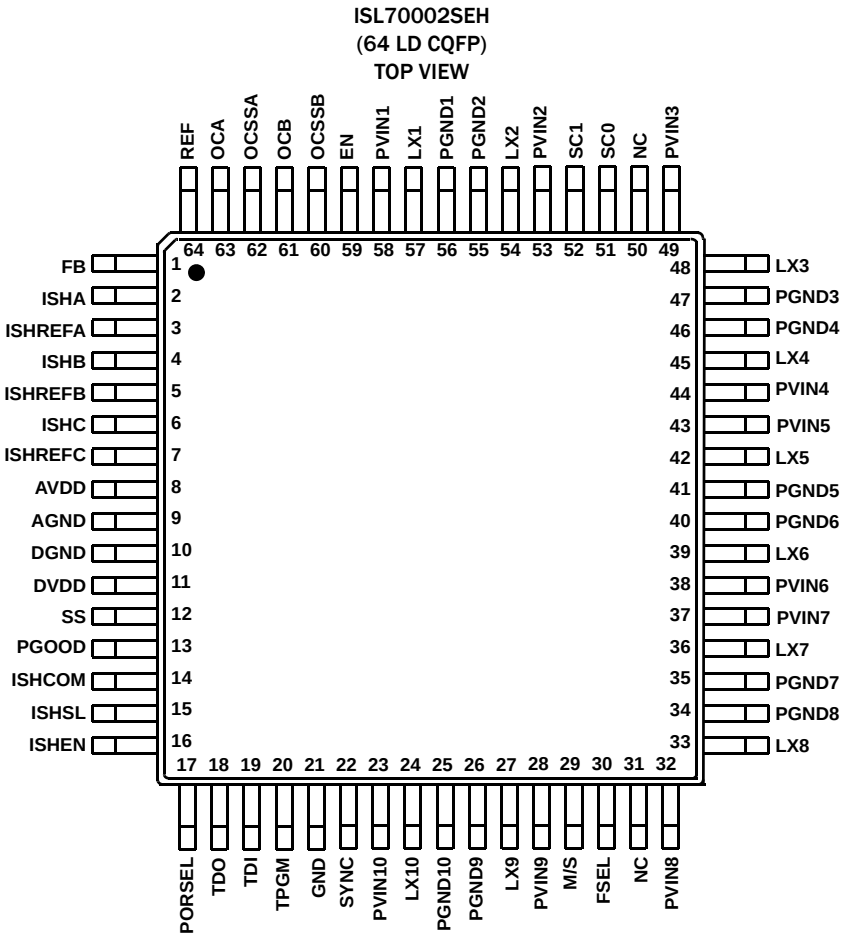
Ordering Information

ORDERING NUMBER	PART NUMBER (Notes 1, 2)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962R1220201VXC	ISL70002SEHVF	-55 to +125	64 Ld CQFP	R64.A
5962R1220201V9A	ISL70002SEHVX	-55 to +125	Die	
ISL70002SEHF/PROTO	ISL70002SEHF/PROTO	-55 to +125	64 Ld CQFP	R64.A
ISL70002SEHX/SAMPLE	ISL70002SEHX/SAMPLE	-55 to +125	Die	
ISL70002SEHEVAL1Z	Evaluation Board			

NOTE:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISL70002SEH. For more information on MSL please see techbrief TB363.

Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	FB	This pin is the voltage feedback input to the internal error amplifier. Connect a resistor from FB to VOUT and from FB to AGND to adjust the output voltage in accordance with Equation 1: $V_{OUT} = V_{REF} \cdot [1 + (R_T/R_B)]$ (EQ. 1) Where: V_{OUT} = Output voltage V_{REF} = Reference voltage (0.6V typical) R_T = Top divider resistor (Must be 1kΩ) R_B = Bottom divider resistor The top divider resistor must be 1kΩ to mitigate SEE. Connect a 4.7nF ceramic capacitor across RT to mitigate SEE and to improve stability margins. If using current share, tie FB of the Master to FB of the Slave.
2, 4, 6	ISHA/B/C	If configured as a current share Master (ISHSL = DGND, ISHEN = DVDD), the ISHA/B/C pins are outputs that provides a current equal to 25 times the redundant A/B/C error amp output currents plus ISHREFA/B/C (nominally 100µA each). If configured as a current share Slave (ISHSL = DVDD, ISHEN = DVDD), the ISHA/B/C pins are inputs that become the Slave's redundant A/B/C error amp output current. If using current share, tie ISHA/B/C of the Master to ISHA/B/C of the Slave. If not using current share, tie ISHA/B/C to DVDD. ISHA/B/C are tri-stated prior to a valid POR and when ISHEN = DGND.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION
3, 5, 7	ISHREFA/B/C	If configured as a current share Master (ISHSL = DGND, ISHEN = DVDD), the ISHREFA/B/C pins provide a reference output current equal to 100uA each. If configured as a current share Slave (ISHSL = DVDD, ISHEN = DVDD), the ISHREFA/B/C pins accept a reference input current. For a current share Slave, this input current is used together with the ISHA/B/C current to determine the Master's redundant A/B/C error amp output current. If using current share, tie ISHREFA/B/C of the MASTER to ISHREFA/B/C of the Slave. If not using current share, tie ISHREFA/B/C to DVDD. The purpose of the reference current is to reduce the impact of external noise coupling onto ISHA/B/C. ISHREFA/B/C are tri-stated prior to a valid POR and when ISHEN = DGND.
8	AVDD	This pin is the bias supply input to the internal analog control circuitry. Locally filter this pin to AGND using a 1Ω resistor and a 1µF ceramic capacitor. Locate both filter components as close as possible to the IC. AVDD should be the same voltage as DVDD and PVINx (±200mV).
9	AGND	This pin is the analog ground associated with the internal analog control circuitry. Connect this pin directly to the PCB ground plane.
10	DGND	This pin is the digital ground associated with the internal digital control circuitry. Connect this pin directly to the PCB ground plane.
11	DVDD	This pin is the bias supply input to the internal digital control circuitry. Locally filter this pin to DGND using a 1Ω resistor and a 1µF ceramic capacitor. Locate both filter components as close as possible to the IC. DVDD should be the same voltage as AVDD and PVINx (±200mV).
12	SS	This pin is the soft-start input. Connect a ceramic capacitor from this pin to DGND to set the soft-start output ramp time in accordance with Equation 2: $t_{SS} = C_{SS} \cdot V_{REF} / I_{SS}$ (EQ. 2) Where: t_{SS} = Soft-start output ramp time C_{SS} = Soft-start capacitor V_{REF} = Reference voltage (0.6V typical) I_{SS} = Soft-start charging current (23µA typical) Soft-start time is adjustable from approximately 2ms to 200ms. The range of the soft-start capacitor should be 82nF to 8.2µF, inclusive. If using current share, C_{SS} of the Slave should be at least twice the C_{SS} of the Master.
13	PGOOD	This pin is the power-good output. This pin is an open drain logic output that is pulled to DGND when the output voltage is outside a ±11% typical regulation window. This pin can be pulled up to any voltage from 0V to 5.5V, independent of the supply voltage. A nominal 1kΩ to 10kΩ pull-up resistor is recommended. Bypass this pin to DGND with a 10nF ceramic capacitor to mitigate SEE. If using current share, tie PGOOD of the Master to PGOOD of the Slave.
14	ISHCOM	ISHCOM is a bidirectional communication line between a current share Master and a current share Slave. If using current share, tie ISHCOM of the Master to ISHCOM of the Slave. The Master enables the Slave by resistively (~ 8.5kΩ) pulling ISHCOM high. The Slave indicates an over-current fault condition to the Master by pulling ISHCOM low. To mitigate SET, connect a 47pF ceramic capacitor from ISHCOM to the PCB ground plane. If not using current share this pin should be floated or connected to the PCB ground plane. ISHCOM is tri-stated if ISHEN is low.
15	ISHSL	This pin is a logic input that is used to configure the IC as a current share Master or Slave. Tie this pin to DVDD to configure the IC as a current share Slave. Tie this pin to the PCB ground plane to configure the IC as a current share Master, or if the current share feature is not being used.
16	ISHEN	This pin is an input that enables/disables the current share feature. To enable the current share feature, tie this pin to DVDD. To disable the current share feature, tie this pin to the PCB ground plane.
17	PORSEL	This pin is the input for selecting the rising and falling POR (Power-On-Reset) thresholds. For a nominal 5V supply, connect this pin to DVDD. For a nominal 3.3V supply, connect this pin to DGND. For nominal supply voltages between 5V and 3.3V, connect this pin to DGND.
18	TDO	This pin is the test data output of the internal BIT circuitry. Connect this pin to the PCB ground plane.
19	TDI	This pin is the test data input of the internal BIT circuitry. Connect this pin to the PCB ground plane.
20	TPGM	This pin is a trim input and is used to adjust various internal circuitry. Connect this pin to the PCB ground plane.
21	GND	This pin is connected to an internal metal die trace that serves as a sensitive node noise shield. Connect this pin to the PCB ground plane.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION
22	SYNC	When SYNC is configured as an output (clock Master Mode, M/S = DVDD), this pin drives the SYNC input of another ISL70002SEH with a square ware that is inverted (~180° out-of-phase) from the Master clockdriving the Master PWM circuits. When configured as an input (clock Slave Mode, M/S = DGND), this pin uses the SYNC output from another ISL70002SEH or an external clock to drive the clock Slave PWM circuitry. If synchronizing to an external clock, the clock must be SEE hardened and the frequency must be within the range of 400kHz to 1.2MHz.
23, 28, 32, 37, 38, 43, 44, 49, 53, 58	PVINx	These pins are the power supply inputs to the corresponding internal power blocks. These pins must be connected to a common power supply rail, which must fall in the range of 3V to 5.5V. Bypass these pins directly to PGNDx with ceramic capacitors located as close as possible to the IC. PVINx should be the same voltage as DVDD and AVDD (±200mV).
24, 27, 33, 36, 39, 42, 45, 48, 54, 57	LXx	These pins are the outputs of the corresponding internal power blocks and should be connected to the output filter inductor. Internally, these pins are connected to the synchronous MOSFET power switches.
25, 26, 34, 35, 40, 41, 46, 47, 55, 56	PGNDx	These pins are the power grounds associated with the corresponding internal power blocks. These pins also provide the ground path for the metal package lid. Connect these pins directly to the PCB ground plane. These pins should also connect to the negative terminals of the input and output capacitors. Locate the input and output capacitors as close as possible to the IC.
29	M/S	This pin is the clock Master/Slave input for selecting the direction of the bi-directional SYNC pin. For SYNC = Output (Master Mode), connect this pin to DVDD. For SYNC = Input (Slave Mode), connect this pin to the PCB ground plane.
30	FSEL	This pin is the oscillator frequency select input. Tie this pin to DVDD to select a 1MHz nominal oscillator frequency. Tie this pin to the PCB ground plane to select a 500kHz nominal oscillator frequency.
31, 50	NC	These are No Connect pins that are not connected to anything internally. They should be connected to the PCB ground plane.
51, 52	SC0/1	These pins are inputs that comprise a 2-bit code to select the slope compensation (SC) current ramp referred to the output as shown below. SC1 = DVDD, SC0 = DVDD: SC = 6.6A/µs for FSEL = DGND SC1 = DVDD, SC0 = DGND: SC = 3.3A/µs for FSEL = DGND SC1 = DGND, SC0 = DVDD: SC = 1.6A/µs for FSEL = DGND SC1 = DGND, SC0 = DGND: SC = 0.8A/µs for FSEL = DGND SC1 = DVDD, SC0 = DVDD: SC= 13.4A/µs for FSEL = DVDD SC1 = DVDD, SC0 = DGND: SC = 6.7A/µs for FSEL = DVDD SC1 = DGND, SC0 = DVDD: SC = 3.4A/µs for FSEL = DVDD SC1 = DGND, SC0 = DGND: SC = 1.7A/µs for FSEL = DVDD If using current share, SC0 and SC1 of the Slave MUST match the Master SC0 and SC1.
59	EN	This pin is the enable input to the IC. This is a comparator type input with a rising threshold of 0.6V and programmable hysteresis. Driving this pin above 0.6V enables the IC. Bypass this pin to the PCB ground plane with a 10nF ceramic capacitor to mitigate SEE.
60, 62	OCSSB/A	This pin is a switch to AGND that is active during the soft-start period. It is used to set the redundant A/B peak overcurrent limit threshold during soft-start. Connect a resistor from OCSSx to OCx in accordance with the following equation: ROCSSx 600mV / [(IOCSSx - IOCx) /100,000] where IOCx is the desired peak overcurrent limit during normal operation and IOCSSx is the desired peak current limit threshold during soft-start.
61, 63	OCB/A	This pin is a source follower output that is used to set the redundant A/B peak overcurrent limit threshold during normal operation. Connect a resistor from this pin to the PCB ground plane in accordance with the following equation: ROCx = 600mV / (IOCx /100,000), where IOCx is the desired peak current limit threshold during normal operation.
64	REF	This pin is the internal reference voltage output. Bypass this pin to the PCB ground plane with a 220nF ceramic capacitor located as close as possible to the IC. The bypass capacitor is needed to mitigate SEE. No current (sourcing or sinking) is available from this pin. If using current share, tie REF of the Master to REF of the Slave through a 10Ω resistor.

Typical Application Schematic

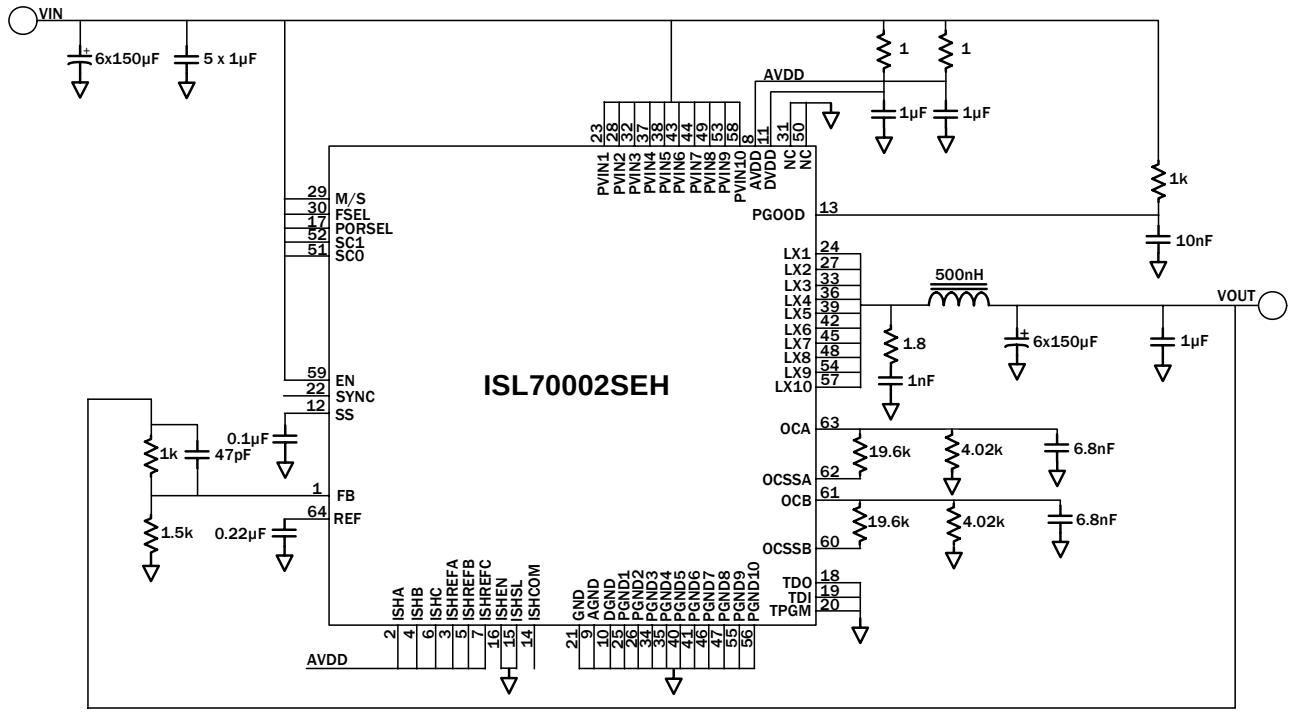


FIGURE 3. SINGLE UNIT OPERATION

Typical Application Schematic (Continued)

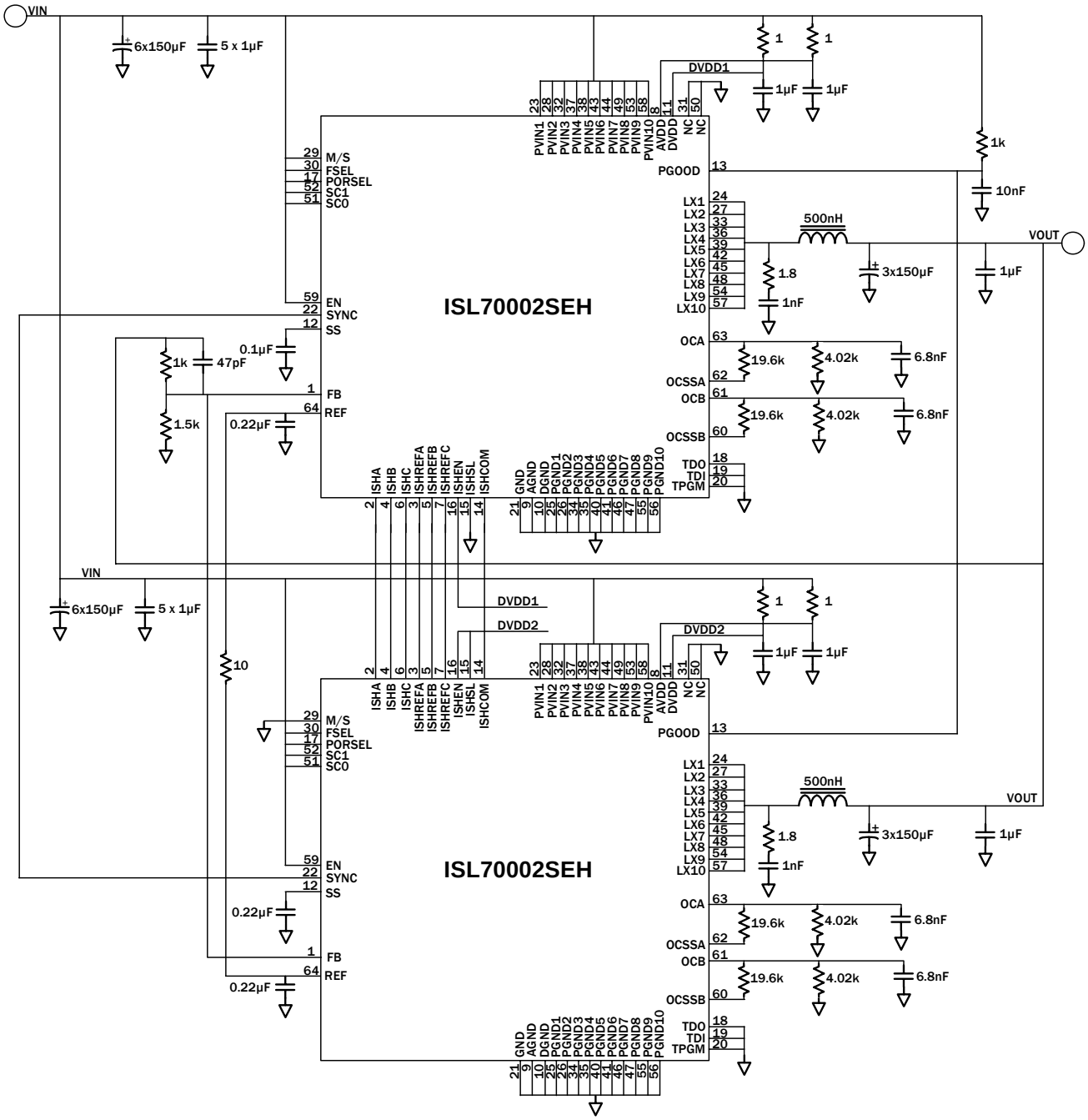


FIGURE 4. TWO PHASE OPERATION WITH CURRENT SHARING

Absolute Maximum Ratings (Note 3)

AVDD . . . . . AGND - 0.3V to AGND + 6.2V
DVDD . . . . . DGND - 0.3V to DGND + 6.2V
LXx, PVINx (Note 8) . . . . . PGNDx - 0.3V to PGNDx + 6.2V
AVDD - AGND, DVDD - DGND . . . . . PVINx - PGNDx ± 0.3V
Signal pins (Note 6) . . . . . AGND - 0.3V to AVDD + 0.3V
Digital control pins (Note 7) . . . . . DGND - 0.3V to DVDD + 0.3V
PGOOD . . . . . DGND - 0.3V to DGND + 6.2V
SS. . . . . DGND - 0.3V to DGND + 2.5V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CQFP Package (Notes 4, 5)	34	1.5

Operating Junction Temperature Range . . . . . -55°C to +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

AVDD. . . . . AGND + 3V to 5.5V
DVDD. . . . . DGND + 3V to 5.5V
PVINx. . . . . PGNDx + 3V to 5.5V
AVDD - AGND, DVDD - DGND . . . . . PVINx - PGNDx ± 0.1V
Signal pins (Note 6). . . . . AGND to AVDD
Digital control pins (Note 7) . . . . . DGND to DVDD
REF, SS . . . . . Internally Set
GND, TDI, TDO, TPGM . . . . . DGND
I_{LXx} (T_J ≤ +150°C). . . . . 0A to 1.2A
Ambient Temperature Range . . . . . -55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. Absolute Maximum Ratings assume operation in a heavy ion environment.
4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the package underside.
6. EN, FB, ISHx, ISHREFx, OCx, OCSSx, PORSEL and REF pins.
7. FSEL, GND, ISHCOM, ISHEN, ISHRSL, M/S, SYNC, SC0, SC1, TDI, TDO and TPGM pins.
8. The 6.2V absolute maximum rating must be met for a 20MHz bandwidth limited observation at the device pins. In addition, for a 600MHz bandwidth limited observation, the peak transient voltage on PVINx (measured to PGNDx) must be less than 7.1V with a duration above 6.2 V of less than 10ns, and the peak transient voltage on LXx (measured to PGNDx) must be less than 7.9V with a duration above 6.2 V of less than 10ns.

Electrical Specifications

Unless otherwise noted, V_{IN} = AVDD = DVDD = PVINx = EN = FSEL = M/S = SC0 = SC1= 3V to 5.5V; GND = AGND = DGND = PGNDx = ISHx = ISHCOM = ISHEN = ISHREFx = ISHSL = TDI = TDO = TPGM = 0V; FB = 0.65V; PORSEL = V_{IN} for 4.5V ≤ V_{IN} ≤ 5.5V and GND for V_{IN} < 4.5V; LXx = SYNC = Open Circuit; OCx is connected to OCSSx with a 10kΩ resistor; OCx is connected to GND with a 4.99kΩ resistor shunted by a 6.8nF capacitor; PGOOD is pulled up to V_{IN} with a 1kΩ resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; T_A = T_J = -55°C to +125°C; Post 100krad(Si). (Note 6).

PARAMETER	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNITS
POWER SUPPLY					
Operating Supply Current (Current Share Disabled)	V_{IN} = 5.5V		70	105	mA
	V_{IN} = 3.6V		43	65	mA
Standby Supply Current (Current Share Disabled)	V_{IN} = 5.5V, EN = GND, ISHEN = GND		2.5	6	mA
	V_{IN} = 3.6V, EN = GND, ISHEN = GND		2	4	mA
Operating Supply Current (Current Share Enabled, Current Share Master)	V_{IN} = ISHEN = 5.5V, ISHCOM = Open Circuit		70	120	mA
Operating Supply Current (Current Share Enabled, Current Share Slave)	V_{IN} = ISHEN = ISHSL = 5.5V, ISHCOM Pulled to V_{IN} with 1kΩ, M/S = GND, ISHx = ISHREFx = -100µA, SYNC = External 1MHz Clock		70	120	mA
Standby Supply Current (Current Share Enabled, Current Share Slave)	V_{IN} = ISHEN = ISHSL = 5.5V, EN = M/S = GND, SYNC = External 1MHz Clock		3.0	7	mA
	V_{IN} = ISHEN = ISHSL = 5.5V, M/S = GND, SYNC = External 1MHz Clock, ISHCOM = GND		7.3	11	mA
OUTPUT VOLTAGE & CURRENT					
Reference Voltage		0.594	0.6	0.606	V

Electrical Specifications Unless otherwise noted, V_{IN} = AVDD = DVDD = PVINx = EN = FSEL = M/S = SC0 = SC1= 3V to 5.5V; GND = AGND = DGND = PGNDx = ISHx = ISHCOM = ISHEN = ISHREFx = ISHSL = TDI = TDO = TPGM = 0V; FB = 0.65V; PORSEL = V_{IN} for 4.5V ≤ V_{IN} ≤ 5.5V and GND for V_{IN} < 4.5V; LXx = SYNC = Open Circuit; OCx is connected to OCSSx with a 10kΩ resistor; OCx is connected to GND with a 4.99kΩ resistor shunted by a 6.8nF capacitor; PGOOD is pulled up to V_{IN} with a 1kΩ resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; T_A = T_J = -55°C to +125°C; Post 100krad(Si). (Note 6). **(Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNITS
Output Voltage Tolerance	V_{OUT} = 0.8V to 2.5V, I_{OUT} = 0A to 12A (Notes 11, 12)	-2		2	%
Error Amp Input Offset Voltage	V_{IN} = 5.5V, V_{REF} = 600mV, Test Mode	-1		3	mV
Feedback (FB) Input Leakage Current	V_{IN} = 5.5V, V_{FB} = 600mV	-1.5		1.5	µA
Sustained Output Current	V_{IN} = 3V, V_{OUT} = 1.8V, OCA = OCB = PVIN (Note 13)	16	22		A
PWM CONTROL LOGIC					
Internal Oscillator Tolerance	FSEL = V_{IN} or GND	-15		15	%
External Oscillator Range	M/S = GND	0.4		1.2	MHz
Minimum LXx On Time	V_{IN} = 5.5V, Test Mode		200	275	ns
Minimum LXx Off Time	V_{IN} = 5.5V, Test Mode		0	50	ns
Minimum LXx On Time	V_{IN} = 3V, Test Mode		225	300	ns
Minimum LXx Off Time	V_{IN} = 3V, Test Mode		0	50	ns
PORSEL, Master/Slave (M/S), SC1, SC0, ISHSL, ISHEN, FSEL Input Voltage	Input High Threshold	V_{IN} -0.5	1.3		V
	Input Low Threshold		1.2	0.5	V
PORSEL, Master/Slave (M/S), SC1, SC0, ISHSL, ISHEN, FSEL Input Leakage Current	V_{IN} = 5.5V	-1		1	µA
Synchronization (SYNC) Input Voltage	Input High Threshold, M/S = GND	2.3	1.7		V
	Input Low Threshold, M/S = GND		1.5	1	V
Synchronization (SYNC) Input Leakage Current	V_{IN} = 5.5V, M/S = GND, SYNC = V_{IN} or GND	-1		1	µA
Synchronization (SYNC) Output Voltage	V_{IN} - V_{OH} @ I_{OH} = -1mA		0.1	0.4	V
	V_{OL}@ I_{OL} = 1mA		0.1	0.4	V
POWER BLOCKS					
Upper Device $r_{DS(ON)}$	V_{IN} = 3V, 4A load, All Power Blocks in Parallel, Test Mode (Note 9)		20	40	mΩ
Lower Device $r_{DS(ON)}$	V_{IN} = 3V, 4A load, All Power Blocks in Parallel, Test Mode (Note 9)		15	30	mΩ
LXx Output Leakage	V_{IN} = 5.5V, EN = LXx = GND, Single LXx Output	-1			µA
	V_{IN} = LXx = 5.5V, EN = GND, Single LXx Output			10	µA
Deadtime (Note 12)	Within a Single Power Block or between Power Blocks	2.2	25		ns
Efficiency (Note 12)	V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 6A, FSEL = GND		88		%
	V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 6A		90		%
POWER-ON RESET					
VIN POR	Rising Threshold, PORSEL = V_{IN}	4.1	4.3	4.45	V
	Hysteresis, PORSEL = V_{IN}	225	325	425	mV
	Rising Threshold, PORSEL = GND	2.65	2.8	2.95	V
	Hysteresis, PORSEL = GND	70	140	240	mV
Enable (EN) Input Voltage	Rising/Falling Threshold	0.56	0.6	0.64	V
Enable (EN) Input Leakage Current	V_{IN} = 5.5V, EN = V_{IN} or GND	-3		3	µA

Electrical Specifications Unless otherwise noted, V_{IN} = AVDD = DVDD = PVINx = EN = FSEL = M/S = SC0 = SC1= 3V to 5.5V; GND = AGND = DGND = PGNDx = ISHx = ISHCOM = ISHEN = ISHREFx = ISHSL = TDI = TDO = TPGM = 0V; FB = 0.65V; PORSEL = V_{IN} for 4.5V ≤ V_{IN} ≤ 5.5V and GND for V_{IN} < 4.5V; LXx = SYNC = Open Circuit; OCx is connected to OCSSx with a 10kΩ resistor; OCx is connected to GND with a 4.99kΩ resistor shunted by a 6.8nF capacitor; PGOOD is pulled up to V_{IN} with a 1kΩ resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; T_A = T_J = -55°C to +125°C; Post 100krad(Si). (Note 6). **(Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNITS
Enable (EN) Sink Current	EN = 0.3V	6.4	11	16.6	µA
SOFT-START					
Soft-Start Source Current	SS = GND	20	23	27	µA
Soft-Start Discharge ON-Resistance			2.2	4.7	Ω
Soft-Start Discharge Time			256		Clock Cycles
POWER-GOOD SIGNAL					
Rising Threshold	V_{FB} as a % of V_{REF}, Test Mode	107	111	115	%
Rising Hysteresis	V_{FB} as a % of V_{REF}, Test Mode	2	3.5	5	%
Falling Threshold	V_{FB} as a % of V_{REF}, Test Mode	85	89	93	%
Falling Hysteresis	V_{FB} as a % of V_{REF}, Test Mode	2	3.5	5	%
Power-Good Drive	V_{IN} = 3V, PGOOD = 0.4V, EN = GND	7.2			mA
Power-Good Leakage	V_{IN} = PGOOD = 5.5V			1	µA
PROTECTION FEATURES					
Undervoltage Monitor					
Undervoltage Trip Threshold	V_{FB} as a % of V_{REF}, Test mode	71	75	79	%
Undervoltage Recovery Threshold	V_{FB} as a % of V_{REF}, Test mode	84	88	92	%
Overcurrent Monitor					
Overcurrent Trip Level	I_{OCx} = 60µA, Test mode (Note 14)	5.35		7.35	A
	I_{OCx} = 240µA, Test mode (Note 14)	23		26	A
CURENT SHARE					
Slave Load Current	Master Load Current = 12A, V_{IN} = 3.3V, V_{OUT} = 0.8V, SC1 = ISHSL = M/S = 0, SC0 = ISHEN = FSEL = 1, SYNC = 1MHz External, 500nH inductor (Notes 12, 13)	7	12	17	A
	Master Load Current = 12A, V_{IN} = 3.3V, V_{OUT} = 1.8V, SC0 = ISHSL= M/S = 0, SC1 = ISHEN = FSEL = 1, SYNC = 1MHz External, 500nH inductor (Notes 12, 13)	7	12	17	A
	Master Load Current = 12A, V_{IN} = 5.0V, V_{OUT} = 1.8V, SC0 = ISHSL = M/S = 0, SC1 = ISHEN = FSEL = 1, SYNC = 1MHz External, 500nH inductor (Notes 12, 13)	7	12	17	A
	Master Load Current = 12A, V_{IN} = 5.0V, V_{OUT} = 2.5V, ISHSL = M/S = 0, SC0 = SC1 = ISHEN = FSEL = 1, SYNC=1MHz External, 500nH inductor (Notes 12, 13)	7	12	17	A
ISHx, ISHREFx, Tri-State Leakage Current	V_{IN} = 5.5V, EN = GND	-1	0	1	µA
Master ISHCOM Pull-Up Resistance	ISHCOM = -50µA	6.5	10	13	kΩ
Slave ISHCOM Input Leakage Current	V_{IN} = ISHSL = 5.5V	-1		1	µA
Slave ISHCOM Pull-Down Resistance	ISHSL = V_{IN}, EN = GND, ISHCOM = 7.2mA	35	75	125	Ω
Slave ISHCOM Input High Voltage	ISHSL = V_{IN}	42	52	62	% of V_{IN}
Slave ISHCOM Input Low Voltage	ISHSL = V_{IN}	26	36	46	% of V_{IN}
Slave ISHCOM Input Voltage Hysteresis	ISHSL = V_{IN}	7	16	24	% of V_{IN}

Electrical Specifications Unless otherwise noted, V_{IN} = AVDD = DVDD = PVINx = EN = FSEL = M/S = SC0 = SC1= 3V to 5.5V; GND = AGND = DGND = PGNDx = ISHx = ISHCOM = ISHEN = ISHREFx = ISHSL = TDI = TDO = TPGM = 0V; FB = 0.65V; PORSEL = V_{IN} for 4.5V ≤ V_{IN} ≤ 5.5V and GND for V_{IN} < 4.5V; LXx = SYNC = Open Circuit; OCx is connected to OCSSx with a 10kΩ resistor; OCx is connected to GND with a 4.99kΩ resistor shunted by a 6.8nF capacitor; PGOOD is pulled up to V_{IN} with a 1kΩ resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; T_A = T_J = -55°C to +125°C; Post 100krad(Si). (Note 6). **(Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNITS
ISHSL Input Leakage Current		-1		1	µA
ISHSL Input High Voltage		V_{IN} - 0.5	1.3		V
ISHSL Input Low Voltage			1.2	0.5	V
SLOPE COMPENSATION					
	SC1 = SC0 = V_{IN}	5.9	13.4	17.7	A/µs
	SC1 = V_{IN}, SC0 = GND	3.0	6.7	8.8	A/µs
	SC1 = GND, SC0 = V_{IN}	1.5	3.4	4.5	A/µs
	SC1 = SC0 = GND	0.7	1.7	2.2	A/µs
	FSEL = GND, SC1 = SC0 = V_{IN}	2.9	6.6	8.8	A/µs
	FSEL = GND, SC1 = V_{IN}, SC0 = GND	1.4	3.3	4.5	A/µs
	FSEL = GND, SC1 = GND, SC0 = V_{IN}	0.7	1.6	2.2	A/µs
	FSEL = GND, SC1 = SC0 = GND	0.3	0.8	1.2	A/µs

NOTES:

9. Typical values shown reflect T_A = T_J = +25°C operation and are not guaranteed.
10. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C and +125°C, unless otherwise specified.
11. Limits do not include tolerance of external feedback resistors. The 0A to 12A output current range may be reduced by Minimum LXx On Time and Minimum LXx Off Time specifications.
12. Limits established by characterization or analysis and are not production tested.
13. Tested sequencially on LX2, LX6 and LX9.
14. Tested sequencially on LX2 and LX6 at 535mA to 735mA and 2.3A to 2.6A.
15. Tested in accordance with MIL-STD-883, method 1019, condition A.

Typical Performance Curves

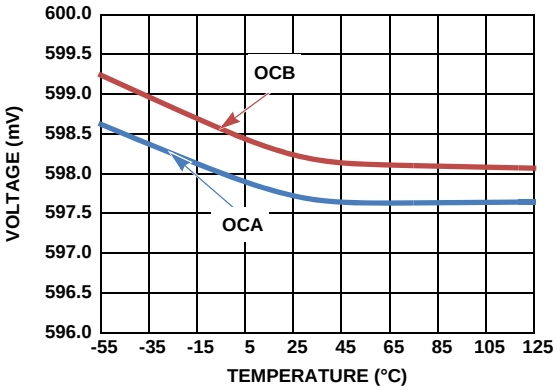


FIGURE 5. OVERCURRENT REFERENCE VOLTAGE

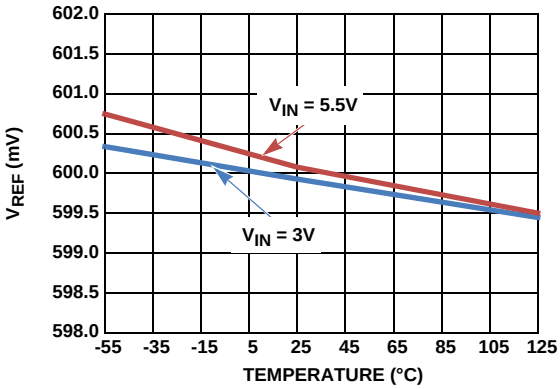


FIGURE 6. REF VOLTAGE vs V_{IN}

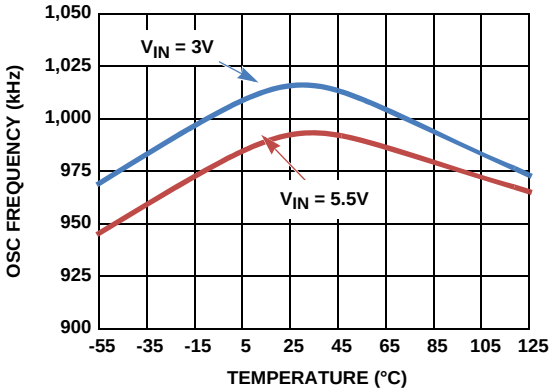


FIGURE 7. OSC FREQUENCY vs V_{IN}

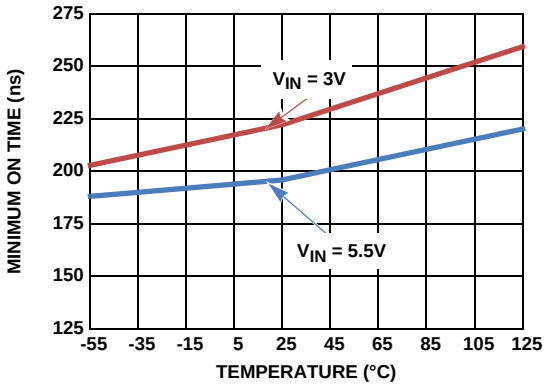


FIGURE 8. LXx MINIMUM ON TIME vs V_{IN}

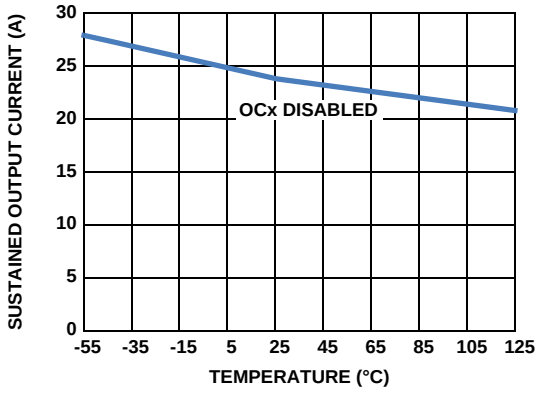


FIGURE 9. SUSTAINED OUTPUT CURRENT WITH OVERCURRENT DISABLED

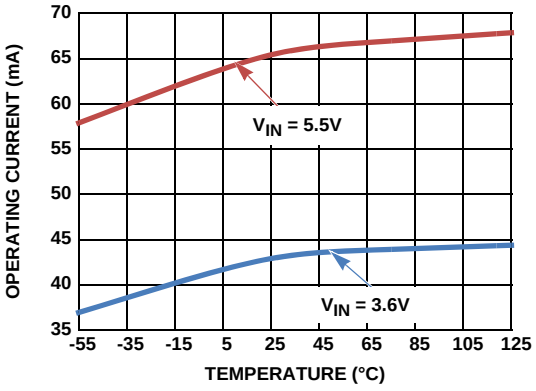


FIGURE 10. OPERATING CURRENT vs V_{IN}

Typical Performance Curves (Continued)

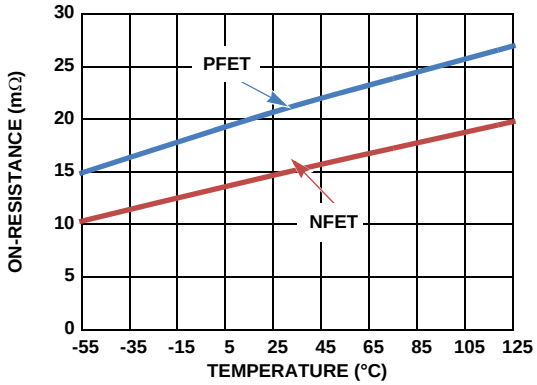
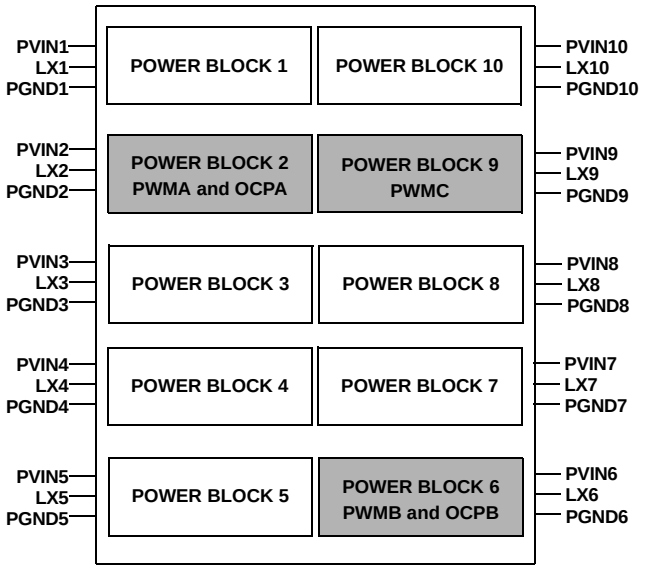


FIGURE 11. LX ON-RESISTANCE, ALL POWER BLOCKS IN PARALLEL, V_{IN} = 3V

Functional Description

The ISL70002SEH is a monolithic, fixed frequency, current-mode synchronous buck regulator. Two ISL70002SEH devices can be used to provide a total DC/DC solution for FPGAs, CPLDs, DSPs and CPUs.



Note: Shaded Blocks indicate pilot current and overcurrent sensors.

FIGURE 12. POWER BLOCK DIAGRAM

Power Blocks

The power output stage of the regulator consists of ten power blocks that are paralleled to provide full 12A output current capability. The block diagram in Figure 12 shows a top level view of the individual power blocks.

Each power block has a power supply input pin, PVINx, a phase output pin, LXx, and a power supply ground pin, PGNDx. All PVINx pins must be connected to a common power supply rail and all PGNDx pins must be connected to a common ground. LXx pins should be connected to the output inductor based on the required load current, but must include the LX2, LX6 and LX9 pins. For example, if 6A of output current is needed, any five LXx pins can be connected to the inductor as long as three of them are the LX2, LX6 and LX9 pins. The unused LXx pins should be left unconnected. Connecting all ten LXx pins to the output inductor provides a maximum 12A of output current at +150°C die temperature. See the "Typical Application Schematic" on page 6 for pin connection guidance.

Power blocks 2, 6 and 9 contain the master pilot devices, which provides current feedback and this is why they must be connected to the output inductor.

Main Control Loop

During normal operation, the internal top power switch is turned on at the beginning of each clock cycle. Current in the output inductor ramps up until the current comparator trips and turns off the top power MOSFET. Then the bottom power MOSFET turns on and the inductor current ramps down for the rest of the cycle.

The current comparator compares the output current at the current ripple peak to the scaled pilot current. The error amplifier monitors V_{OUT} and compares it with an internal reference voltage. The output voltage of the error amplifier creates a proportional current to the pilot. If V_{OUT} is low, the current level of the pilot is increased and the trip off current level of the output is increased. The increased output current raises V_{OUT} until it is in agreement with the reference voltage.

Output Voltage Selection

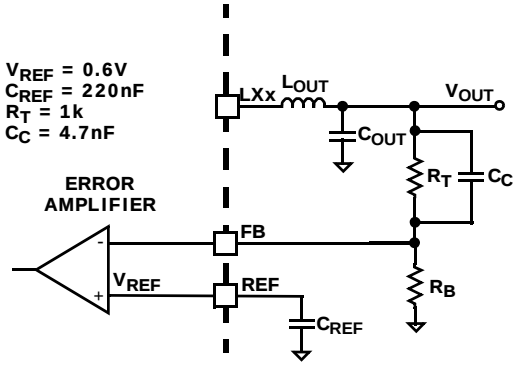


FIGURE 13. OUTPUT VOLTAGE SELECTION

The output voltage of the ISL70002SEH can be adjusted using an external resistor divider as shown in Figure 13. R_T should be selected as 1kΩ to mitigate SEE. R_T should be shunted by a 4.7nF ceramic capacitor, C_C, to mitigate SEE and to improve loop stability margins. The REF pin should be bypassed to AGND with a 220nF ceramic capacitor to mitigate SEE. It should be noted that no current (sourcing or sinking) is available from the REF pin. R_B can be determined from Equation 3. The designer can configure the output voltage from 0.8V to 85% of the input voltage.

$$R_B = R_T \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}} \quad \text{(EQ. 3)}$$

The minimum on time determines the lowest output voltage, so when VIN = 5.5V and the switching frequency is 500kHz this parameter limits the regulated output voltage to about 0.8V or greater. It increases at the 1MHz switching frequency to about 1.6V or greater. The minimum on time increases by about 9% at V_{IN} = 3V, but the 500kHz output voltage is not limited by the minimum on time and the 1MHz minimum V_{OUT} is approximately 0.9V.

Switching Frequency/Synchronization

The ISL70002SEH features an internal oscillator running at a fixed frequency of either 500kHz or 1MHz ±15% over recommended operating conditions. When the FSEL pin is grounded the oscillator operated at 500kHz, and if FSEL is connected to DVDD it operates at 1MHZ.

The regulator can be configured to run from the internal oscillator or can be synchronized to another ISL70002SEH or an SEE hardened external clock with a frequency range of 500kHz to 1MHz (±20%).

To run the regulator from the internal oscillator, connect the M/S pin to DVDD. In this case the output of the internal oscillator

appears on the SYNC pin. To synchronize the regulator to the SYNC output of another ISL70002SEH regulator or to an SEE hardened external clock, connect the M/S pin to DGND. In this case the SYNC pin is an input that accepts an external synchronizing signal. When M/S is connected to DGND, the ISL70002SEH is synchronized 180° out-of-phase with respect to the SYNC input of a Master configured regulator SYNC output or to an external clock.

Two Phase Operation

The ISL70002SEH is capable of operating 2 ICs as a single Two Phase regulator with nearly twice the load current capacity. In this mode, a redundant Current Sharing bus balances the load current between the two devices and communicates any fault conditions. One ISL70002SEH is designated the Master and the other the Slave. The Master ISHSL pin is connected to DGND and the Slave ISHSL pin is connected to DVDD. The ISHEN pins on both Master and Slave are connected to DVDD. The SYNC, ISHA, ISHB, ISHC, ISHREFA, ISHREFB, ISHREFC, ISHCOM and FB pins are connected from the Master to the Slave and the REF pins are tied with a 10Ω resistor. Configured this way, the two phase regulator nearly doubles the load current capacity, limited only by the Current Share Match tolerance.

The ISL70002SEH ICs operate 180° out-of-phase to minimize the input ripple current, effectively operating as a single IC at twice the switching frequency. The Master phase uses the falling edge of the SYNC clock to initiate the Master switching cycle with the non-overlap period before the rising edge of LX, while the Slave phase internally inverts the SYNC input and uses the falling edge of the inverted copy to start it's switching cycle. This is independent of whether the Master phase is configured for an external clock (Master M/S = DGND) or its internal clock (Master M/S = DVDD). The Master Error Amplifier and Compensation controls the two phase regulator while the Slave Error Amplifier is disabled. The schematic in Figure 3 shows the complete connections for the Master and Slave.

Operation Initialization

The ISL70002SEH initializes based on the state of the power-on reset (POR) monitor of the PVINx inputs and the state of the EN input. Successful initialization prompts a soft-start interval and the regulator begins slowly ramping the output voltage. Once the commanded output voltage is within the proper window of operation, the power-good signal changes state from low to high indicating proper regulator operation.

Power-On Reset

The POR circuitry prevents the controller from attempting to soft-start before sufficient bias is present at the PVINx pins.

The POR threshold of the PVINx pins is controlled by the PORSEL pin. For a nominal 5V supply voltage, PORSEL should be connected to DVDD. For a nominal 3.3V supply voltage, PORSEL should be connected to DGND. For nominal supply voltages between 5V and 3.3V, PORSEL should be connected to DGND. The POR rising and falling thresholds are shown in the "Electrical Specifications" table on page 9.

Hysteresis between the rising and falling thresholds insures that small perturbations on PVINx seen during turn-on/turn-off of the regulator do not cause inadvertent turn-off/turn-on of the regulator. When the PVINx pins are below the POR rising threshold, the internal synchronous power MOSFET switches are turned off and the LXx pins are held in a high-impedance state.

Enable and Disable

After the POR input requirement is met, the ISL70002SEH remains in shutdown until the voltage at the enable input rises above the enable threshold. As shown in Figure 14, the enable circuit features a comparator type input. In addition to simple logic on/off control, the enable circuit allows the level of an external voltage to precisely gate the turn-on/turn-off of the regulator. An internal I_{EN} current sink with a typical value of 11µA is only active when the voltage on the EN pin is below the enable threshold. The current sink pulls the EN pin low. As $V_{CONTROL}$ rises, the enable level is not set exclusively by the resistor divider from $V_{CONTROL}$. With the current sink active, the enable level is defined by Equation 4. R1 is the resistor from the EN pin to $V_{CONTROL}$ and R2 is the resistor from the EN pin to the AGND pin.

$$V_{ENABLE} = V_{REF} \cdot \left[1 + \frac{R1}{R2}\right] + I_{EN} \cdot R1 \quad \text{(EQ. 4)}$$

Once the voltage at the EN pin reaches the enable threshold, the I_{EN} current sink turns off.

With the part enabled and the I_{EN} current sink off, the disable level is set by the resistor divider. The disable level is defined by Equation 5.

$$V_{DISABLE} = V_{REF} \cdot \left[1 + \frac{R1}{R2}\right] \quad \text{(EQ. 5)}$$

The difference between the enable and disable levels provides adjustable hysteresis so that noise on $V_{CONTROL}$ does not interfere with the enabling or disabling of the regulator.

The EN pin should be bypassed to the AGND pin with a 10nF ceramic capacitor to mitigate SEE.

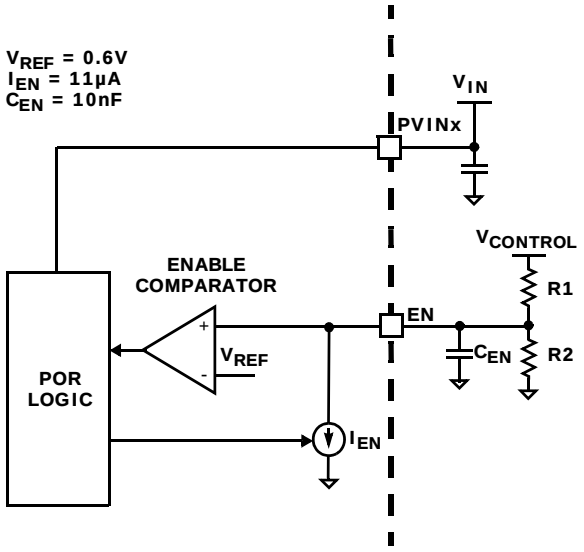


FIGURE 14. ENABLE CIRCUIT

Soft-Start

Once the POR and enable circuits are satisfied, the regulator initiates a soft-start. Figure 15 shows that the soft-start circuit clamps the error amplifier reference voltage to the voltage on an external soft-start capacitor connected to the SS pin. The soft-start capacitor is charged by an internal I_{SS} current source (23µA typical). As the soft-start capacitor is charged, the output voltage slowly ramps to the set point determined by the reference voltage and the feedback network. Once the voltage on the SS pin is equal to the internal reference voltage (600mV), the soft-start interval is complete though the SS pin voltage continues to rise to approximately 1.4V. PGOOD is ENABLED after SS reached to 1.4V. The controlled ramp of the output voltage reduces the inrush current during start-up. The soft-start output ramp interval is defined in Equation 6 and is adjustable from approximately 2ms to 200ms. The value of the soft-start capacitor, C_{SS}, should range from 82nF to 8.2µF, inclusive. The peak inrush current can be computed from Equation 7. The soft-start interval should be selected long enough to insure that the peak in-rush current plus the peak output load current does not exceed the SS overcurrent trip level of the regulator.

$$t_{SS} = C_{SS} \cdot \frac{V_{REF}}{I_{SS}} \quad \text{(EQ. 6)}$$

$$I_{INRUSH} = C_{OUT} \cdot \frac{V_{OUT}}{t_{SS}} \quad \text{(EQ. 7)}$$

The soft-start capacitor is immediately discharged by a 2.2Ω resistor whenever POR conditions are not met or EN is pulled low. The soft-start discharge time is equal to 256 clock cycles.

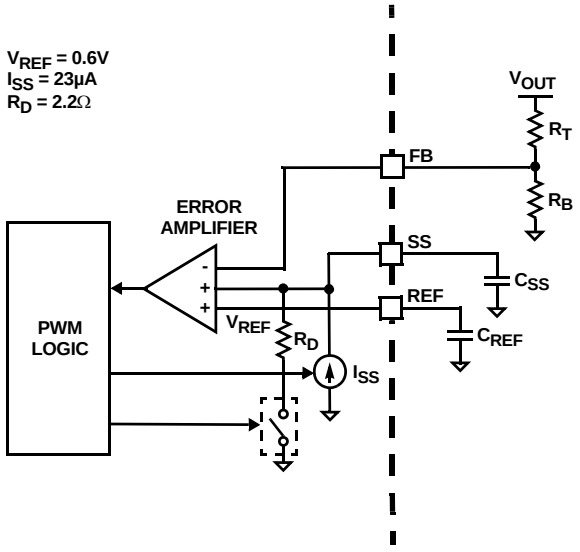


FIGURE 15. SOFT-START CIRCUIT

Power-Good

The power-good (PGOOD) pin is an open-drain logic output which indicates when the output voltage of the regulator is within regulation limits. The power-good pin pulls low during shutdown and remains low when the controller is enabled. After a successful soft-start, the PGOOD pin releases and the voltage rises with an external pull-up resistor. The power-good signal transitions low immediately when the EN pin is pulled low.

The power-good circuitry monitors the FB pin and compares it to the rising and falling thresholds shown in the “Electrical Specifications” table on page 10. If the feedback voltage exceeds the typical rising limit of 111% of the reference voltage, the PGOOD pin pulls low. The PGOOD pin continues to pull low until the feedback voltage falls to a typical of 107.5% of the reference voltage. If the feedback voltage drops below a typical of 89% of the reference voltage, the PGOOD pin pulls low. The PGOOD pin continues to pull low until the feedback voltage rises to a typical 92.5% of the reference voltage. The PGOOD pin then releases and signals the return of the output voltage within the power-good window.

The PGOOD pin can be pulled up to any voltage from 0V to 5.5V, independent of the supply voltage. The pull-up resistor should have a nominal value from 1kΩ to 10kΩ. The PGOOD pin should be bypassed to DGND with a 10nF ceramic capacitor to mitigate SEE.

Slope Compensation

The SC0 and SC1 pins select four levels of Current Mode Slope Compensation. In Current Mode buck regulators, when the duty cycle approaches and exceeds 50% the regulator will operate in sub-harmonic oscillation without Slope Compensation. Slope Compensation is widely considered unnecessary if the duty cycle is held below 40% and provides better phase margin. Transient duty cycles must be taken into consideration when selecting the level of Slope Compensation. The following table describes the amount of effective current that is added the output powerstage signal that is used in the PWM modulator.

TABLE 1.

FSEL	SC1	SC0	SLOPE COMP (A/µs)
DGND	DGND	DGND	0.8
DGND	DGND	DVDD	1.6
DGND	DVDD	DGND	3.3
DGND	DVDD	DVDD	6.6
DVDD	DGND	DGND	1.7
DVDD	DGND	DVDD	3.4
DVDD	DVDD	DGND	6.7
DVDD	DVDD	DVDD	13.4

Fault Monitoring and Protection

The ISL70002SEH actively monitors output voltage and current to detect fault conditions. Fault conditions trigger protective measures to prevent damage to the regulator and external load device.

Undervoltage Protection

A hysteretic comparator monitors the FB pin of the regulator. The feedback voltage is compared to an undervoltage threshold that is a fixed percentage of the reference voltage. Once the

comparator trips on two consecutive switching cycles, indicating a valid undervoltage condition, the undervoltage protection logic shuts down the regulator. If the feedback voltage rises back above the undervoltage threshold plus a specified amount of hysteresis outlined in the “Electrical Specifications” table on page 10 after the first detection and before the second, normal operation continues.

After the regulator shuts down, it enters a delay interval, equivalent to the selected soft-start interval. The undervoltage counter is reset entering the delay interval. The protection logic initiates a normal soft-start once the delay interval ends. If the output successfully soft-starts, the power-good signal goes high and normal operation continues. If undervoltage conditions continue to exist during the soft-start interval, the undervoltage counter must overflow before the regulator shuts down again. This hiccup mode continues indefinitely until the output soft-starts successfully.

Overcurrent Protection

A pilot devices integrated into the PMOS transistor of Power Blocks 2 and 6 samples the inductor current each cycle. This current feedback is scaled and compared to an overcurrent threshold based on the overcurrent resistor connected from OCx to AGND.

If the sampled current exceeds the overcurrent threshold, an overcurrent counter increments. If the sampled current falls below the threshold before the counter overflows, the counter is reset. Once the overcurrent counter reaches 2, the regulator shuts down.

After the regulator shuts down, it enters a delay interval, equivalent to the soft-start interval, allowing the device to cool. The overcurrent counter is reset entering the delay interval. The protection logic initiates a normal soft-start once the delay interval ends. If the output successfully soft-starts, the power-good signal goes high and normal operation continues. If overcurrent conditions continue to exist during the soft-start interval, the overcurrent counter must overflow before the regulator shut downs the output again. This hiccup mode continues indefinitely until the output soft-starts successfully.

Component Selection Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a power converter. It is assumed the reader is familiar with many of the basic skills and techniques referenced below. In addition to this guide, Intersil provides a complete evaluation board that includes schematic, BOM, and an example PCB layout.

Output Filter Design

The output inductor and the output capacitor bank together form a low-pass filter responsible for smoothing the pulsating voltage at the phase node. The filter must also provide the transient energy until the regulator can respond. Since the filter has low bandwidth relative to the switching frequency, it limits the system transient response. The output capacitors must supply or sink current while the current in the output inductor increases or decreases to meet the load demand.

OUTPUT CAPACITOR SELECTION

The critical load parameters in choosing the output capacitors are the maximum size of the load step (ΔI_{STEP}), the load-current slew rate (di/dt), and the maximum allowable output voltage deviation under transient loading (ΔV_{MAX}). Capacitors are characterized according to their capacitance, ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance).

At the beginning of a load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount shown in Equation 8.

$$\Delta V_{MAX} \approx \left[ESL \times \frac{di}{dt}\right] + [ESR \times \Delta I_{STEP}] \quad \text{(EQ. 8)}$$

The filter capacitors selected must have sufficiently low ESL and ESR such that the total output voltage deviation is less than the maximum allowable ripple.

Most capacitor solutions rely on a mixture of high frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but larger ESR. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

Ceramic capacitors with X7R dielectric are recommended. Alternately, a combination of low ESR solid tantalum capacitors and ceramic capacitors with X7R dielectric may be used.

The ESR of the bulk capacitors is responsible for most of the output voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current, a voltage, $V_{P-P(MAX)}$, develops across the bulk capacitor according to Equation 9.

$$V_{P-P(MAX)} = ESR \times \left[\frac{(V_{IN} - V_{OUT})V_{OUT}}{L_{OUT} \times f_s \times V_{IN}}\right] \quad \text{(EQ. 9)}$$

OUTPUT INDUCTOR SELECTION

Once the output capacitors are selected, the maximum allowable ripple voltage, $V_{P-P(MAX)}$, determines the lower limit on the inductance as shown in Equation 10.

$$L_{OUT} \geq ESR \times \left[\frac{(V_{IN} - V_{OUT})V_{OUT}}{f_s \times V_{IN} \times V_{P-P(MAX)}}\right] \quad \text{(EQ. 10)}$$

Since the output capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductor must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 11 gives the upper limit on output inductance for the case when the trailing edge of the current transient causes the greater output voltage deviation than the leading edge. Equation 12 addresses the leading edge. Normally, the trailing edge dictates the inductance selection because duty cycles are usually <50%. Nevertheless, both inequalities should be evaluated, and inductance should be governed based on the lower of the two results. In each equation, L_{OUT} is the output inductance, C_{OUT} is

the total output capacitance and $\Delta I_{L(P-P)}$ is the peak to peak ripple current in the output inductor.

$$L_{OUT} \leq \frac{2 \cdot C_{OUT} \cdot V_{OUT}}{(\Delta I_{STEP})^2}\left[\Delta V_{MAX} - (\Delta I_{L(P-P)} \cdot ESR)\right] \quad \text{(EQ. 11)}$$

$$L_{OUT} \leq \frac{2 \cdot C_{OUT}}{(\Delta I_{STEP})^2}\left[\Delta V_{MAX} - (\Delta I_{L(P-P)} \cdot ESR)\right]\left(V_{IN} - V_{OUT}\right) \quad \text{(EQ. 12)}$$

The other concern when selecting an output inductor is to insure there is adequate slope compensation when the regulator is operated above 40% duty cycle. In most cases, the maximum slope compensation setting (SC1 = DVDD, SC0 = DVDD provides sufficient phase margin, therefore this is the recommended configuration.

Input Capacitor Selection

Input capacitors are responsible for sourcing the AC component of the input current flowing into the switching power devices. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the switching power devices which is related to duty cycle. The maximum RMS current required by the regulator is closely approximated by Equation 13.

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}} \sqrt{1 + \frac{1}{3} \times \left(\frac{V_{IN} - V_{OUT}}{I_{OUT} \times L_{OUT} \times f_s} \times \frac{V_{OUT}}{V_{IN}}\right)^2} \quad \text{(EQ. 13)}$$

The important parameters to consider when selecting an input capacitor are the voltage rating and the RMS ripple current rating. For reliable operation, select capacitors with voltage ratings at least 1.5x greater than the maximum input voltage. The capacitor RMS ripple current rating should be higher than the largest RMS ripple current required by the circuit.

A combination of low ESR tantalum capacitors and ceramic capacitors with X7R dielectric are recommended. The ISL70002SEH requires a minimum effective input capacitance of 100µF for stable operation.

PCB Design

PCB design is critical to high-frequency switching regulator performance. Careful component placement and trace routing are necessary to reduce voltage spikes and minimize undesirable voltage drops. Selection of a suitable thermal interface material is also required for optimum heat dissipation and to provide lead strain relief.

PCB Plane Allocation

Four layers of two ounce copper are recommended. Layer 2 should be a dedicated ground plane with all critical component ground connections made with vias to this layer. Layer 3 should be a dedicated power plane split between the input and output power rails. Layers 1 and 4 should be used primarily for signals, but can also provide additional power and ground islands as required.

PCB Component Placement

Components should be placed as close as possible to the IC to minimize stray inductance and resistance. Prioritize the placement of bypass capacitors on the pins of the IC in the order shown: REF, SS, AVDD, DVDD, PVINx (high frequency capacitors), EN, PGOOD, PVINx (bulk capacitors).

Locate the output voltage resistive divider as close as possible to the FB pin of the IC. The top leg of the divider should connect directly to the POL (Point Of Load) and the bottom leg of the divider should connect directly to AGND. The junction of the resistive divider should connect directly to the FB pin.

A small series R-C snubber connected from the LXx pins to the PGNDx pins may be used to damp high frequency ringing on the LXx pins if desired.

PCB Layout

Use a small island of copper to connect the LXx pins of the IC to the output inductor on layers 1 and 4. Void the copper on layers 2 and 3 adjacent to the island to minimize capacitive coupling to the power and ground planes. Place most of the island of layer 4 to minimize the amount of copper that must be voided from the ground plane (layer 2).

Keep all other signal traces as short as possible.

For an example layout refer to AN1732.

Thermal Management

For optimum thermal performance, place a pattern of vias on the top layer of the PCB directly underneath the IC. Connect the vias to the ground plane on layer 2, which serves as a heatsink. To insure good thermal contact, thermal interface material such as a Sil-Pad or thermally conductive epoxy should be used to fill the gap between the vias and the bottom of the IC.

Lead Strain Relief

The package leads protrude from the bottom of the package and the leads are slightly bent to provide strain relief.

Weight Characteristics

Weight of Packaged Device

1.43 Grams typical

Die Characteristics

Die Dimensions

8300µm x 8300µm (327 mils x 327 mils)
Thickness: 300µm ± 25.4µm (12 mils ± 1 mil)

Interface Materials

GLASSIVATION

Type: Silicon Oxide and Silicon Nitride
Thickness: 0.3µm ± 0.03µm and 1.2µm ± 0.12µm

TOP METALLIZATION

Type: AlCu (0.5%)
Thickness: 2.7µm ±0.4µm

SUBSTRATE

Type: Silicon
Isolation: Junction

BACKSIDE FINISH

Silicon

ASSEMBLY RELATED INFORMATION

Substrate and Metal Lid Potential

PGND

ADDITIONAL INFORMATION

Worst Case Current Density

$< 2 \times 10^5$ A/cm^2

Transistor Count

28,160

Layout Characteristics

Step and Repeat

8300µm x 8300µm

Metallization Mask Layout

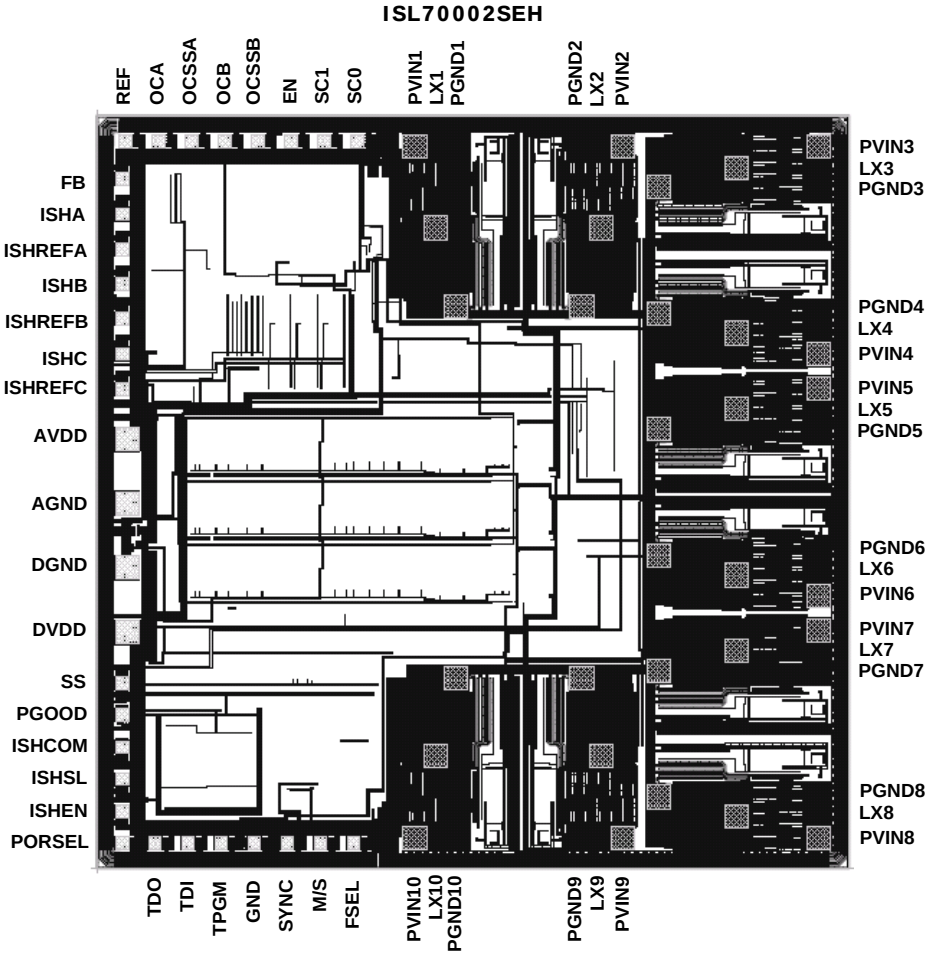


TABLE 2. LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES SIZE (0.001")
FB	1	275	7497	135	135	1.5
ISHA	2	275	7117	135	135	1.5
ISHREFA	3	275	6737	135	135	1.5
ISHB	4	275	6357	135	135	1.5
ISHREFB	5	275	5977	135	135	1.5
ISHC	6	275	5597	135	135	1.5
ISHREFC	7	275	5217	135	135	1.5
AVDD	8	335	4672	254	254	3
AGND	9	335	3972	254	254	3
DGND	10	335	3272	254	254	3
DVDD	11	335	2572	254	254	3
SS	12	275	2021	135	134	1.5
PGOOD	13	275	1671	135	135	1.5
1SHCOM	14	275	1321	135	135	1.5
ISHSL	15	275	971	135	135	1.5
ISHEN	16	275	621	135	135	1.5
PORSEL	17	275	275	135	135	1.5
TDO	18	635	275	135	135	1.5
TDI	19	995	275	135	135	1.5
TPGM	20	1355	275	135	135	1.5
GND	21	1715	275	135	135	1.5
SYNC	22	2075	275	135	135	1.5
M/S	23	2435	275	135	135	1.5
FSEL	24	2795	275	135	135	1.5
PVIN10	25	3463	336	254	254	3
LX10	26	3693	1222	254	254	3
PGND10	27	3905	2074	254	254	3
PGND9	28	5281	2074	254	254	3
LX9	29	5494	1222	254	254	3
PVIN9	30	5723	336	254	254	3
PVIN8	31	6115	778	254	254	3
LX8	32	6967	566	254	254	3
PGND8	33	7853	336	254	254	3
PGND7	34	6115	2154	254	254	3
LX7	35	6967	2366	254	254	3
PVIN7	36	7853	2596	254	254	3
PVIN6	37	7853	2965	254	254	3
LX6	38	6967	3195	254	254	3
PGND6	39	6115	3408	254	254	3

TABLE 2. LAYOUT X-Y COORDINATES (Continued)

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES SIZE (0.001")
PGND5	40	6115	4784	254	254	3
LX5	41	6967	4996	254	254	3
PVIN5	42	7853	5226	254	254	3
PVIN4	43	7853	5595	254	254	3
LX4	44	6967	5825	254	254	3
PGND4	45	6115	6037	254	254	3
PGND3	46	7853	7855	254	254	3
LX3	47	6967	7625	254	254	3
PVIN3	48	6115	7413	254	254	3
PVIN2	49	5723	7855	254	254	3
LX2	50	5494	6969	254	254	3
PGND2	51	5281	6117	254	254	3
PGND1	52	3905	6117	254	254	3
LX1	53	3693	6969	254	254	3
PVIN1	54	3463	7855	254	254	3
SC0	55	2836	7914	135	135	1.5
SC1	56	2476	7914	135	135	1.5
EN	57	2116	7914	135	135	1.5
OCSSB	58	1756	7914	135	135	1.5
OCB	59	1396	7914	135	135	1.5
OCSSA	60	1036	7914	135	135	1.5
OCA	61	676	7914	135	135	1.5
REF	62	316	7914	135	135	1.5

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 30, 2012	FN8264.1	Figure 2 on page 1changed “Slave” to “Master” to CH1 and added “at 86.4MeV/mg/cm2" to Figure Title. “Soft-Start” on page 16 changed in 2nd to last sentence “...range from 8.2nF...” to “...range from 82nF...” “LAYOUT X-Y COORDINATES” on page 20 changed in Bond Wires column for “ISHB” from “1.51” to “1.5”
March 27, 2012	FN8264.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL70002SEH

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

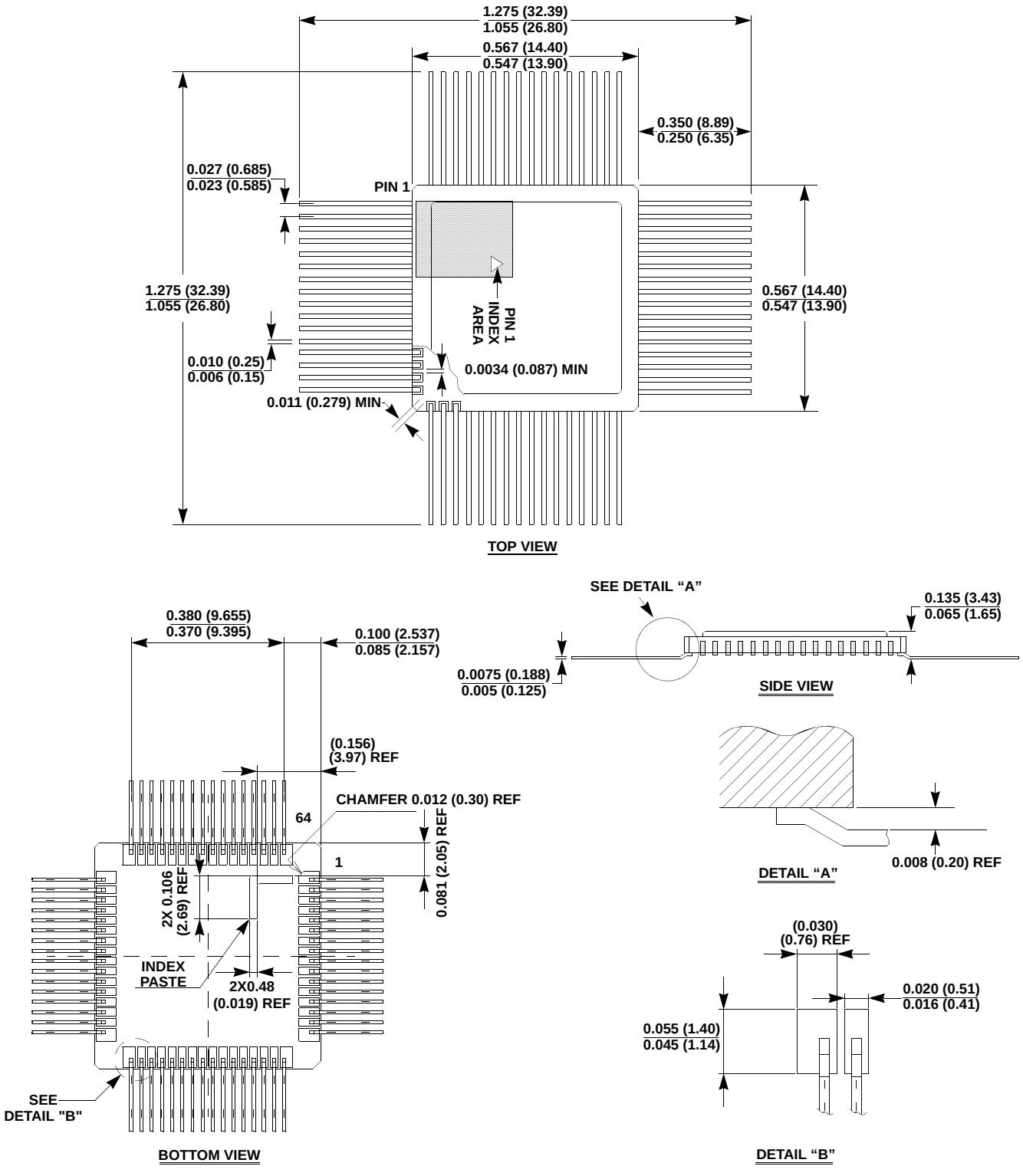
FITs are available from our website at: http://rel.intersil.com/reports/search.php

Package Outline Drawing

R64.A

64 CERAMIC QUAD FLATPACK PACKAGE (CQFP)

Rev 3, 1/12



NOTES:

1. **All dimensions are in inches (millimeters).**